



**THE DATASHEET OF  
DMP3068L-13**



## Product Summary

$V_{(BR)DS}$	$R_{DS(ON)}$ max	Package	$I_D$ max $T_A = +25^\circ C$
-30V	72m $\Omega$ @ $V_{GS} = -10V$	SOT-23	-3.9A
	85m $\Omega$ @ $V_{GS} = -4.5V$		-3.6A

## Description and Applications

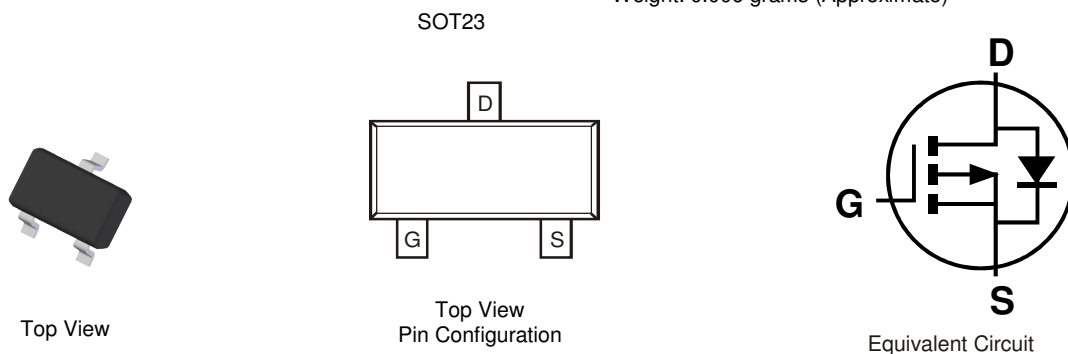
This new generation MOSFET is designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic.  
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Lead-Free Plating (Matte Tin Finish Annealed over Alloy 42 Leadframe).
- Terminals: Solderable per MIL-STD-202, Method 208 <sup>Ⓔ</sup>
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)

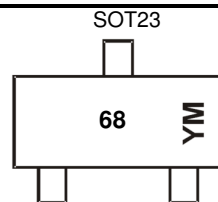


## Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3068L-7	SOT23	3,000/Tape & Reel
DMP3068L-13	SOT23	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



68 = Product Type Marking Code  
 YM = Date Code Marking  
 Y or  $\bar{Y}$  = Year (ex: B = 2014)  
 M or  $\bar{M}$  = Month (ex: 9 = September)

### Date Code Key

Year	2014	2015	2016	2017	2018	2019	2020
Code	B	C	D	E	F	G	H

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25 °C unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V <sub>DSS</sub>	-30	V
Gate-Source Voltage			V <sub>GSS</sub>	±12	V
Drain Current (Note 6) V <sub>GS</sub> = -10V	Steady State	T <sub>A</sub> = +25 °C T <sub>A</sub> = +70 °C	I <sub>D</sub>	-3.3 -2.6	A
	t < 10s	T <sub>A</sub> = +25 °C T <sub>A</sub> = +70 °C	I <sub>D</sub>	-3.9 -3.2	A
Pulsed Drain Current (Pulse width ≤ 10 μs, Duty Cycle ≤ 1%)			I <sub>DM</sub>	-18	A

**Thermal Characteristics**

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			P <sub>D</sub>	0.7	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State		R <sub>θJA</sub>	182	°C/W
	t < 10s			133	
Total Power Dissipation (Note 6)			P <sub>D</sub>	1.2	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		R <sub>θJA</sub>	103	°C/W
	t < 10s			75	
Operating and Storage Temperature Range			T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25 °C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250 μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.5	—	-1.3	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	57	72	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.2A V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.0A V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -2.0A V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -1.0A
			64	85		
			80	120		
			107	165		
Diode Forward Voltage	V <sub>SD</sub>	—	—	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.0A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	708	—	pF	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	57	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	47	—	pF	
Gate Resistance	R <sub>G</sub>	—	14	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>G</sub>	—	7.3	—	nC	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4A
Total Gate Charge (V <sub>GS</sub> = -10V)	Q <sub>G</sub>	—	15.9	—	nC	
Gate-Source Charge	Q <sub>GS</sub>	—	1.2	—	nC	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4A
Gate-Drain Charge	Q <sub>GD</sub>	—	1.7	—	nC	
Turn-On Delay Time	t <sub>d(on)</sub>	—	3.5	—	ns	
Rise Time	t <sub>r</sub>	—	15.8	—	ns	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -4A, R <sub>G</sub> = 6.0Ω
Turn-Off Delay Time	t <sub>d(off)</sub>	—	70.3	—	ns	
Fall Time	t <sub>f</sub>	—	33.9	—	ns	

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1in. square copper plate.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

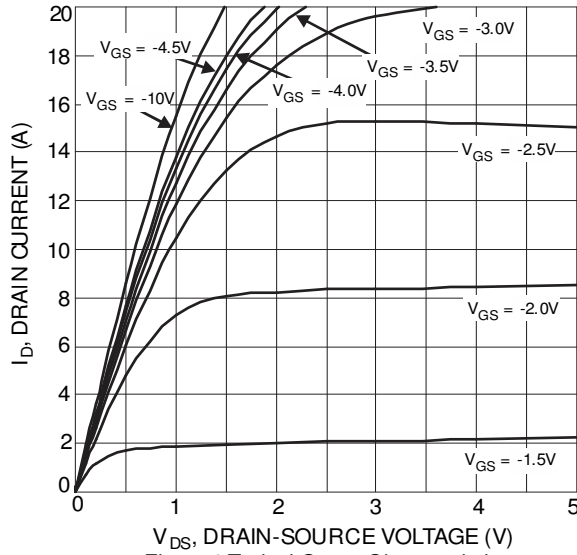


Figure 1 Typical Output Characteristics

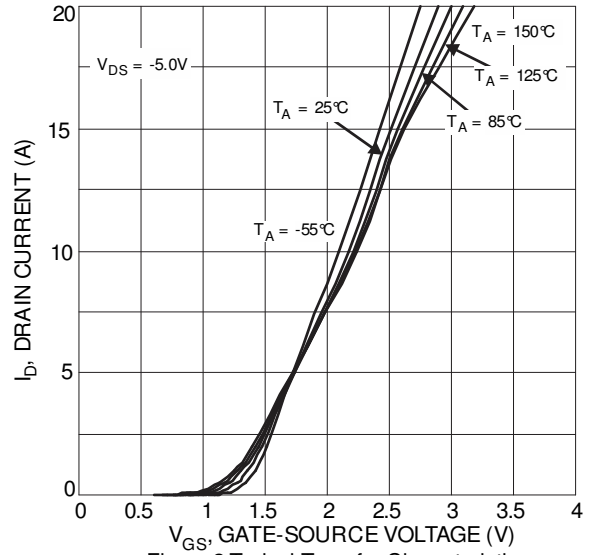


Figure 2 Typical Transfer Characteristics

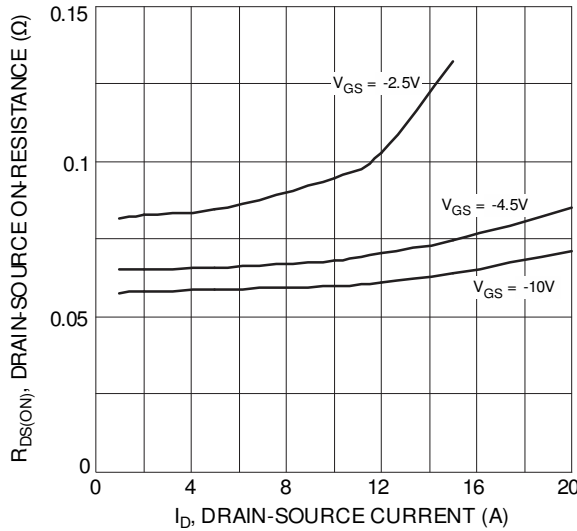


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

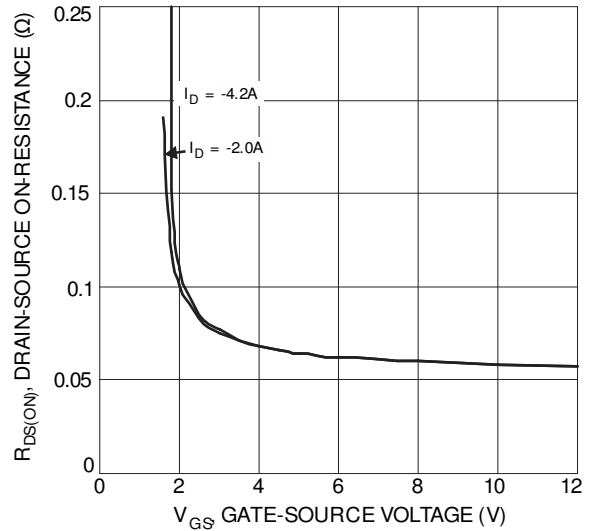


Figure 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

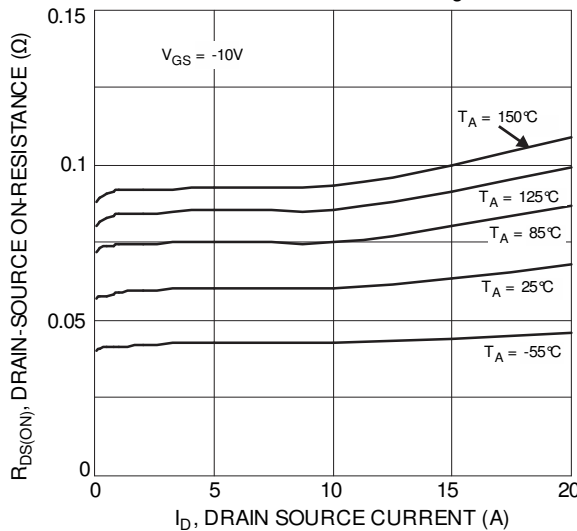


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

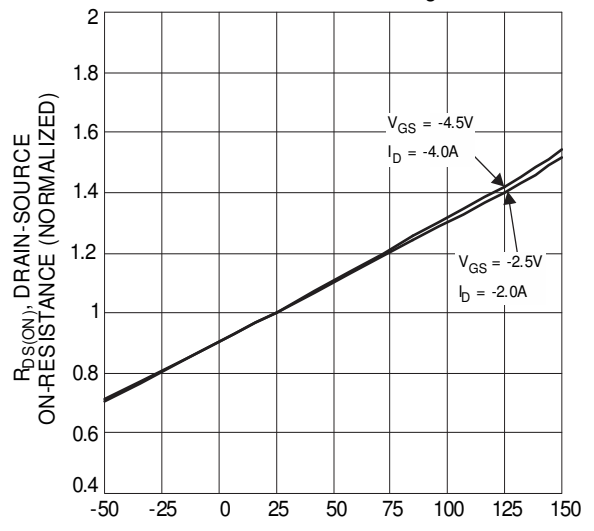


Figure 6 On-Resistance Variation with Temperature

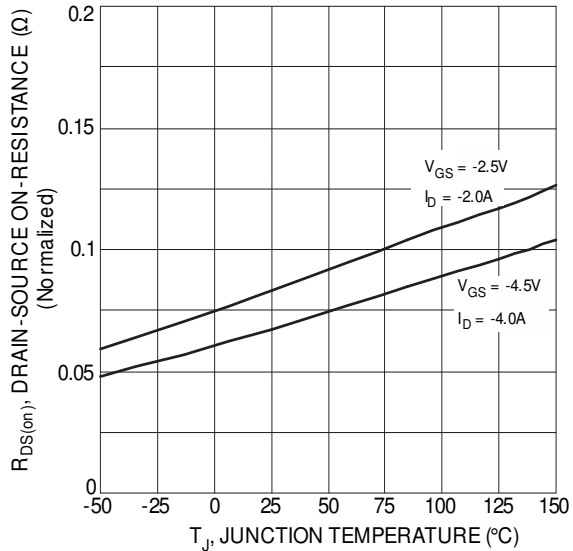


Figure 7 On-Resistance Variation with Temperature

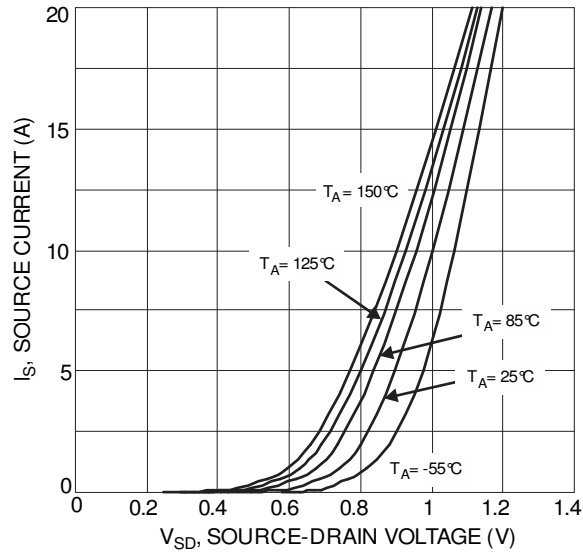


Figure 9 Diode Forward Voltage vs. Current

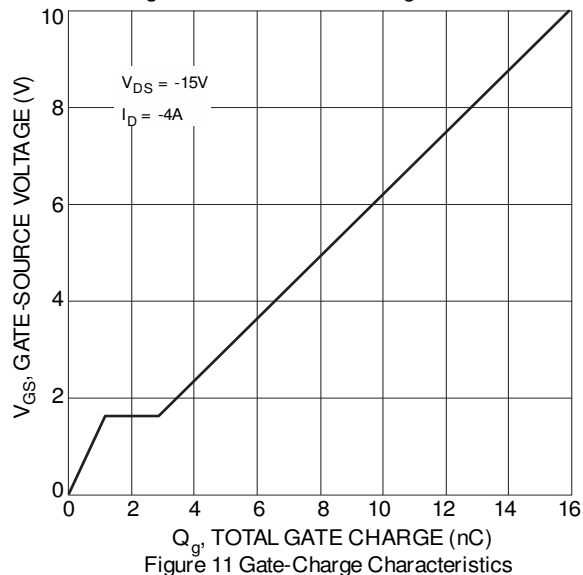


Figure 11 Gate-Charge Characteristics

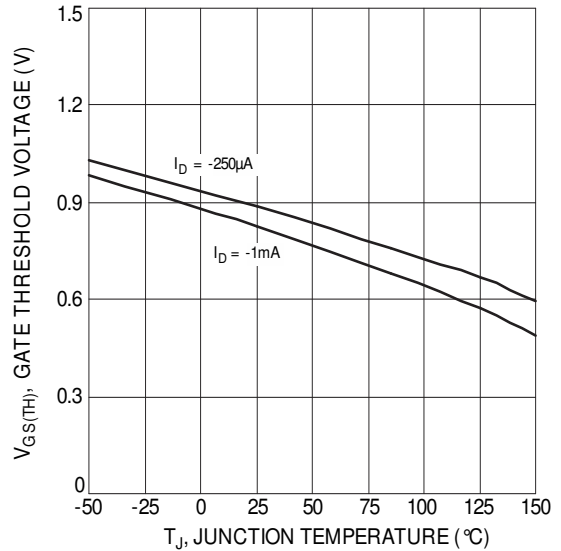


Figure 8 Gate Threshold Variation vs. Ambient Temperature

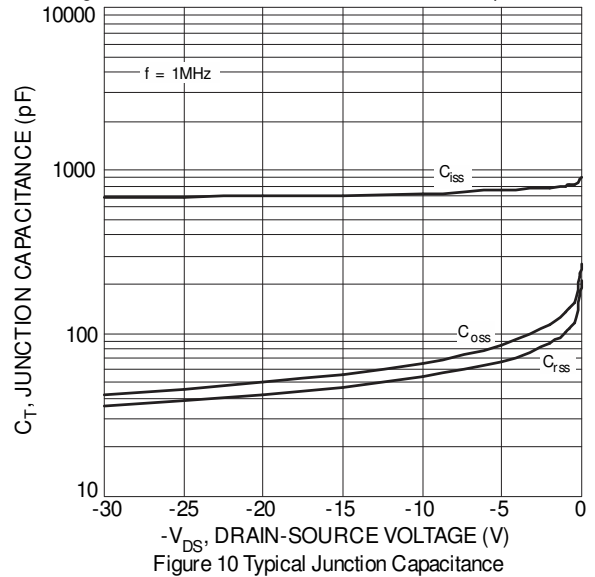


Figure 10 Typical Junction Capacitance

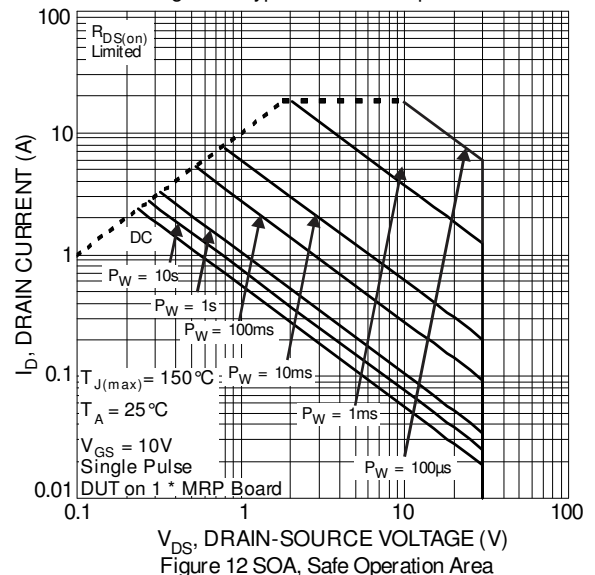
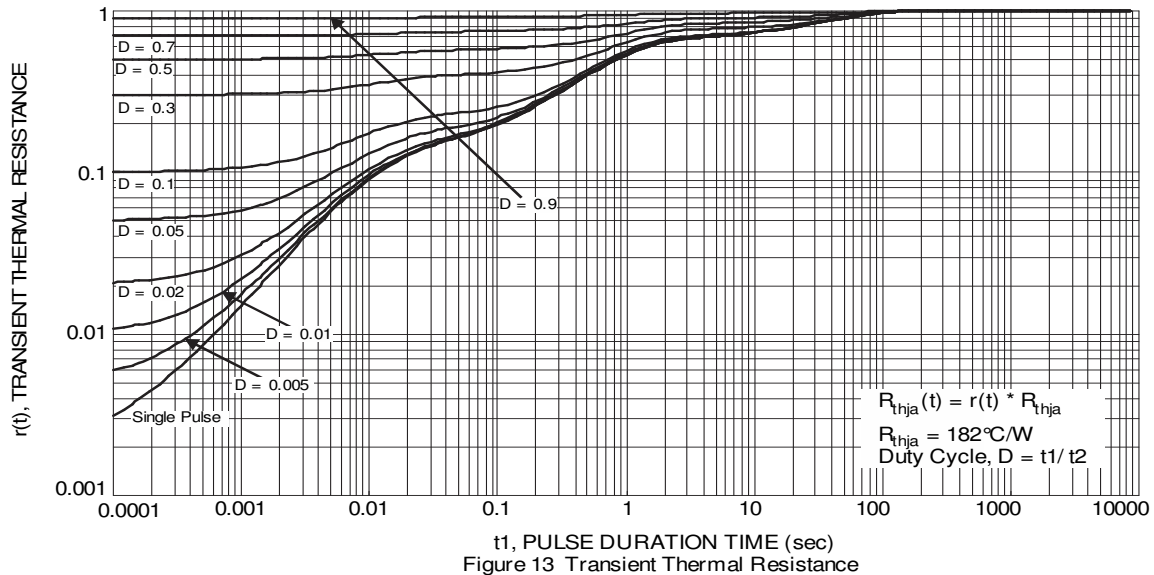
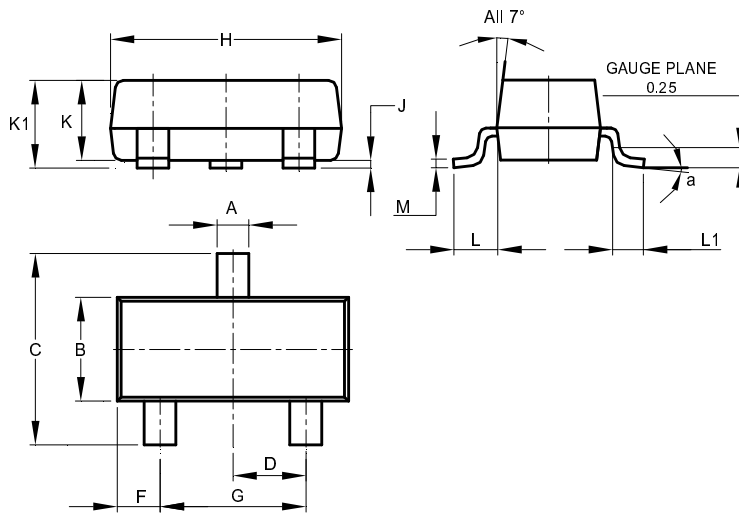


Figure 12 SOA, Safe Operation Area



**Package Outline Dimensions**

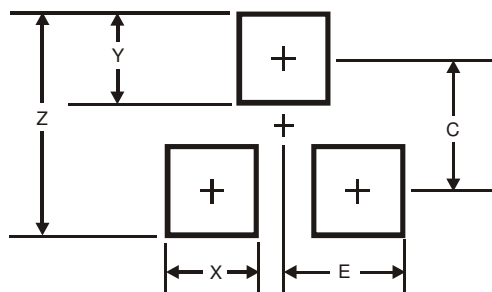
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest the version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	8°		
All Dimensions in mm			

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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