



**THE DATASHEET OF
LMP91050MME/NOPB**



LMP91050 Configurable AFE for Nondispersive Infrared (NDIR) Sensing Applications

1 Features

- Programmable Gain Amplifier
- *Dark Signal* Offset Cancellation
- Supports External Filtering
- Common-Mode Generator and 8-Bit DAC
- Key Specifications
 - Programmable Gain 167 to 7986 V/V
 - Low Noise (0.1 to 10 Hz) 0.1 μ V_{RMS}
 - Gain Drift 100 ppm/°C (Maximum)
 - Phase Delay Drift 500 ns (Maximum)
 - Power Supply Voltage Range 2.7 to 5.5 V

2 Applications

- NDIR Sensing
- Demand Control Ventilation
- Building Monitoring
- CO₂ Cabin Control — Automotive
- Alcohol Detection — Automotive
- Industrial Safety and Security
- GHG and Freons Detection Platforms

3 Description

The LMP91050 device is a programmable integrated Sensor Analog Front End (AFE) optimized for thermopile sensors, as typically used in NDIR applications. It provides a complete signal path solution between a sensor and microcontroller that generates an output voltage proportional to the thermopile voltage. The programmability of the LMP91050 enables it to support multiple thermopile sensors with a single design as opposed to the multiple discrete solutions.

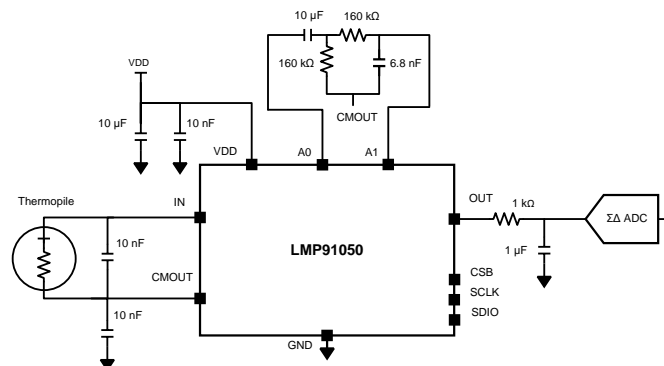
The LMP91050 features a programmable gain amplifier (PGA), *dark phase* offset cancellation, and an adjustable common-mode generator (1.15 V or 2.59 V) which increases output dynamic range. The PGA offers a low-gain range of 167 V/V to 1335 V/V plus a high-gain range of 1002 V/V to 7986 V/V which enables the user to use thermopiles with different sensitivities. The PGA is highlighted by low-gain drift (100 ppm/°C), output offset drift (1.2 mV/°C at G = 1002 V/V), phase delay drift (500 ns) and noise specifications (0.1 μ V_{RMS} 0.1 to 10Hz).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| LMP91050 | VSSOP (10) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Configurable AFE for NDIR



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (March 2013) to Revision E | Page |
|---|------|
| <ul style="list-style-type: none"> • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 1 | 1 |

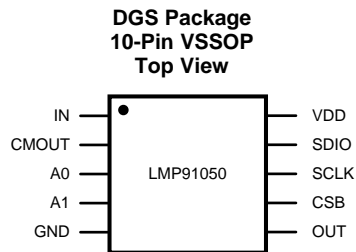
| Changes from Revision C (April 2012) to Revision D | Page |
|---|------|
| <ul style="list-style-type: none"> • Changed layout of National Data Sheet to TI format 17 | 17 |

5 Description (continued)

The offset cancellation circuitry compensates for the *dark signal* by adding an equal and opposite offset to the input of the second stage, thus removing the original offset from the output signal. This offset cancellation circuitry allows optimized usage of the ADC full scale and relaxes ADC resolution requirements.

The LMP91050 allows extra signal filtering (high-pass, lowpass or bandpass) through dedicated pins A0 and A1, in order to remove out of band noise. The user can program through the on board SPI interface. Available in a small form factor 10-pin package, the LMP91050 operates from –40 to 105°C.

6 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|-------|------------------------|---|
| NO. | NAME | | |
| 1 | IN | Analog Input | Signal Input |
| 2 | CMOUT | Analog Output | Common-Mode Voltage Output |
| 3 | A0 | Analog Output | First Stage Output |
| 4 | A1 | Analog Input | Second Stage Input |
| 5 | GND | Power | Ground |
| 6 | OUT | Analog Output | Signal Output, reference to the same potential as CMOUT |
| 7 | CSB | Digital Input | Chip Select, active low |
| 8 | SCLK | Digital Input | Interface Clock |
| 9 | SDIO | Digital Input / Output | Serial Data Input / Output |
| 10 | VDD | Power | Positive Supply |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

| | MIN | MAX | UNIT |
|---------------------------------------|------|-----------|------|
| Supply Voltage (VDD) | –0.3 | 6 | V |
| Voltage at Any Pin | –0.3 | VDD + 0.3 | V |
| Input Current at Any Pin | | 5 | mA |
| Junction Temperature ⁽⁴⁾ | | 150 | °C |
| Storage Temperature, T _{stg} | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) For soldering specifications: see product folder at www.ti.com and [SNOA549](#).
- (4) The maximum power dissipation is a function of T_J(MAX), θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is P_DMAX = (T_J(MAX) - T_A) / θ_{JA}. All numbers apply for packages soldered directly onto a PC board.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1250 |
| | | Machine Model | ±250 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|-------------------------------------|-----|-----|------|
| Supply Voltage | 2.7 | 5.5 | V |
| Junction Temperature ⁽²⁾ | –40 | 105 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | LMP91050 | UNIT |
|---|-------------|------|
| | DGS (VSSOP) | |
| | 10 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 176 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, unless otherwise specified. All other limits apply to T_A = T_J = +25°C.⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN ⁽²⁾ | TYP ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|--|---|--------------------|--------------------|--------------------|-------|
| POWER SUPPLY | | | | | |
| VDD Supply voltage | | 2.7 | 3.3 | 5.5 | V |
| IDD Supply current | All analog block ON | 3.1 | 3.7 | 4.2 | mA |
| | Power-down supply current | 45 | 85 | 121 | µA |
| OFFSET CANCELLATION (OFFSET DAC) | | | | | |
| Resolution | | | 256 | | steps |
| LSB | All gains | | 33.8 | | mV |
| DNL | | –1 | | 2 | LSB |
| Error | Output referred offset error, all gains | | ±100 | | mV |
| Offset adjust range | Output referred, all gains | 0.2 | | VDD – 0.2 | V |
| DAC settling time | | | 480 | | µs |
| PROGRAMMABLE GAIN AMPLIFIER (PGA) 1ST STAGE, R_L = 10 kΩ, C_L = 15 pF | | | | | |
| IBIAS Bias current | | | 5 | | pA |
| | T _A = –40°C to +85°C | | | 200 | |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics (continued)

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, unless otherwise specified. All other limits apply to TA = TJ = +25°C.⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN ⁽²⁾ | TYP ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|--|--|---|--------------------|--------------------|---------------------|--------|
| VINMAX_HGM | Max input signal high-gain mode | Referenced to CMOUT voltage, it refers to the maximum voltage at the IN pin before clipping; It includes dark voltage of the thermopile and signal voltage. | | ±2 | | mV |
| VINMAX_LGM | Max input signal low-gain mode | | | ±12 | | mV |
| VOS | Input offset voltage | | | -165 | | µV |
| G_HGM | Gain high-gain mode | | | 250 | | V/V |
| G_LGM | Gain low-gain mode | | | 42 | | V/V |
| GE | Gain error | Both HGM and LGM | | 2.5% | | |
| VOUT | Output voltage range | | 0.5 | | VDD – 0.5 | V |
| PhDly | Phase delay | 1-mV input step signal, HGM, VOUT measured at Vdd/2 | | 6 | | µs |
| TCPHDly | Phase delay variation with temperature | 1-mV input step signal, HGM, VOUT measured at Vdd/2, | | 416 | | ns |
| SSBW | Small signal bandwidth | Vin = 1mVpp, Gain = 250 V/V | | 18 | | kHz |
| Cin | Input capacitance | | | 100 | | pF |
| PROGRAMMABLE GAIN AMPLIFIER (PGA) 2ND STAGE, RS = 1 kΩ, CL = 1 µF | | | | | | |
| VINMAX | Max input signal | GAIN = 4 V/V | | 1.65 | | V |
| VINMIN | Min input signal | | | 0.82 | | V |
| G | Gain | Programmable in 4 steps | 4 | | 32 | V/V |
| GE | Gain error | Any gain | | 2.5 | | % |
| VOUT | Output voltage range | | 0.2 | | VDD – 0.2 | V |
| PhDly | Phase delay | 100-mV input sine 35-kHz signal, Gain = 8, VOUT measured at 1.65 V, RL = 10 kΩ | | 1 | | µs |
| TCPHDly | Phase delay variation with temperature | 250-mV input step signal, Gain = 8, VOUT measured at Vdd/2 | | 84 | | ns |
| SSBW | Small signal bandwidth | Gain = 32 V/V | | 360 | | kHz |
| Cin | Input capacitance | | | 5 | | pF |
| CLOAD, OUT | OUT pin load capacitance | Series RC | | 1 | | µF |
| RLOAD, OUT | OUT pin load resistance | Series RC | | 1 | | kΩ |
| COMBINED AMPLIFIER CHAIN SPECIFICATION | | | | | | |
| en | Input-referred noise density | Combination of both current and voltage noise, with a 86kΩ source impedance at 5Hz, Gain = 7986 | | 30 | | nV/√Hz |
| | Input-referred integrated noise | Combination of both current and voltage noise, with a 86kΩ source impedance 0.1Hz to 10Hz, Gain = 7986 | | 0.1 | 0.12 ⁽⁴⁾ | µVrms |
| G | Gain | PGA1 GAIN = 42, PGA2 GAIN = 4 | | 167 | | V/V |
| | | PGA1 GAIN = 42, PGA2 GAIN = 8 | | 335 | | |
| | | PGA1 GAIN = 42, PGA2 GAIN = 16 | | 669 | | |
| | | PGA1 GAIN = 42, PGA2 GAIN = 32 | | 1335 | | |
| | | PGA1 GAIN = 250, PGA2 GAIN = 4 | | 1002 | | |
| | | PGA1 GAIN = 250, PGA2 GAIN = 8 | | 2004 | | |
| | | PGA1 GAIN = 250, PGA2 GAIN = 16 | | 4003 | | |
| | | PGA1 GAIN = 250, PGA2 GAIN = 32 | | 7986 | | |
| GE | Gain error | Any gain | | 5% | | |

(4) Specified by design and characterization. Not tested on shipped production material.

Electrical Characteristics (continued)

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, unless otherwise specified. All other limits apply to T_A = T_J = +25°C.⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN ⁽²⁾ | TYP ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|------------------------------|--|---|--------------------|--------------------|--------------------|--------|
| TCCGE | Gain temp coefficient ⁽⁵⁾ | T _A = -40°C to +85°C | | | 100 | ppm/°C |
| PSRR | Power supply rejection ratio | DC, 3-V to 3.6-V supply, gain = 1002 V/V | 90 | 110 | | dB |
| PhDly | Phase delay | 1-mV input step signal, Gain = 1002, V _{OUT} measured at V _{DD} /2 | | 9 | | μs |
| TCPHdy | Phase delay variation with temperature ⁽⁶⁾ | 1-mV input step signal, Gain=1002, V _{OUT} measured at V _{DD} /2, T _A = -40°C to +85°C | | | 500 | ns |
| TCVOS | Output offset voltage temperature drift ⁽⁵⁾ | Gain = 167 V/V, T _A = -40°C to +85°C | -0.525 | | 0.525 | mV/°C |
| | | Gain = 335 V/V, T _A = -40°C to +85°C | -0.6 | | 0.6 | |
| | | Gain = 669 V/V, T _A = -40°C to +85°C | -0.9 | | 0.9 | |
| | | Gain = 1335 V/V, T _A = -40°C to +85°C | -1.5 | | 1.5 | |
| | | Gain = 1002 V/V, T _A = -40°C to +85°C | -1.2 | | 1.2 | |
| | | Gain = 2004 V/V, T _A = -40°C to +85°C | -1.9 | | 1.9 | |
| | | Gain = 4003 V/V, T _A = -40°C to +85°C | -3.7 | | 3.7 | |
| | | Gain = 7986V/V, T _A = -40°C to +85°C | -7.1 | | 7.1 | |
| COMMON-MODE GENERATOR | | | | | | |
| VCM | Common-mode voltage | Programmable, see Common-Mode Generation | | 1.15 or 2.59 | | V |
| | VCM accuracy | | | 2% | | |
| CLOAD | CMOut load capacitance | | | 10 | | nF |

(5) TCCGE and TCVOS are calculated by taking the largest slope between -40°C and 25°C linear interpolation and 25°C and 85°C linear interpolation.

(6) TCPHdy is largest change in phase delay between -40°C and 25°C measurements and 25°C and 85°C measurements.

7.6 SPI Interface

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, C_L = 15 pF, unless otherwise specified. All other limits apply to T_A = T_J = +25°C.⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN ⁽²⁾ | TYP ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|----------------------------------|-------------------------------|---------------------------------|--------------------|--------------------|--------------------|------|
| V _{IH} | Logic input high | | 0.7 × VDD | | | V |
| V _{IL} | Logic input low | | | | 0.8 | V |
| V _{OH} | Logic output high | | 2.6 | | | V |
| V _{OL} | Logic output low | | | | 0.4 | V |
| I _{IH} /I _{IL} | Input digital leakage current | | -100 | | 100 | nA |
| | | T _A = -40°C to +85°C | -200 | | 200 | |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

7.7 Timing Characteristics

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, C_L = 15 pF, unless otherwise specified. All other limits apply to T_A = T_J = +25°C.⁽¹⁾

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

Timing Characteristics (continued)

The following specifications apply for $V_{DD} = 3.3\text{ V}$, $V_{CM} = 1.15\text{ V}$, $C_L = 15\text{ pF}$, unless otherwise specified. All other limits apply to $T_A = T_J = +25^\circ\text{C}$.⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN ⁽²⁾ | TYP ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|------------|--|--------------------|--------------------|--------------------|------|
| t_{WU} | Wake-up time | | 1 | | ms |
| f_{SCLK} | Serial clock frequency | | | 10 | MHz |
| t_{PH} | SCLK pulse width high | $0.4 / f_{SCLK}$ | | | ns |
| t_{PL} | SCLK pulse width low | $0.4 / f_{SCLK}$ | | | ns |
| t_{CSS} | CSB set-up time | 10 | | | ns |
| t_{CSH} | CSB hold time | 10 | | | ns |
| t_{SU} | SDI set-up time prior to rise edge of SCLK | 10 | | | ns |
| t_{SH} | SDI hold time prior to rise edge of SCLK | 10 | | | ns |
| t_{DOD1} | SDO disable time after rise edge of CSB | | | 45 | ns |
| t_{DOD2} | SDO disable time after 16 th rise edge of SCLK | | | 45 | ns |
| t_{DOE} | SDO enable time from the fall edge of 8 th SCLK | | | 35 | ns |
| t_{DOA} | SDO access time after the fall edge of SCLK | | | 35 | ns |
| t_{DOH} | SDO hold time after the fall edge of SCLK | 5 | | | ns |
| t_{DOR} | SDO rise time | | 5 | | ns |
| t_{DOF} | SDO fall time | | 5 | | ns |

- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

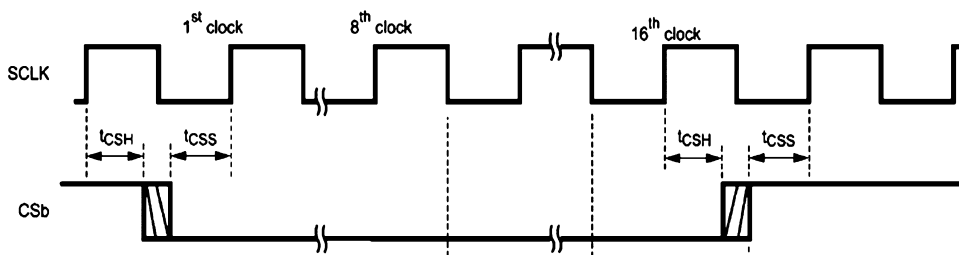


Figure 1. SPI Timing Diagram

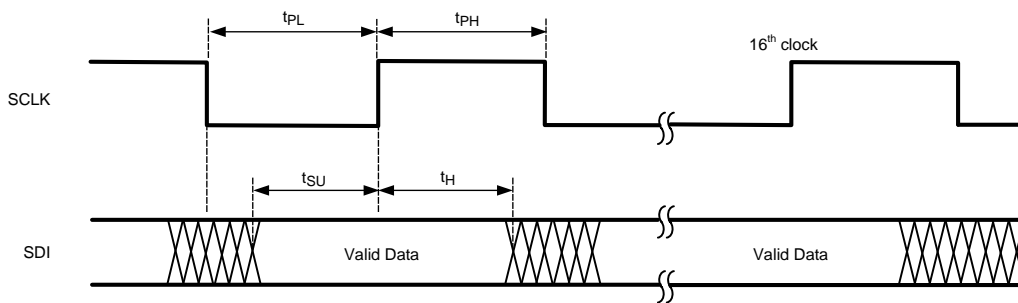
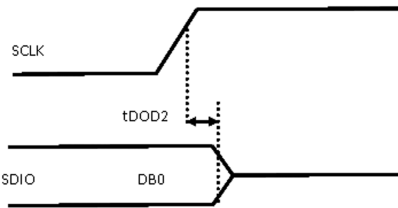
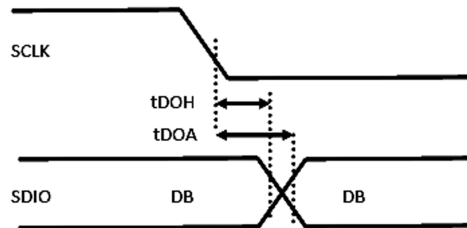
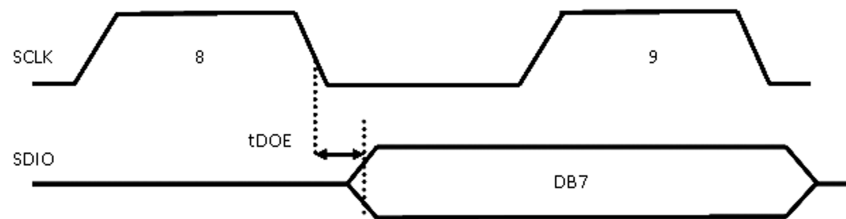
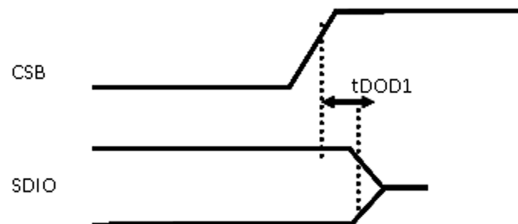
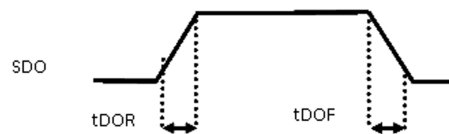


Figure 2. SPI Set-Up Hold Time


Figure 3. SDO Disable Time After 16th Rise Edge of SCLK

Figure 4. SDO Access Time (t_{DOA}) and SDO Hold Time (t_{DOH}) After the Fall Edge of SCLK

Figure 5. SDO Enable Time from the Fall Edge of 8th SCLK

Figure 6. SDO Disable Time after Rise Edge of CSB

Figure 7. SDO Rise and Fall Times

7.8 Typical Characteristics

VDD = +3.3 V, VCM = 1.15 V, and T_A = 25°C unless otherwise noted

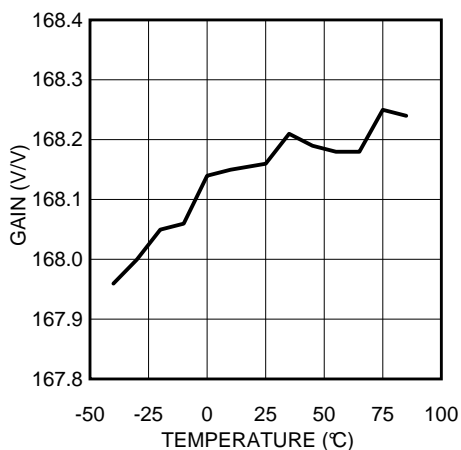


Figure 8. Gain = 167 V/V vs. Temperature

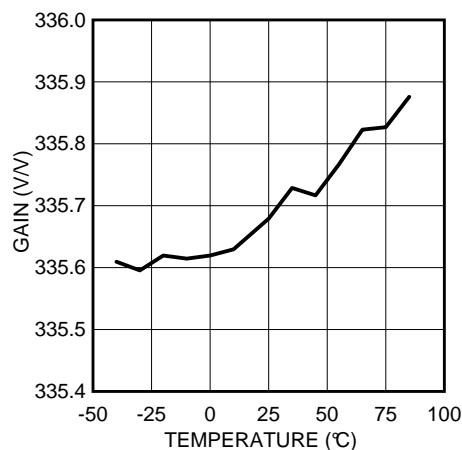


Figure 9. Gain = 335 V/V vs. Temperature

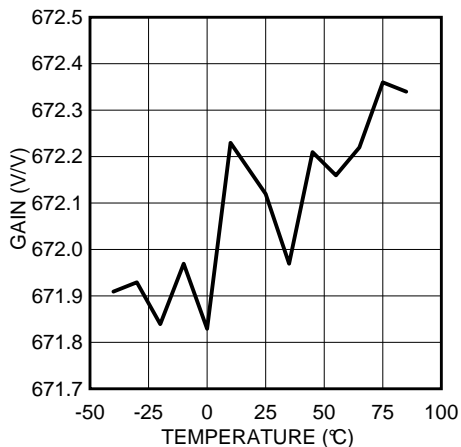


Figure 10. Gain = 669 V/V vs. Temperature

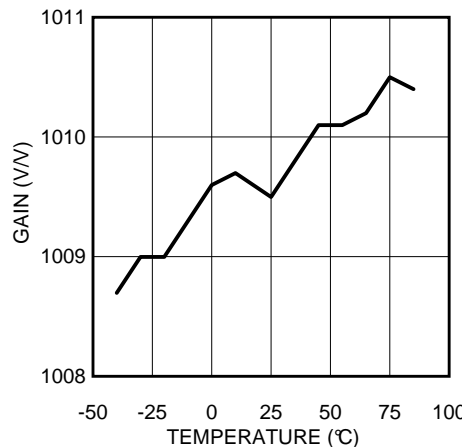


Figure 11. Gain = 1002 V/V vs. Temperature

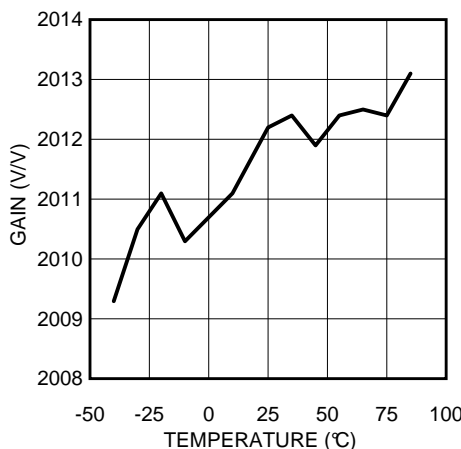


Figure 12. Gain = 2004 V/V vs. Temperature

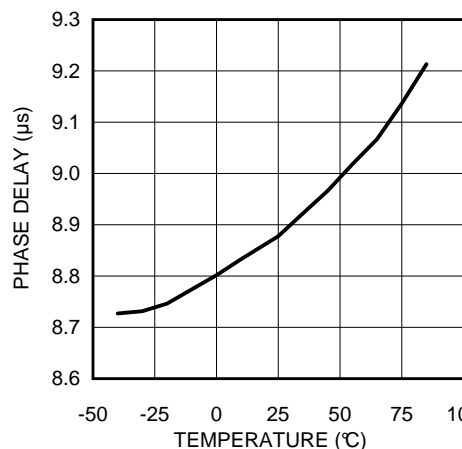
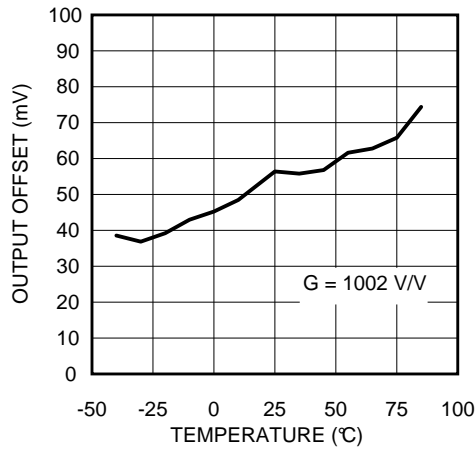
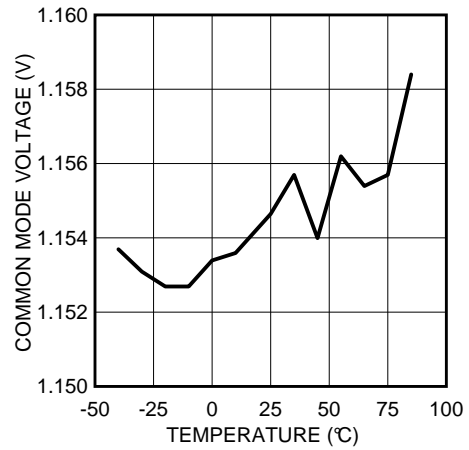
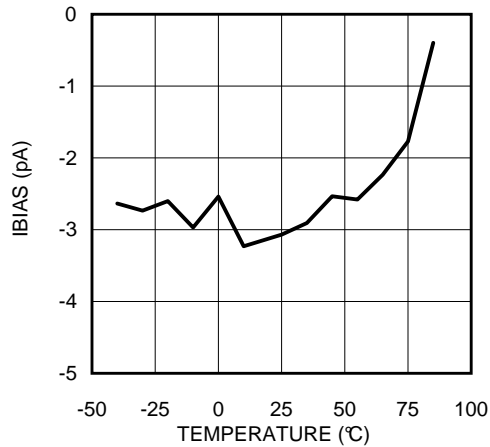
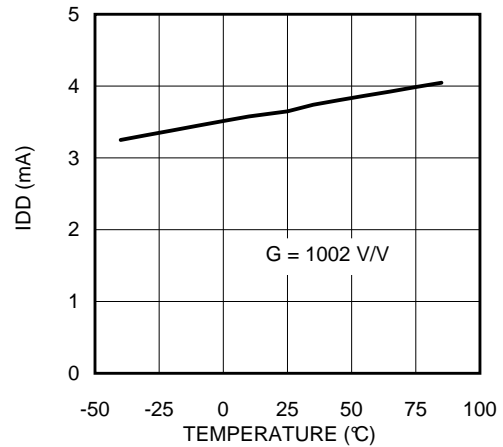
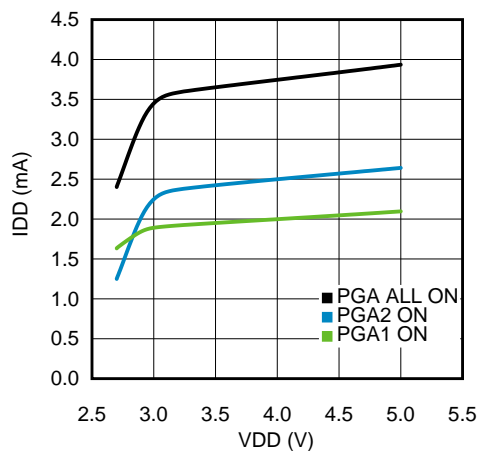
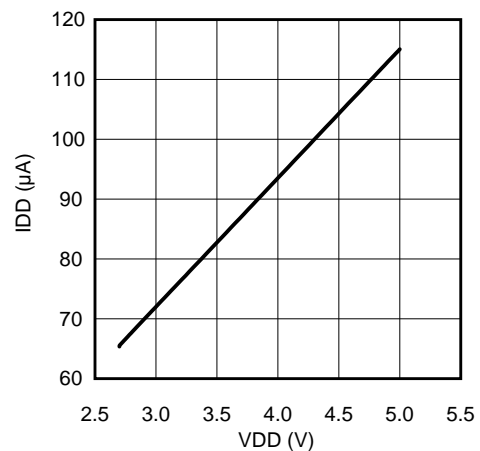


Figure 13. Phase Delay vs. Temperature

Typical Characteristics (continued)

 VDD = +3.3 V, VCM = 1.15 V, and T_A = 25°C unless otherwise noted

Figure 14. Output Offset vs. Temperature

Figure 15. Common-Mode Voltage vs. Temperature

Figure 16. Input Bias Current vs. Temperature

Figure 17. Supply Current vs. Temperature

Figure 18. Supply Current vs. Supply Voltage

Figure 19. Power-Down Supply Current vs. Supply Voltage

Typical Characteristics (continued)

VDD = +3.3 V, VCM = 1.15 V, and T_A = 25°C unless otherwise noted

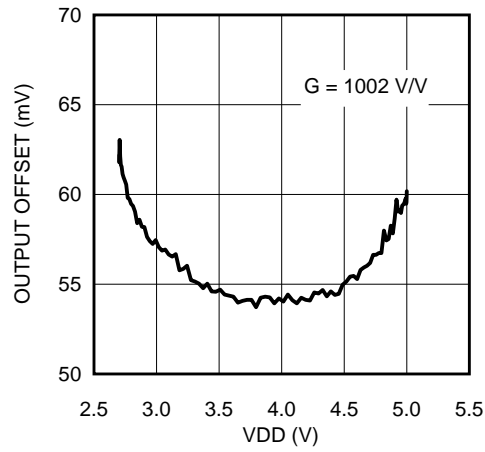


Figure 20. Output Offset vs. Supply Voltage

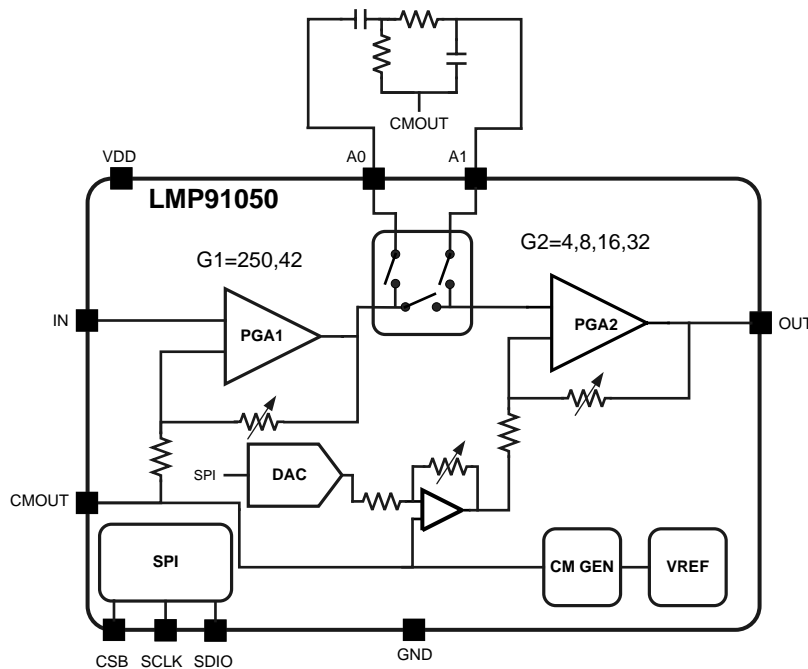
8 Detailed Description

8.1 Overview

The input channel of the LMP91050 features two programmable gain stages that give the user flexibility in optimizing the system gain. Access to the inter-stage connection between the gain blocks also allows the inclusion of appropriate filtering if needed. The internal DAC allows the DC offset of the output voltage to be adjusted independently of the common-mode voltage supplied to the sensor, enabling the sampled signal to be centered within the ADC full-scale input range.

The following paragraphs discuss the LMP91050’s features in more detail.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Programmable Gain Amplifier

The LMP91050 offers two programmable gain modes (low or high) with four programmable gain settings each. The purpose of the gain mode is to enable thermopiles with larger dark voltage levels. All gain settings are accessible through bits GAIN1 and GAIN2[1:0]. The low-gain mode has a range of 167 V/V to 1335 V/V while the high-gain mode has a range of 1002 V/V to 7986 V/V. The PGA is referenced to the internally generated VCM. Input signal, referenced to this VCM voltage, should be within ± 2 mV (see VINMAX_HGM specification) in high-gain mode. In the low gain mode the first stage will provide a gain of 42 V/V instead of 250 V/V, thus allowing a larger maximum input signal up to ± 12 mV (VINMAX_LGM).

Table 1. Gain Modes

| BIT SYMBOL | GAIN |
|------------|------------------|
| GAIN1 | 0: 250 (default) |
| | 1: 42 |

Feature Description (continued)

Table 1. Gain Modes (continued)

| BIT SYMBOL | GAIN |
|-------------|-----------------|
| GAIN2 [1:0] | 00: 4 (default) |
| | 01: 8 |
| | 10: 16 |
| | 11: 32 |

8.3.2 External Filter

The LMP91050 offers two different measurement modes selectable through EXT_FILT bit. EXT_FILT bit is present in the Device configuration register and is programmable through SPI.

Table 2. Measurement Modes

| BIT SYMBOL | MEASUREMENT MODE |
|------------|---|
| EXT_FILT | 0: The signal from the thermopile is being processed by the internal PGAs, without additional external decoupling or filtering (default). |
| | 1: The signal from the thermopile is being processed by the first internal PGA and fed to the A0 pin. An external low pass, high pass or band pass filter can be connected through pins A0, A1. |

An external filter can be applied when EXT_FILT = 1. A typical band pass filter is shown in the picture below. Resistor and capacitor can be connected to the CMOUT pin of the LMP91050 as shown. Discrete component values have been added for reference.

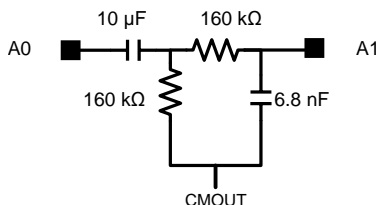


Figure 21. Typical Bandpass Filter

8.3.3 Offset Adjust

Procedure of the offset adjust is to first measure the *dark signal*, program the DAC to adjust, and then measure in a second cycle the residual of the dark signal for further signal manipulation within the µC. The signal source is expected to have an offset component (dark signal) larger than the actual signal. During the *dark phase*, the time when no light is detected by the sensor, the µC can program LMP91050 internal DAC to compensate for a measured offset. A low output offset voltage temperature drift (TCVOS) ensures system accuracy over temperature. See Figure 22 below which plots the maximum TCVOS allowed over a given temperature drift in order to achieve n bit system accuracy.

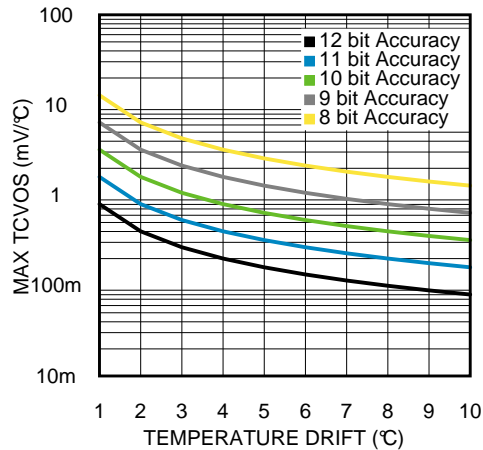


Figure 22. System Accuracy vs. TCVOS and Temperature Drift

8.3.4 Common-Mode Generation

As the offset of the sensor is bipolar, there is a need to supply a VCM to the sensor. This can be programmed as 1.15 V or 2.59 V (approximately mid rail of 3.3-V or 5-V supply). TI does not recommend to use 2.59-V VCM with a 3.3-V supply

8.3.5 CSB

Chip Select is a active-low signal. CSB needs to be asserted throughout a transaction. That is, CSB should not pulse between the Instruction Byte and the Data Byte of a single transaction.

NOTE

CSB de-assertion always terminates an on-going transaction, if it is not already complete. Likewise, CSB assertion will always bring the device into a state, ready for next transaction, regardless of the termination status of a previous transaction.

CSB may be permanently tied low for a 2-wire SPI communication protocol.

8.3.5.1 SCLK

SCLK can idle High or Low for a write transaction. However, for a READ transaction, SCLK must idle high. SCLK features a Schmitt-triggered input and although it has hysteresis, TI recommends to keep SCLK as clean as possible to prevent glitches from inadvertently spoiling the SPI frame.

8.4 Device Functional Modes

To read the registers of the LMP91050, the SDIO mode enable register must be written using a special sequence, as described in the *SDIO Mode* section. During the reading process, the analog OUT pin is still active, as normal. There are no other special modes for the device.

8.5 Programming

8.5.1 SPI Interface

An SPI interface is available in order to program the device parameters like PGA gain of two stages, enabling external filter, enabling power for PGAs, offset adjust and common-mode (VCM) voltage.

8.5.1.1 Interface Pins

The Serial Interface consists of SDIO (Serial Data Input / Output), SCLK (Serial Interface Clock) and CSB (Chip Select Bar). The serial interface is write-only by default. Read operations are supported after unlocking the SDIO_MODE_PASSWD. This is discussed in detail later in the document.

Programming (continued)

8.5.1.2 Communication Protocol

Communication on the SPI normally involves Write and Read transactions. Write transaction consists of single Write Command Byte, followed by single Data byte. The following figure shows the SPI Interface Protocol for write transaction.

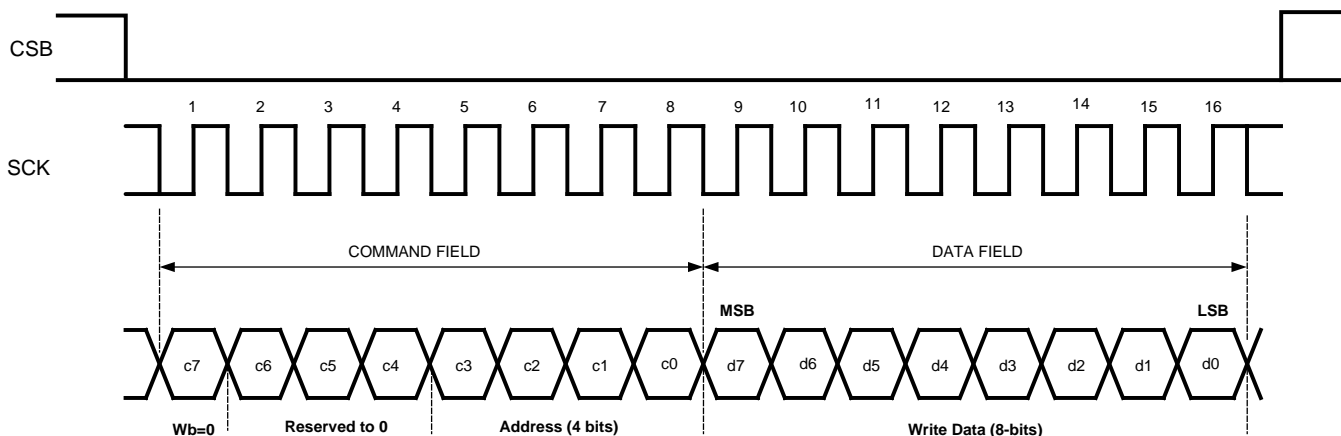
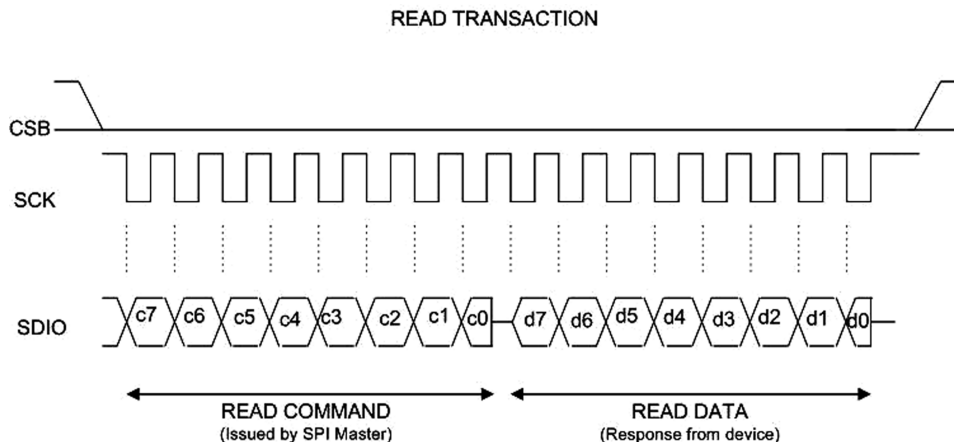


Figure 23. SPI Interface Protocol

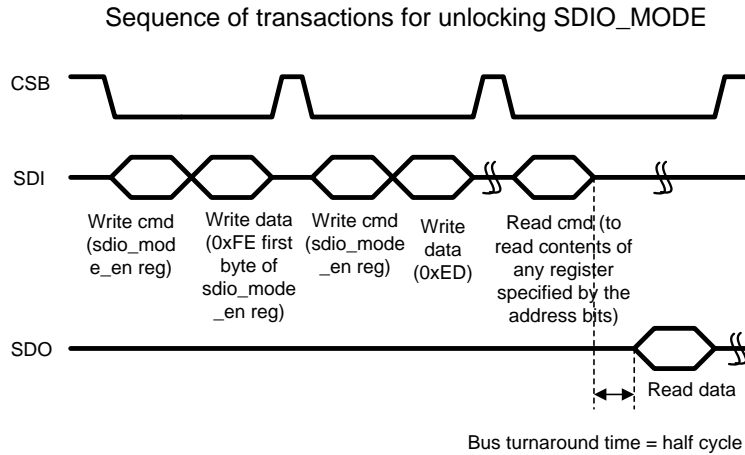
For Read transactions, user first needs to write into a SDIO mode enable register for enabling the SPI read mode. Once the device is enabled for Reading, the data is driven out on the SDIO pin during the Data field of the Read Transaction. SDIO pin is designed as a bidirectional pin for this purpose. Figure 24 shows the Read transaction. The sequence of commands that need to be issued by the SPI Master to enable SPI read mode is shown in Figure 25.



Note: Read command is issued by the SPI Master, who after issuing the c0 (LSBit of the command byte) bit should relinquish the data line (high-Z) after meeting the hold timing(10ns) and stop SCK idling high.

Figure 24. Read Transaction

Programming (continued)



Note:

1. Once the SDIO_mode is unlocked. The user can read as many registers as long as nothing else is written to sdio_mode_en register to disturb the state of SDIO_mode
2. The separate signals SDI and SDO are given in the figure for the sake of understanding. However, only one signal SDIO exists in the design

Figure 25. Enable SDIO Mode for Reading SPI Registers

8.5.1.3 Registers Organization

Configuring the device is achieved using Write of the designated registers in the device. All the registers are organized into individually addressable byte-long registers that have a unique address. The format of the Write/Read instruction is as shown below.

Table 3. Write / Read Instruction Format

| Bit[7] | Bit[6:4] | Bit[3:0] |
|-----------------------|---------------|----------|
| 0 : Write Instruction | Reserved to 0 | Address |
| 1 : Read Instruction | | |

8.6 Register Maps

This section describes the programmable registers and the associated programming sequence, if any, for the device. Table 4 shows the summary listing of all the registers that are available to the user and their power-up values.

Table 4. Register Descriptions

| Title | Address (Hex) | Type | Power-up/Reset Value (Hex) |
|----------------------|---------------|-----------------------------|----------------------------|
| Device Configuration | 0x0 | Read-Write | 0x0 |
| | | (Read allowed in SDIO Mode) | |
| DAC Configuration | 0x1 | Read-Write | 0x80 |
| | | (Read allowed in SDIO Mode) | |
| SDIO Mode Enable | 0xF | Write-only | 0x0 |

8.6.1 Device Configuration

Table 5. Device Configuration Register (Address 0x0)

| Bit | Bit Symbol | Description |
|-------|------------|--|
| 7 | RESERVED | Reserved to 0. |
| [6:5] | EN | 00: PGA1 OFF PGA2 OFF (default) 01: PGA1 OFF, PGA2 ON 10: PGA1 ON, PGA2 OFF 11: PGA1 ON, PGA2 ON |
| 4 | EXT_FILT | 0: PGA1 to PGA2 direct (default) 1: PGA1 to PGA2 via external filter |
| 3 | CMN_MODE | 0 : 1.15V (default) 1 : 2.59V |
| [2:1] | GAIN2 | 00: 4 (default) 01: 8 10: 16 11: 32 |
| 0 | GAIN1 | 0: 250 (default) 1: 42 |

8.6.2 DAC Configuration

The output DC level will shift according to the formula $V_{out_shift} = -33.8mV * (NDAC - 128)$.

Table 6. DAC Configuration Register (Address 0x1)

| Bit | Bit Symbol | Description |
|-------|------------|--|
| [7:0] | NDAC | 128 (0x80): $V_{out_shift} = -33.8mV * (128 - 128) = 0mV$ (default) |

8.6.3 SDIO Mode

Write-only

Table 7. SDIO Mode Enable Register (Address 0xf)

| Bit | Bit Symbol | Description |
|-------|--------------|---|
| [7:0] | SDIO_MODE_EN | To enter SDIO Mode, write the successive sequence 0xFE and 0xED. Write anything other than this sequence to get out of mode. |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 26 shows a typical NDIR sensing circuit with a bandpass filter with a high frequency cutoff of approximately 100 Hz. The lowpass filter at the output has a cutoff of approximately 110 Hz.

9.2 Typical Application

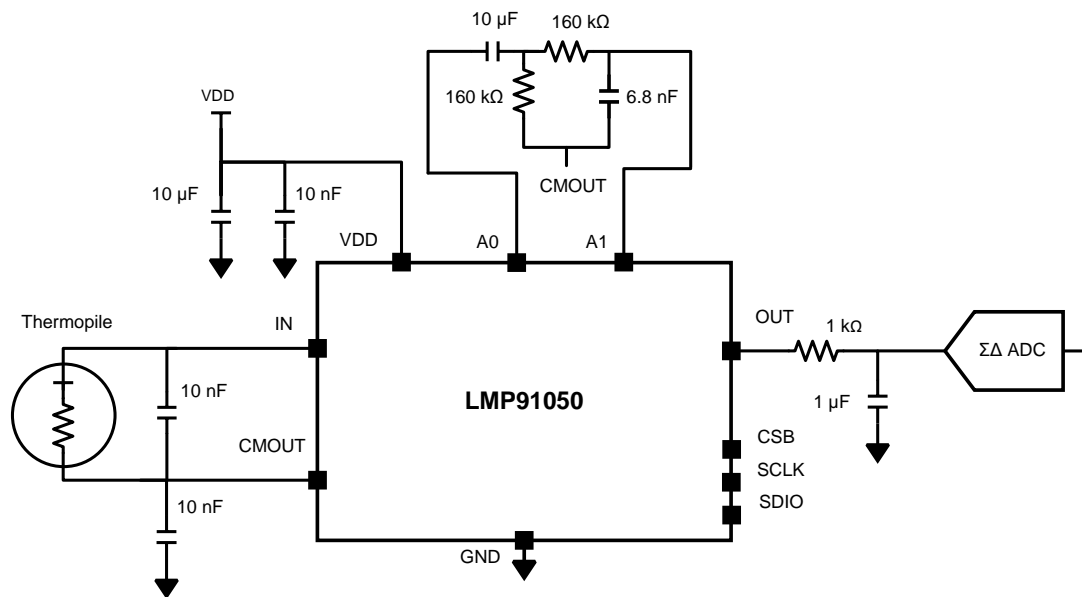


Figure 26. Typical NDIR Sensing Application Circuit

9.2.1 Design Requirements

The design requirements for using the LMP91050 in an application basically include the following:

- Determine the characteristics of the thermopile and the appropriate gain and common mode voltage that will maximize the dynamic range of the sensor. Consult the manufacturer's data sheet.
- Selecting an analog-to-digital converter that supports the needed resolution and update rate.
- Determining the bandwidth of the inter-stage low-pass filter to limit the noise imposed on the signal
- An SPI interface to a microcontroller or other logic device is required in order to configure the LMP91050.

9.2.2 Detailed Design Procedure

The basic design procedure is as follows:

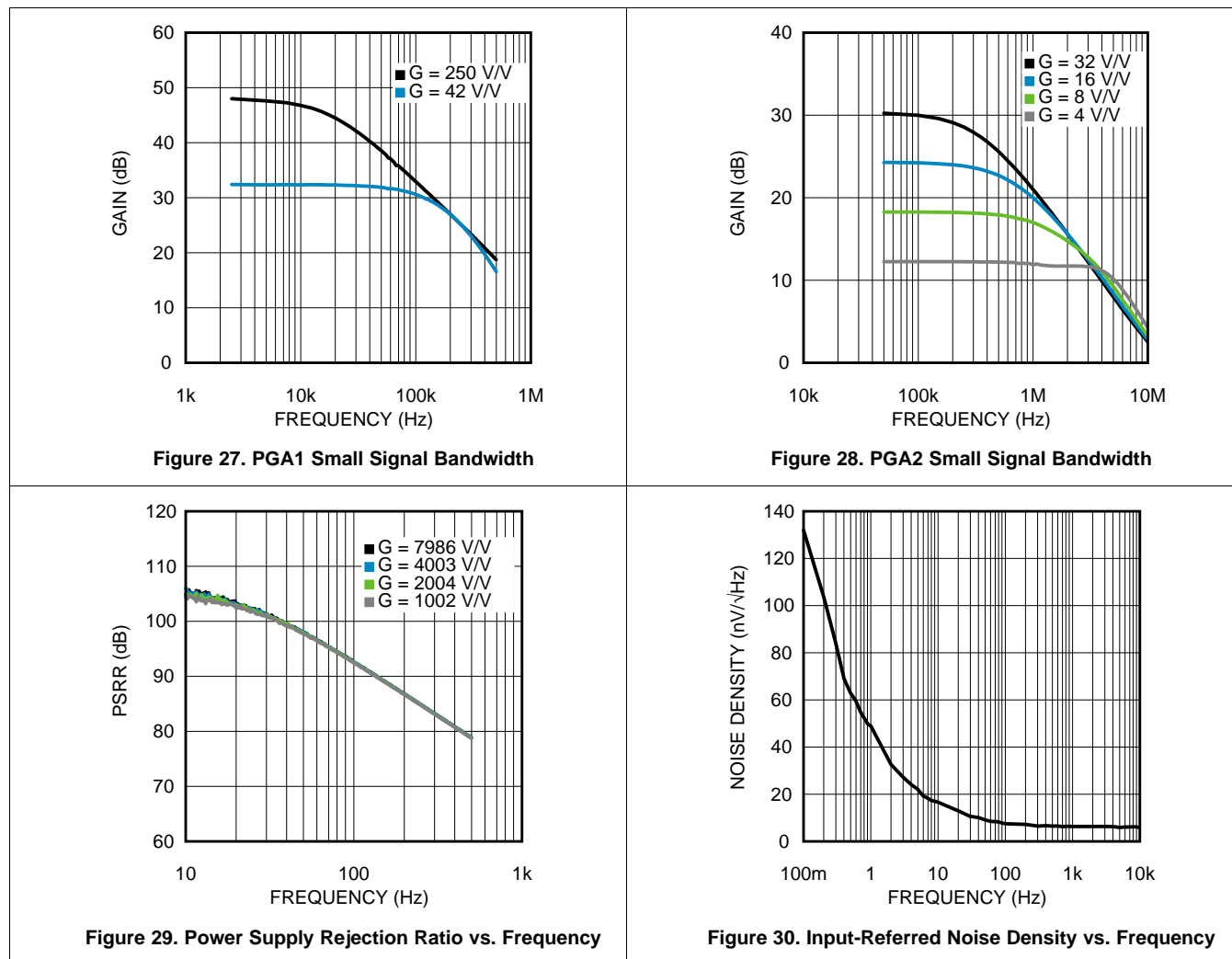
- Select the appropriate inter-stage bandpass filter bandwidth. Note that the common mode voltage (CMOUT) is connected to both the thermopile and the bandpass filter, as shown in Figure 26.
- TI recommends that a lowpass filter be inserted between the OUT pin and the input to the ADC, to further reduce noise on the signal and prevent aliasing.
- Power supply bypassing as shown in figure 32 is recommended.
- Based on the thermopile characteristics, select the common-mode voltage and gain to be programmed into the LMP91050. CMOU should be selected to center the expected dynamic range of the thermopile within the full scale range of the ADC to the best extent possible. The gain should be selected to maximize the

Typical Application (continued)

signal range at the ADC input, but should allow some headroom below full scale to prevent clipping. The gain should also compensate, if possible, for any loss due to the filters in the signal path.

- The internal DAC can be programmed to further optimize the signal range on the OUT pin. See [Offset Adjust](#) for further information.

9.2.3 Application Curves



Typical Application (continued)

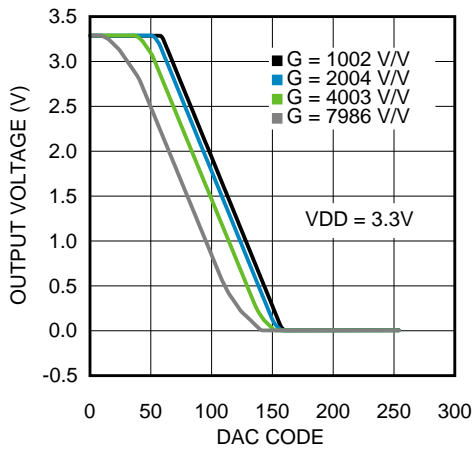


Figure 31. DAC DC Sweep With VDD = 3.3 V

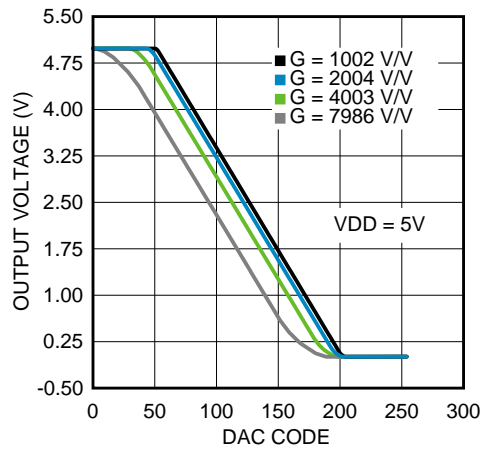


Figure 32. DAC DC Sweep With VDD = 5 V

10 Power Supply Recommendations

Because the LMP91050 is used in a sampled data system, care must be taken to maintain power supply noise below an acceptable level, which will depend on the requirements of the application. In all cases, follow the manufacturer's design recommendations for the power conditioning device used in the system. The LMP91050 offers excellent power supply rejection over a wide range of frequencies, but adequate power supply bypassing should always be used (see Figure 26). If using a switching supply, additional filtering may be required particularly if the switcher harmonics fall within the passband of the filters used in the system. Ensure that the selected power conditioning device is capable of sourcing the current required by the LMP91050.

11 Layout

11.1 Layout Guidelines

Figure 33 shows a layout example for the LMP91050. All components should be placed as close as possible to the device, especially the bypass capacitors to VDD (CBypass1 and CBypass2).

11.2 Layout Example

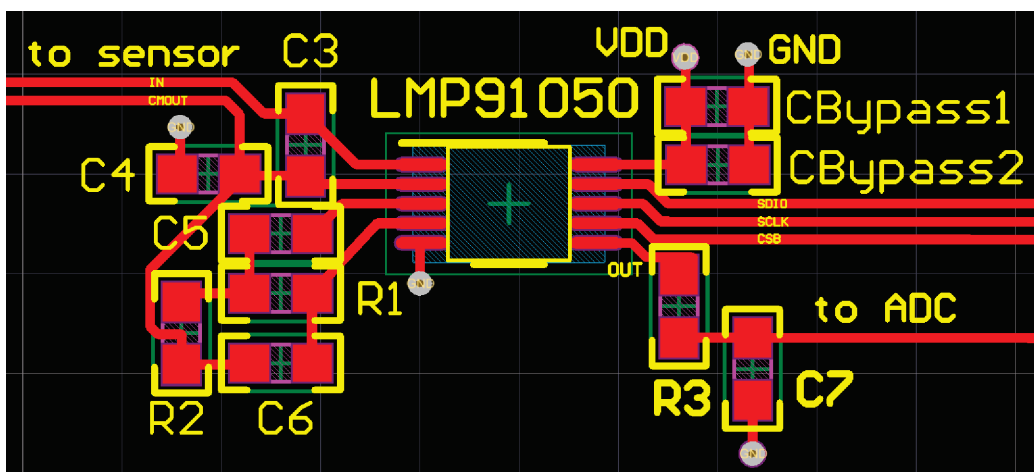


Figure 33. LMP91050 Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMP91050MM/NOPB | ACTIVE | VSSOP | DGS | 10 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 105 | AN8A | Samples |
| LMP91050MME/NOPB | ACTIVE | VSSOP | DGS | 10 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 105 | AN8A | Samples |
| LMP91050MMX/NOPB | ACTIVE | VSSOP | DGS | 10 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 105 | AN8A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP91050MM/NOPB | VSSOP | DGS | 10 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP91050MME/NOPB | VSSOP | DGS | 10 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP91050MMX/NOPB | VSSOP | DGS | 10 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP91050MM/NOPB | VSSOP | DGS | 10 | 1000 | 210.0 | 185.0 | 35.0 |
| LMP91050MME/NOPB | VSSOP | DGS | 10 | 250 | 210.0 | 185.0 | 35.0 |
| LMP91050MMX/NOPB | VSSOP | DGS | 10 | 3500 | 367.0 | 367.0 | 35.0 |

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

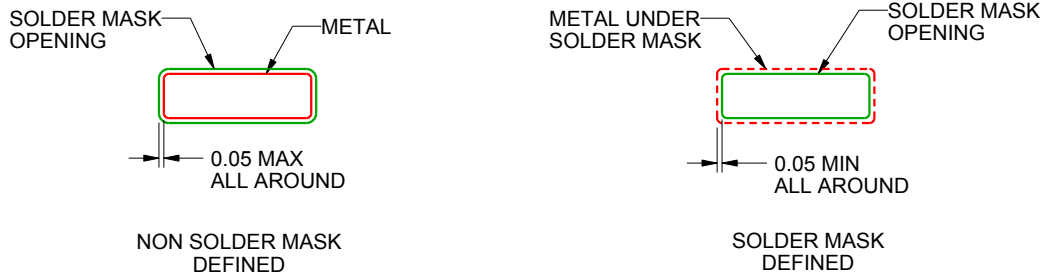
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management