THE DATASHEET OF

LMR24210TL/NOPB

LMR24210 42-V_{IN}, 1-A Step-Down Voltage Regulator in DSBGA Package

1 Features

- Input Voltage Range of 4.5 V to 42 V
- Output Voltage Range of 0.8 V to 24 V
- Output Current up to 1 A
- Integrated low $R_{DS(ON)}$ Synchronous MOSFETs for High Efficiency
- Up to 1 MHz Switching Frequency
- Low Shutdown I_Q, 25 µA Typical
- Programmable Soft Start
- No Loop Compensation Required
- COT With ERM Architecture
- Tiny Overall Solution Reduces System Cost
- Integrated Synchronous MOSFETs Provides High Efficiency at Low Output Voltages
- Stable with Low ESR Capacitors
- 28-Bump DSBGA Packaging
- Create a custom design using the LMR24010 with the WEBENCH® Power Designer

2 Applications

- Point-of-Load Conversions from 5V, 12V and 24V Rails
- Space Constrained Applications
- Industrial Distributed Power Applications
- Power Meters

3 Description

The LMR24210 synchronously rectified buck converter features all required functions to implement a highly efficient and cost effective buck regulator. It is capable of supplying 1 A to loads with an output voltage as low as 0.8 V. Dual N-channel synchronous MOSFET switches allow a low component count, thus reducing complexity and minimizing board size.

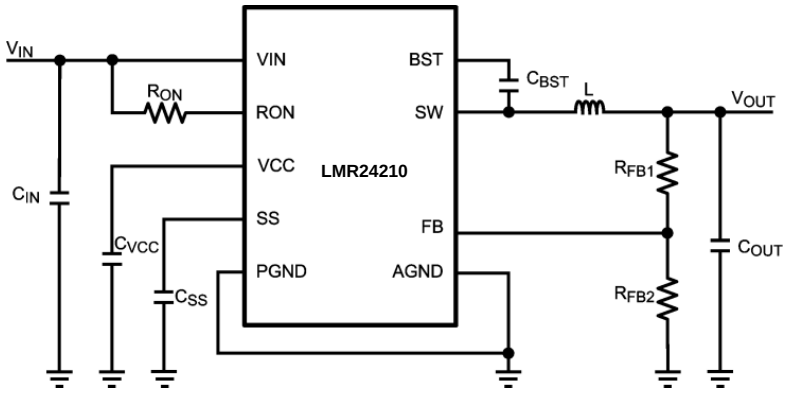
Different from most other COT regulators, the LMR24210 does not rely on output capacitor ESR for stability, and is designed to work exceptionally well with ceramic and other very low ESR output capacitors. It requires no loop compensation, results in a fast load transient response and simple circuit implementation. The operating frequency remains nearly constant with line variations due to the inverse relationship between the input voltage and the on-time. The operating frequency can be externally programmed up to 1 MHz. Protection features include V_{CC} under-voltage lock-out, output overvoltage protection, thermal shutdown, and gate-drive undervoltage lockout. The LMR24210 is available in the small DSBGA low profile chip-scale package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LMR24010	DSBGA (28)	3.676 mm × 2.48 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

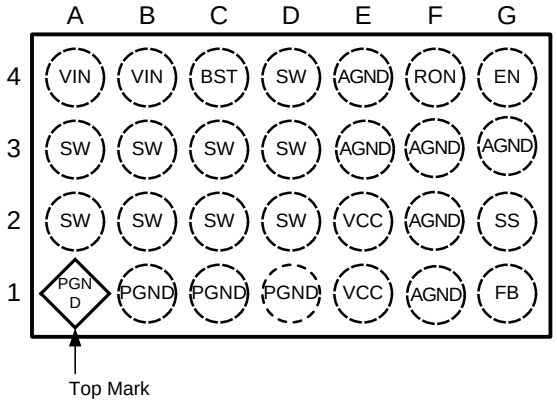
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2013) to Revision H	Page
• Editorial changes only; add WEBENCH links	1

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Semiconductor data sheet to TI format	1

5 Pin Configuration and Functions

YPA Package
28-Bump DSGBA
Top View



Pin Descriptions

PIN		DESCRIPTION	
NO.	NAME		
A2, A3, B2, B3, C2, C3, D2, D3, D4	SW	Switching node	Internally connected to the source of the main MOSFET and the drain of the Synchronous MOSFET. Connect to the inductor.
A4, B4	VIN	Input supply voltage	Supply pin to the device. Nominal input range is 4.5 V to 42 V.
C4	BST	Connection for bootstrap capacitor	Connect a 33-nF capacitor from the SW pin to this pin. An internal diode charges the capacitor during the main MOSFET off-time.
E3, E4, F1, F2, F3, G3	AGND	Analog ground	Ground for all internal circuitry other than the PGND pin.
G2	SS	Soft start	An 8-µA internal current source charges an external capacitor to provide the soft- start function.
G1	FB	Feedback	Internally connected to the regulation and over-voltage comparators. The regulation setting is 0.8V at this pin. Connect to feedback resistors.
G4	EN	Enable	Connect a voltage higher than 1.26V to enable the regulator. Leaving this input open circuit enables the device at internal UVLO level.
F4	RON	On-time control	An external resistor from the VIN pin to this pin sets the main MOSFET on-time.
E1, E2	VCC	Start-up regulator output	Nominally regulated to 6 V. Connect a capacitor of not less than 680 nF between the VCC and AGND pins for stable operation.
A1, B1, C1, D1	PGND	Power ground	Synchronous MOSFET source connection. Tie to a ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

See notes(1)(2)

VIN, RON to AGND	-0.3V to 43.5V
SW to AGND	-0.3V to 43.5V
SW to AGND (Transient)	-2V (< 100ns)
VIN to SW	-0.3V to 43.5V
BST to SW	-0.3V to 7V
All Other Inputs to AGND	-0.3V to 7V
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T_J)	150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

See note(1)

Supply Voltage Range (VIN)	4.5V to 42V
Junction Temperature Range (T_J)	−40°C to +125°C
Thermal Resistance (θ_{JA}) 28-ball DSBGA(2)	50°C/W
For soldering specifications see SNOA549	

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see *Electrical Characteristics* .
(2) θ_{JA} calculations were performed in general accordance with JEDEC standards JESD51–1 to JESD51–11.

6.4 Electrical Characteristics

Specifications with standard type are for T_J = 25°C only; limits in **boldface type** apply over the full operating junction temperature (T_J) range. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18V, V_{OUT} = 3.3 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
START-UP REGULATOR, V_{CC}						
V_{CC}	V_{CC} output voltage	C_{CC} = 680nF, no load	**5.0**	6.0	**7.2**	V
V_{IN} - V_{CC}	V_{IN} - V_{CC} dropout voltage	I_{CC} = 20mA		350		mV
I_{VCCL}	V_{CC} current limit (2)	V_{CC} = 0V	**40**	65		mA
$V_{CC-UVLO}$	V_{CC} under-voltage lockout threshold (UVLO)	V_{IN} increasing	**3.55**	3.75	**3.95**	V
$V_{CC-UVLO-HYS}$	V_{CC} UVLO hysteresis	V_{IN} decreasing – DSBGA package		150		mV
$t_{VCC-UVLO-D}$	V_{CC} UVLO filter delay			3		µs
I_{IN}	I_{IN} operating current	No switching, V_{FB} = 1V		0.7	**1**	mA
I_{IN-SD}	I_{IN} operating current, Device shutdown	V_{EN} = 0V		25	**40**	µA
SWITCHING CHARACTERISTICS						
$R_{DS-UP-ON}$	Main MOSFET $R_{DS(on)}$			0.18	**0.375**	Ω
$R_{DS-DN-ON}$	Syn. MOSFET $R_{DS(on)}$			0.11	**0.225**	Ω
V_{G-UVLO}	Gate drive voltage UVLO	V_{BST} - V_{SW} increasing		3.3	**4**	V
SOFT START						
I_{SS}	SS pin source current	V_{SS} = 0.5V		11		µA
CURRENT LIMIT						
I_{CL}	Syn. MOSFET current limit threshold	LMR24210	**1.2**	1.8	**2.6**	A
ON/OFF TIMER						
t_{on}	ON timer pulse width	V_{IN} = 10V, R_{ON} = 100 kΩ		1.38		µs
		V_{IN} = 30V, R_{ON} = 100 kΩ		0.47		
t_{on-MIN}	ON timer minimum pulse width			150		ns
t_{off}	OFF timer pulse width			260		ns
ENABLE INPUT						
V_{EN}	EN Pin input threshold	V_{EN} rising	**1.13**	1.18	**1.23**	V
V_{EN-HYS}	Enable threshold hysteresis	V_{EN} falling		90		mV
REGULATION AND OVERVOLTAGE COMPARATOR						
V_{FB}	In-regulation feedback voltage	V_{SS} ≥ 0.8V T_J = −40°C to +125°C	**0.784**	0.8	**0.816**	V
V_{FB-OV}	Feedback overvoltage threshold		**0.888**	0.920	**0.945**	V
I_{FB}	FB pin current			5		nA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	T_J rising		165		°C
T_{SD-HYS}	Thermal shutdown temperature hysteresis	T_J falling		20		°C

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

6.5 Typical Characteristics

Unless otherwise specified all curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V (Figure 26) T_A = 25°C.

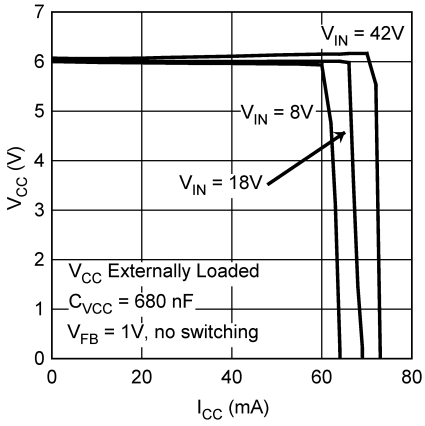


Figure 1. V_{CC} vs I_{CC}

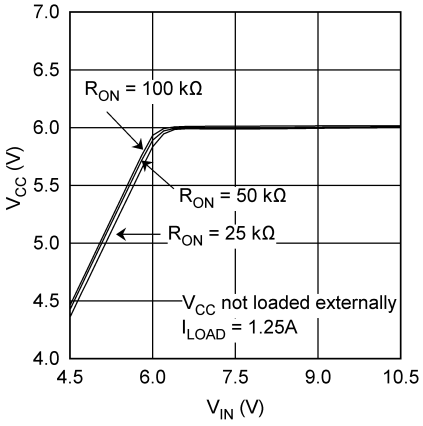


Figure 2. V_{CC} vs V_{IN}

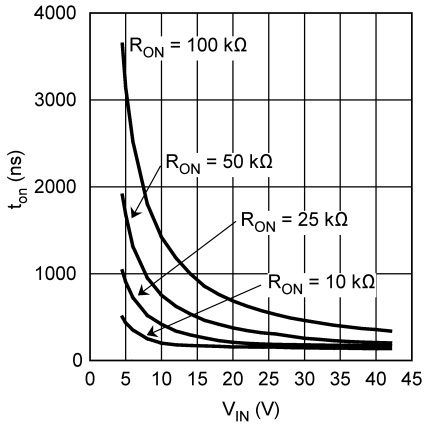


Figure 3. T_{on} vs V_{IN}

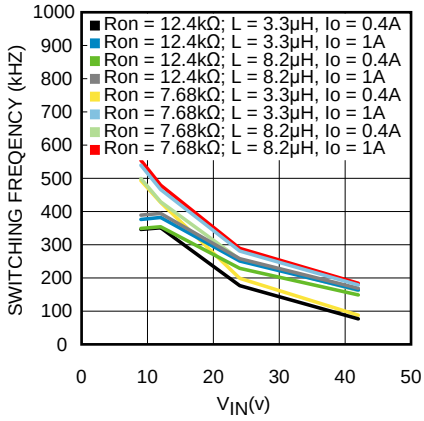


Figure 4. Switching Frequency, F_{SW} vs V_{IN}, V_{OUT}=0.8v,

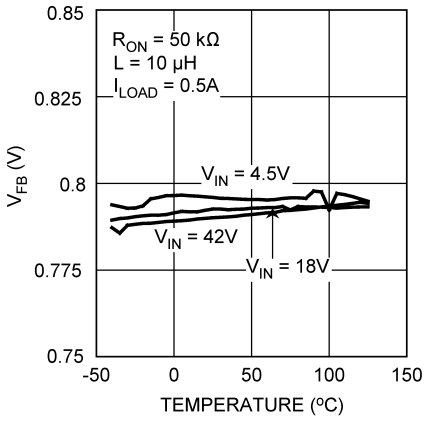


Figure 5. V_{FB} vs Temperature

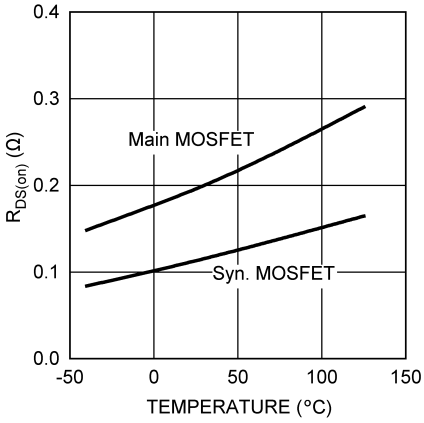
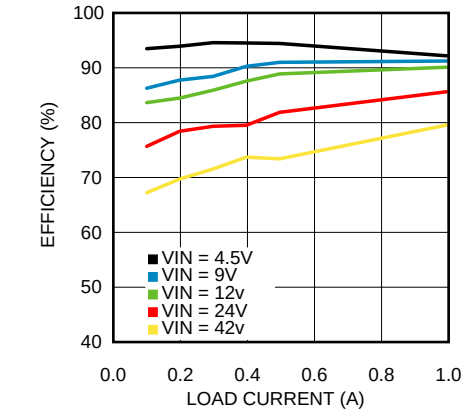


Figure 6. $R_{DS(on)}$ vs Temperature

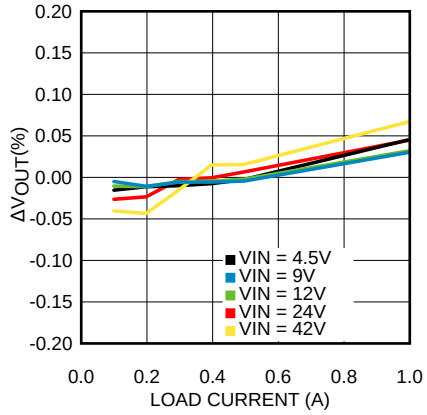
Typical Characteristics (continued)

Unless otherwise specified all curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V (Figure 26) T_A = 25°C.



V_{OUT} = 3.3 V

Figure 7. Efficiency vs Load Current



V_{OUT} = 3.3 V

Figure 8. V_{OUT} Regulation vs Load Current

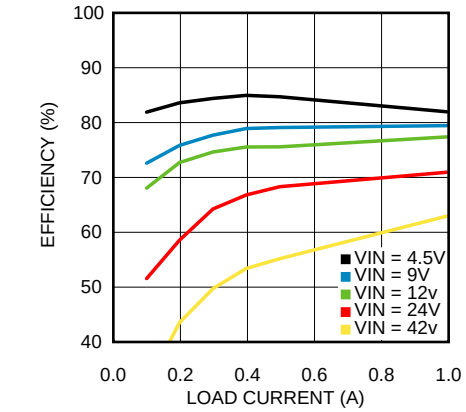
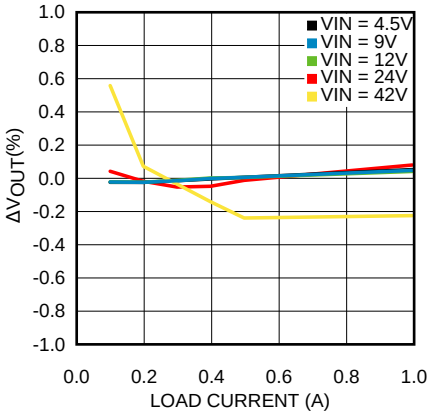
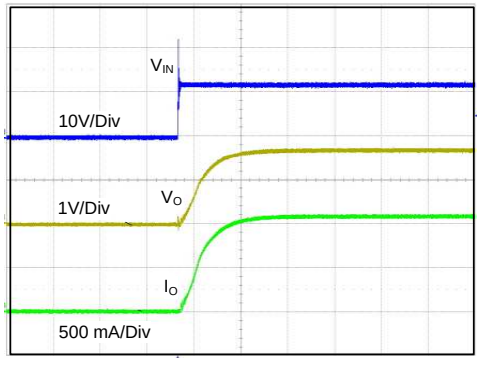


Figure 9. Efficiency vs Load Current (V_{OUT} = 0.8v)



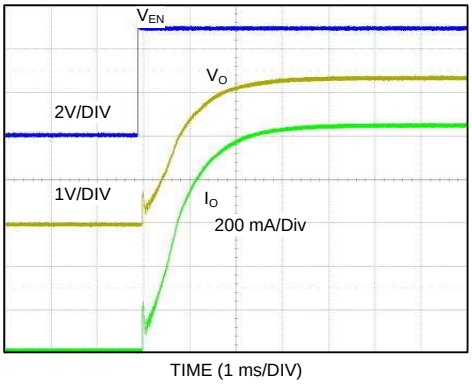
V_{OUT} = 0.8 V

Figure 10. V_{OUT} Regulation vs Load Current



V_{OUT} = 3.3 V, 1-A Loaded

Figure 11. Power Up

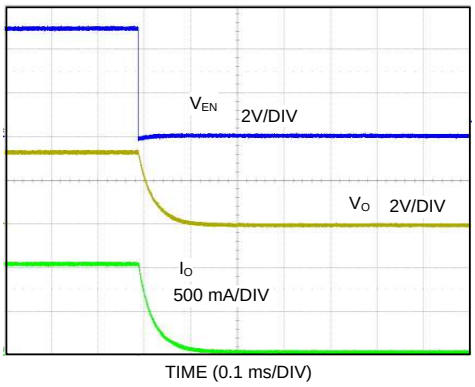


V_{OUT} = 3.3 V, 1-A Loaded

Figure 12. Enable Transient

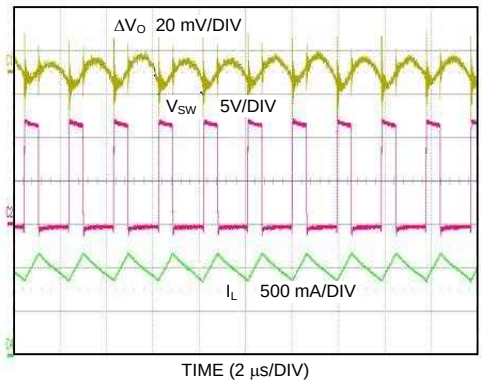
Typical Characteristics (continued)

Unless otherwise specified all curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V (Figure 26) T_A = 25°C.



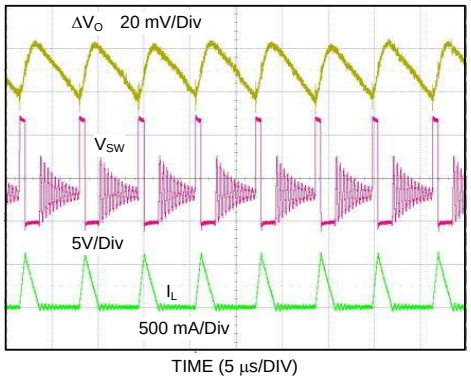
V_{OUT} = 3.3 V, 1 A Loaded

Figure 13. Shutdown Transient



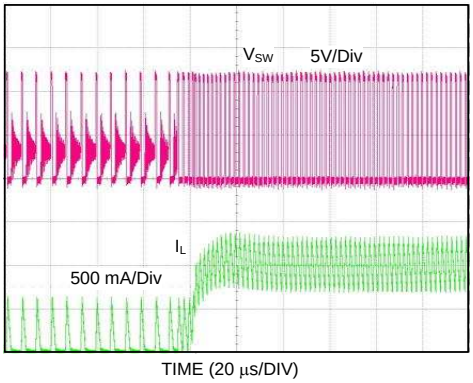
V_{OUT} = 3.3 V, 1 A Loaded

Figure 14. Continuous Mode Operation



V_{OUT} = 3.3 V, 0.5 A Loaded

Figure 15. Discontinuous Mode Operation



V_{OUT} = 3.3 V, 0.5 A to 1 A Load

Figure 16. DCM to CCM Transition

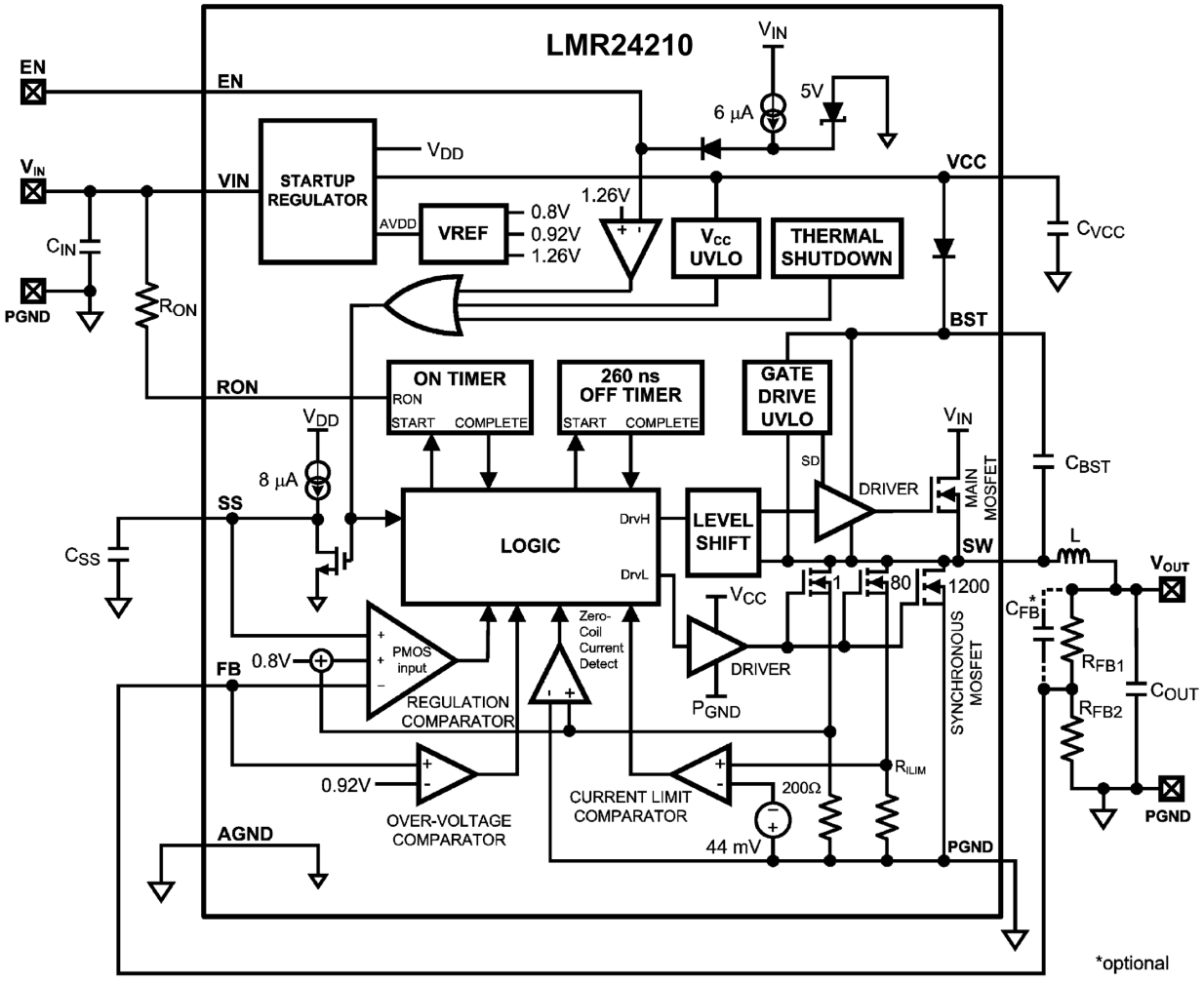
7 Detailed Description

7.1 Overview

The LMR24210 step-down switching regulator features all required functions to implement a cost effective, efficient buck power converter capable of supplying 1 A to a load. It contains dual N-channel main and synchronous MOSFETs. The constant on-time (COT) regulation scheme requires no loop compensation, results in fast load transient response and simple circuit implementation. The regulator can function properly even with an all ceramic output capacitor network, and does not rely on the output capacitor's ESR for stability. The operating frequency remains constant with line variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection circuit, with the limit set internally at 1.8 A, inhibits the main MOSFET until the inductor current level subsides.

The LMR24210 can be applied in numerous applications and can operate efficiently for inputs as high as 42 V. Protection features include output overvoltage protection, thermal shutdown, V_{CC} undervoltage lockout and gate-drive undervoltage lockout. The LMR24210 is available in a small DSBGA chip-scale package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 COT Control Circuit Overview

COT control is based on a comparator and a one-shot on-timer, with the output voltage feedback (feeding to the FB pin) compared with an internal reference of 0.8 V. If the voltage of the FB pin is below the reference, the main MOSFET is turned on for a fixed on-time determined by a programming resistor R_{ON} and the input voltage V_{IN}, upon which the on-time varies inversely. Following the on-time, the main MOSFET remains off for a minimum of 260 ns. Then, if the voltage of the FB pin is below the reference, the main MOSFET is turned on again for another on-time period. The switching will continue to achieve regulation.

The regulator will operate in the discontinuous conduction mode (DCM) at a light load, and the continuous conduction mode (CCM) with a heavy load. In the DCM, the current through the inductor starts at zero and ramps up to a peak during the on-time, and then ramps back to zero before the end of the off-time. It remains zero and the load current is supplied entirely by the output capacitor. The next on-time period starts when the voltage at the FB pin falls below the internal reference. The operating frequency in the DCM is lower and varies larger with the load current as compared with the CCM. Conversion efficiency is maintained since conduction loss and switching loss are reduced with the reduction in the load and the switching frequency respectively. The operating frequency in the DCM can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT} (V_{IN} - 1) \times L \times 1.18 \times 10^{20} \times I_{OUT}}{(V_{IN} - V_{OUT}) \times R_{ON}^{2}} \quad (1)$$

In the CCM, the current flows through the inductor in the entire switching cycle, and never reaches zero during the off-time. The operating frequency remains relatively constant with load and line variations. The CCM operating frequency can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT}}{1.3 \times 10^{-10} \times R_{ON}} \quad (2)$$

Consider and Equation 5 when choosing the switching frequency.

The output voltage is set by two external resistors R_{FB1} and R_{FB2}. The regulated output voltage is

$$V_{OUT} = 0.8\ V \times (R_{FB1} + R_{FB2}) / R_{FB2} \quad (3)$$

7.3.2 Start-up Regulator (V_{CC})

A start-up regulator is integrated within the LMR24210. The input pin VIN can be connected directly to a line voltage up to 42 V. The V_{CC} output regulates at 6 V, and is current limited to 65 mA. Upon power up, the regulator sources current into an external capacitor C_{VCC}, which is connected to the VCC pin. For stability, C_{VCC} must be at least 680 nF. When the voltage on the VCC pin is higher than the undervoltage lockout (UVLO) threshold of 3.75 V, the main MOSFET is enabled and the SS pin is released to allow the soft-start capacitor C_{SS} to charge.

The minimum input voltage is determined by the dropout voltage of the regulator and the V_{CC} UVLO falling threshold (≅ 3.7 V). If V_{IN} is less than ≅ 4 V, the regulator shuts off and V_{CC} goes to zero.

7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to a 0.8-V internal reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at the FB pin falls below 0.8 V. The main MOSFET stays on for the on-time, causing the output voltage and consequently the voltage of the FB pin to rise above 0.8 V. After the on-time period, the main MOSFET stays off until the voltage of the FB pin falls below 0.8V again. Bias current at the FB pin is nominally 5 nA.

7.3.4 Zero Coil Current Detect

The current of the synchronous MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operation, which improves the efficiency at a light load.

Feature Description (continued)

7.3.5 Overvoltage Comparator

The voltage at the FB pin is compared to a 0.92-V internal reference. If it rises above 0.92 V, the on-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage or the output load changes suddenly. Once the OVP is activated, the main MOSFET remains off until the voltage at the FB pin falls below 0.92 V. The synchronous MOSFET stays on to discharge the inductor until the inductor current reduces to zero, and then switches off.

7.3.6 On-Time Timer, Shutdown

The on-time of the LMR24210 main MOSFET is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{on} = \frac{1.3 \times 10^{-10} \times R_{ON}}{V_{IN}} \quad (4)$$

The inverse relationship of t_{on} and V_{IN} gives a nearly constant frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150 ns. The on-timer has a limiter to ensure a minimum of 150 ns for t_{on}. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times 150 \text{ ns}} \quad (5)$$

The LMR24210 can be remotely shutdown by pulling the voltage of the EN pin below 1 V. In this shutdown mode, the SS pin is internally grounded, the on-timer is disabled, and bias currents are reduced. Releasing the EN pin allows normal operation to resume because the EN pin is internally pulled up.

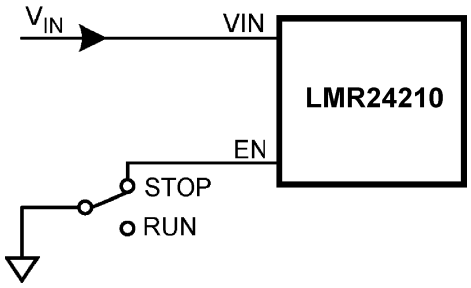


Figure 17. Shutdown Implementation

7.3.7 Current Limit

Current limit detection is carried out during the off-time by monitoring the re-circulating current through the synchronous MOSFET. Referring to the *Functional Block Diagram*, when the main MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 1.8 A, the current limit comparator toggles, and as a result disabling the start of the next on-time period. The next switching cycle starts when the re-circulating current falls back below 1.8 A (and the voltage at the FB pin is below 0.8 V). The inductor current is monitored during the on-time of the synchronous MOSFET. As long as the inductor current exceeds 1.8 A, the main MOSFET remains inhibited to achieve current limit. The operating frequency is lower during current limit due to a longer off-time.

Figure 18 illustrates an inductor current waveform. On average, the output current I_{OUT} is the same as the inductor current I_L, which is the average of the rippled inductor current. In case of current limit (the current limit portion of Figure 18), the next on-time will not initiate until the current drops below 1.8A (assume the voltage at the FB pin is lower than 0.8 V). During each on-time the current ramps up an amount equal to:

$$I_{LR} = \frac{(V_{IN} - V_{OUT}) \times t_{on}}{L} \quad (6)$$

During current limit, the LMR24210 operates in a constant current mode with an average output current $I_{OUT(CL)}$ equal to 1.8 A + I_{LR} / 2.

Feature Description (continued)

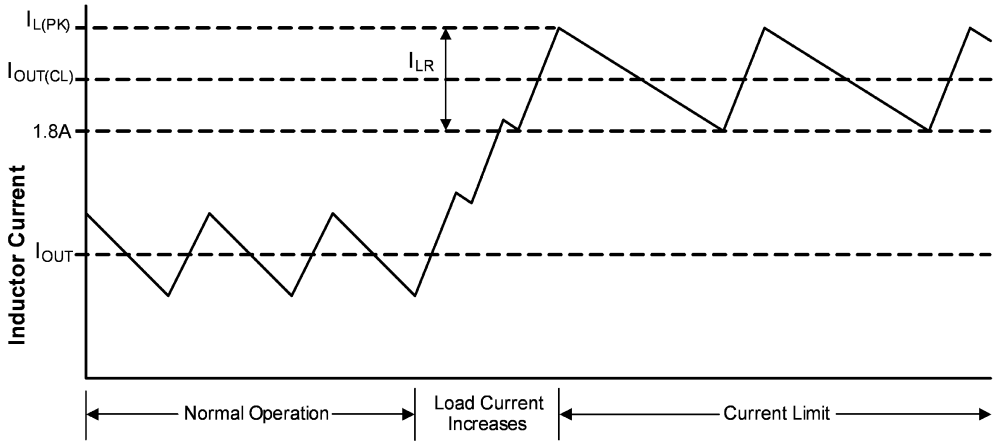


Figure 18. Inductor Current - Current Limit Operation

7.3.8 N-Channel Mosfet and Driver

The LMR24210 integrates an N-channel main MOSFET and an associated floating high voltage main MOSFET gate driver. The gate drive circuit works in conjunction with an external bootstrap capacitor C_{BST} and an internal high voltage diode. C_{BST} connecting between the BST and SW pins powers the main MOSFET gate driver during the main MOSFET on-time. During each off-time, the voltage of the SW pin falls to approximately –1 V, and C_{BST} charges from V_{CC} through the internal diode. The minimum off-time of 260 ns provides enough time for charging C_{BST} in each cycle.

7.3.9 Soft Start

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing startup stresses and current surges. Upon turnon, after V_{CC} reaches the undervoltage threshold, an 8-µA internal current source charges up an external capacitor C_{SS} connecting to the SS pin. The ramping voltage at the SS pin (and the non-inverting input of the regulation comparator as well) ramps up the output voltage V_{OUT} in a controlled manner.

The soft start time duration to reach steady state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / 8\ \mu A = 0.8\ V \times C_{SS} / 8\ \mu A \quad (7)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (8)$$

Use of a 4.7-nF capacitor results in a 0.5-ms soft-start duration. This is a recommended value. Note that high values of C_{SS} capacitance causes more output voltage drop when a load transient goes across the DCM-CCM boundary. If a fast load transient response is desired for steps between DCM and CCM mode the softstart capacitor value must be less than 18 nF (which corresponds to a soft-start time of 1.8 ms).

An internal switch grounds the SS pin if any of the following three cases happens: (i) V_{CC} is below the UVLO threshold; (ii) a thermal shutdown occurs; or (iii) the EN pin is grounded. Alternatively, the output voltage can be shut off by connecting the SS pin to ground using an external switch. Releasing the switch allows the SS pin to ramp up and the output voltage to return to normal. The shutdown configuration is shown in Figure 19.

Feature Description (continued)

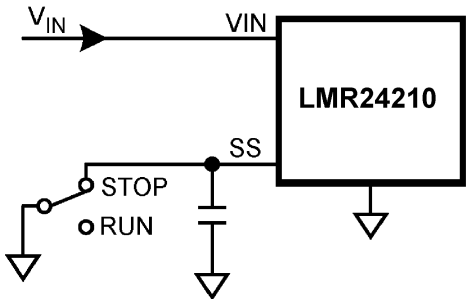


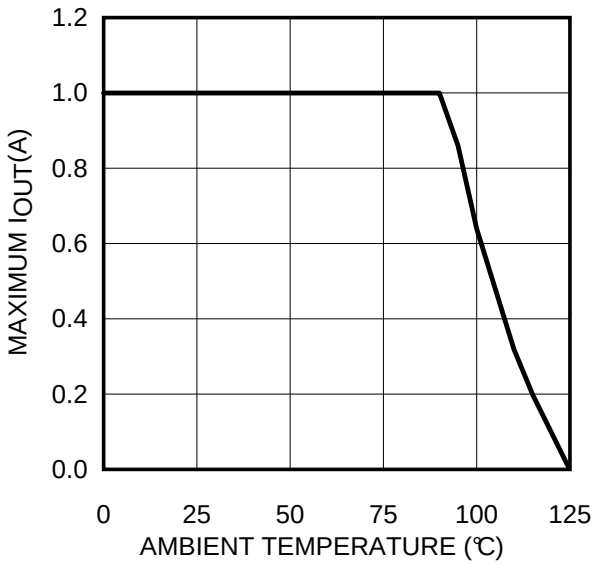
Figure 19. Alternate Shutdown Implementation

7.3.10 Thermal Protection

The junction temperature of the LMR24210 should not exceed the maximum limit. Thermal protection is implemented by an internal Thermal Shutdown circuit, which activates (typically) at 165°C to make the controller enter a low power reset state by disabling the main MOSFET, disabling the on-timer, and grounding the SS pin. Thermal protection helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C), the SS pin is released, and normal operation resumes.

7.3.11 Thermal Derating

Temperature rise increases with frequency, load current, input voltage and smaller board dimensions. On a typical board, the LMR24210 is capable of supplying 1 A below an ambient temperature of 90°C under worst case operation with input voltage of 42 V. Figure 20 shows a thermal derating curve for the output current without thermal shutdown against ambient temperature up to 125°C. Obtaining 1-A output current is possible at higher temperature by increasing the PCB ground plane area, adding airflow or reducing the input voltage or operating frequency.



θ_{JA}=40°C/W, V_{OUT} = 3.3 V, f_{SW} = 500 kHz.
(tested on the evaluation board)

Figure 20. Thermal Derating Curve

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMR24210 voltage regulator features all required functions to implement a highly efficient and cost-effective buck regulator. It is capable of supplying 1 A to loads with an output voltage as low as 0.8 V. Dual N-channel synchronous MOSFET switches allow a low component count, thus reducing complexity and minimizing board size.

8.2 Typical Application

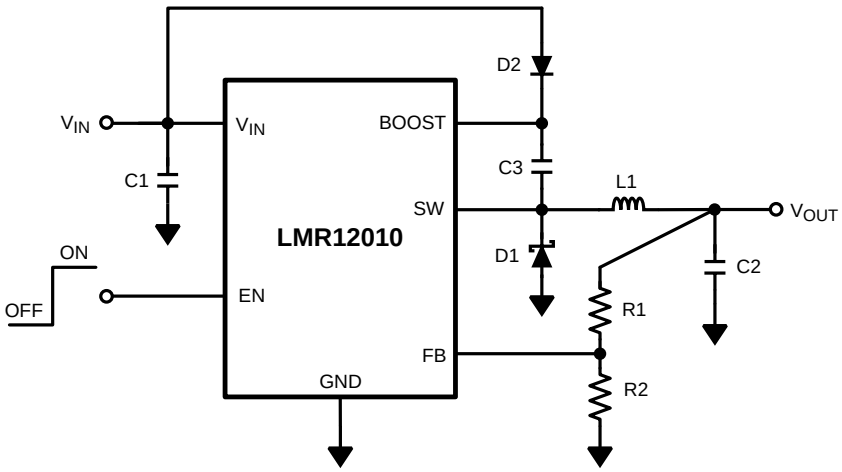


Figure 21. Typical Application Schematic

8.2.1 Detailed Design Procedure

8.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR24010 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Typical Application (continued)

8.2.1.2 External Components

The following guidelines can be used to select external components.

R_{FB1} and R_{FB2}: Choose these resistors from standard values in the range of 1 kΩ to 10 kΩ, satisfying the following ratio:

$$R_{FB1} / R_{FB2} = (V_{OUT} / 0.8\ V) - 1 \quad (9)$$

For V_{OUT} = 0.8 V, the FB pin can be connected to the output directly with a pre-load resistor drawing more than 20 µA. This is needed because the converter operation needs a minimum inductor current ripple to maintain good regulation when no load is connected.

R_{ON}: Equation 2 can be used to select R_{ON} if a desired operating frequency is selected. But the minimum value of R_{ON} is determined by the minimum on-time. It can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} \times 150\ ns}{1.3 \times 10^{-10}} \quad (10)$$

If R_{ON} calculated from Equation 2 is smaller than the minimum value determined in Equation 10, select a lower frequency to re-calculate R_{ON} by Equation 2. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged. The relationship of $V_{IN(MAX)}$ and R_{ON} is shown in Figure 22.

On the other hand, the minimum off-time of 260 ns can limit the maximum duty ratio.

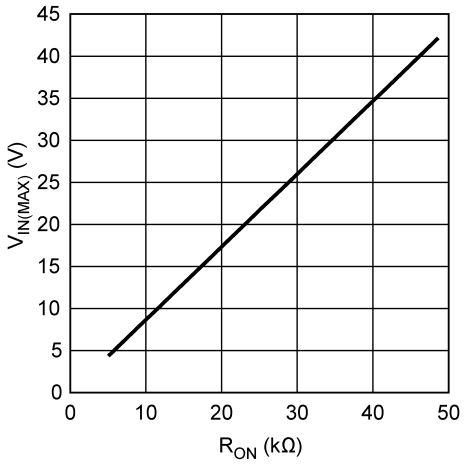


Figure 22. Maximum V_{IN} For Selected R_{ON}

L: The main parameter affected by the inductor is the amplitude of inductor current ripple (I_{LR}). Once I_{LR} is selected, L can be determined by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{LR} \times f_{SW} \times V_{IN}}$$

where

- V_{IN} is the maximum input voltage and
- f_{SW} is determined from Equation 2. (11)

If the output current I_{OUT} is determined, by assuming that $I_{OUT} = I_L$, the higher and lower peak of I_{LR} can be determined. Beware that the higher peak of I_{LR} should not be larger than the saturation current of the inductor and current limits of the main and synchronous MOSFETs. Also, the lower peak of I_{LR} must be positive if CCM operation is required.

Typical Application (continued)

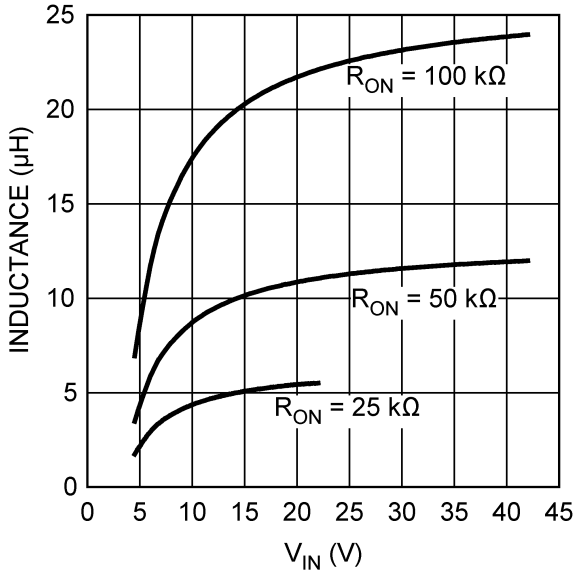


Figure 23. Inductor Selection for V_{OUT} = 3.3 V

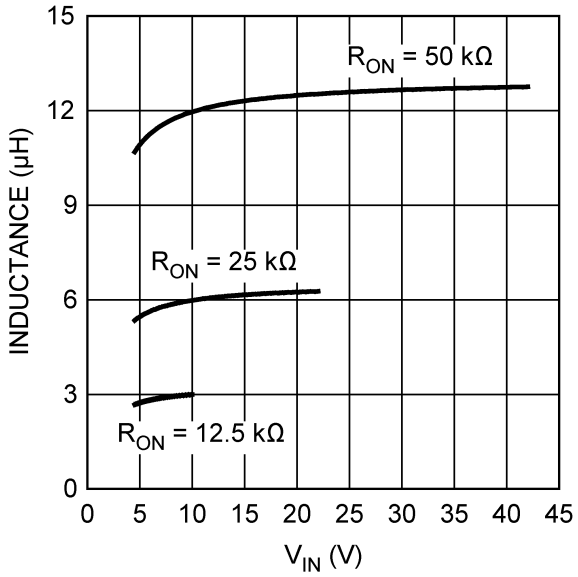


Figure 24. Inductor Selection for V_{OUT} = 0.8 V

Figure 23 and Figure 24 show curves on inductor selection for various V_{OUT} and R_{ON}. For small R_{ON}, according to Equation 10, V_{IN} is limited. Some curves are therefore limited as shown in the figures.

C_{VCC}: The capacitor on the V_{CC} output provides not only noise filtering and stability, but also prevents false triggering of the V_{CC} UVLO at the main MOSFET on/off transitions. C_{VCC} should be no smaller than 680 nF for stability, and should be a good quality, low ESR, ceramic capacitor.

C_{OUT} and C_{OUT3}: C_{OUT} should generally be no smaller than 10 µF. Experimentation is usually necessary to determine the minimum value for C_{OUT}, as the nature of the load may require a larger value. A load which creates significant transients requires a larger C_{OUT} than a fixed load.

C_{OUT3} is a small value ceramic capacitor located close to the LMR24210 to further suppress high frequency noise at V_{OUT}. TI recommends a 100-nF capacitor.

Typical Application (continued)

C_{IN} and C_{IN3}: The function of C_{IN} is to supply most of the main MOSFET current during the on-time, and limit the voltage ripple at the VIN pin, assuming that the voltage source connecting to the VIN pin has finite output impedance. If the voltage source's dynamic impedance is high (effectively a current source), C_{IN} supplies the average input current, but not the ripple current.

At the maximum load current, when the main MOSFET turns on, the current to the VIN pin suddenly increases from zero to the lower peak of the inductor's ripple current and ramps up to the higher peak value. It then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, C_{IN} must be capable of supplying this average load current during the maximum on-time. C_{IN} is calculated from:

$$C_{IN} = \frac{I_{OUT} \times t_{on}}{\Delta V_{IN}}$$

where

- I_{OUT} is the load current
- t_{on} is the maximum on-time
- ΔV_{IN} is the allowable ripple voltage at V_{IN}

(12)

The purpose of the C_{IN3} is to help avoid transients and ringing due to long lead inductance at the VIN pin. A low ESR 0.1-µF ceramic chip capacitor located close to the LMR24210 is recommended.

C_{BST}: A 33-nF high-quality ceramic capacitor with low ESR is recommended for C_{BST} since it supplies a surge current to charge the main MOSFET gate driver at turnon. Low ESR also helps ensure a complete recharge during each off-time.

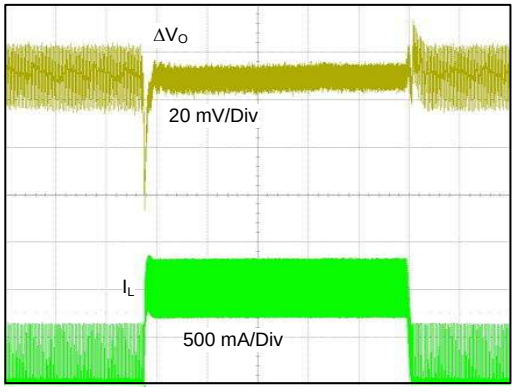
C_{SS}: The capacitor at the SS pin determines the soft-start time; that is, the time for the reference voltage at the regulation comparator and the output voltage to reach their final value. The time is determined from Equation 13:

$$t_{SS} = \frac{C_{SS} \times 0.8V}{8\ \mu A}$$

(13)

C_{FB}: If the output voltage is higher than 1.6 V, C_{FB} is needed in the DCM to reduce the output ripple. The recommended value for C_{FB} is 10 nF.

8.2.2 Application Curve



V_{OUT} = 3.3 V, 0.2 A to 1 A Load

Figure 25. Load Transient

9 Layout

9.1 Layout Considerations

The LMR24210 regulation, overvoltage, and current limit comparators are very fast and may respond to short duration noise pulses. Layout is therefore critical for optimum performance. It must be as neat and compact as possible, and all external components must be as close to their associated pins of the LMR24210 as possible. Refer to the *Functional Block Diagram*, the loop formed by C_{IN}, the main and synchronous MOSFET internal to the LMR24210, and the PGND pin must be as small as possible. The connection from the PGND pin to C_{IN} must be as short and direct as possible. Add vias to connect the ground of C_{IN} to a ground plane, located as close as possible to the capacitor. The bootstrap capacitor C_{BST} should be connected as close to the SW and BST pins as possible, and the connecting traces should be thick. The feedback resistors and capacitor R_{FB1}, R_{FB2}, and C_{FB} must be close to the FB pin. A long trace running from V_{OUT} to R_{FB1} is generally acceptable since this is a low impedance node. Ground R_{FB2} directly to the AGND pin. Connect the output capacitor C_{OUT} to the load and tied directly to the ground plane. Connect the inductor L close to the SW pin with as short a trace as possible to reduce the potential for EMI (electromagnetic interference) generation. If it is expected that the internal dissipation of the LMR24210 produces excessive junction temperature during normal operation, making good use of the PC board's ground plane can help considerably to dissipate heat. Additionally the use of thick traces, where possible, can help conduct heat away from the LMR24210. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

9.2 Layout Examples

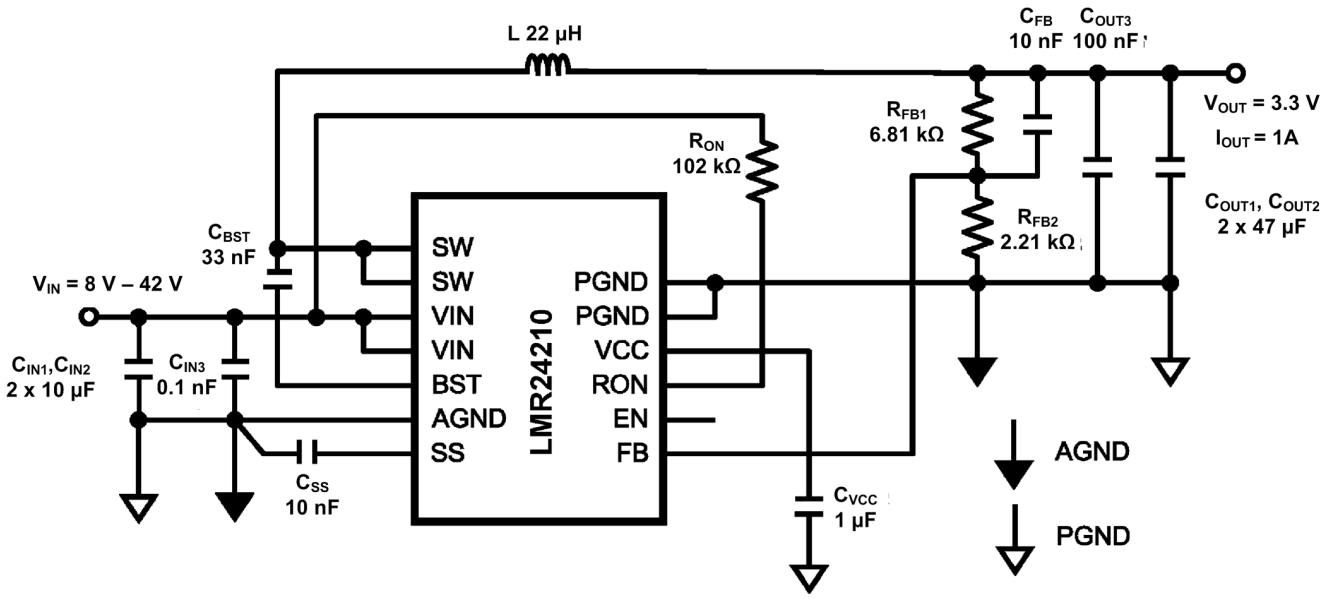


Figure 26. Typical Application Schematic for V_{OUT} = 3.3 V

Layout Examples (continued)

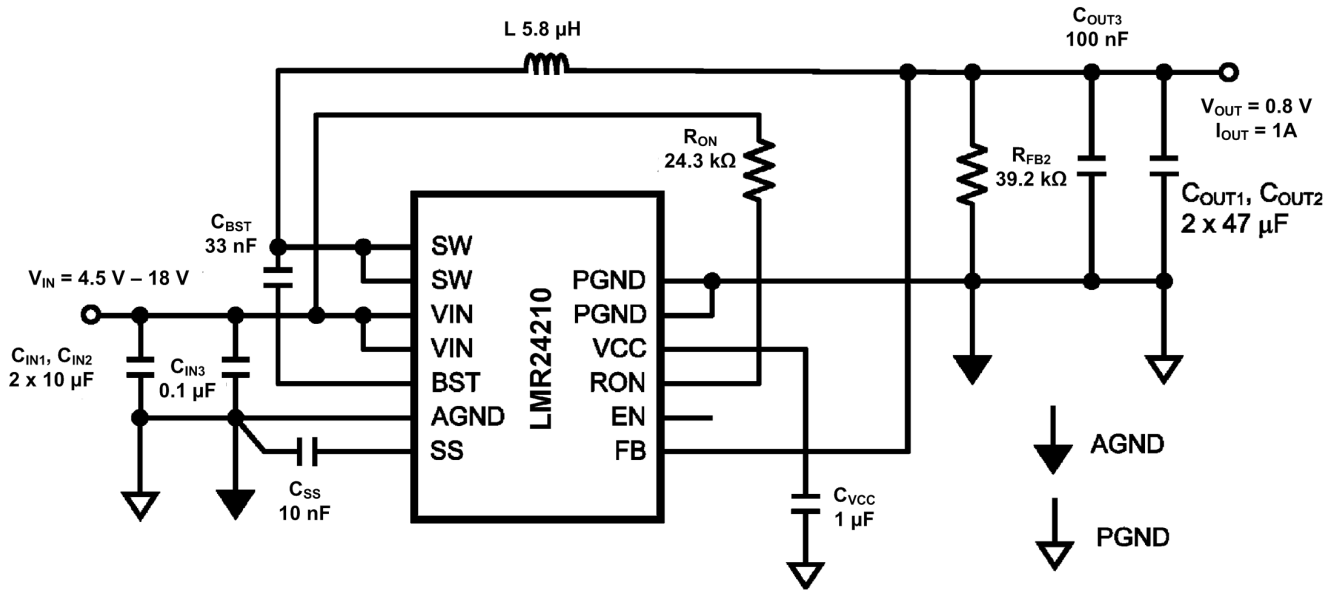


Figure 27. Typical Application Schematic for V_{OUT} = 0.8 V

9.3 Package Considerations

The die has exposed edges and can be sensitive to ambient light. For applications with direct high intensitiy ambient red, infrared, LED or natural light TI recommends shielding the device from the light source to avoid abnormal behavior.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Custom Design With WEBENCH® Tools

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- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR24210TL/NOPB	ACTIVE	DSBGA	YPA	28	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SJ5B	Samples
LMR24210TLX/NOPB	ACTIVE	DSBGA	YPA	28	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SJ5B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

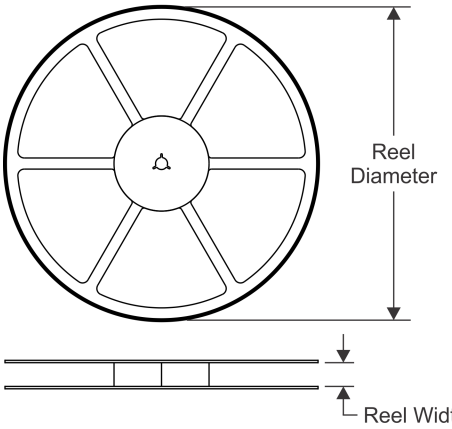
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

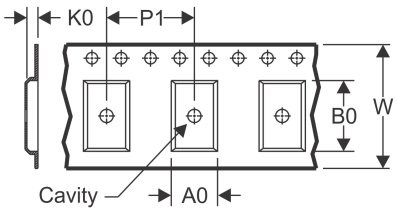
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

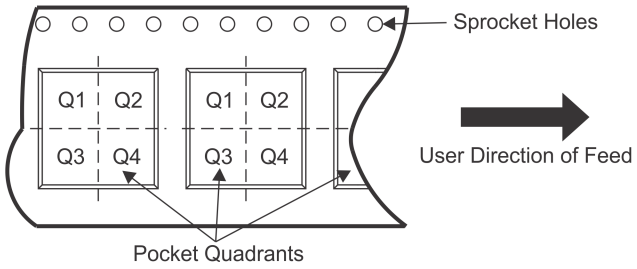


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

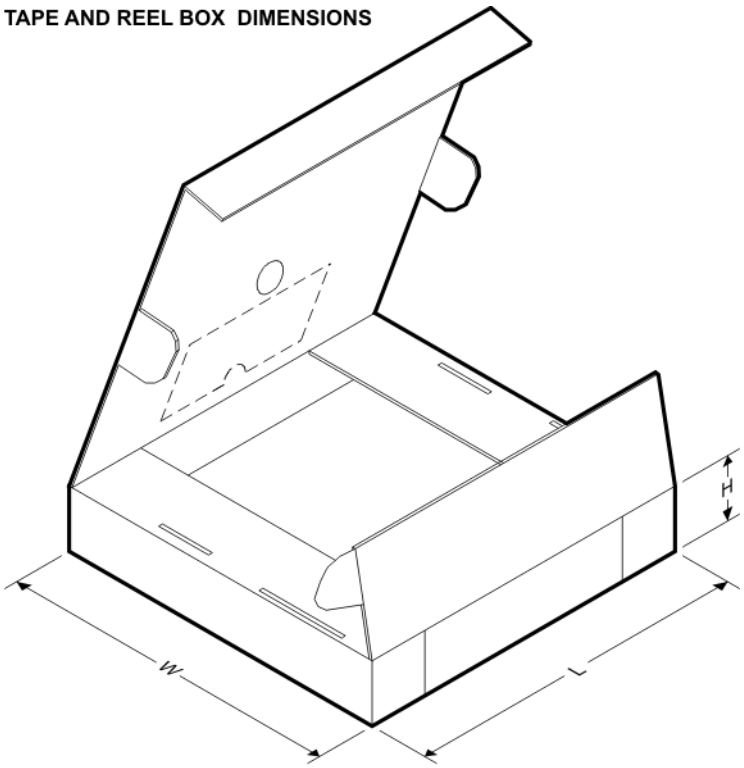
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR24210TL/NOPB	DSBGA	YPA	28	250	178.0	12.4	2.64	3.84	0.76	8.0	12.0	Q1
LMR24210TLX/NOPB	DSBGA	YPA	28	1000	178.0	12.4	2.64	3.84	0.76	8.0	12.0	Q1

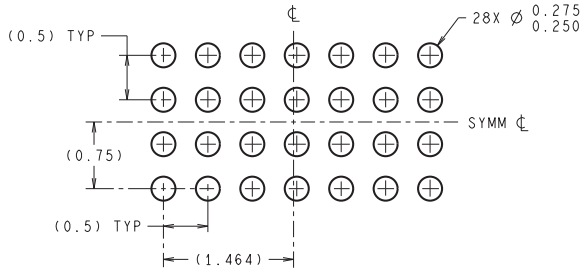
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

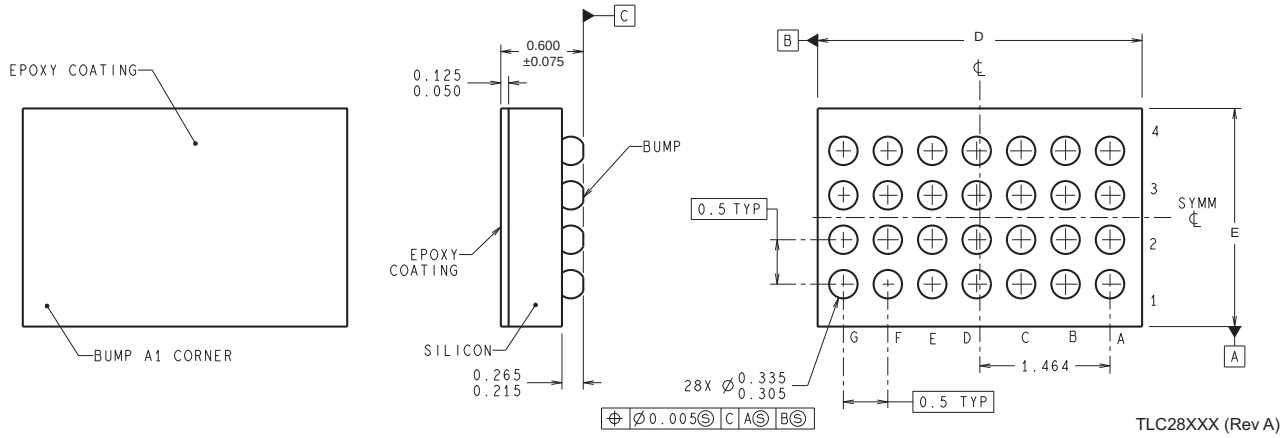
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR24210TL/NOPB	DSBGA	YPA	28	250	210.0	185.0	35.0
LMR24210TLX/NOPB	DSBGA	YPA	28	1000	210.0	185.0	35.0

YPA0028



LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



TLC28XXX (Rev A)

D: Max = 3.676 mm, Min =3.615 mm

E: Max = 2.48 mm, Min = 2.419 mm

4215064/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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- Texas Instruments Information

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- Shortage Management
- Alternative Solution
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