



**THE DATASHEET OF
SN75462DR**



SN55461 THRU SN55463 SN75461 THRU SN75463 DUAL PERIPHERAL DRIVERS

SLRS022A – DECEMBER 1976 – REVISED OCTOBER 1995

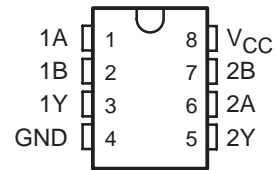
PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) With Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

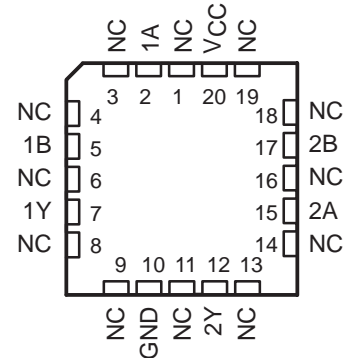
SUMMARY OF SERIES 55461/75461

| DEVICE | LOGIC | PACKAGES |
|---------|-------|----------|
| SN55461 | AND | FK, JG |
| SN55462 | NAND | FK, JG |
| SN55463 | OR | FK, JG |
| SN75461 | AND | D, P |
| SN75462 | NAND | D, P |
| SN75463 | OR | D, P |

SN55461, SN55462, SN55463 . . . JG PACKAGE
SN75461, SN75462, SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462, SN55463 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55453B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, and SN55463/SN75463 are dual peripheral AND, NAND, and OR drivers respectively (assuming positive logic), with the output of the gates internally connected to the bases of the npn output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of -55°C to 125°C . Series SN75461 drivers are characterized for operation from 0°C to 70°C .

SN55461 THRU SN55463
SN75461 THRU SN75463
DUAL PERIPHERAL DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | SN55' | SN75' | UNIT |
|---|------------------------------|------------|------|
| Supply voltage, V_{CC} (see Note 1) | 7 | 7 | V |
| Input voltage, V_I | 5.5 | 5.5 | V |
| Intermitter voltage (see Note 2) | 5.5 | 5.5 | V |
| Off-state output voltage, V_O | 35 | 35 | V |
| Continuous collector or output current (see Note 3) | 400 | 400 | mA |
| Peak collector or output current ($t_W \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4) | 500 | 500 | mA |
| Continuous total power dissipation | See Dissipation Rating Table | | |
| Operating free-air temperature range, T_A | -55 to 125 | 0 to 70 | °C |
| Storage temperature range, T_{STG} | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds, T_C | FK package | 260 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | JG package | 300 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D or P package | 260 | °C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values are with respect to network GND unless otherwise specified.
 2. This is the voltage between two emitters A and B.
 3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
 4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ | DERATING FACTOR | $T_A = 70^\circ\text{C}$ | $T_A = 125^\circ\text{C}$ |
|---------|-----------------------------|--------------------------------|--------------------------|---------------------------|
| | POWER RATING | ABOVE $T_A = 25^\circ\text{C}$ | POWER RATING | POWER RATING |
| D | 725 mW | 5.8 mW/°C | 464 mW | – |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 210 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW | – |

recommended operating conditions

| | SN55' | | | SN75' | | | UNIT |
|---------------------------------------|-------|-----|-----|-------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V_{IH} | 2 | | | 2 | | | V |
| Low-level input voltage, V_{IL} | 0.8 | | | 0.8 | | | V |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |



SN55461 THRU SN55463 SN75461 THRU SN75463 DUAL PERIPHERAL DRIVERS

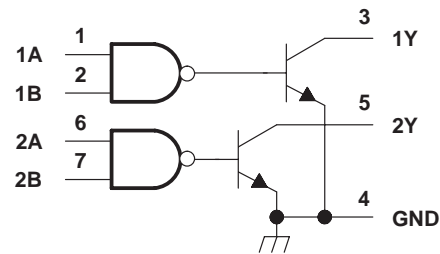
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

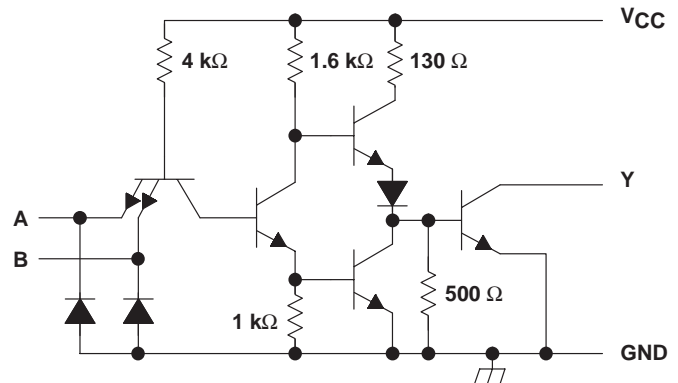


FUNCTION TABLE
(each driver)

| A | B | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

positive logic: $Y = AB$ or $\overline{A + B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS† | SN55461 | | | SN75461 | | | UNIT |
|--|--|---------|------|------|---------|------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | | -1.2 | -1.5 | | -1.2 | -1.5 | V |
| I_{OH} High-level output current | $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 35 \text{ V}$ | | | 300 | | | 100 | μA |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$ | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | | 40 | | | 40 | μA |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | -1 | -1.6 | | -1 | -1.6 | mA |
| I_{CCH} Supply current, outputs high | $V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$ | | 8 | 11 | | 8 | 11 | mA |
| I_{CCL} Supply current, outputs low | $V_{CC} = \text{MAX}$, $V_I = 0$ | | 56 | 76 | | 56 | 76 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|------------|-----|-----|------|
| t_{PLH} Propagation delay time, low-to-high-level output | $I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1 | | 30 | 55 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output | | | 25 | 40 | |
| t_{TLH} Transition time, low-to-high-level output | | | 8 | 20 | |
| t_{THL} Transition time, high-to-low-level output | | | 10 | 20 | |
| V_{OH} High-level output voltage after switching | SN55461 | $V_S - 10$ | | | mV |
| | SN75461 | $V_S - 10$ | | | |



SN55461 THRU SN55463 SN75461 THRU SN75463 DUAL PERIPHERAL DRIVERS

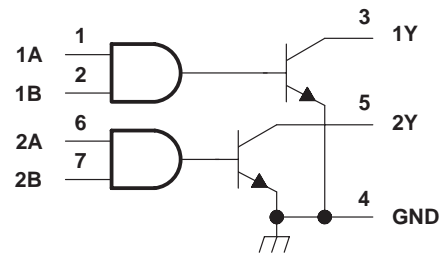
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logic symbol†



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Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

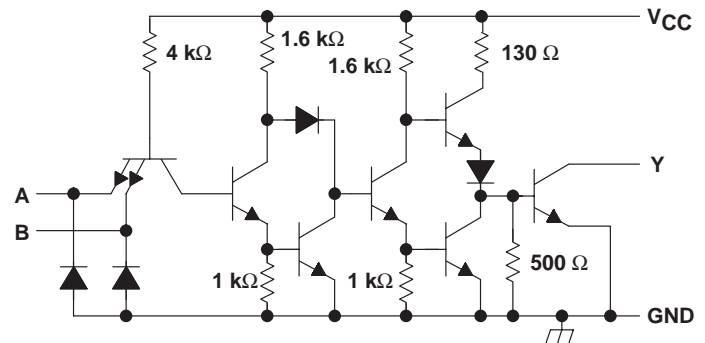


FUNCTION TABLE
(each driver)

| A | B | Y |
|---|---|---------------|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

positive logic:
 $Y = \overline{AB}$ or $\overline{A + B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS† | SN55462 | | SN75462 | | UNIT |
|--|---|---------|------|---------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | -1.2 | -1.5 | -1.2 | -1.5 | V |
| I_{OH} High-level output current | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 35 \text{ V}$ | | 300 | | 100 | μA |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$ | 0.25 | 0.5 | 0.25 | 0.4 | V |
| | $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$ | 0.5 | 0.8 | 0.5 | 0.7 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | 1 | | 1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | 40 | | 40 | μA |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | -1.1 | -1.6 | -1.1 | -1.6 | mA |
| I_{CCH} Supply current, outputs high | $V_{CC} = \text{MAX}$, $V_I = 0$ | 13 | 17 | 13 | 17 | mA |
| I_{CCL} Supply current, outputs low | $V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$ | 61 | 76 | 61 | 76 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------------|-----|-----|------|
| t_{PLH} Propagation delay time, low-to-high-level output | $I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1 | | 45 | 65 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output | | | 30 | 50 | |
| t_{TLH} Transition time, low-to-high-level output | | | 13 | 25 | |
| t_{THL} Transition time, high-to-low-level output | | | 10 | 20 | |
| V_{OH} High-level output voltage after switching | SN55462 | $V_S - 10$ | | | mV |
| | SN75462 | $V_S - 10$ | | | |



SN55461 THRU SN55463 SN75461 THRU SN75463 DUAL PERIPHERAL DRIVERS

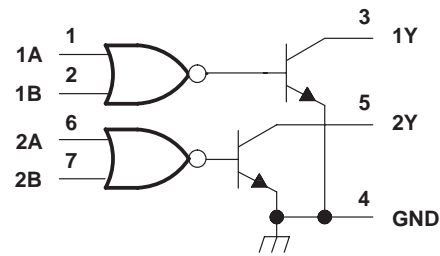
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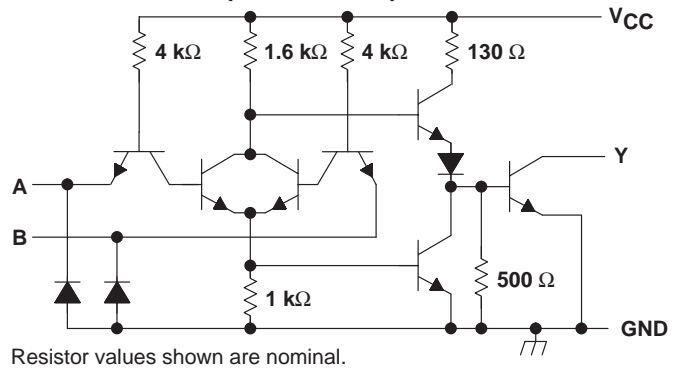


FUNCTION TABLE (each driver)

| A | B | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

positive logic:
 $Y = A + B \text{ or } \overline{A} \overline{B}$

schematic (each driver)



electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS† | SN55463 | | SN75463 | | UNIT |
|--|--|---------|------|---------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | -1.2 | -1.5 | -1.2 | -1.5 | V |
| I_{OH} High-level output current | $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{OH} = 35 \text{ V}$ | | 300 | | 100 | μA |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 100 \text{ mA}$ | 0.25 | 0.5 | 0.25 | 0.4 | V |
| | $V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 300 \text{ mA}$ | 0.5 | 0.8 | 0.5 | 0.7 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | 1 | | 1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ | | 40 | | 40 | μA |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | -1 | -1.6 | -1 | -1.6 | mA |
| I_{CCH} Supply current, outputs high | $V_{CC} = \text{MAX}, V_I = 5 \text{ V}$ | 8 | 11 | 8 | 11 | mA |
| I_{CCL} Supply current, outputs low | $V_{CC} = \text{MAX}, V_I = 0$ | 58 | 76 | 58 | 76 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

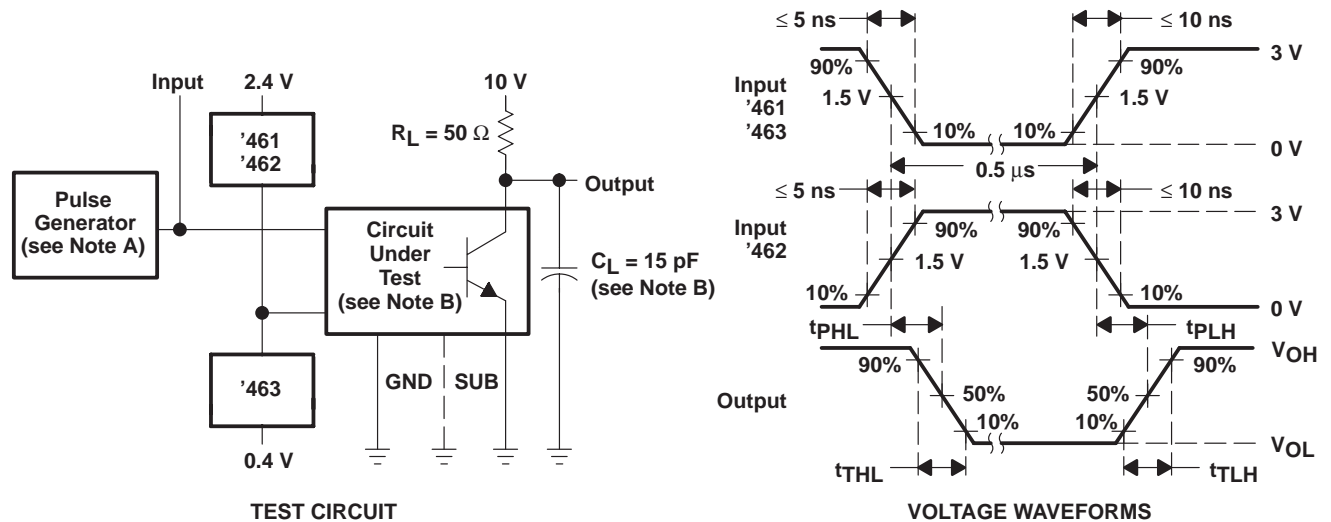
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|------------|-----|-----|------|
| t_{PLH} Propagation delay time, low-to-high-level output | $I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50 \Omega,$ See Figure 1 | | 30 | 55 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output | | | 25 | 40 | |
| t_{TLH} Transition time, low-to-high-level output | | | 8 | 25 | |
| t_{THL} Transition time, high-to-low-level output | | | 10 | 25 | |
| V_{OH} High-level output voltage after switching | SN55463 | $V_S - 10$ | | mV | |
| | SN75463 | $V_S - 10$ | | | |



SN55461 THRU SN55463
SN75461 THRU SN75463
DUAL PERIPHERAL DRIVERS

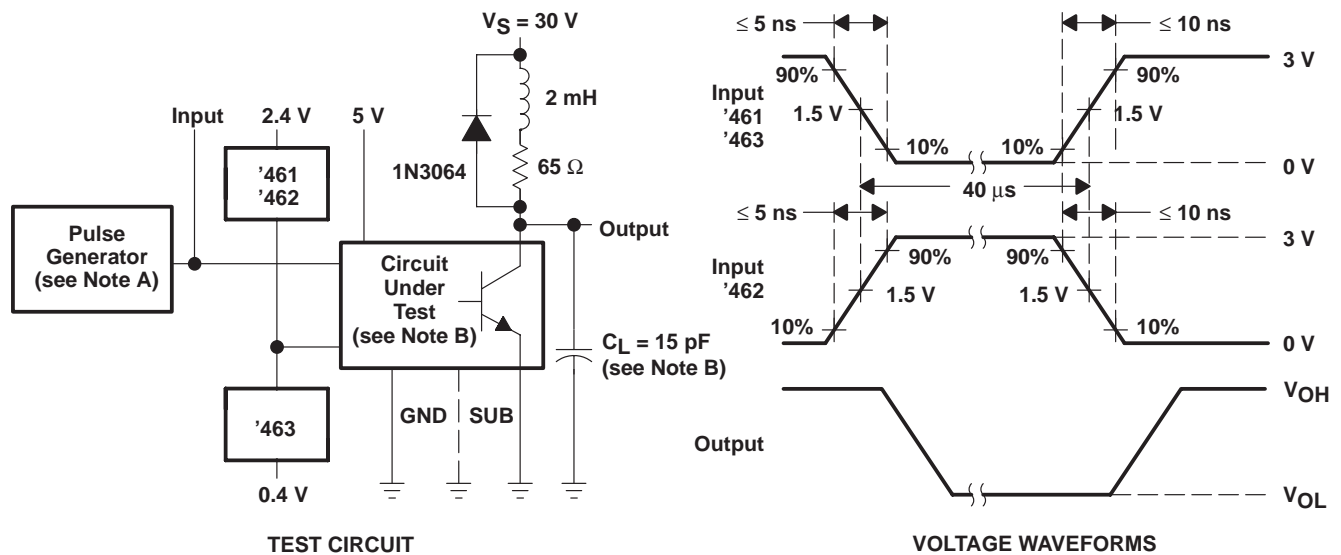
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms for Switching Times



- NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/12908BPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510 /12908BPA | Samples |
| M38510/12908BPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510 /12908BPA | Samples |
| SN75462D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75462 | Samples |
| SN75462DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75462 | Samples |
| SN75462P | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75462P | Samples |
| SN75462PE4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75462P | Samples |
| SN75463P | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75463P | Samples |
| SNJ55462FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ55 462FK | Samples |
| SNJ55462JG | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ55462JG | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75462DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75462DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

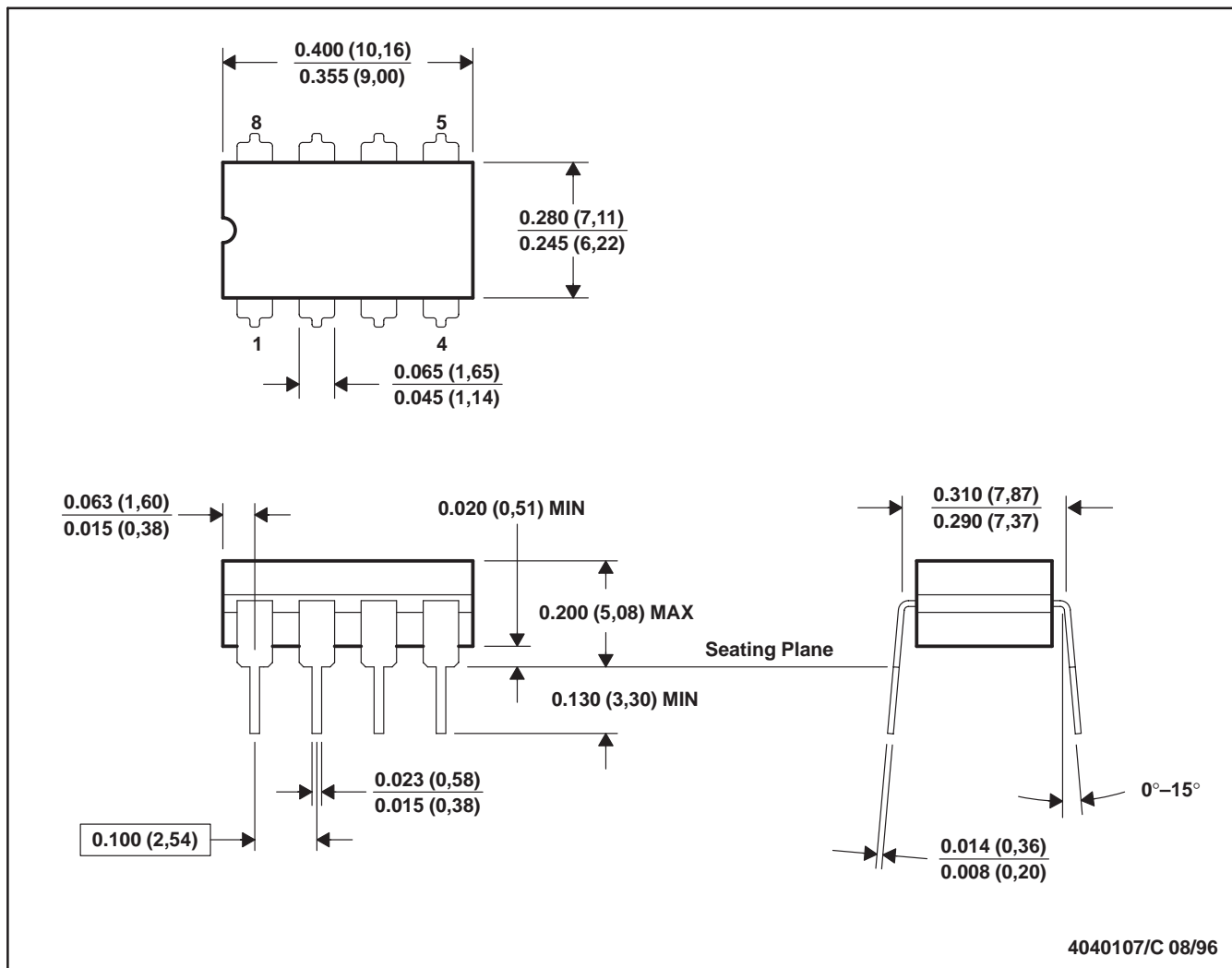
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



4040107/C 08/96

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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