THE DATASHEET OF

TLV1117LV15DCYT

TLV1117LV 1-A, Positive Fixed-Voltage, Low-Dropout Regulator

1 Features

- 1.5% Typical Accuracy
- Low I_Q: 100 µA (Maximum)
  - 500 Times Lower Than Standard 1117 Devices
- V_{IN}: 2 V to 5.5 V
  - Absolute Maximum V_{IN} = 6 V
- Stable With 0-mA Output Current
- Low Dropout: 455 mV at 1 A for V_{OUT} = 3.3 V
- High PSRR: 65 dB at 1 kHz
- Minimum Ensured Current Limit: 1.1 A
- Stable With Cost-Effective Ceramic Capacitors:
  - With 0-Ω ESR
- Temperature Range: –40°C to 125°C
- Thermal Shutdown and Overcurrent Protection
- Available in SOT-223 Package
  - See *Mechanical, Packaging, and Orderable Information* at the end of this document for a complete list of available voltage options.

2 Applications

- Set Top Boxes
- TVs and Monitors
- PC Peripherals, Notebooks, Motherboards
- Modems and Other Communication Products
- Switching Power Supply Post-Regulation

3 Description

The TLV1117LV series of low-dropout (LDO) linear regulators is a low input voltage version of the popular TLV1117 voltage regulator.

The TLV1117LV is an extremely low-power device that consumes 500 times lower quiescent current than traditional 1117 voltage regulators, making the device suitable for applications that mandate very low standby current. The TLV1117LV family of LDOs is also stable with 0 mA of load current; there is no minimum load requirement, making the device an ideal choice for applications where the regulator must power very small loads during standby in addition to large currents on the order of 1 A during normal operation. The TLV1117LV offers excellent line and load transient performance, resulting in very small magnitude undershoots and overshoots of output voltage when the load current requirement changes from less than 1 mA to more than 500 mA.

A precision bandgap and error amplifier provides 1.5% accuracy. A very high power-supply rejection ratio (PSRR) enables use of the device for post-regulation after a switching regulator. Other valuable features include low output noise and low-dropout voltage.

The device is internally compensated to be stable with 0-Ω equivalent series resistance (ESR) capacitors. These key advantages enable the use of cost-effective, small-size ceramic capacitors. Cost-effective capacitors that have higher bias voltages and temperature derating can also be used if desired.

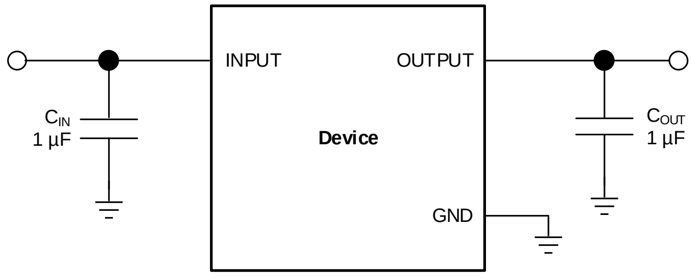
The TLV1117LV series is available in a SOT-223 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV1117LV	SOT-223 (4)	6.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

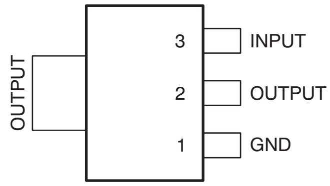
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2011) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Replaced front-page figure	1
• Deleted *Dissipation Ratings* table	4

Changes from Original (May, 2011) to Revision A	Page
• Changed front-page figure	1

5 Pin Configuration and Functions

DCY Package
4 Pins (SOT-223)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	3	I	Input pin. See *Input and Output Capacitor Requirements* in the *Application and Implementation* section for more details.
OUT	2, Tab	O	Regulated output voltage pin. See *Input and Output Capacitor Requirements* for more details.
GND	1	—	Ground pin.

6 Specifications

6.1 Absolute Maximum Ratings

At T_J = 25°C (unless otherwise noted). All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{OUT}	–0.3	6	V
Current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	2		5.5	V
V_{OUT}	0		5.5	V
I_{OUT}	0		1	A

6.4 Thermal Information

THERMAL METRIC(1)		TLV1117LV DCY (SOT-223) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	47.2	
$R_{\theta JC(top)}$	Junction-to-board thermal resistance	12	
ψ_{JT}	Junction-to-top characterization parameter	6.1	
ψ_{JB}	Junction-to-board characterization parameter	11.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At $V_{IN} = V_{OUT(nom)}$ + 1.5 V; I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2		5.5	V
V_{OUT}	DC output accuracy	V_{OUT} > 2 V			–1.5%		1.5%	
		1.5 V ≤ V_{OUT} < 2 V			–2%		2%	
		1.2 V ≤ V_{OUT} < 1.5 V			–40		40	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA				1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 1 A				1	35	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 x $V_{OUT(nom)}$	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		115		mV
				I_{OUT} = 500 mA		285		mV
				I_{OUT} = 800 mA		455		mV
				I_{OUT} = 1 A		570	800	mV
			V_{OUT} ≥ 3.3 V	I_{OUT} = 200 mA		90		mV
				I_{OUT} = 500 mA		230		mV
				I_{OUT} = 800 mA		365		mV
				I_{OUT} = 1 A		455	700	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$			1.1			A
I_Q	Quiescent current	I_{OUT} = 0 mA				50	100	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA, f = 100 Hz				65		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 2.8 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA				60		μV_{RMS}
t_{STR}	Startup time(2)	C_{OUT} = 1.0 µF, I_{OUT} = 1 A				100		µs
UVLO	Undervoltage lockout	V_{IN} rising				1.95		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing				165		°C
		Reset, temperature decreasing				145		°C
T_J	Operating junction temperature				–40		125	°C

(1) V_{DO} is measured for devices with $V_{OUT(nom)}$ = 2.5 V so that V_{IN} = 2.45 V.
(2) Startup time = time from when V_{IN} asserts to when output is sustained at a value greater than or equal to 0.98 × $V_{OUT(nom)}$.

6.6 Typical Characteristics

At $V_{IN} = V_{OUT(nom)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = 25$°C, unless otherwise noted.

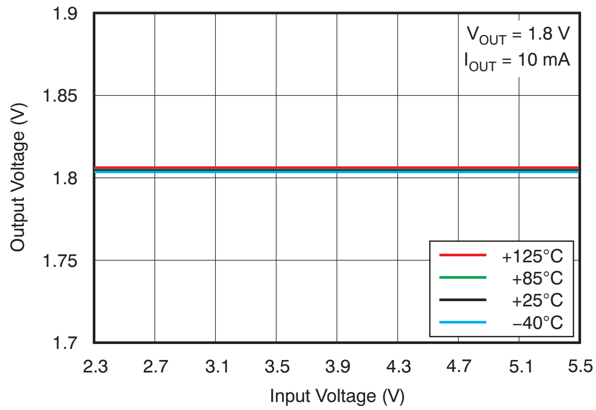


Figure 1. Line Regulation

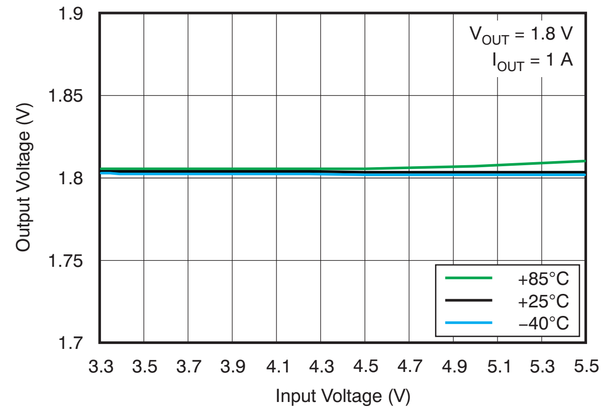


Figure 2. Line Regulation

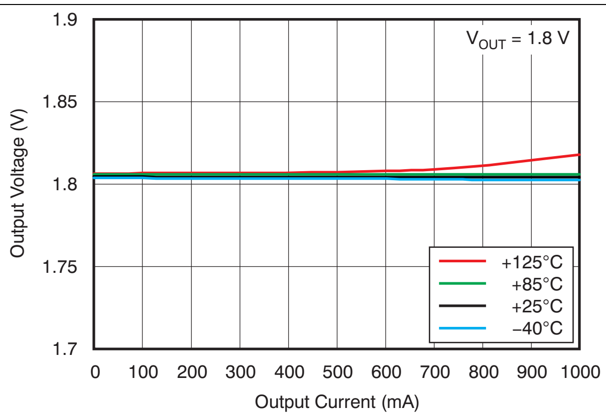


Figure 3. Load Regulation

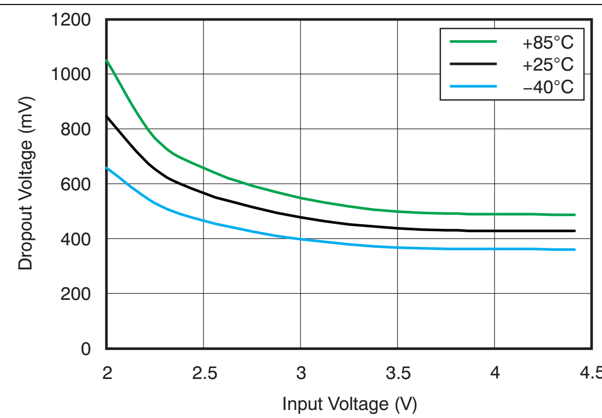


Figure 4. Dropout Voltage vs Input

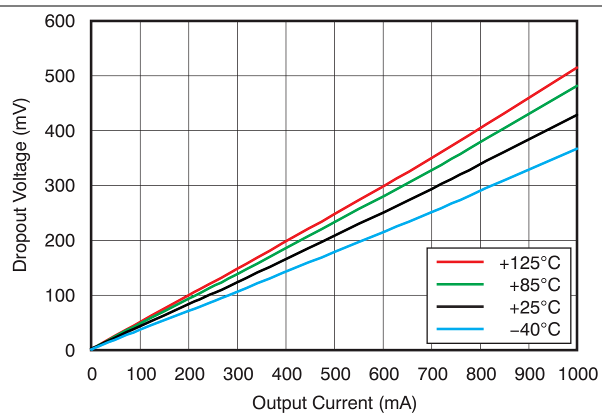


Figure 5. Dropout Voltage vs Output

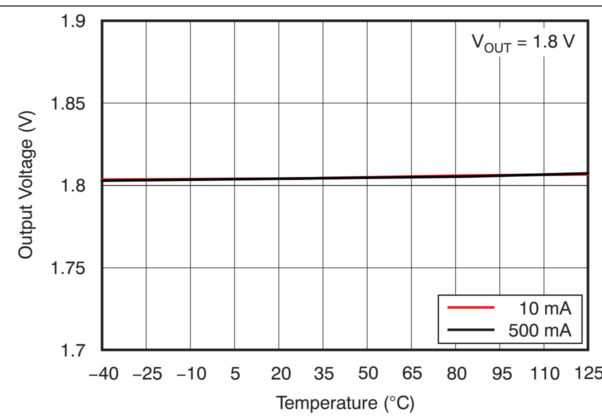


Figure 6. Output Voltage vs Temperature

Typical Characteristics (continued)

At $V_{IN} = V_{OUT(nom)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = 25$°C, unless otherwise noted.

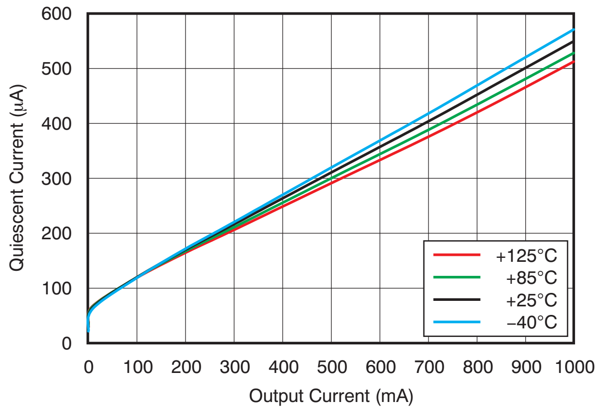


Figure 7. Quiescent Current vs Load

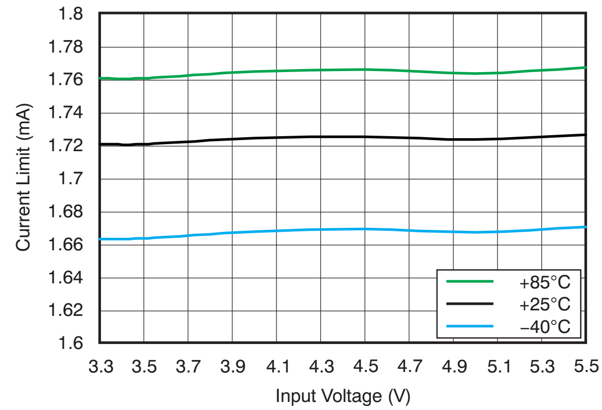


Figure 8. Current Limit vs Input Voltage

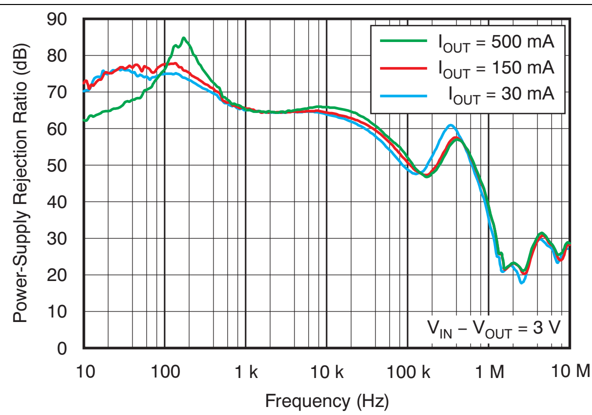


Figure 9. Power-Supply Rejection Ratio vs Frequency

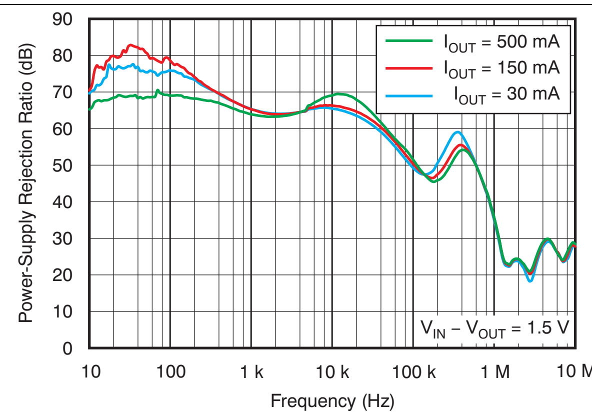


Figure 10. Power-Supply Rejection Ratio vs Frequency

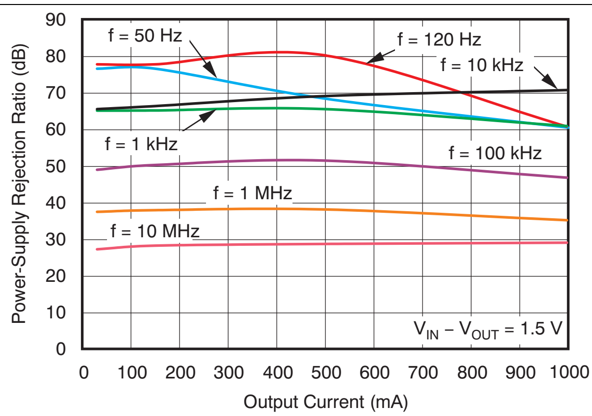


Figure 11. Power-Supply Rejection Ratio vs Output Current

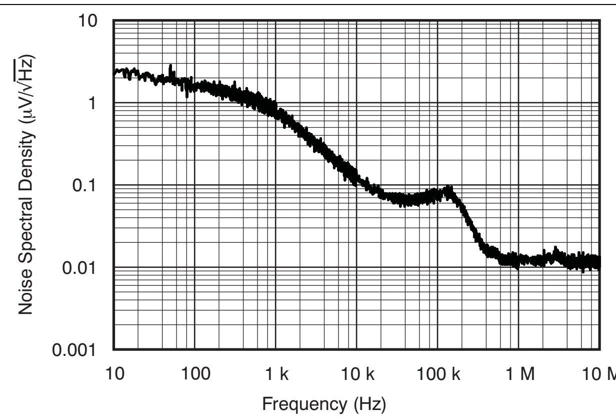


Figure 12. Spectral Noise Density vs Frequency

Typical Characteristics (continued)

At $V_{IN} = V_{OUT(nom)}$ + 1.5 V; I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C, unless otherwise noted.

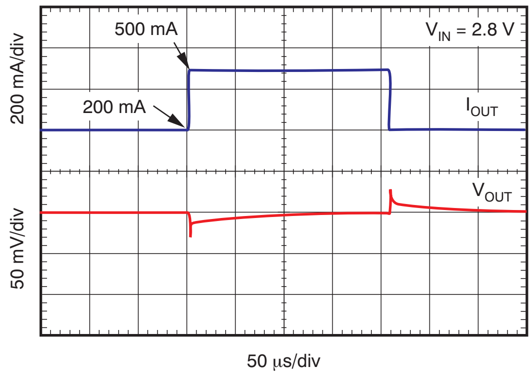


Figure 13. Load Transient Response 200 mA to 500 mA, C_{OUT} = 1 µF

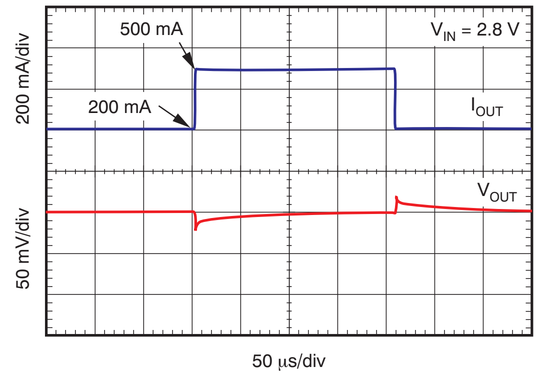


Figure 14. Load Transient Response 200 mA to 500 mA, C_{OUT} = 10 µF

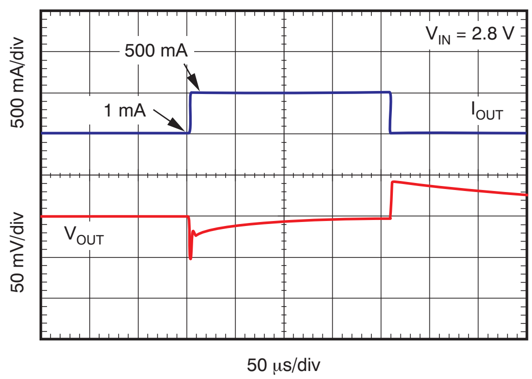


Figure 15. Load Transient Response 1 mA to 500 mA, C_{OUT} = 1 µF

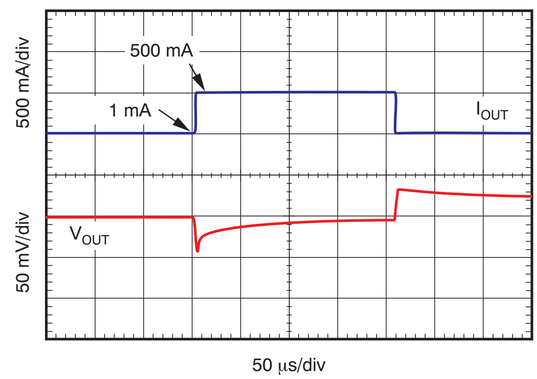


Figure 16. Load Transient Response 1 mA to 500 mA, C_{OUT} = 10 µF

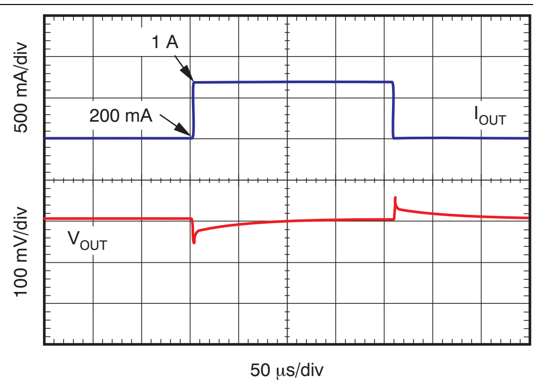


Figure 17. Load Transient Response 200 mA to 1 A, C_{OUT} = 1 µF

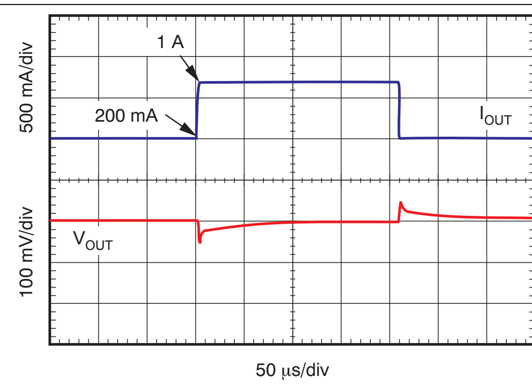


Figure 18. Load Transient Response 200 mA to 1 A, C_{OUT} = 10 µF

Typical Characteristics (continued)

At $V_{IN} = V_{OUT(nom)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = 25°C$, unless otherwise noted.

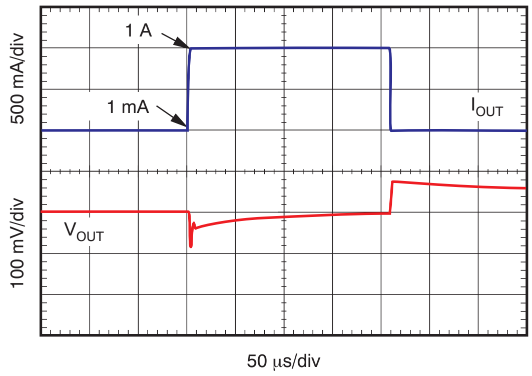


Figure 19. Load Transient Response 1 mA to 1 A, C_{OUT} = 1 µF

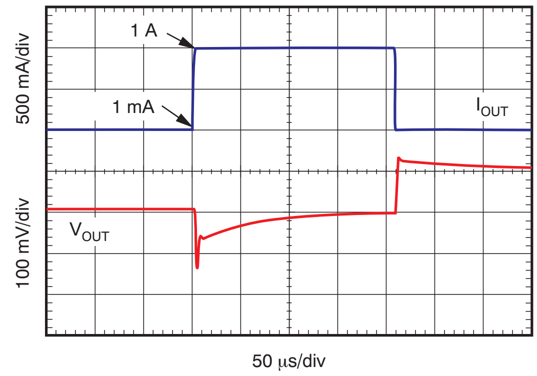


Figure 20. Load Transient Response 1 mA to 1 A, C_{OUT} = 10 µF

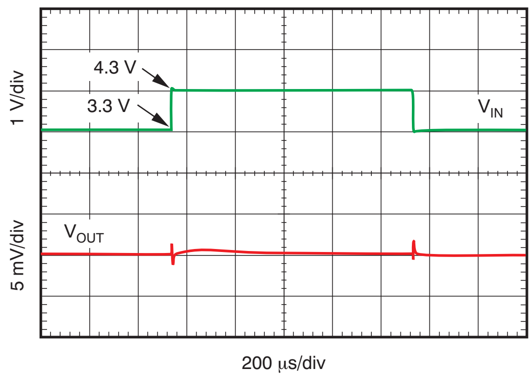


Figure 21. Line Transient Response V_{OUT} = 1.8 V, I_{OUT} = 10 mA

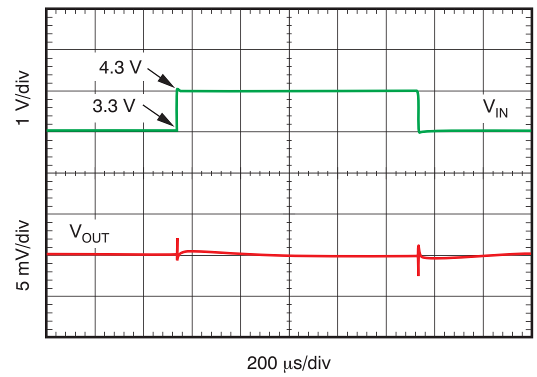


Figure 22. Line Transient Response V_{OUT} = 1.8 V, I_{OUT} = 500 mA

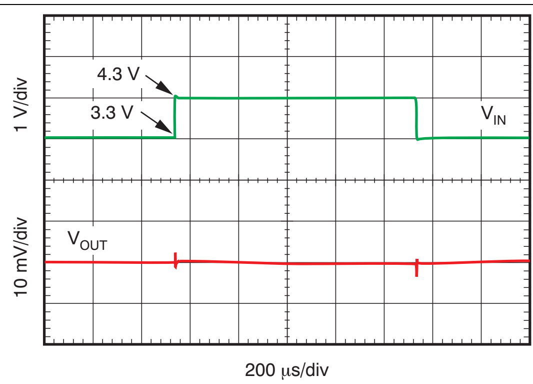


Figure 23. Line Transient Response V_{OUT} = 1.8 V, I_{OUT} = 1 A

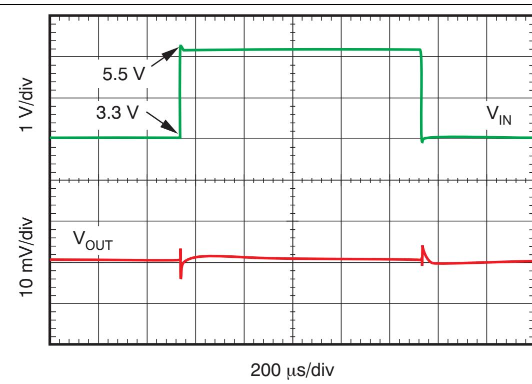


Figure 24. Line Transient Response V_{OUT} = 1.8 V, I_{OUT} = 10 mA

Typical Characteristics (continued)

At $V_{IN} = V_{OUT(nom)} + 1.5$ V; $I_{OUT} = 10$ mA, $C_{OUT} = 1.0$ µF, and $T_A = 25°C$, unless otherwise noted.

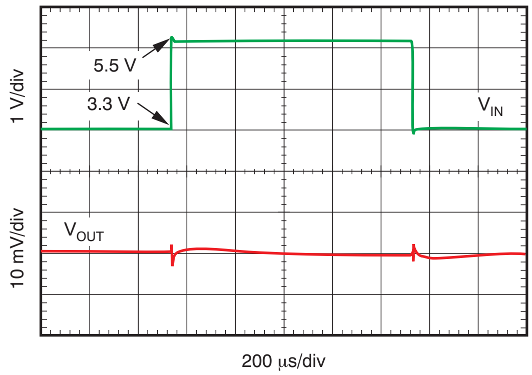


Figure 25. Line Transient Response $V_{OUT} = 1.8$ V, $I_{OUT} = 500$ mA

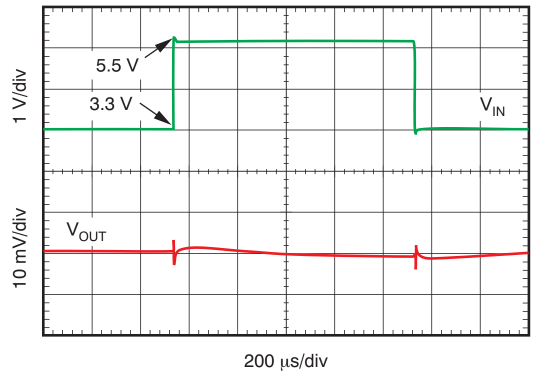


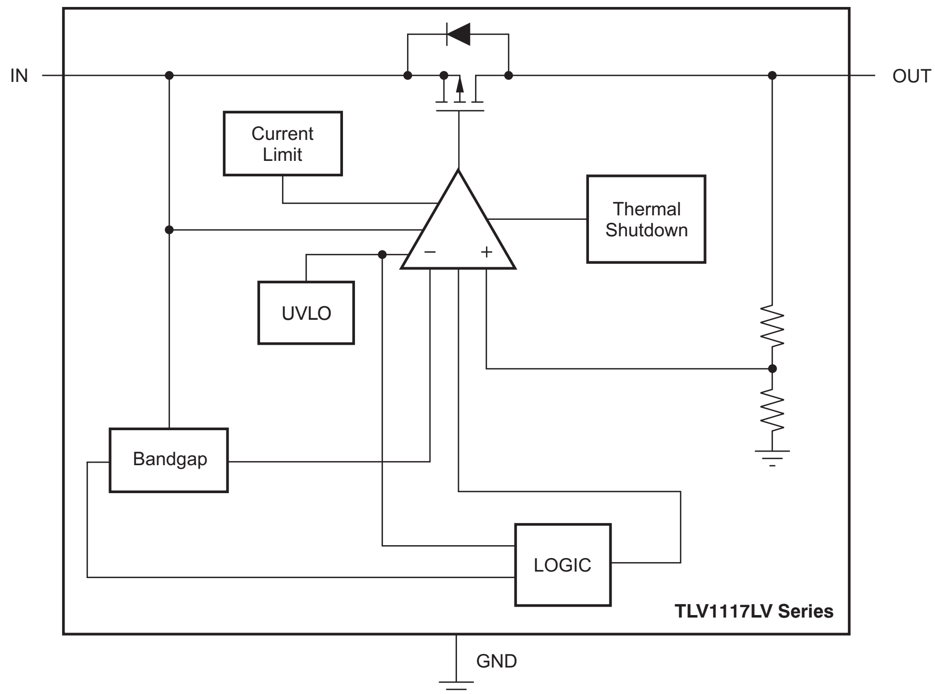
Figure 26. Line Transient Response $V_{OUT} = 1.8$ V, $I_{OUT} = 1$ A

7 Detailed Description

7.1 Overview

The TLV1117LV family of devices are a series of low quiescent current, high PSRR LDOs capable of handling up to 1 A of load current. These devices feature an integrated current limit, thermal shutdown, bandgap reference, and UVLO circuit blocks.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TLV1117LV internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and can be calculated by the formula: $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details

The PMOS pass element in the TLV1117LV device has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.2 Dropout Voltage

The TLV1117LV uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} – V_{OUT})$ approaches dropout.

Feature Description (continued)

7.3.3 Undervoltage Lockout

The TLV1117LV uses an undervoltage lockout (UVLO) circuit keep the output shut off until internal circuitry operating properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.
- The device die temperature is lower than the thermal shutdown temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV1117LV is a low quiescent current linear regulator designed for high current applications. Unlike typical high current linear regulators, the TLV1117LV series consume significantly less quiescent current. These devices deliver excellent line and load transient performance. The device is low noise, and exhibits a very good PSRR. As a result, it is ideal for high current applications that require very sensitive power-supply rails.

This family of regulators offers both current limit and thermal protection. The operating junction temperature range of the device is –40°C to +125°C.

8.2 Typical Application

Figure 27 shows a typical application circuit.

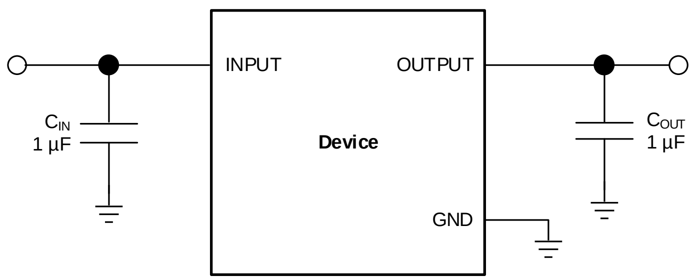


Figure 27. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input Voltage	2.5 V to 3.3 V
Output Voltage	1.8 V
Output Current	500 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

For stability, 1.0-µF ceramic capacitors are required at the output. Higher-valued capacitors improve transient performance. TI recommends the X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. Unlike traditional linear regulators that need a minimum ESR for stability, the TLV1117LV series are ensured to be stable with no ESR. Therefore, cost-effective ceramic capacitors can be used with these devices. Effective output capacitance that takes bias, temperature, and aging effects into consideration must be greater than 0.5 µF to ensure stability of the device.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low-ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located physically close to the power source. If source impedance is greater than 2 Ω, a 0.1-µF, the input capacitor may also be necessary to ensure stability.

8.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude.

8.2.3 Application Curves

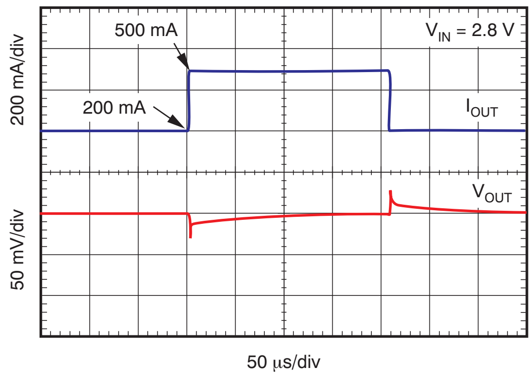


Figure 28. Load Transient Response 200 mA to 500 mA, C_{OUT} = 1 µF

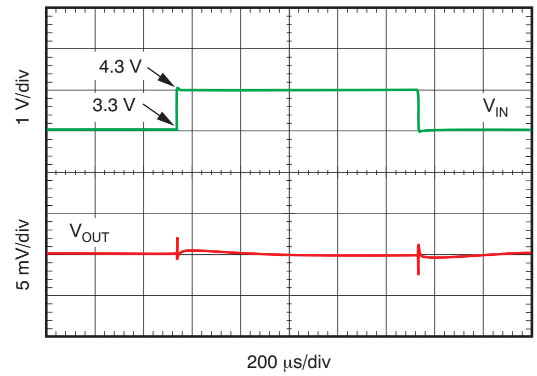


Figure 29. Line Transient Response V_{OUT} = 1.8 V, I_{OUT} = 500 mA

8.3 Do's and Don'ts

Place input and output capacitors as close to the device as possible.

Use a ceramic output capacitor.

Do not use an electrolytic output capacitor.

Do not exceed the device absolute maximum ratings.

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the TLV1117LV. Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during startup or load transient events.

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve characteristic AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. Higher value ESR capacitors may degrade PSRR performance.

10.2 Layout Example

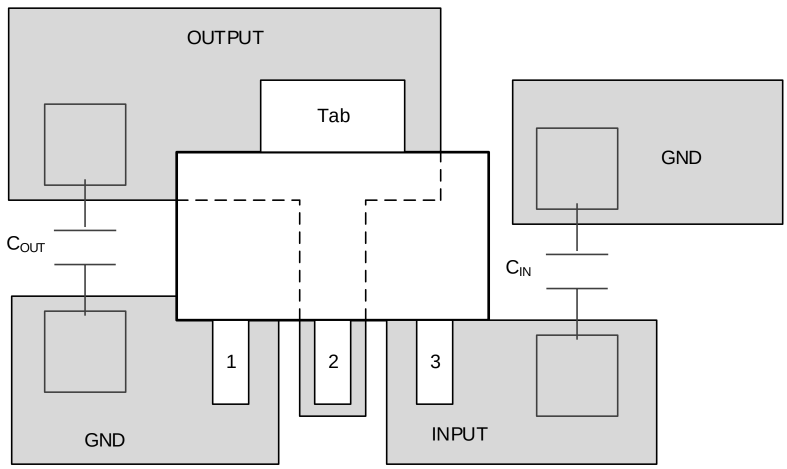


Figure 30. Layout Example

10.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV1117LV has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV1117LV into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1:

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \quad (1)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV1117LV. The TLV1117LV33EVM-714 evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV1117LV is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 3. Available Options(1)

PRODUCT	V_{OUT}
TLV1117LV**xxyyyz**	**xx** is nominal output voltage (for example 33 = 3.3 V) **yyy** is Package Designator **z** is Package Quantity

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

- *TLV1117LV33EVM-714 Evaluation Module User's Guide*, SLVU449.

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV1117LV12	Click here	Click here	Click here	Click here	Click here
TLV1117LV15	Click here	Click here	Click here	Click here	Click here
TLV1117LV18	Click here	Click here	Click here	Click here	Click here
TLV1117LV25	Click here	Click here	Click here	Click here	Click here
TLV1117LV28	Click here	Click here	Click here	Click here	Click here
TLV1117LV30	Click here	Click here	Click here	Click here	Click here
TLV1117LV33	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117LV12DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SI	Samples
TLV1117LV12DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SI	Samples
TLV1117LV15DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VR	Samples
TLV1117LV15DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VR	Samples
TLV1117LV18DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SH	Samples
TLV1117LV18DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SH	Samples
TLV1117LV25DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VS	Samples
TLV1117LV25DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VS	Samples
TLV1117LV28DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VT	Samples
TLV1117LV28DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VT	Samples
TLV1117LV30DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VU	Samples
TLV1117LV30DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	VU	Samples
TLV1117LV33DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TJ	Samples
TLV1117LV33DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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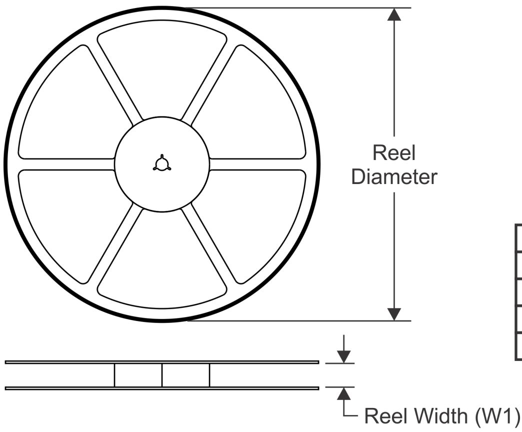
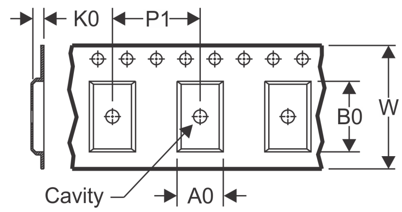
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

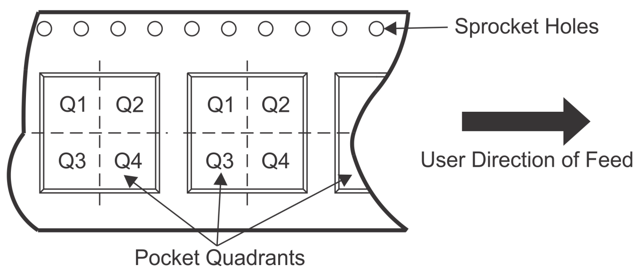


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

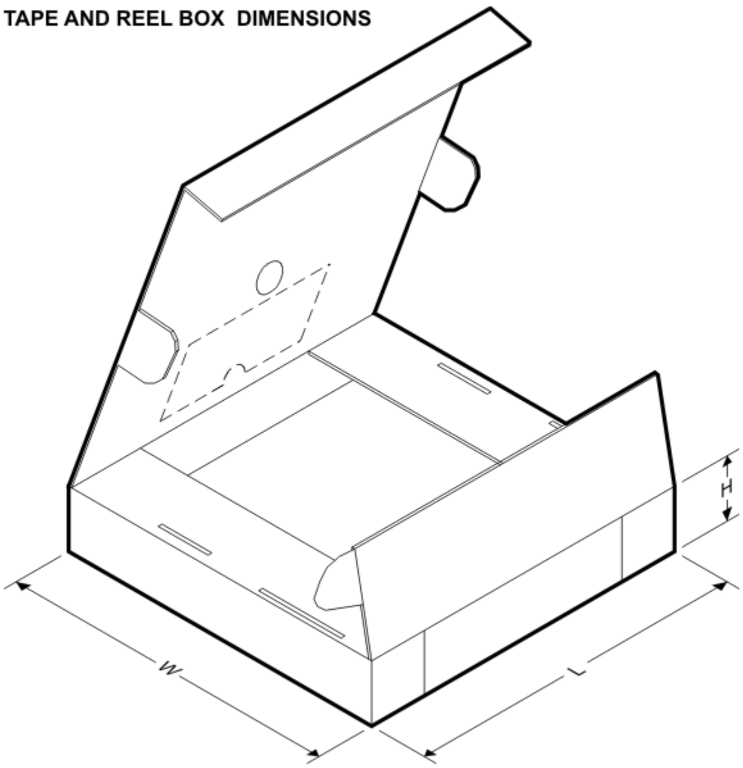


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117LV12DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV12DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV12DCYT	SOT-223	DCY	4	250	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV12DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV15DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV15DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV15DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV15DCYT	SOT-223	DCY	4	250	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV18DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV18DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV18DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV18DCYT	SOT-223	DCY	4	250	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV25DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV25DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV25DCYT	SOT-223	DCY	4	250	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV25DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV28DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV28DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117LV30DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV30DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV30DCYT	SOT-223	DCY	4	250	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV30DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV33DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV33DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV33DCYT	SOT-223	DCY	4	250	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117LV33DCYT	SOT-223	DCY	4	250	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

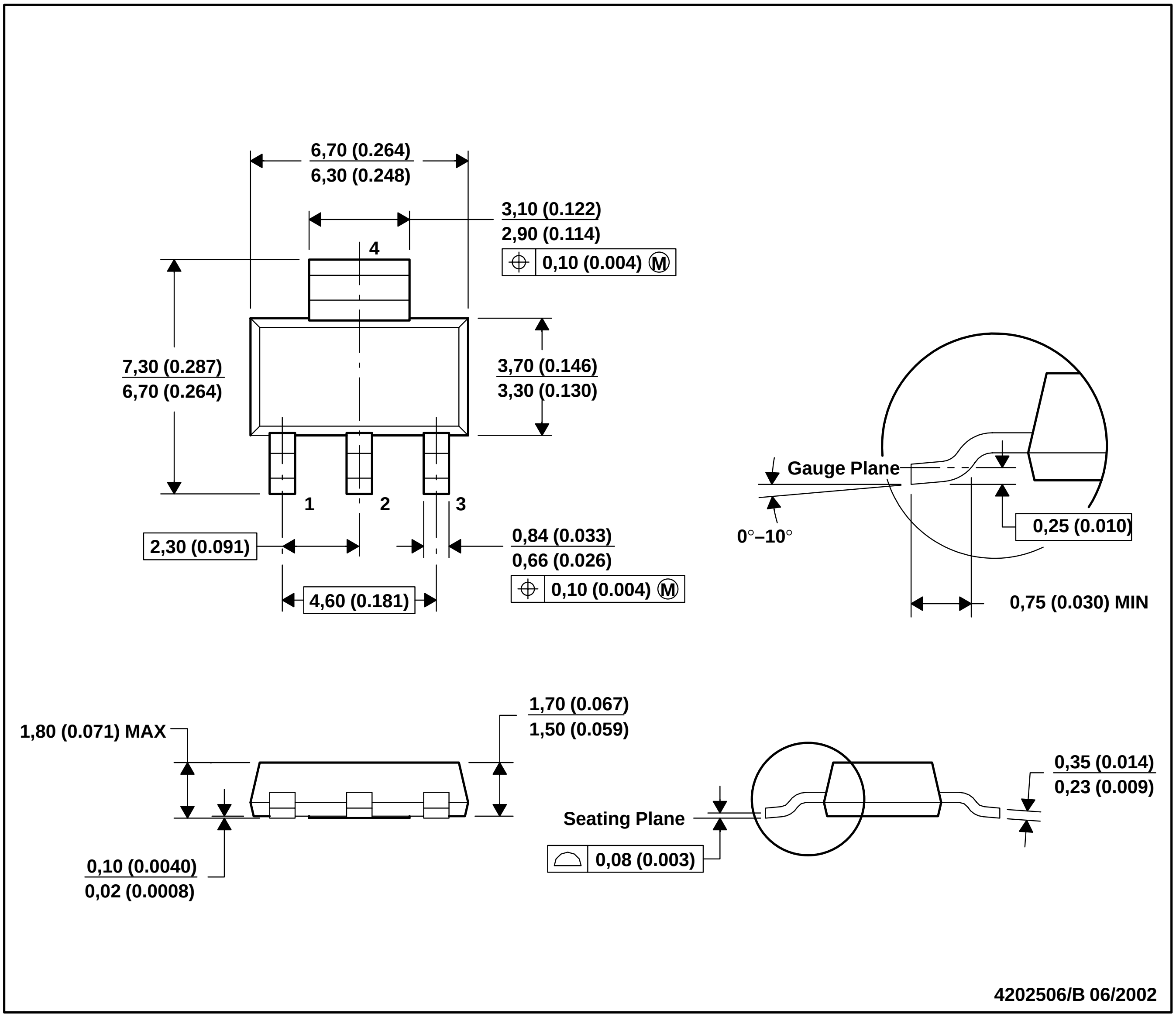


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117LV12DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV12DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117LV12DCYT	SOT-223	DCY	4	250	350.0	334.0	47.0
TLV1117LV12DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV15DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV15DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117LV15DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV15DCYT	SOT-223	DCY	4	250	350.0	334.0	47.0
TLV1117LV18DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0

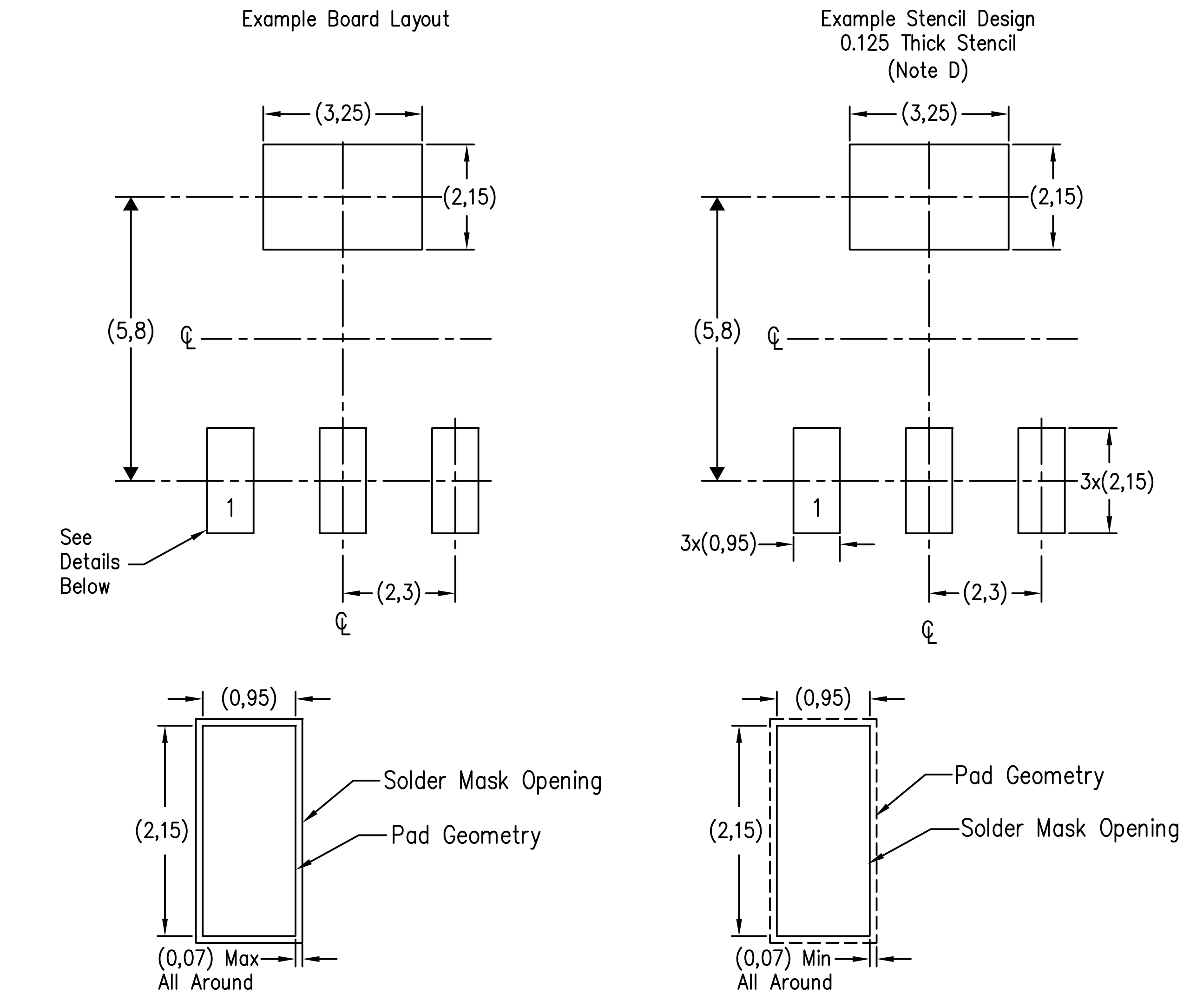
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117LV18DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117LV18DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV18DCYT	SOT-223	DCY	4	250	350.0	334.0	47.0
TLV1117LV25DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV25DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117LV25DCYT	SOT-223	DCY	4	250	350.0	334.0	47.0
TLV1117LV25DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV28DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV28DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV30DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV30DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117LV30DCYT	SOT-223	DCY	4	250	350.0	334.0	47.0
TLV1117LV30DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV33DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV33DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117LV33DCYT	SOT-223	DCY	4	250	350.0	334.0	47.0
TLV1117LV33DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



Example, non–solder mask defined pad.
(Preferred)

Example, solder mask defined pad.

4210278/C 07/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.