



**THE DATASHEET OF  
TLV70133DBVT**



## 24-V Input Voltage, 150-mA, Ultralow I<sub>Q</sub> Low-Dropout Regulators

### FEATURES

- **Wide Input Voltage Range: 2.5 V to 24 V**
- **Low 3.2- $\mu$ A Quiescent Current**
- **Ground Pin Current: 3.4  $\mu$ A at 100-mA I<sub>OUT</sub>**
- **Stable with Any Capacitor (> 0.47  $\mu$ F)**
- **Available in SOT23-5 Package**
- **Operating Junction Temperature:  
–40°C to +125°C**

### APPLICATIONS

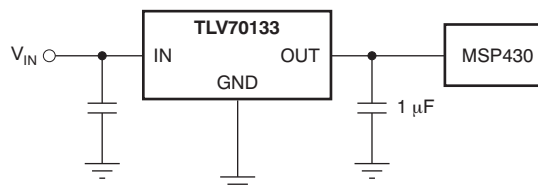
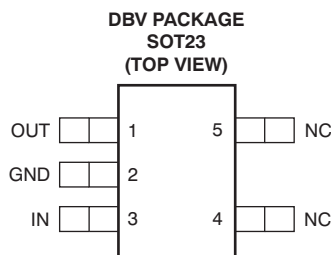
- **Ultralow Power Microcontrollers**
- **E-Meters**
- **Fire Alarms/Smoke Detector Systems**
- **Handset Peripherals**
- **Industrial/Automotive Applications**
- **Remote Controllers**
- **Zigbee™ Networks**
- **PDA's**
- **Portable, Battery-Powered Equipment**

### DESCRIPTION

The TLV701xx series of low-dropout (LDO) regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power management attachment to low-power microcontrollers, such as the [MSP430](#).

The TLV701xx operates over a wide operating input voltage of 2.5 V to 24 V. Thus, it is an excellent choice for both battery-powered systems as well as industrial applications that see large line transients.

The TLV701xx is available in a 3-mm × 3-mm SOT23-5 package that is ideal for cost-effective board manufacturing.


**PRODUCT PREVIEW**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**AVAILABLE OPTIONS<sup>(1)</sup>**

PRODUCT	V <sub>OUT</sub>
TLV701xxyyyz	<b>XX</b> is nominal output voltage (for example, 30 = 3.0 V) <b>YYY</b> is Package Designator <b>Z</b> is Package Quantity

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage <sup>(2)</sup>	IN	-0.3	24	V
Current source	OUT	Internally limited		
Temperature	Operating junction, T <sub>J</sub>	-40	+150	°C
	Storage, T <sub>stg</sub>	-65	+150	°C
Electrostatic Discharge Rating <sup>(3)</sup>	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.
- (3) ESD testing is performed according to the respective JEDEC standard.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		TLV701XX	UNITS
		DBV	
		5 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	213.1	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	110.9	
θ <sub>JB</sub>	Junction-to-board thermal resistance	97.4	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	22.0	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	78.4	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

PRODUCT PREVIEW

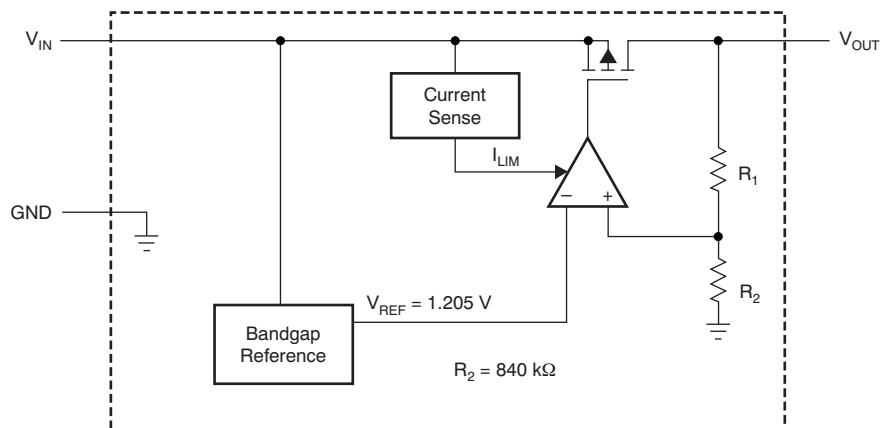
**ELECTRICAL CHARACTERISTICS:  $T_A = +25^\circ\text{C}$**

All values are at  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ , and  $C_{OUT} = 1\text{ }\mu\text{F}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TLV701xx			UNIT	
		MIN	TYP	MAX		
$V_O$	Input voltage range			24	V	
	Output voltage range	1.2		5	V	
$V_{OUT}$	DC output accuracy	-2		2	%	
$\Delta V_O$ for $\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 1\text{ V} < V_{IN} < 24\text{ V}$		20	50	mV
$\Delta V_O$ for $\Delta I_{OUT}$	Load regulation	$1\text{ mA} < I_{OUT} < 10\text{ mA}$		6		mV
		$1\text{ mA} < I_{OUT} < 50\text{ mA}$		19		mV
		$1\text{ mA} < I_{OUT} < 100\text{ mA}$		29	50	mV
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$I_{OUT} = 10\text{ mA}$		75		mV
		$I_{OUT} = 50\text{ mA}$		400		mV
$I_{CL}$	Output current limit	$V_{OUT} = 0\text{ V}$		160	1000	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{ mA}$		3.2	4.5	$\mu\text{A}$
		$I_{OUT} = 100\text{ mA}$		3.4	5.5	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$f = 100\text{ kHz}$ , $C_{OUT} = 10\text{ }\mu\text{F}$		60		dB

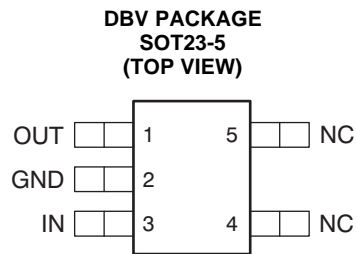
(1)  $V_{IN} = V_{OUT(NOM)} - 0.1\text{ V}$ .

**FUNCTIONAL BLOCK DIAGRAM**



**PRODUCT PREVIEW**

## PIN CONFIGURATIONS



**Table 1. Pin Descriptions**

TLV701xx		
NAME	DBV	DESCRIPTION
GND	2	Ground
IN	3	Unregulated input voltage.
OUT	1	Regulated output voltage. Any capacitor 1 $\mu$ F or greater between this pin and ground is needed for stability.
NC	4, 5	No connection. This pin can be left open or tied to ground for improved thermal performance.

TYPICAL CHARACTERISTICS

LINE REGULATION

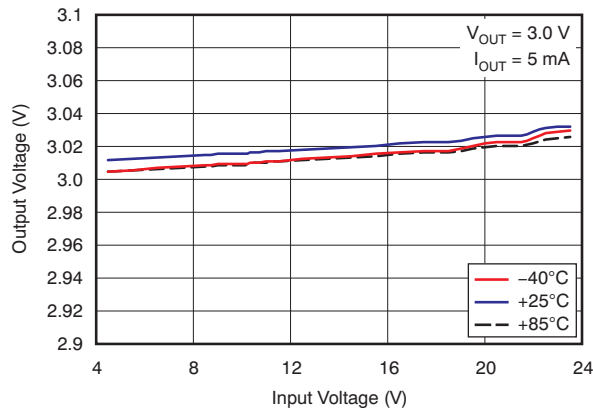


Figure 1.

LOAD REGULATION  
( $V_{OUT} = 3.0\text{ V}$ )

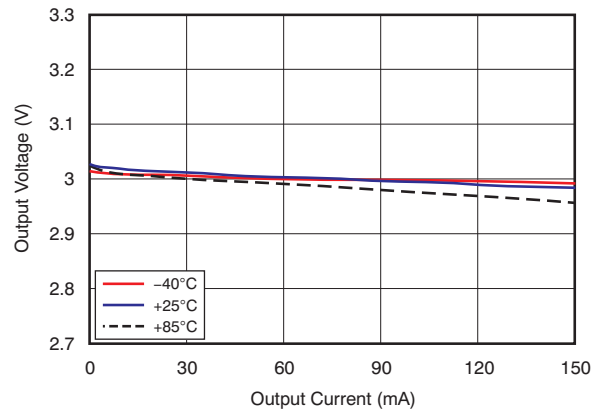


Figure 2.

OUTPUT VOLTAGE vs  
JUNCTION TEMPERATURE

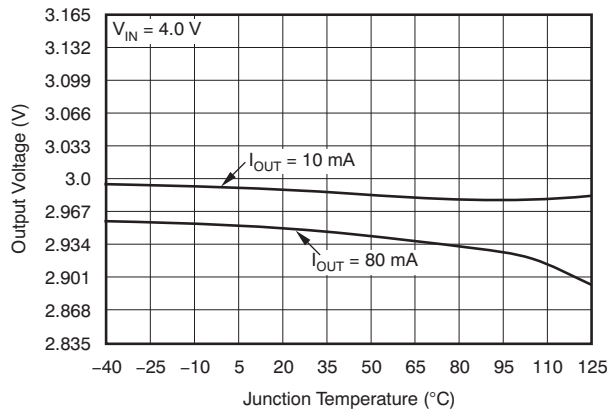


Figure 3.

DROPOUT VOLTAGE vs INPUT VOLTAGE

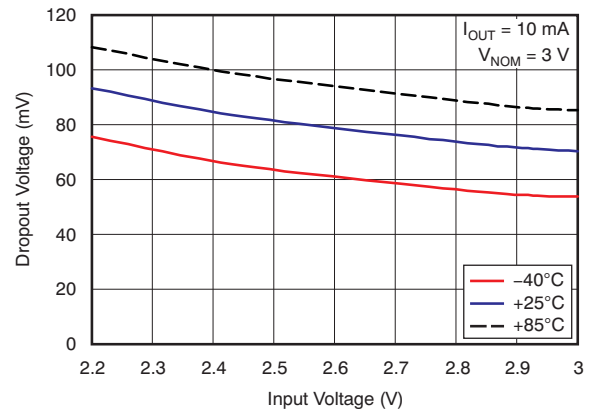


Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

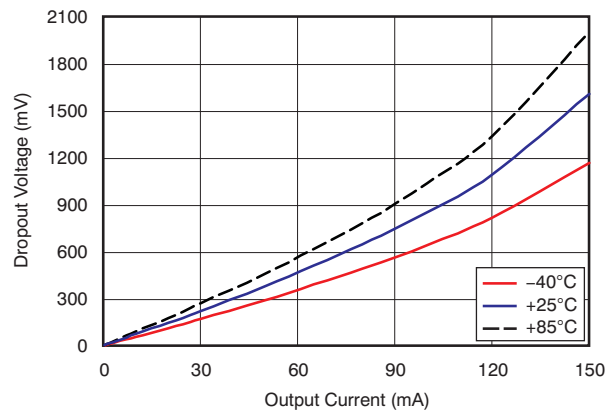


Figure 5.

GROUND CURRENT vs JUNCTION TEMPERATURE

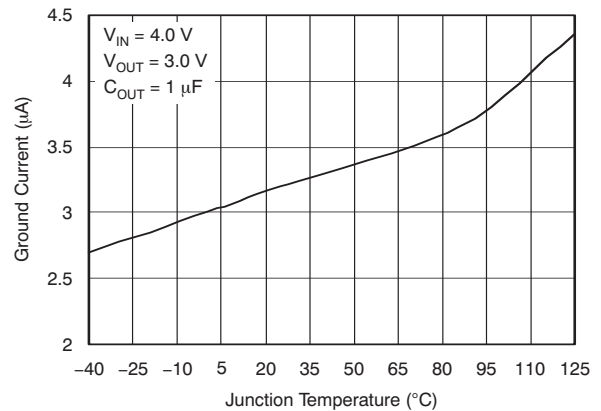


Figure 6.

PRODUCT PREVIEW

**TYPICAL CHARACTERISTICS (continued)**

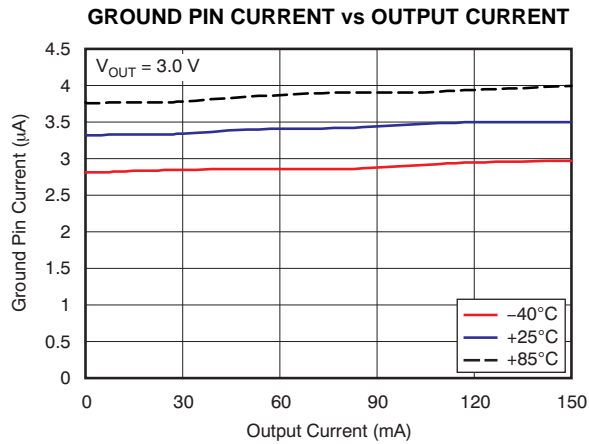


Figure 7.

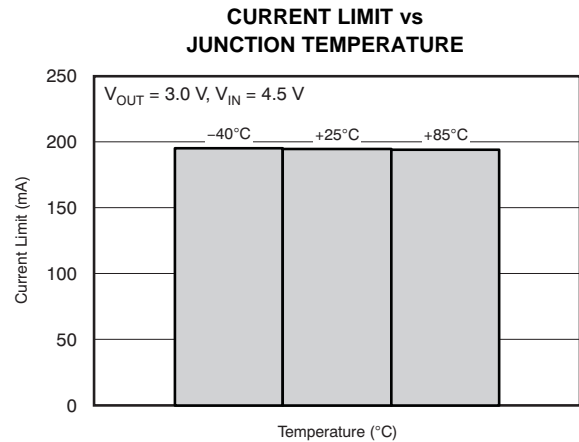


Figure 8.

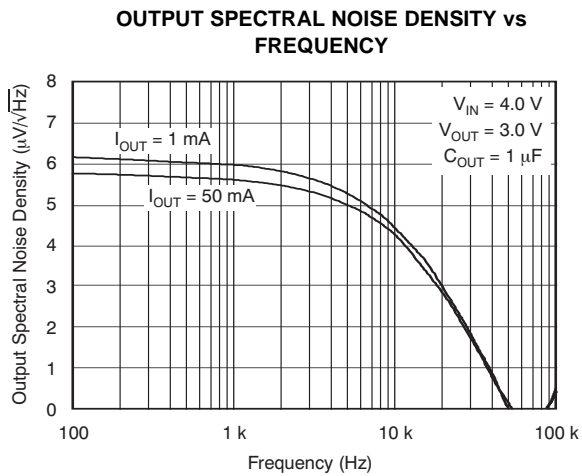


Figure 9.

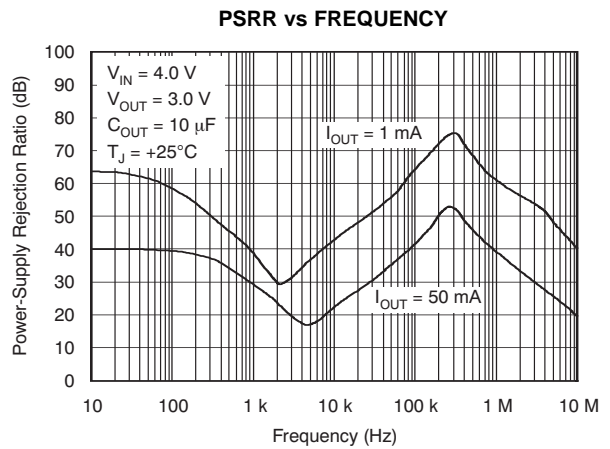


Figure 10.

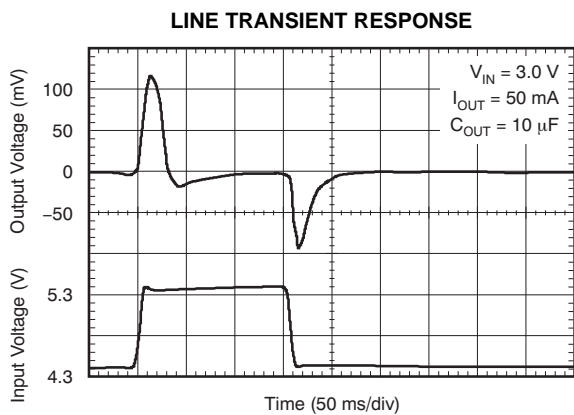


Figure 11.

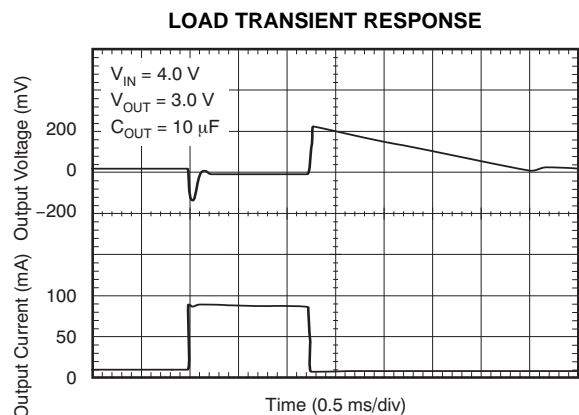


Figure 12.

PRODUCT PREVIEW

## APPLICATION INFORMATION

The TLV701xx series of devices belong to a family of ultralow,  $I_Q$ , low-dropout (LDO) regulators.  $I_Q$  remains fairly constant over the complete output load current and temperature range. The devices are ensured to operate over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TLV701 requires a 1- $\mu\text{F}$  or larger capacitor connected between OUT and GND for stability. Ceramic or tantalum capacitors can be used. Larger value capacitors result in better transient and noise performance.

Although an input capacitor is not required for stability, when a 0.1- $\mu\text{F}$  or larger capacitor is placed between IN and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large, fast rise time load transients are anticipated.

### BOARD LAYOUT RECOMMENDATIONS

Input and output capacitors should be placed as close to the device pins as possible. To avoid interference of noise and ripple on the board, it is recommended that the board be designed with separate ground planes for  $V_{\text{IN}}$  and  $V_{\text{OUT}}$ , with the ground plane connected only at the device GND pin. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

### POWER DISSIPATION AND JUNCTION TEMPERATURE

To ensure reliable operation, worst-case junction temperature should not exceed  $+125^{\circ}\text{C}$ . This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(\text{max})}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(\text{max})}$ .

The maximum power dissipation limit is determined using [Equation 1](#):

$$P_{D(\text{max})} = \frac{T_{J\text{max}} - T_A}{R_{\theta\text{JA}}} \quad (1)$$

where:

$T_{J\text{max}}$  is the maximum allowable junction temperature.

$R_{\theta\text{JA}}$  is the thermal resistance junction-to-ambient for the package.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using [Equation 2](#):

$$P_D = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} \quad (2)$$

Power dissipation that results from quiescent current is negligible.

### REGULATOR PROTECTION

The TLV701xx series of LDO regulators use a PMOS-pass transistor that has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TLV701xx features internal current limiting. During normal operation, the TLV701xx limits output current to approximately 250 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the rated maximum operating junction temperature of  $+125^{\circ}\text{C}$ . Continuously running the device under conditions where the junction temperature exceeds  $+125^{\circ}\text{C}$  degrades device reliability.

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 2](#).

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70130DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YBVA	<a href="#">Samples</a>
TLV70130DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YBVA	<a href="#">Samples</a>
TLV70133DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YBWA	<a href="#">Samples</a>
TLV70133DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YBWA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

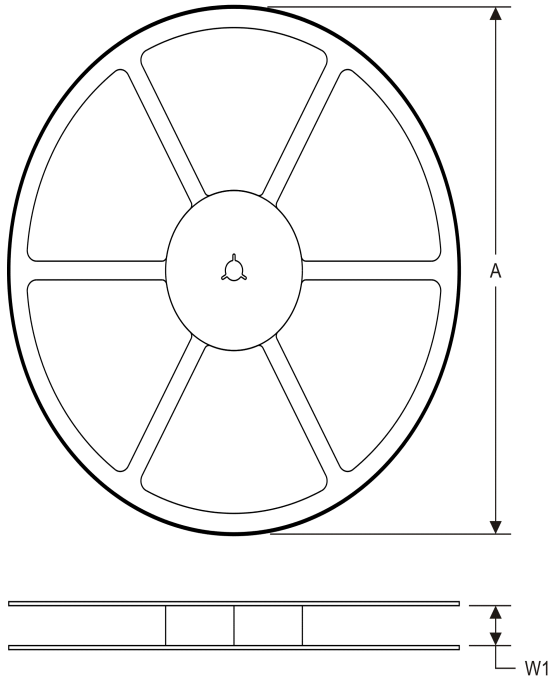
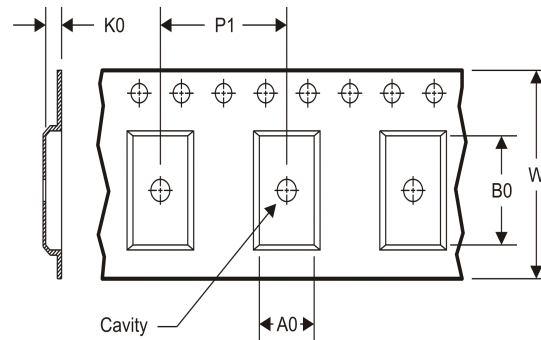
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70130DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70130DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70133DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70133DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70130DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70130DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70133DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70133DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

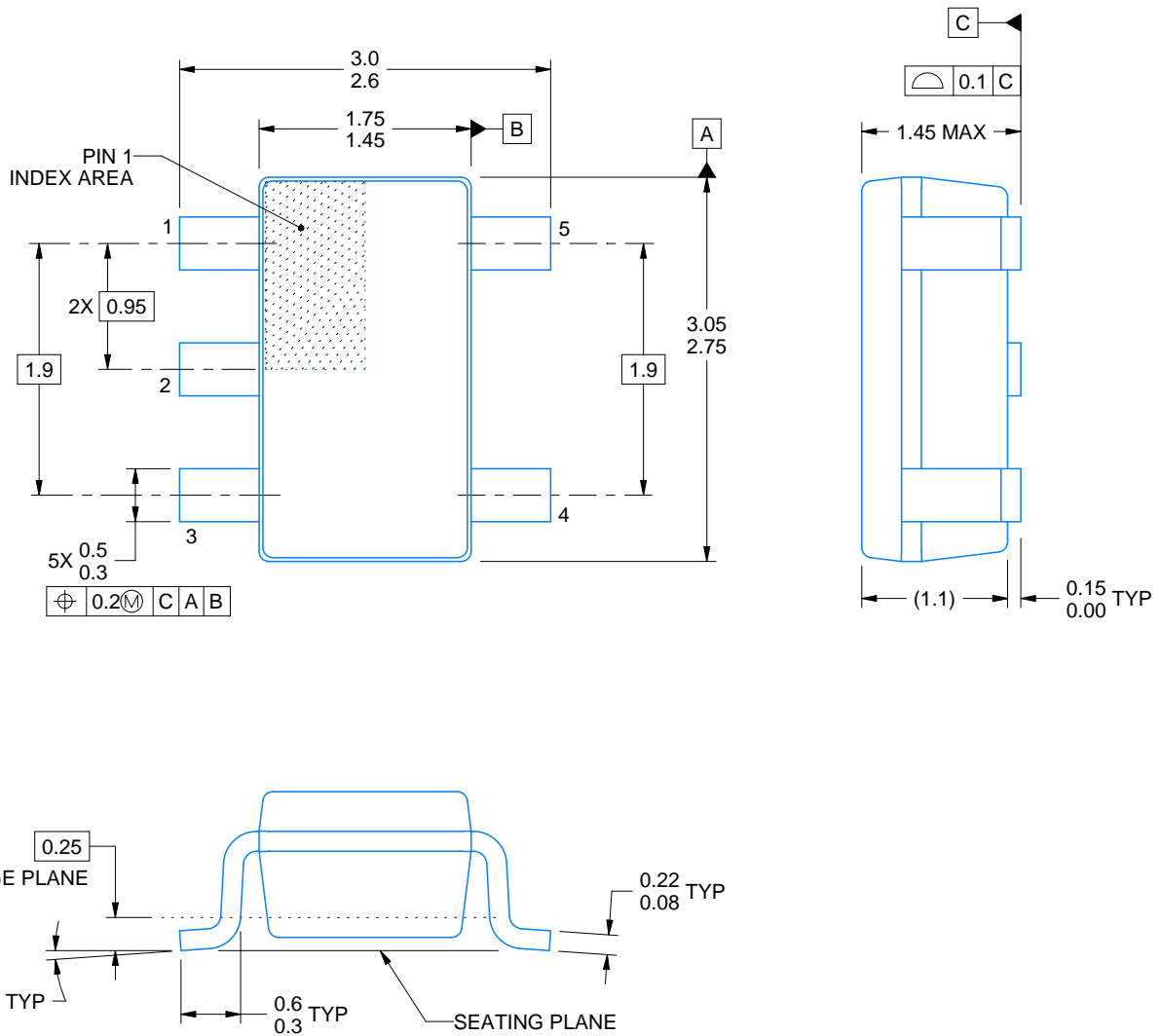


DBV0005A

# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

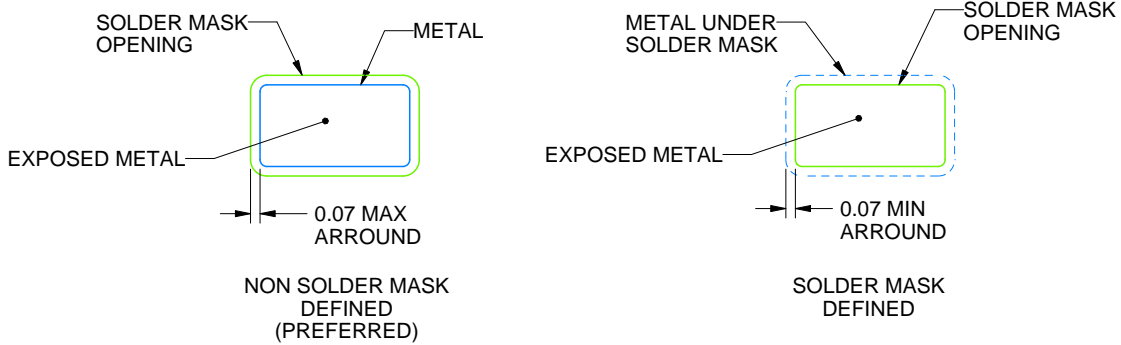
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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