# MIC5167

## 1MHz, 6A, Integrated Switch, High-Efficiency, Synchronous Buck DDR Memory Terminator

## General Description

The MIC5167 is a high-efficiency, 6A, integrated switch, synchronous regulator designed for use as a double data rate (DDR) or quad data rate (QDR) terminator. The MIC5167 is optimized for highest efficiency, achieving more than 94% efficiency while still switching at 1MHz over a broad range. The device works with a small 0.4µH inductor and 300µF output capacitor. The MIC5167 offers a simple, low-cost, JEDEC-compliant solution for terminating high-speed, low-voltage, digital buses (i.e. DDR, DDR2, DDR3, DDR3L, DDR3UL, DDR4, SCSI, GTL, SSTL, HSTL, LV-TTL, LV-PECL, and LV_ECL) with a Power-Good (PG) output.

The output voltage is controlled externally by input to the VDDQ pin. The output voltage is one-half the voltage applied to the VDDQ pin. The output voltage can be adjusted down to 0.6V to address low-voltage power needs. The MIC5167 will source 6A and sink up to 6A.

A window comparator monitors the output voltage and controls the PG output. If the output voltage is outside ±15% limit of VREF the PG is driven low.

The MIC5167 is available in a 24-pin 4mm x 4mm MLF® with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

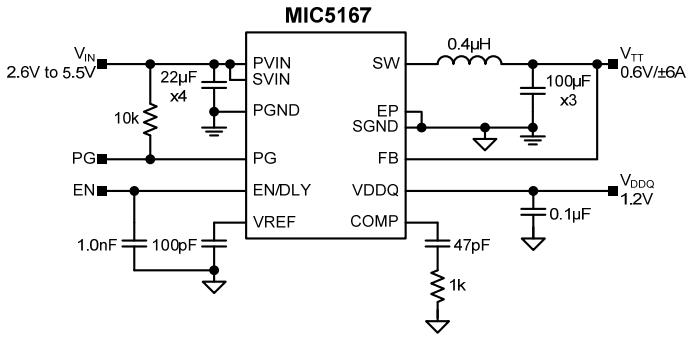
## Features

- Input voltage range: 2.6V to 5.5V
- $V_{TT}$ voltage adjustable down to 0.35V
- Output load current up to ±6A
- Power-Good (PG) fault flag
- Efficiency > 94% across a broad load range
- Ultra-fast transient response
- Easy RC compensation
- 100% maximum duty cycle
- Fully-integrated MOSFET switches
- Micropower shutdown
- Thermal-shutdown and current-limit protection
- 24-pin 4mm x 4mm MLF®
- –40°C to +125°C junction temperature range

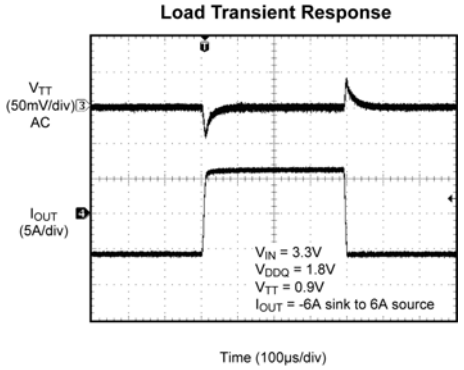
## Applications

- Double data rate (DDR) or quad data rate (QDR) memory terminator
- High power density point-of-load conversion
- Servers and routers
- DVD recorders / Blu-ray players
- Computing peripherals
- Base stations
- FPGAs, DSP, and low-voltage ASIC power

## Typical Application




**MIC5167 ±6A Synchronous Buck DDR Terminator**

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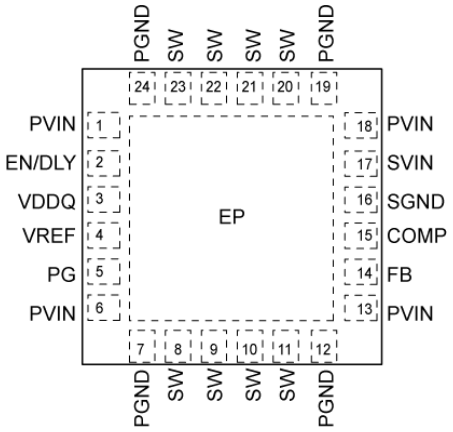
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

## Ordering Information

| Part Number | Voltage | Junction Temperature Range | Package | Lead Finish |
|---|---|---|---|---|
| MIC5167YML | Adjustable | –40°C to +125°C | 24-Pin 4x4 MLF® | Pb-Free |

**Note:**
MLF® is a GREEN RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

## Pin Configuration




**24-Pin 4mm x 4mm MLF® (ML)**

## Pin Description

| Pin Number | Pin Name | Description |
|---|---|---|
| 1, 6, 13, 18 | PVIN | Power Supply Voltage (Input): The PVIN pins are the input supply to the internal P-Channel Power MOSFET. A 22µF ceramic is recommended for bypassing at each PVIN pin. The SVIN pin must be connected to the PVIN pin. |
| 2 | EN/DLY | Enable/Delay (Input): This pin is internally fed with a 1µA current source from SVIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V. This pin is pulled low when the input voltage is lower than the UVLO threshold. |
| 3 | VDDQ | VDDQ (Input): VDDQ is connected to an internal precession divider which provides the reference voltage (VREF). |
| 4 | VREF | VTT Reference (Output): This output provides an output of the internal reference voltage VDDQ/2. Connect a 100pF capacitor to ground at this pin. |
| 5 | PG | PG (Output): This is an open drain output that indicates when the output voltage is within ±15% of its nominal voltage. The PG flag is asserted without delay when the enable is set low or when the output goes outside ±15% the window threshold. |
| 14 | FB | Feedback (Input): Input to the error amplifier. |
| 15 | COMP | Compensation pin (Input): The MIC5167 uses an internal compensation network containing a fixed-frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor to the COMP pin will add the necessary pole and zero for voltage mode loop stability using low value, low-ESR ceramic capacitors. |
| 16 | SGND | Signal Ground: Internal signal ground for all low power circuits. |

## Pin Description (Continued)

| Pin Number | Pin Name | Description |
|---|---|---|
| 17 | SVIN | Signal Power Supply Voltage (Input): This pin is connected externally to the PVIN pin. A 22µF ceramic capacitor from the SVIN pin to SGND must be placed next to the IC. |
| 7, 12, 19, 24 | PGND | Power Ground: Internal ground connection to the source of the internal N-Channel MOSFETs. |
| 8, 9, 10, 11, 20, 21, 22, 23 | SW | Switch (Output): This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high-frequency, high-power connection; therefore traces should be kept as short and as wide as practical. |
| EP | GND | Exposed Pad (Power): Must be connected to a GND plane for full output power to be realized. |

## Absolute Maximum Ratings[1,2]

$PV_{IN}$ to PGND ..... –0.3V to 6V
$SV_{IN}$ to PGND ..... –0.3V to $PV_{IN}$
$V_{DDQ}$ to PGND ..... –0.3V to $PV_{IN}$
$V_{SW}$ to PGND ..... –0.3V to $PV_{IN}$
$V_{EN/DLY}$ to PGND ..... –0.3V to $PV_{IN}$
$V_{PG}$ to PGND ..... –0.3V to $PV_{IN}$
PGND to SGND ..... –0.3V to 0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... 260°C

## Operating Ratings[3]

Supply Voltage ($PV_{IN}$,$SV_{IN}$) ..... 2.6V to 5.5V
Supply Voltage ($V_{DDQ}$) ..... 0.7V to $PV_{IN}$
Power-Good (PG) Voltage ($V_{PG}$) ..... 0V to $PV_{IN}$
Enable Input ($V_{EN/DLY}$) ..... 0V to $PV_{IN}$
Junction Temperature ($T_J$) ..... –40°C ≤ $T_J$ ≤ +125°C
Package Thermal Resistance
4mm x 4mm MLF®-24 ($\theta_{JC}$) ..... 14°C/W
4mm x 4mm MLF®-24 ($\theta_{JA}$) ..... 40°C/W

## Electrical Characteristics[4]

$SV_{IN}$ = $PV_{IN}$ = $V_{EN/DLY}$ = 3.3V, $V_{FB}$ = $V_{TT}$ = 0.6V, $T_A$ = 25°C, unless noted. **Bold** values indicate –40°C< $T_J$ < +125°C.

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Power Input Supply** | | | | | |
| Input Voltage Range ($PV_{IN}$) | | **2.6** | | **5.5** | V |
| Undervoltage Lockout (UVLO) Trip Level | $PV_{IN}$ Rising | **2.4** | 2.5 | **2.6** | V |
| UVLO Hysteresis | | | 280 | | mV |
| Quiescent Supply Current | $V_{FB}$ = 0.9V (not switching) | | 0.85 | **1.3** | mA |
| Shutdown Current | $V_{EN/DLY}$ = 0V | | 5 | **10** | µA |
| **$V_{TT}$ Output** | | | | | |
| $V_{TT}$ Output Voltage | $V_{DDQ}$ =1.2V | **0.588** | 0.6 | **0.612** | V |
| Load Regulation | $V_{FB}$ =0.6V, $I_{OUT}$ = -6A to +6A | | 0.4 | | % |
| Line Regulation | $V_{FB}$ = 0.6V; $V_{IN}$ = 2.6 to 5.5V, $I_{LOAD}$= 100mA | | 0.2 | | % |
| FB Pin Bias Current | $V_{FB}$ = 0.6V | | 10 | | nA |
| **Enable Control** | | | | | |
| EN/DLY Threshold Voltage | | **1.14** | 1.24 | **1.34** | V |
| EN Hysteresis | | | 20 | | mV |
| EN/DLY Source Current | $V_{EN/DLY}$ = 0.5V; $V_{IN}$ = 2.9V and $V_{IN}$ = 5.5V | **0.7** | 1.0 | **1.3** | µA |
| **Oscillator** | | | | | |
| Switching Frequency | $I_{OUT}$ = 0A | 0.8 | 1.0 | 1.2 | MHz |
| Maximum Duty Cycle | $V_{FB}$ ≤ 0.5V | 100 | | | % |
| **Short-Current Protection** | | | | | |
| Sourcing Current Limit | $V_{FB}$ = 0.5V | **6.5** | 9 | **14** | A |
| **Internal FETs** | | | | | |
| Top-MOSFET $R_{DS(ON)}$ | $V_{FB}$ = 0.5V, $I_{SW}$ = 1A | | 30 | | mΩ |
| Bottom-MOSFET $R_{DS(ON)}$ | $V_{FB}$ = 0.9V, $I_{SW}$ = -1A | | 25 | | mΩ |
| SW Leakage Current | $PV_{IN}$ = 5.5V, $V_{SW}$ = 5.5V, $V_{EN}$ = 0V | | | **60** | µA |
| $V_{IN}$ Leakage Current | $PV_{IN}$ = 5.5V, $V_{SW}$ = 0V, $V_{EN}$ = 0V | | | **25** | |

## Electrical Characteristics[4] (Continued)

$SV_{IN}$ = $PV_{IN}$ = $V_{EN/DLY}$ = 3.3V, $V_{FB}$ = $V_{TT}$ = 0.6V, $T_A$ = 25°C, unless noted. **Bold** values indicate –40°C< $T_J$ < +125°C.

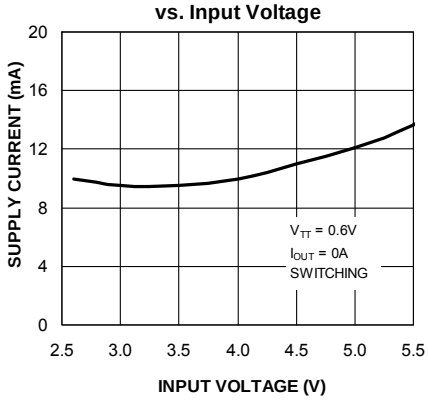
| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Power-Good (PG)** | | | | | |
| PG Window | Threshold % of $V_{TT}$ from $V_{REF}$ | ±10 | ±15 | ±20 | % |
| Hysteresis | | | 2.5 | | % |
| PG Output Low Voltage | $I_{PG}$ = 5mA (sinking), $V_{FB}$ = 0.4V; $V_{EN}$ = $V_{IN}$ | | 130 | | mV |
| PG Leakage Current | $V_{PG}$ = 5.5V; $V_{FB}$ = 0.625V | | | 1.0 | µA |
| | | | | **2.0** | |
| **Thermal Protection** | | | | | |
| Over-Temperature Shutdown | $T_J$ Rising | | 160 | | °C |
| Over-Temperature Shutdown Hysteresis | | | 20 | | °C |

**Notes:**

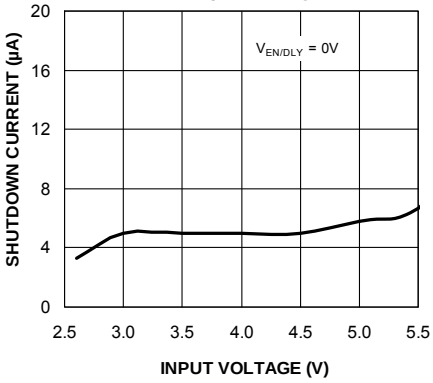
1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended.
3. The device is not guaranteed to function outside its operating rating.
4. Specification for packaged product only.

## Typical Characteristics

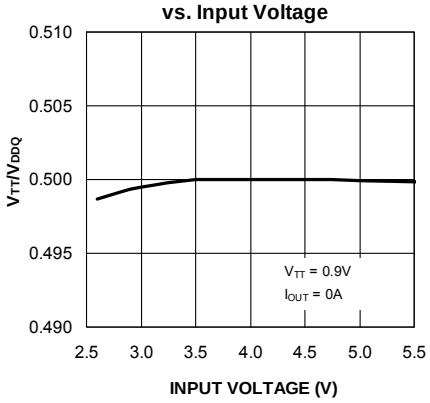
**$V_{IN}$ Operating Supply Current vs. Input Voltage**



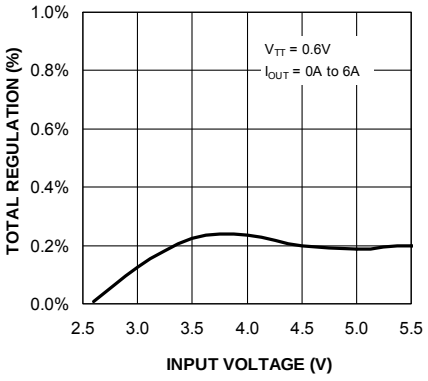

**$V_{IN}$ Shutdown Current vs. Input Voltage**



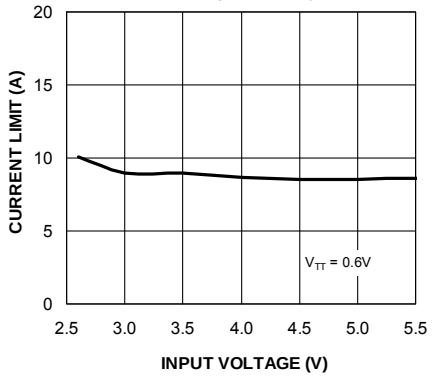

**$V_{TT}/V_{DDQ}$ Tracking Ratio vs. Input Voltage**



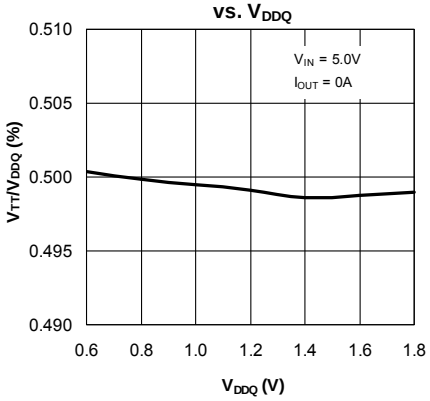

**Load Regulation vs. Input Voltage**



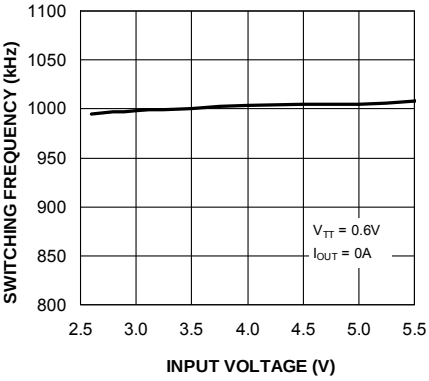

**Current Limit vs. Input Voltage**



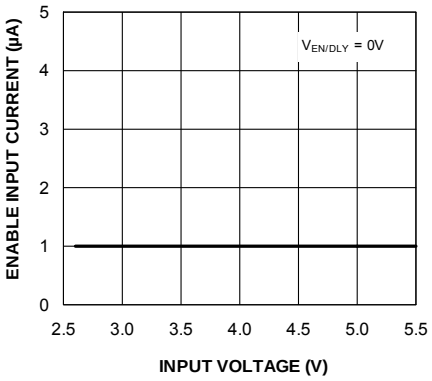

**$V_{TT}/V_{DDQ}$ Tracking Ratio vs. $V_{DDQ}$**



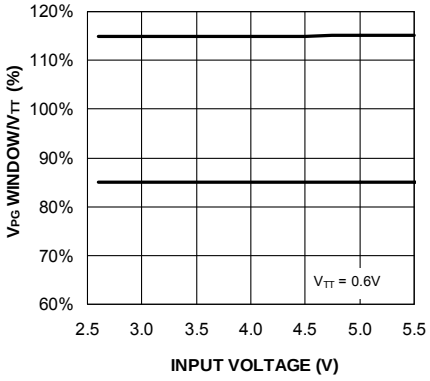

**Switching Frequency vs. Input Voltage**




**Enable Input Current vs. Input Voltage**

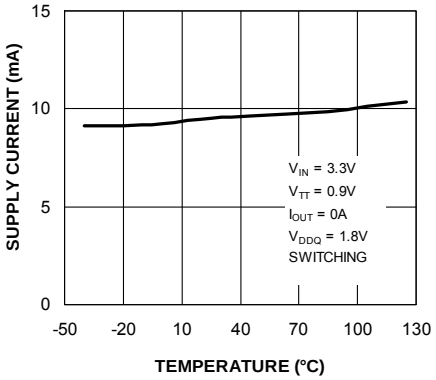



**Power Good Window/$V_{TT}$ Ratio vs. Input Voltage**

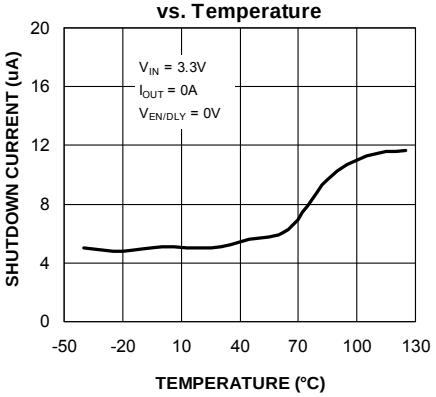


## Typical Characteristics (Continued)

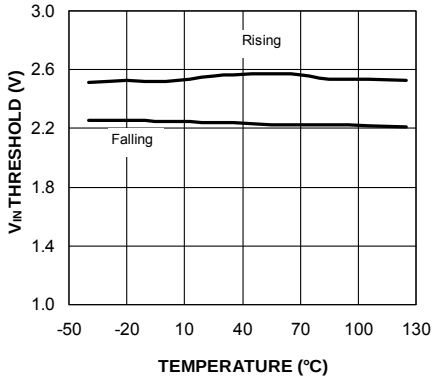
**$V_{IN}$ Operating Supply Current vs. Temperature**



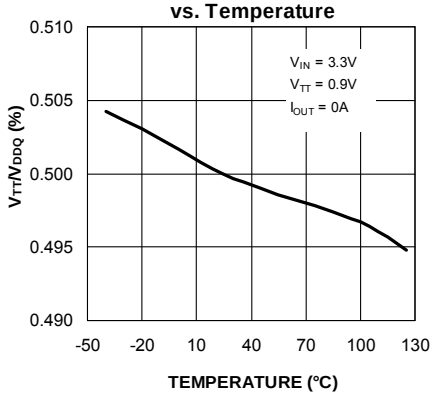

**$V_{IN}$ Shutdown Current vs. Temperature**



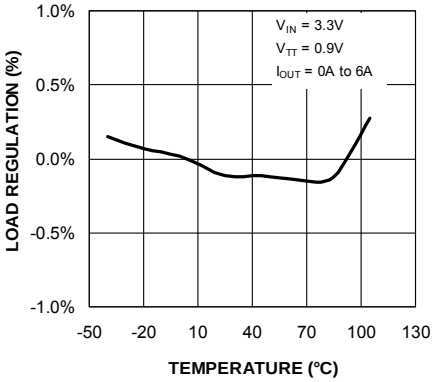

**$V_{IN}$ UVLO Threshold vs. Temperature**



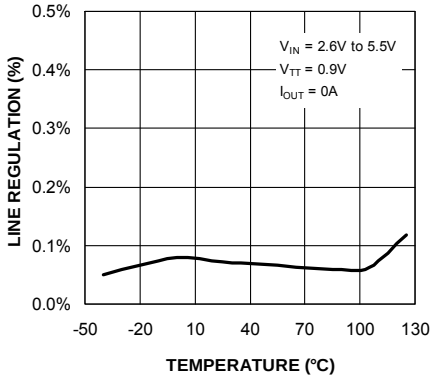

**$V_{TT}/V_{DDQ}$ Tracking Ratio vs. Temperature**



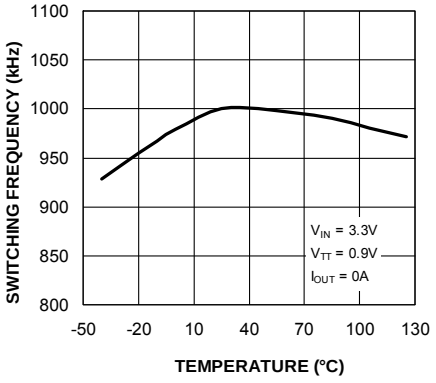

**Load Regulation vs. Temperature**



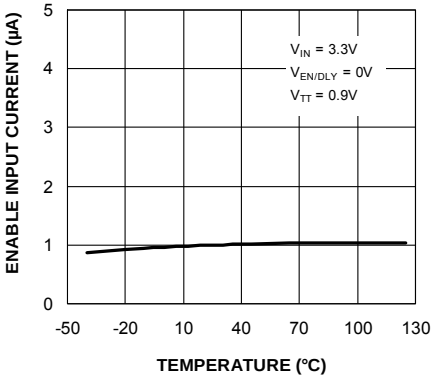

**Line Regulation vs. Temperature**



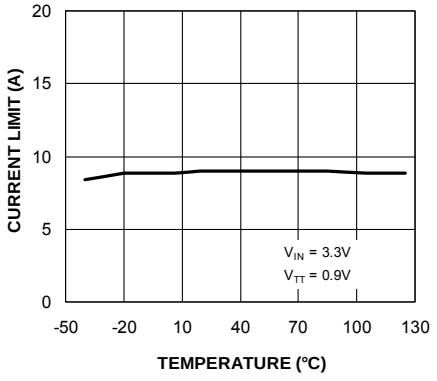

**Switching Frequency vs. Temperature**




**Enable Input Current vs. Temperature**

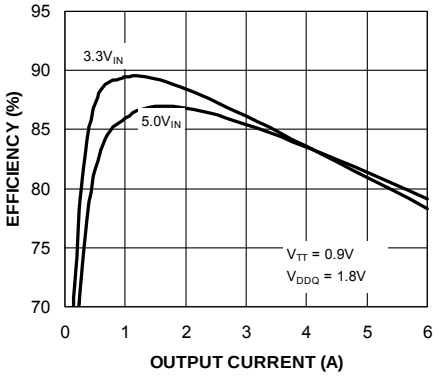



**Current Limit vs. Temperature**

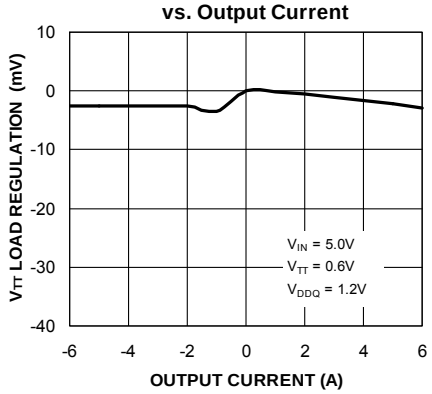


## Typical Characteristics (Continued)

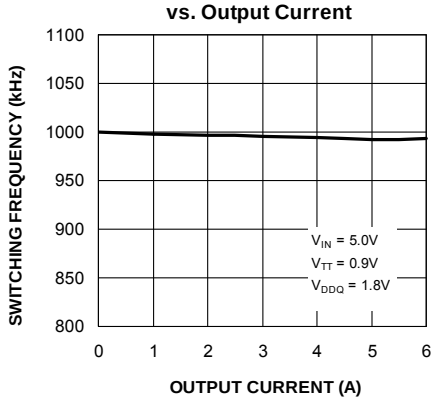
**Efficiency vs. Output Current**



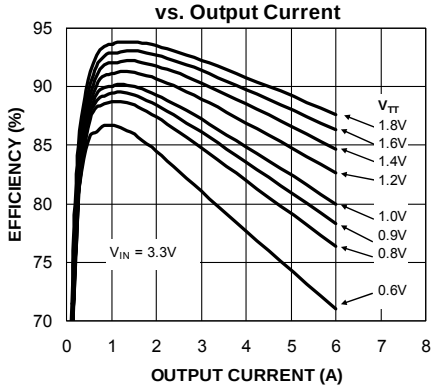

**$V_{TT}$ Load Regulation vs. Output Current**



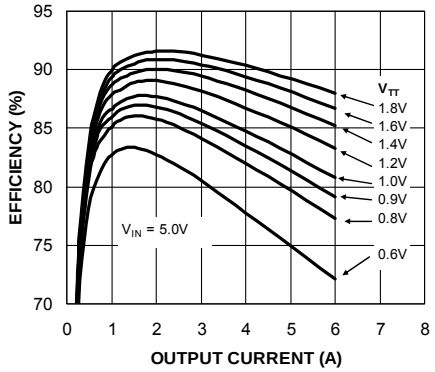

**Switching Frequency vs. Output Current**




**Efficiency ($V_{IN}$ = 3.3V) vs. Output Current**

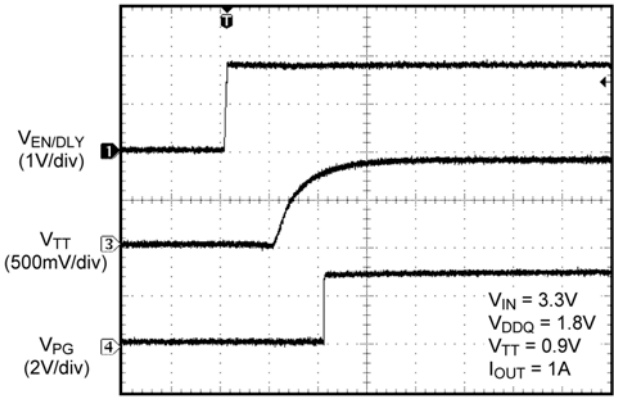



**Efficiency ($V_{IN}$ = 5.0V) vs. Output Current**



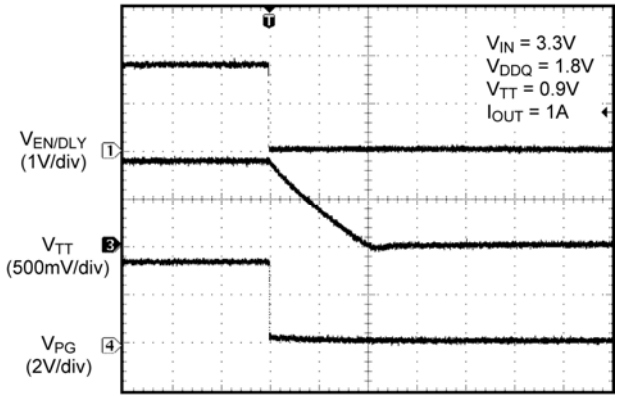
## Functional Characteristics

**Enable Turn-On Delay and Raise Time**



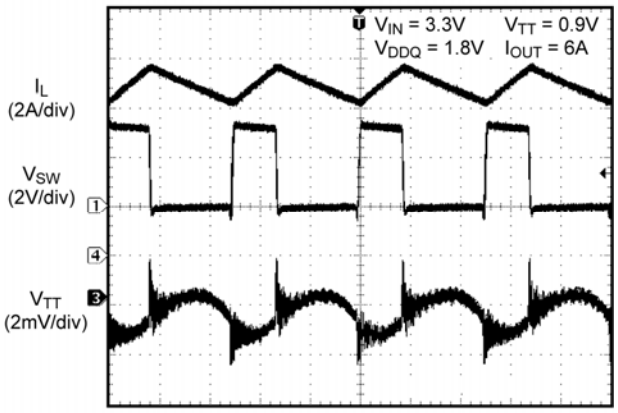

Time (40µs/div)

**Enable Turn-Off**



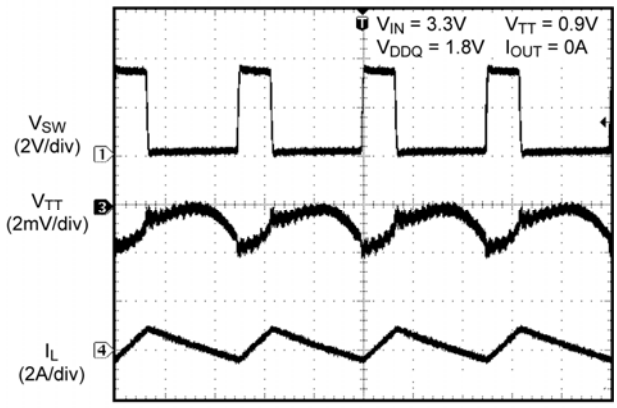

Time (100µs/div)

**Switching Waveforms; $I_{OUT}$ = 6A**



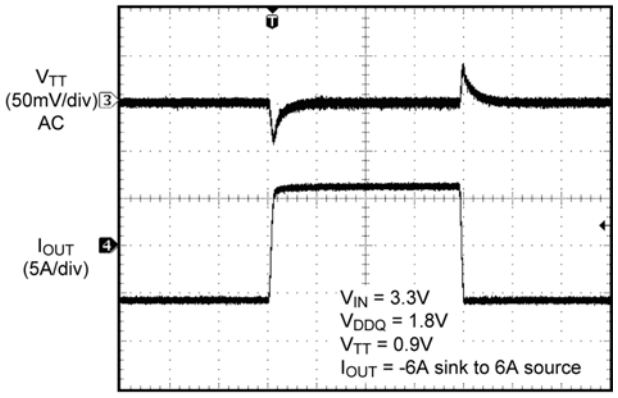

Time (400ns/div)

**Switching Waveforms; $I_{OUT}$ = 0A**




Time (400ns/div)

**Load Transient Response**




Time (100µs/div)

## Functional Diagram

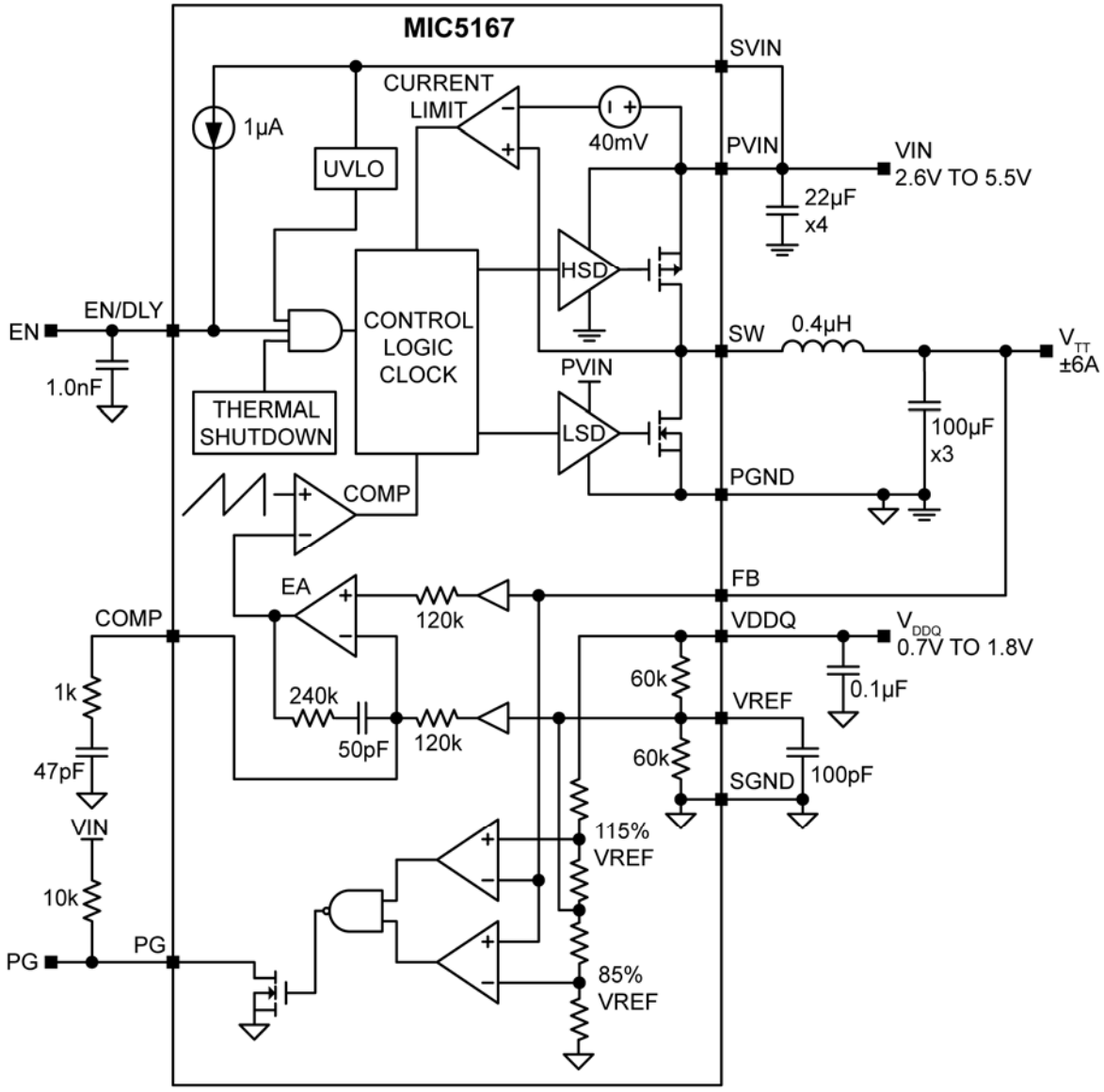



**Figure 1. MIC5167 Block Diagram**

## Application Information

DDR memory requires two power supplies, one for the memory chip, referred to as VDDQ and the other for a termination supply $V_{TT}$, which is one-half VDDQ. With memory speeds in excess of 300MHz, the memory system bus must be treated as transmission lines. To maintain good signal integrity the memory bus must be terminated to minimize signal reflections. Figure 2 shows the simplified termination circuit. Each control, address and data lines have these termination resistors RS and RT connected to them.

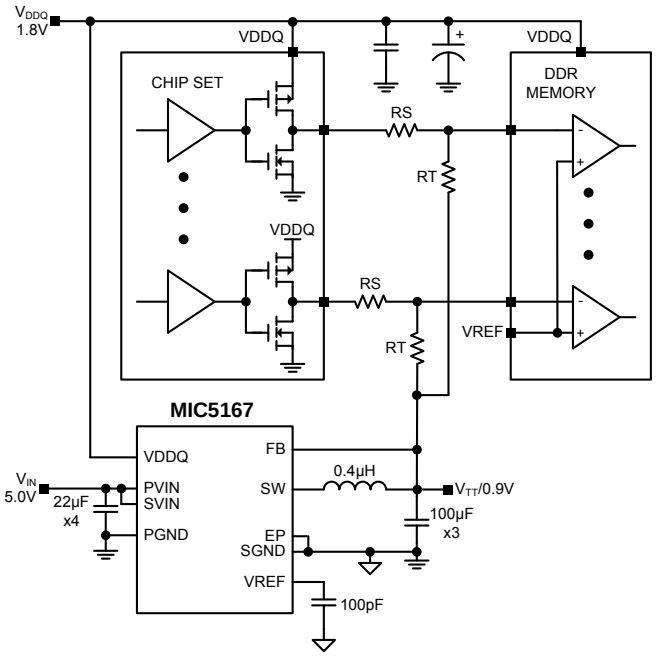



**Figure 2. DDR Memory Termination Circuit**

Bus termination provides a means to increase signaling speed while maintaining good signal integrity. The termination network consists of a series resistor (RS) and a terminating resistor (RT). Values of $R_S$ range between 10Ω to 30Ω with a typical of 22Ω, while $R_T$ ranges from 22Ω to 28Ω with a typical value of 25Ω. $V_{TT}$ will dynamically sink and source current to maintain a termination voltage under all conditions. This method of bus termination reduces common mode noise, settling time, voltage swings, EMI/RFI and improves slew rates.

$V_{DDQ}$ powers all the memory IC's, memory drivers and receivers for all the memory bits in the DDR memory system. When the driver is logic low $V_{TT}$ sources current. When the driver is logic high $V_{TT}$ sinks current. The MIC5167 regulates $V_{TT}$ to VDDQ/2 during sourcing or sinking current. The power dissipated in RS (bus resistance) and RT (termination resistance) is $V_{TT}$ squared divided by their respective resistance.

Since the voltage across the resistance is VDDQ/2, the power dissipated is one-quarter the power of a termination voltage of VDDQ. The memory bits are not usually all at a logic high or logic low at the same time so the $V_{TT}$ supply is usually not sinking or sourcing much current.

### $V_{TT}$

$V_{TT}$ is regulated to $V_{REF}$. Due to high speed signaling, the load current seen by $V_{TT}$ is constantly changing. To maintain adequate transient response, large OS-CON and ceramics are recommended on $V_{TT}$. The proper combination and placement of the OS-CON and ceramic capacitors is important to reduce both ESR and ESL such that high-current and high-speed transients do not exceed the dynamic voltage tolerance requirement of $V_{TT}$. The larger OS-CON capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is important to reduce the effects of PCB trace inductance.

When $V_{TT}$ is sinking current, the external power supply that powers the MIC5167 ($PV_{IN}$) must be able to sink current-to-ground; otherwise, the supply voltage will start to increase. It is crucial that this external power supply must also be able to source and sink current.

### VDDQ

The VDDQ input on the MIC5167 is used to create the internal reference voltage for $V_{TT}$. The reference voltage is generated from an internal resistor divider network of two 60kΩ resistors, generating a reference voltage $V_{REF}$ that is $V_{DDQ}$/2. The VDDQ input should be Kelvin connected as close as possible to the memory supply voltage.

Since the reference is simply $V_{DDQ}$/2, any perturbations on VDDQ will also appear at half the amplitude on the reference. For this reason, both ceramics and low-ESR bulk capacitors such as OS-CON are recommended on the $V_{DDQ}$ supply. This will aid in performance by improving the source impedance over a wide frequency range.

### Feedback

The feedback (FB) pin provides the path for the error amplifier to regulate $V_{TT}$. The FB input must also be Kelvin connected to the $V_{TT}$ bypass capacitors. If the FB input is connected to close to the MIC5167, the IR drop of the PCB trace can cause the $V_{TT}$ voltage at the memory chip to be too low. Placing the MIC5167 as close as possible to the DDR memory will improve the load regulation performance.

The feedback trace is a noise sensitive input and should be routed away from the switch node. A 0.1µF capacitor placed next to the IC can help filter any high frequency noise that may cause $V_{TT}$ errors.

**Enable/Delay Pin**

The internal circuits are held off until EN/DLY input reaches the enable threshold of 1.24V. A 1µA current source out of the IC is used to charge the delay capacitor. The delay time is simply the time it takes 1µA to charge $C_{EN/DLY}$ to 1.25V. Therefore:

$$t_{EN/DLY} = \frac{1.24 \times C_{EN/DLY}}{1 \times 10^{-6}}$$

The enable/delay pin is pulled low when the input voltage is lower than the UVLO threshold, ensuring that the delay start up voltage starts at zero.

**Power-Good (PG)**

The power-good output provides a under and over voltage fault flag. The PG output remains high as long as $V_{TT}$ is within ±15% range of $V_{REF}$ and goes low if output moves beyond this range.

**VREF**

A minimum capacitor value of 100pF from $V_{REF}$-to-ground is required to remove high-frequency signals reflected from the source (see Figure 3). Large capacitance values (>1500pF) should be avoided. Values greater than 1500pF slow down $V_{REF}$ and detract from the reference voltage's ability to track $V_{DDQ}$ during high-speed load transients.

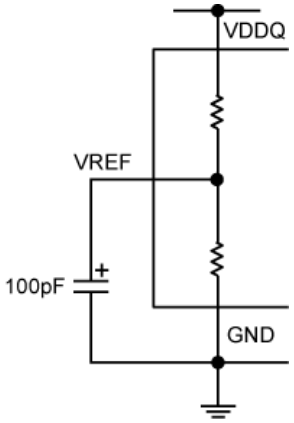



**Figure 3. $V_{REF}$ Follows $V_{DDQ}$**

VREF can also be manipulated for different applications. A separate voltage source can be used to externally set the reference point, bypassing the divider network. Also, external resistor to $V_{REF}$ divider network can be added to shift the reference point up or down.

**PWM**

The MIC5167 is a voltage mode, Pulse Width Modulation (PWM) controller. By controlling the ratio of on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC5167 will run at 100% duty cycle.

The MIC5167 provides constant switching at 1MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, very low power is dissipated during the off period.

PWM control provides fixed frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

## Component selection

**Input Capacitor**

A 22µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing. Y5V dielectrics capacitor should not be used. Aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

**Output Capacitor**

The MIC5167 was designed specifically for the use of ceramic output capacitors. The 300µF can be increased to improve transient performance. Since the MIC5167 uses voltage mode control, the control loop is affected by the 180-deg phase shift generated by the complex pole created by the inductor and output capacitor. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC5167.

### Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC5167 is designed for use with a 0.4µH to 4.7µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple current can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the Current Limit of the MIC5167 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC, so it offers some level of protection if the inductor gets too hot. It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the “Efficiency Considerations” below for a more detailed description.

### Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

$$\text{Efficiency } \% = \left( \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of current for battery powered applications.

Reduced current draw from a battery increases the devices operating time, critical in hand held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are simply the power losses due to VI or $I^2R$. For example, power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET $RDS_{(ON)}$ multiplied by the RMS Switch Current squared ($I_{SW}^2$). During the off-cycle, the low-side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor’s DCR and capacitor’s ESR also contribute to the $I^2R$ losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and off at a constant 1MHz frequency and the switching transitions make up the switching losses.

Figure 4 shows an efficiency curve. The portion, from 0A to 1A, efficiency losses are dominated by quiescent current losses, gate drive, transition and core losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

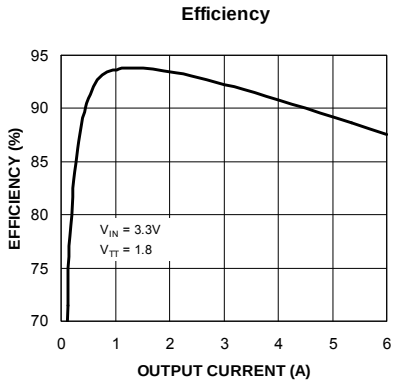



**Figure 4. Efficiency Curve**

The region, 1A to 6A, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, thereby reducing the internal $R_{DS(ON)}$. This improves efficiency by decreasing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses.

**Compensation**

The MIC5167 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100-200kHz, the MIC5167 is capable of extremely fast transient responses.

The MIC5167 is designed to be stable with a typical application using a 1µH inductor and a 100µF ceramic (X5R) output capacitor. These values can be varied dependant upon the tradeoff between size, cost and efficiency, keeping the LC natural frequency $(\frac{1}{2 \times \pi \times \sqrt{L \quad C}})$ ideally less than 26kHz to ensure stability can be achieved. The minimum recommended inductor value is 0.4µH and minimum recommended output capacitor value is 100µF. The tradeoff between changing these values is that with a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

***Current Limit***

The MIC5167 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is over temperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 5 describes the operation of the current limit circuit. Since the actual $R_{DS(ON)}$ of the P-Channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependant upon the $R_{DS(ON)}$ value. Current limit is set to nominal value. Variations in the scale factor K between the Power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

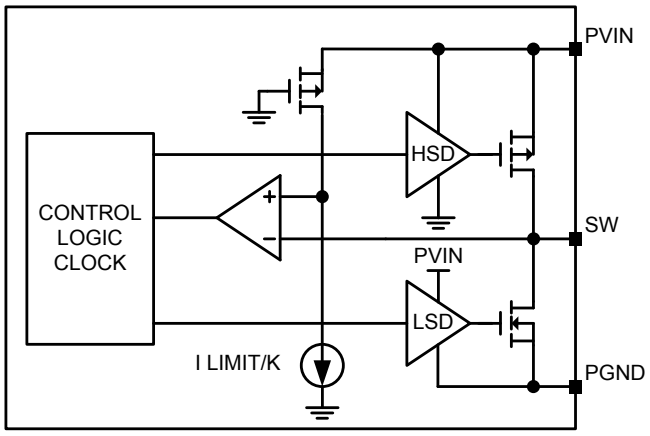



**Figure 5. Current-Limit Detail**

***Thermal Considerations***

The MIC5167 is packaged in a MLF® 4mm x 4mm, a package that has excellent thermal performance. This maximizes heat transfer from the junction to the exposed pad (ePAD) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board.

**Sequencing and Tracking**

The MIC5167 provides PG and EN/DLY pins to provide sequencing and turn on delay capability for connecting multiple voltage regulators together.

***Enable/DLY Pin***

The Enable pin contains a trimmed, 1µA current source which can be used with a capacitor to implement a fixed desired delay in some sequenced power systems. The threshold level for power on is 1.24V with a hysteresis of 20mV.

### *Sequencing Examples*

Sequencing and turn on delay of the MIC5167 can be easily implemented using the PG and EN/DLY pins. The following diagrams illustrate turn on sequencing and turn on sequencing with delay.

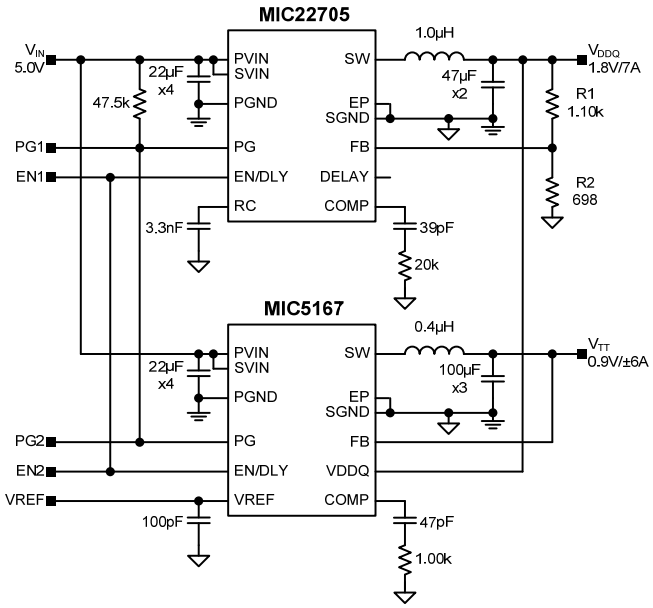



**Figure 6. $V_{TT}$ Turn-On with Delay**

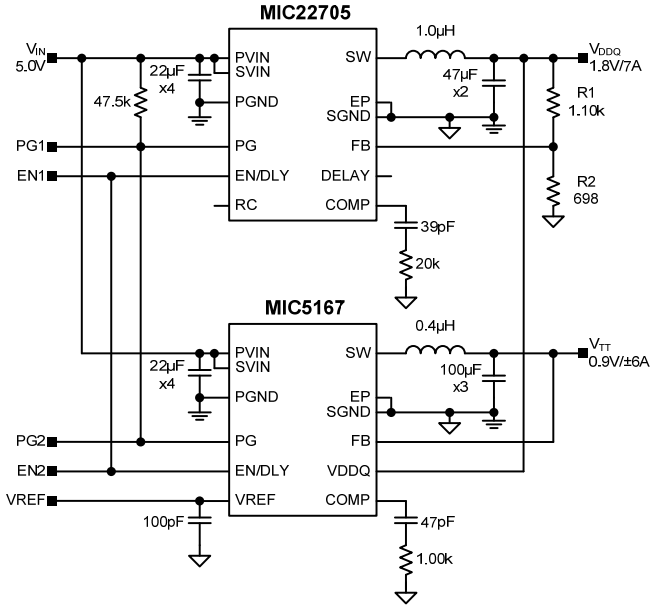
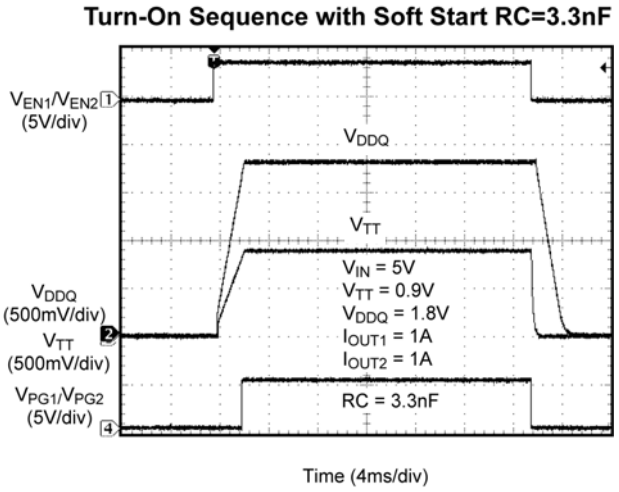
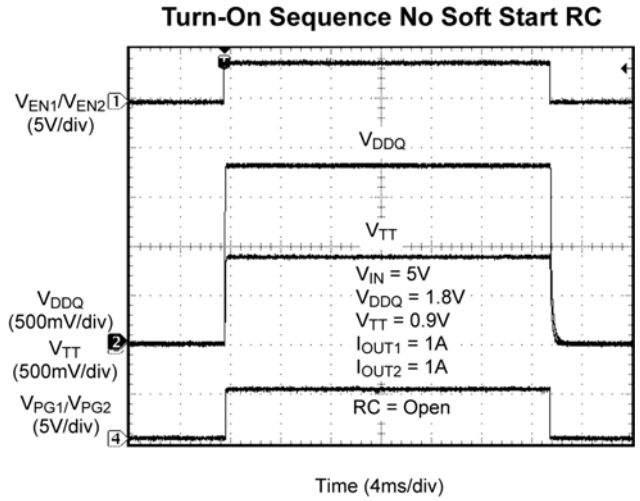



**Figure 7. $V_{TT}$ Turn-On without Delay**



## PCB Layout Guidelines

**Warning!!! To minimize EMI and output noise, follow these layout recommendations.**

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC5167 converter.

### IC

- The 22µF ceramic capacitor, which is connected to the SVIN pin, must be located right at the IC. The SVIN pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the SVIN and SGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

### Input Capacitor

- A 22µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

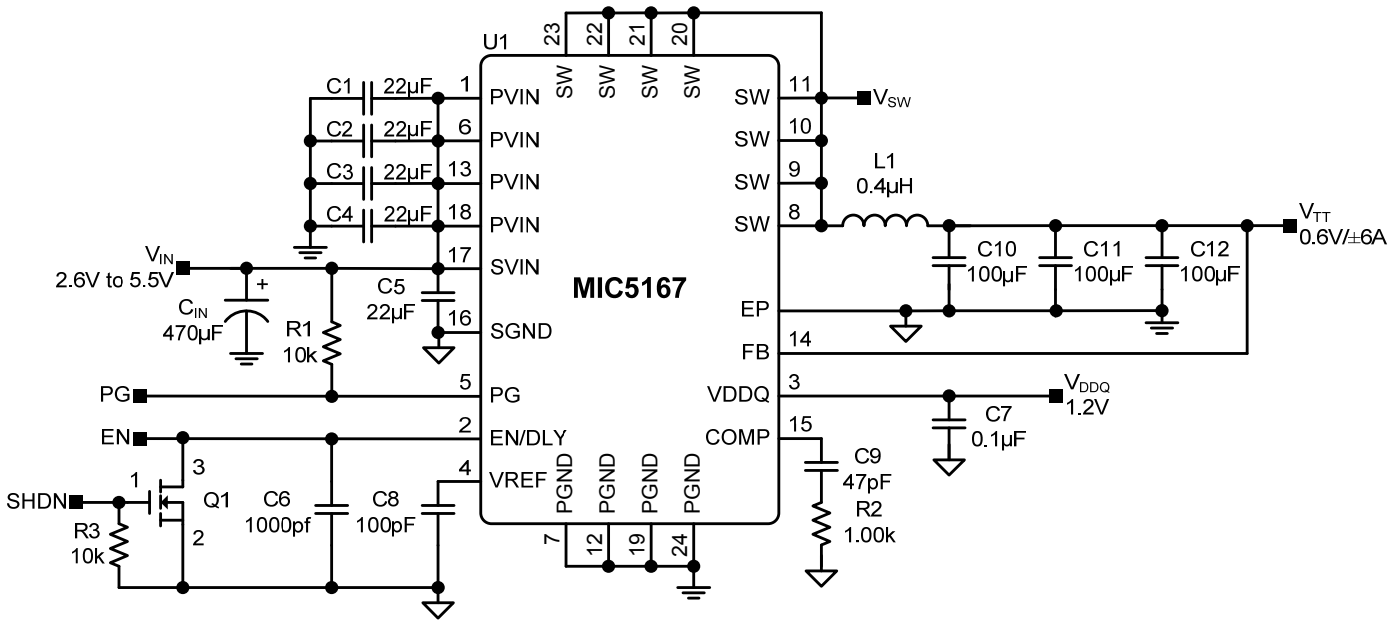
### Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

### Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be place close to the IC with the bottom of R2 connected to SGND.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

## Evaluation Board Schematic

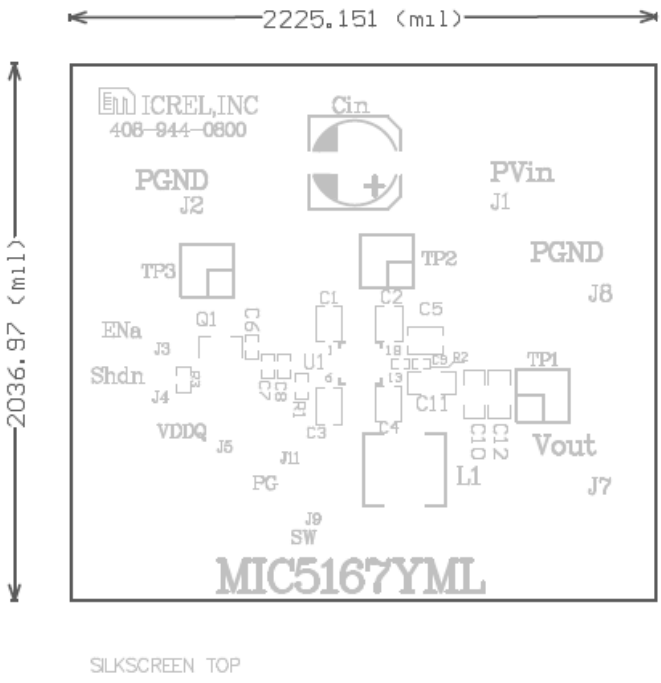


## Bill of Materials

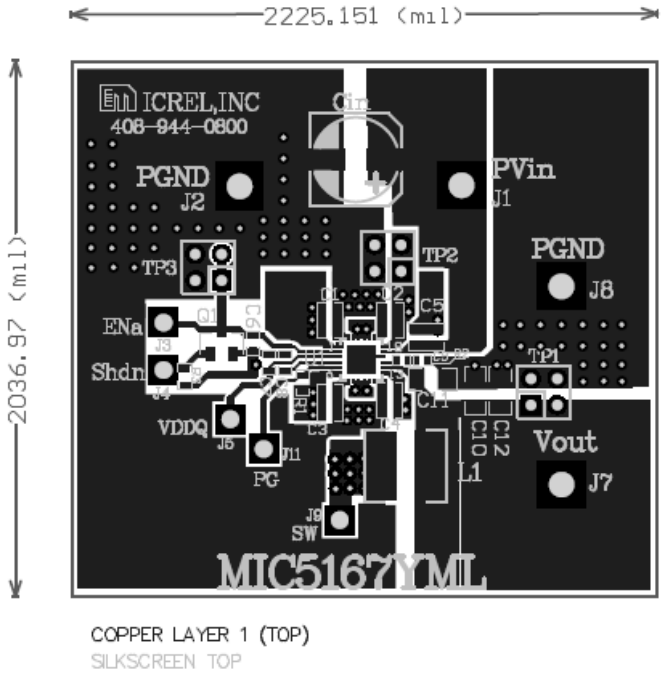
| Item | Part Number | Manufacturer | Description | Qty. |
|---|---|---|---|---|
| C1, C2, C3, C4, C5 | C2012X5R0J226M | TDK | 22µF/6.3V Ceramic Capacitor, X5R, 0805 | 5 |
| | 08056D226MAT | AVX | | |
| | GRM21BR60J226ME39L | Murata | | |
| C6 | VJ0603A102KXA | Vishay | 1000pF/50V Ceramic Capacitor, COG, 0603 | 1 |
| | GRM188R71H102KA01D | Murata | 1000pF/50V Ceramic Capacitor, X7R, 0603 | |
| | C1608C0G1H102J | TDK | 1000pF/50V Ceramic Capacitor, COG, 0603 | |
| C7 | C1608C0G1H104K | TDK | 0.1µF/50V Ceramic Capacitor, X7R, 0603 | 1 |
| C8 | C0603X5R1H101M | TDK | 100pF/50V Ceramic Capacitor, X5R, 0603 | 1 |
| C9 | C1005COG1H470J | TDK | 47pF/50V Ceramic Capacitor, COG, 0402 | 1 |
| C10, C11, C12 | JMK316BJ107ML-T | Taiyo Yuden | 100µF/6.3V Ceramic Capacitor, X5R, 1206 | 3 |
| $C_{IN}$ | B41125A3477M000 | Epcos | 470µF/10V Electrolytic Capacitor, 8x10 | 1 |
| L1 | HCP0704-0R4-R | Coiltronics | 0.4µH, 12A, size 6.8x6.8x4.2mm | 1 |
| R1, R3 | CRCW060310K0FKEA | Vishay Dale | 10.0kΩ Resistor, 0603, 1% | 2 |
| R2 | CRCW06031K00FKEA | Vishay Dale | 1.00kΩ Resistor, 0603, 1% | 1 |
| Q1 | CMDPM7002A | Central Semiconductor | Signal MOSFET, SOT-23-6 | 1 |
| **U1** | **MIC5167YML** | **Micrel, Inc.** | **Integrated 6A DDR Regulator** | **1** |

**Notes:**
1. TDK: www.tdk.com
2. AVX: www.avx.com
3. Murata: www.murata.com
4. Vishay: www.vishay.com
5. BC Components: www.bccomponents.com
6. Coiltronics: www.coiltronics.com
7. Central Semiconductor: www.centralsemi.com
8. **Micrel, Inc.: www.micrel.com**

## PCB Layout Recommendations

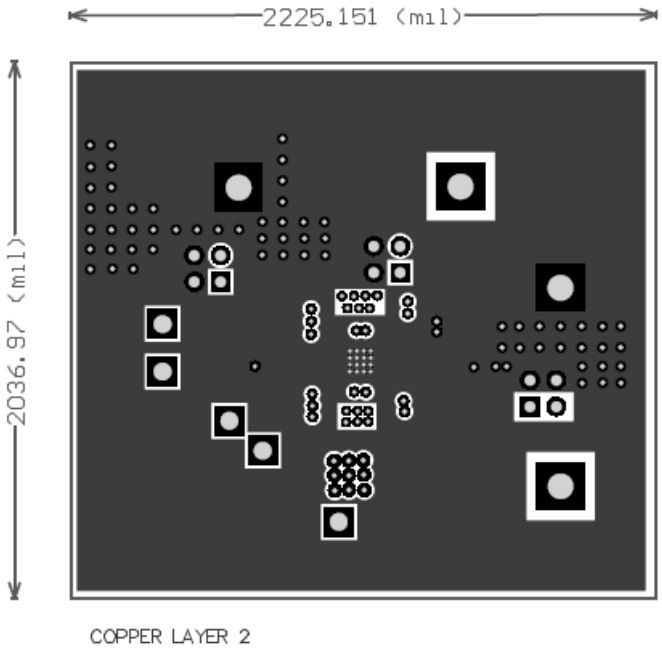



**MIC5167 Evaluation Board Top Silk**

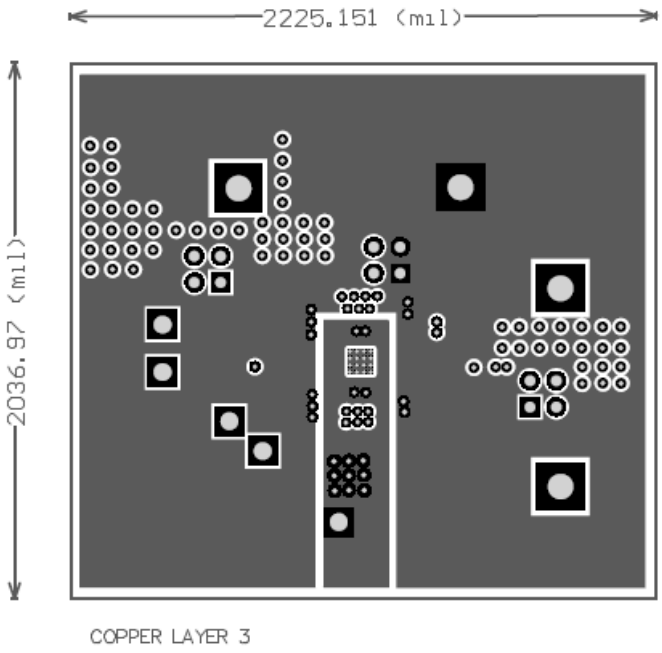



**MIC5167 Evaluation Board Top Layer**

## PCB Layout Recommendations (Continued)

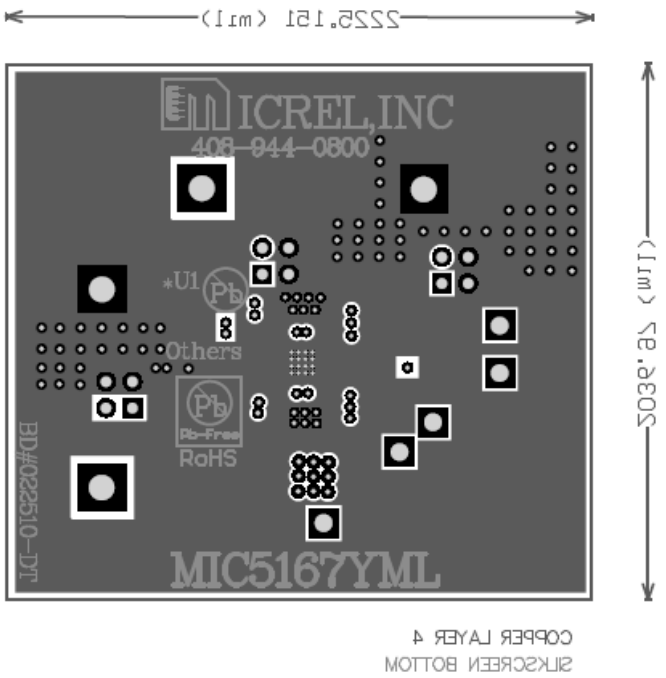



**MIC5167 Evaluation Board Mid-Layer 1 (Ground Plane)**



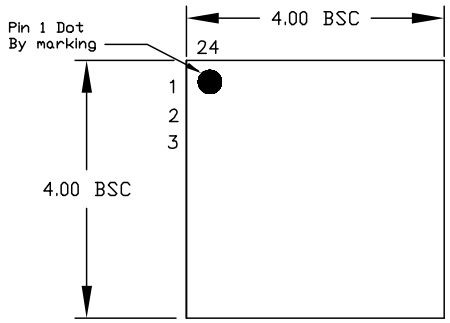

**MIC5167 Evaluation Board Mid-Layer 2**

## PCB Layout Recommendations (Continued)

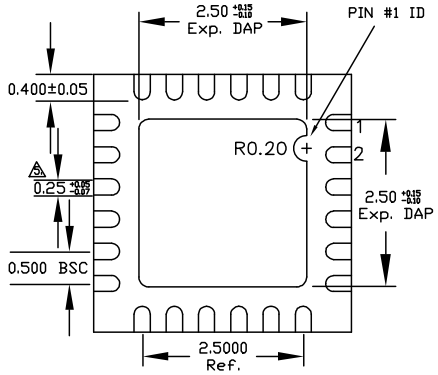



**MIC5167 Evaluation Board Bottom Layer**

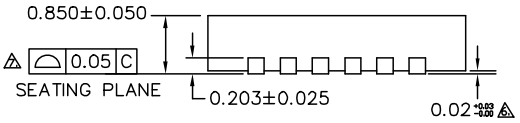
## Package Information




TOP VIEW




BOTTOM VIEW



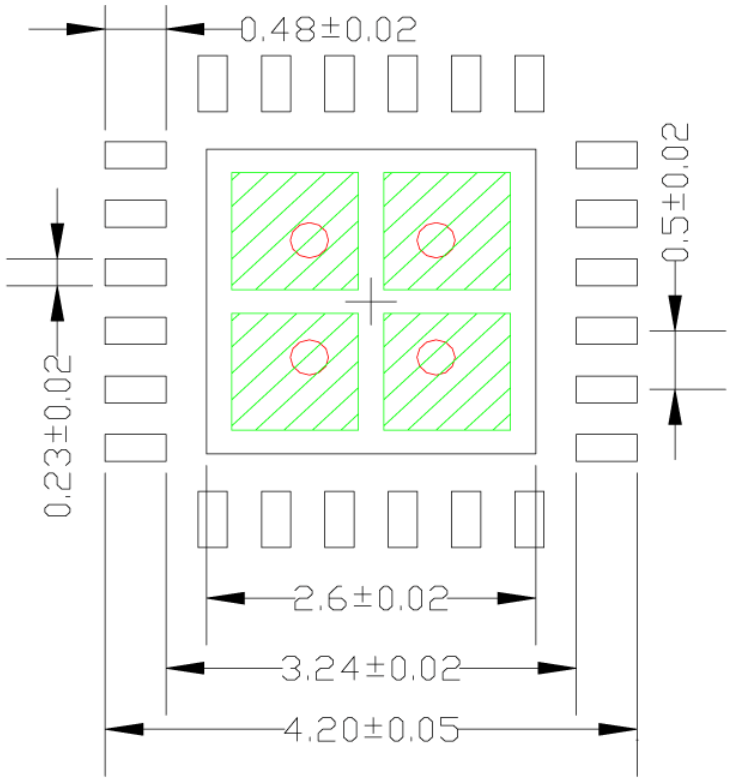

SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

**24-Pin 4mm x 4mm MLF® (ML)**

## Recommended Land Pattern

LP # MLF44Q-24LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted




Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter, 1.00 mm pitch, and it should be connected to GND plane for maximum thermal performance.
Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 1.00x1.00 mm in

**24-Pin 4mm x 4mm MLF® Land Pattern**

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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