



THE DATASHEET OF SG2844DM



Current Mode PWM Controller

Description

The SG1844/45 family of control ICs provides all the required features to implement off-line Fixed Frequency, Current-mode switching power supplies with a minimum number of external components. Current-mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch.

The Bandgap reference is trimmed to $\pm 1\%$ over temperature. Oscillator discharge current is trimmed to less than $\pm 10\%$. The SG1844/45 has under-voltage lockout, current-limiting circuitry and start-up current of less than 1mA. The totem-pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N-channel device. Both operate up to a maximum duty cycle range of zero to $<50\%$ due to an internal toggle flip-flop which blanks the output off every other clock cycle. The SG1844/45 is specified for operation over the full military ambient temperature range of -55°C to 125°C . The SG3844/45 is designed for the commercial range of 0°C to 70°C .

Features

- Optimized for Off-Line Control
- Low Start-Up Current ($<1\text{mA}$)
- Automatic Feed Forward Compensation
- Trimmed Oscillator
- Discharge Current
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Undervoltage Lockout with 6V Hysteresis (SG1844 only)
- Double Pulse Suppression
- High-Current Totem-Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Under-voltage Lockout
- SG1844 - 16 Volts
- SG1845 - 8.4 Volts
- Low Shoot-through Current $<75\text{mA}$ Over Temperature

Application

- Available to MIL-STD-883
- Available to DSCC
 - Standard Microcircuit Drawing (SMD)
- SGR1844/45 Rad-Tolerant Version Available

Product Highlight

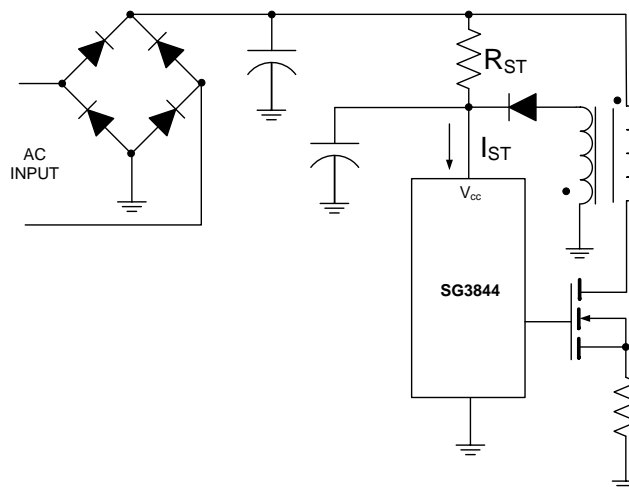
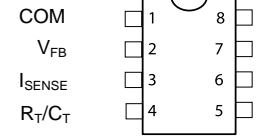
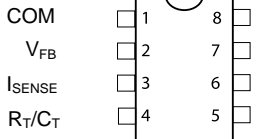
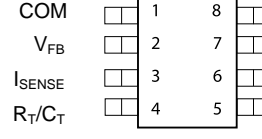
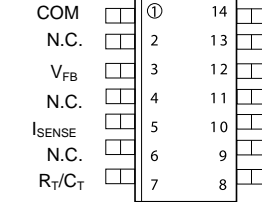


Figure 1 - Product Highlight

Connection Diagrams and Ordering Information

| Ambient Temperature | Type | Package | Part Number | Packaging Type | Connection Diagram |
|---------------------|------|---|--------------|----------------|--|
| 0°C to 70°C | M | 8-PIN PLASTIC DUAL INLINE PACKAGE | SG3844M | PDIP |  <p>M PACKAGE (Top View)</p> <p>M Package: RoHS / Pb-free 100% Matte Tin Lead Finish</p> |
| | | | SG3845M | | |
| -55°C to 125°C | Y | 8-PIN CERAMIC DUAL INLINE PACKAGE | SG1844Y | CERDIP |  <p>Y PACKAGE (Top View)</p> <p>Y Package: PbSn Tin Lead Finish</p> |
| | | | SG1845Y | | |
| | | | SG1844Y-883B | | |
| | | | SG1845Y-883B | | |
| | | | SG1844Y-DESC | | |
| | | | SG1845Y-DESC | | |
| 0°C to 70°C | DM | 8-PIN SMALL OUTLINE INTEGRATED CIRCUIT | SG3844DM | SOIC |  <p>DM PACKAGE (Top View)</p> <p>DM Package: RoHS / Pb-free 100% Matte Tin Lead Finish</p> |
| | | | SG3845DM | | |
| 0°C to 70°C | D | 14-PIN SMALL OUTLINE INTEGRATED CIRCUIT | SG3844D | SOIC |  <p>D PACKAGE (Top View)</p> <p>D Package: RoHS / Pb-free 100% Matte Tin Lead Finish</p> |
| | | | SG3845D | | |

| Ambient Temperature | | Package | Part Number | Packaging Type | Connection Diagram |
|---------------------|---|------------------------------------|--------------|-------------------------------------|---|
| -55°C to 125°C | J | 14-PIN CERAMIC DUAL INLINE PACKAGE | SG1844J | CERDIP | <p>J PACKAGE (Top View) PbSn Lead Finish</p> |
| | | | SG1845J | | |
| | | | SG1844J-883B | | |
| | | | SG1845J-883B | | |
| | | | SG1844J-DESC | | |
| | | | SG1845J-DESC | | |
| -55°C to 125°C | F | 10-PIN CERAMIC FLAT PACK PACKAGE | SG1844F-DESC | FLAT PACK | <p>F PACKAGE (Top View) PbSn Lead Finish</p> |
| | | | SG1845F-DESC | | |
| -55°C to 125°C | L | 20-Pin CERAMIC | SG1844L | Ceramic (LCC) Leadless Chip Carrier | <p>L PACKAGE (Top View) PbSn Lead Finish</p> |
| | | | SG1845L | | |
| | | | SG1844L-883B | | |
| | | | SG1845L-883B | | |
| | | | SG1844L-DESC | | |
| | | | SG1845L-DESC | | |

Notes:

1. Contact factory for DESC part availability.
2. All parts are viewed from the top.
3. Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. SG3844D-TR)
4. Hermetic Packages J, F, L, & Y use Pb37/Sn63 hot solder lead finish, contact factory for availability of RoHS versions.

Absolute Maximum Ratings^{1 - 2}

| Parameter | Value | Units |
|---|--------------|-------|
| Supply Voltage (Low Impedance Source) | 30 | V |
| Output Current (Peak) | ±1 | A |
| Output Current (Continuous) | 350 | mA |
| Output Energy (Capacitive Load) | 5 | μJ |
| Analog Inputs (V_{FB} , I_{SENSE}) | -0.3 to +6.3 | V |
| Error Amplifier Output Sink Current | 10 | mA |
| Operating Junction Temperature | | |
| Hermetic (J, Y, F, L Packages) | 150 | °C |
| Plastic (M, D, DM Packages) | 150 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Lead Temperature (Soldering, 10 Seconds) | 300 | °C |
| RoHS / Pb-free Peak Package Solder Reflow Temp. (40 second max. exposure) | 260 (+0, -5) | °C |
| <i>Notes:</i> | | |
| 1. Exceeding these ratings could cause damage to the device. | | |
| 2. All voltages are with respect to Pin 5. All currents are positive into the specified terminal. | | |

Thermal Data

| Parameter | Value | Units |
|---|-------|-------|
| M Package: | | |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 95 | °C/W |
| DM Package: | | |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 165 | °C/W |
| D Package: | | |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 120 | °C/W |
| Y Package: | | |
| Thermal Resistance-Junction to Case, θ_{JC} | 30 | °C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 130 | °C/W |
| J Package | | |
| Thermal Resistance-Junction to Case, θ_{JC} | 30 | °C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 80 | °C/W |
| F Package | | |
| Thermal Resistance-Junction to Case, θ_{JC} | 80 | °C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 145 | °C/W |
| L Package | | |
| Thermal Resistance-Junction to Case, θ_{JC} | 35 | °C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 120 | °C/W |
| <i>Notes:</i> | | |
| Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. | | |
| The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow. | | |

Recommended Operating Conditions³

| Symbol | Parameter | Recommended Operating Conditions | | | Units |
|--------------------------------------|-------------------------------|----------------------------------|------|------|-------|
| | | Min. | Typ. | Max. | |
| V _S | Supply Voltage Range | | 30 | | V |
| I _{PK} | Output Current (Peak) | | ±1 | | A |
| I _{OUT} | Output Current (Continuous) | | 200 | | mA |
| | Analog Inputs (Pin 2, Pin 3) | 0 | | 2.6 | V |
| E _{AISNK} | Error Amp Output Sink Current | | 5 | | mA |
| OSC _{FR} | Oscillator Frequency Range | 0.1 | | 500 | kHz |
| R _T | Oscillator Timing Resistor | 0.52 | | 150 | kΩ |
| C _T | Oscillator Timing Capacitor | 0.001 | | 1.0 | μF |
| Operating Ambient Temperature Range: | | | | | |
| | SG1844/45 | -55 | | 125 | °C |
| | SG3844/45 | 0 | | 70 | °C |

Note:
3. Range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1844/SG1845 with $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, SG3844/SG3845 with $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, V_{CC} = 15V (Note 7), R_T = 10kΩ, and C_T = 3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

| Symbol | Parameter | Test Conditions | SG1844/SG1845 | | | SG3844/SG3845 | | | Units |
|---------------------------|-------------------------------------|--|---------------|------|------|---------------|------|------|-------|
| | | | Min. | Typ. | Max | Min. | Typ. | Max | |
| Reference Section | | | | | | | | | |
| V _{REF} | Output Voltage | T _J = 25°C, I _O = 1mA | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| V _{REG} | Line Regulation | 12V ≤ V _{IN} ≤ 25V | | 6 | 20 | | 6 | 20 | mV |
| I _{REG} | Load Regulation | 1 ≤ I _O ≤ 20mA | | 6 | 25 | | 6 | 25 | mV |
| | Temperature Stability ⁴ | | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/°C |
| | Total Output Variation ⁴ | Line, Load, Temperature | 4.90 | | 5.10 | 4.82 | | 5.18 | V |
| V _N | Output Noise Voltage ⁴ | 10Hz ≤ f ≤ 10kHz, T _J = 25°C | | 50 | | | 50 | | μV |
| | Long Term Stability ⁴ | T _A = 125°C, 1000hrs | | 5 | 25 | | 5 | 25 | mV |
| V _{REFISC} | Output Short Circuit | | -30 | -100 | -180 | -30 | -100 | -180 | mA |
| Oscillator Section | | | | | | | | | |
| f | Initial Accuracy ⁸ | T _J = 25°C | 47 | 52 | 57 | 47 | 52 | 57 | kHz |
| f _{REG} | Voltage Stability | 12V ≤ V _{CC} ≤ 25V | | .02 | 1 | | 0.2 | 1 | % |
| | Temperature Stability ⁴ | T _{MIN} ≤ T _A ≤ T _{MAX} | | 5 | | | 5 | | % |
| OSC _{PP} | Amplitude | V _{RT/CT} (Peak to Peak) | | 1.7 | | | 1.7 | | V |
| I _{DSG} | Discharge Current | T _J = 25°C | 7.8 | 8.3 | 9.1 | 7.5 | 8.4 | 9.3 | mA |
| | | T _{MIN} ≤ T _A ≤ T _{MAX} | 6.8 | | 9.3 | 7.2 | | 9.5 | mA |

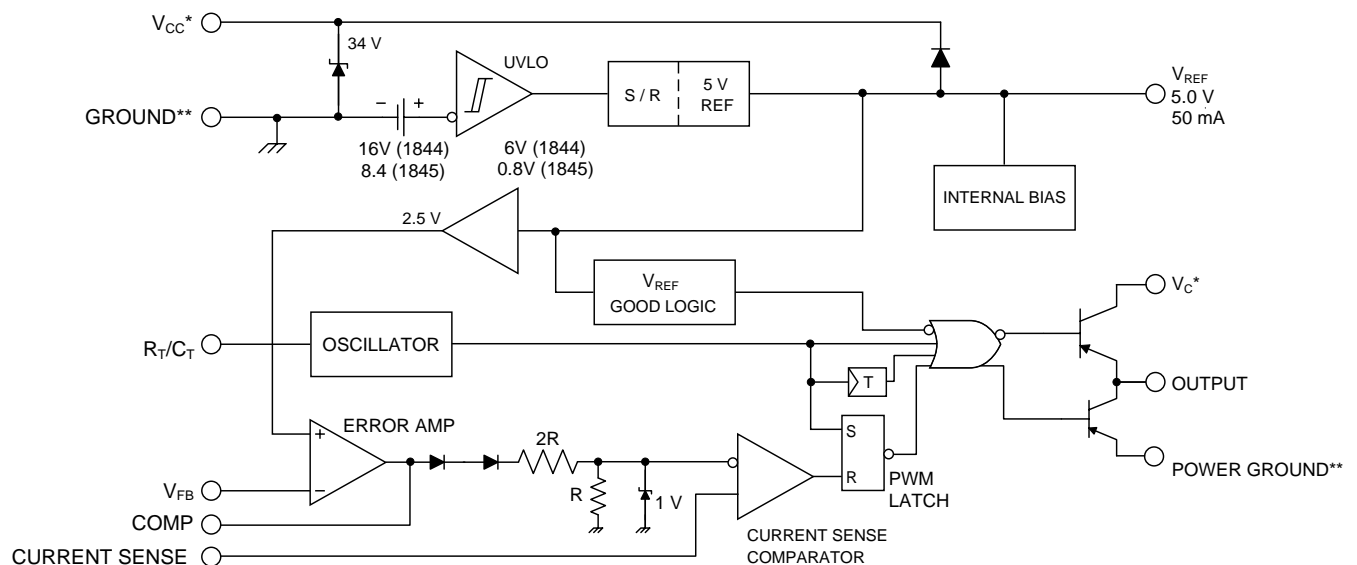
| Symbol | Parameter | Test Conditions | SG1844/SG1845 | | | SG3844/SG3845 | | | Units |
|--------------------------------------|--------------------------------------|---|---------------|------|------|---------------|------|------|-------|
| | | | Min. | Typ. | Max | Min. | Typ. | Max | |
| Error Amplifier Section | | | | | | | | | |
| EA _{IH} | Input Voltage | V _{COMP} = 2.5V | 2.45 | 2.50 | 2.55 | 2.42 | 2.50 | 2.58 | V |
| EA _{IIB} | Input Bias Current | | | -0.3 | -1 | | -0.3 | -2 | μA |
| A _{VOL} | Open Loop Gain | 2V ≤ V _O ≤ 4V | 65 | 90 | | 65 | 90 | | dB |
| EA _{BW} | Unity Gain Bandwidth ⁴ | T _J = 25°C | 0.7 | 1 | | 0.7 | 1 | | MHz |
| PSRR | Power Supply Rejection Ratio | 12V ≤ V _{CC} ≤ 25V | 60 | 70 | | 60 | 70 | | dB |
| EA _{SNK} | Output Sink Current | V _{VFB} = 2.7V, V _{COMP} = 1.1V | 2 | 6 | | 2 | 6 | | mA |
| EA _{SRC} | Output Source Current | V _{VFB} = 2.3V, V _{COMP} = 5V | -0.5 | -0.8 | | -0.5 | -0.8 | | mA |
| EA _{VOH} | V _{OUT} High | V _{VFB} = 2.3V, R _L = 15k to GND | 5 | 6 | | 5 | 6 | | V |
| EA _{VOL} | V _{OUT} Low | V _{VFB} = 2.7V, R _L = 15k to V _{REF} | | 0.7 | 1.1 | | 0.7 | 1.1 | V |
| Current Sense Section | | | | | | | | | |
| CS _{AVOL} | Gain ^{5 & 6} | | 2.85 | 3 | 3.15 | 2.85 | 3 | 3.15 | V/V |
| | Maximum Input Signal ⁵ | V _{COMP} = 5V | 0.9 | 1 | 1.1 | 0.9 | 1 | 1.1 | V |
| PSRR | Power Supply Rejection Ratio | 12V ≤ V _{CC} ≤ 25V | | 70 | | | 70 | | dB |
| CS _{IIB} | Input Bias Current | | | -2 | -10 | | -2 | -10 | μA |
| CS _{DELAY} | Delay to Output ⁴ | | | 150 | 300 | | 150 | 300 | ns |
| Output Section | | | | | | | | | |
| VOL | Output Low Level | I _{SINK} = 20mA | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| | | I _{SINK} = 200mA | | 1.5 | 2.2 | | 1.5 | 2.2 | V |
| VOH | Output High Level | I _{SOURCE} = 200mA | 13 | 13.5 | | 13 | 13.5 | | V |
| | | I _{SOURCE} = 200mA | 12 | 13.5 | | 12 | 13.5 | | V |
| RS | Rise Time ⁴ | T _J = 25°C, C _L = 1nF | | 50 | 150 | | 50 | 150 | ns |
| FT | Fall Time ⁴ | T _J = 25°C, C _L = 1nF | | 50 | 150 | | 50 | 150 | ns |
| Under-Voltage Lockout Section | | | | | | | | | |
| UVLO | Start Threshold | 1844 | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| | | 1845 | 7.8 | 8.4 | 9.0 | 7.8 | 8.4 | 9.0 | V |
| V _S MIN | Min. Operation Voltage After Turn-On | 1844 | 9 | 10 | 11 | 8.5 | 10 | 11.5 | V |
| | | 1845 | 7.0 | 7.6 | 8.3 | 7.0 | 7.6 | 8.2 | V |
| PWM Section | | | | | | | | | |
| DC _{MAX} | Maximum Duty Cycle | | 46 | 48 | 50 | 46 | 48 | 50 | % |
| DC _{MIN} | Minimum Duty Cycle | | | | 0 | | | 0 | % |
| Power Consumption Section | | | | | | | | | |

| Symbol | Parameter | Test Conditions | SG1844/SG1845 | | | SG3844/SG3845 | | | Units |
|----------------|-------------------------------|---|---------------|------|-----|---------------|------|-----|-------|
| | | | Min. | Typ. | Max | Min. | Typ. | Max | |
| I _s | Start-Up Current | | | 0.5 | 1 | | 0.5 | 1 | mA |
| I | Operating Supply Current | V _{F_{FB}} = V _{I_{SENSE}} = 0V | | 11 | 17 | | 11 | 17 | mA |
| Z | V _{CC} Zener Voltage | I _{CC} = 25mA | | 34 | | | 34 | | V |

Note:

- These parameters, although guaranteed, are not 100% tested in production.
- Parameter measured at trip point of latch with V_{F_{FB}} = 0.
- Gain defined as: $A = \Delta V_{COMP} / \Delta V_{I_{SENSE}}$; $0 \leq V_{I_{SENSE}} \leq 0.8V$
- Adjust V_{CC} above the start threshold before setting at 15V.
- Output frequency equals one half of oscillator frequency.

Block Diagram



* - V_{CC} and V_C are internally connected for 8-pin packages.

** - POWER GROUND and GROUND are internally connected for 8-pin packages.

Figure 2 - Block Diagram

Characteristic Curves

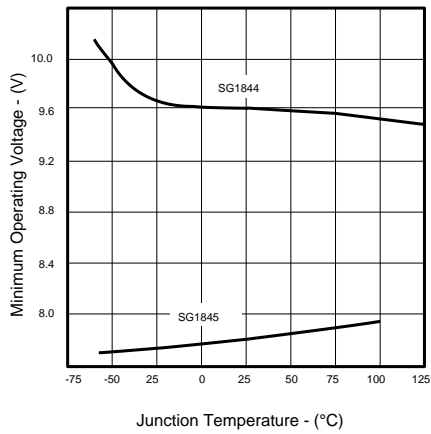


Figure 3 - Drop-out Voltage vs. Temperature

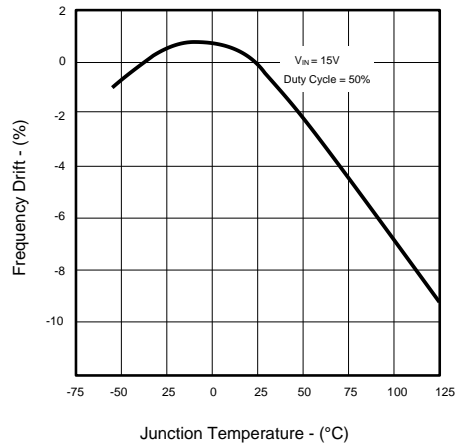


Figure 4 - Oscillator Temperature Stability

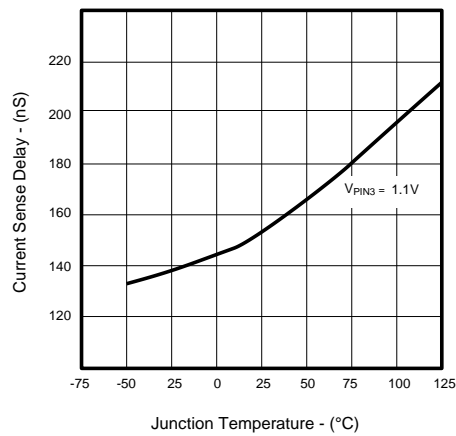


Figure 5 - Current Sense to Output Delay vs. Temperature

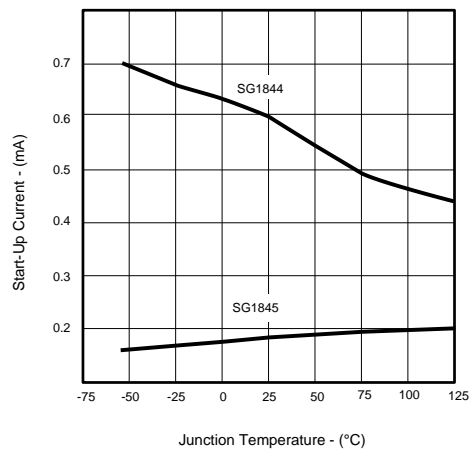


Figure 6 - Start-Up Current vs. Temperature

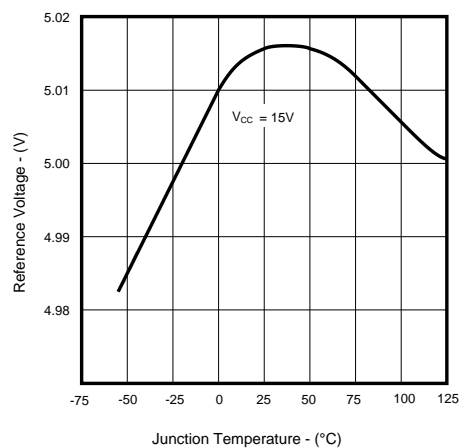


Figure 7 - Reference Voltage vs. Temperature

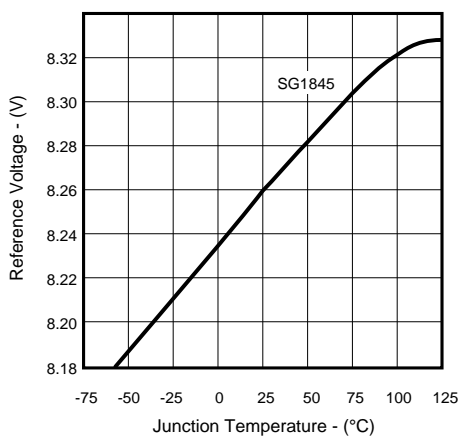


Figure 8 - Start-Up Voltage Threshold vs. Temperature

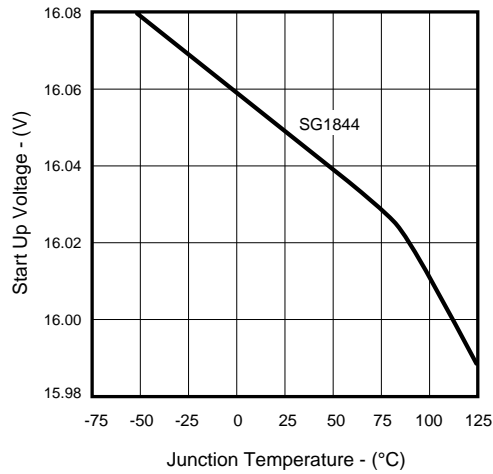


Figure 9 - Start-Up Voltage Threshold vs. Temperature

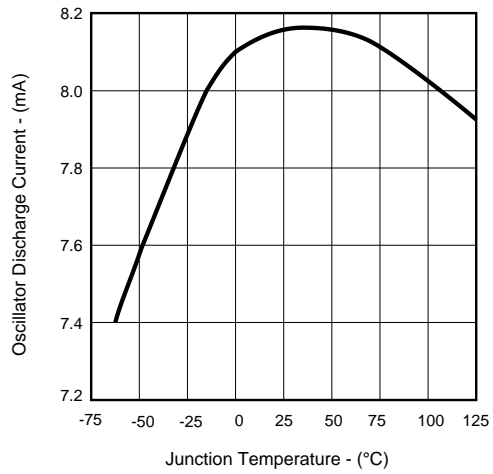


Figure 10 - Oscillator Discharge Current vs. Temperature

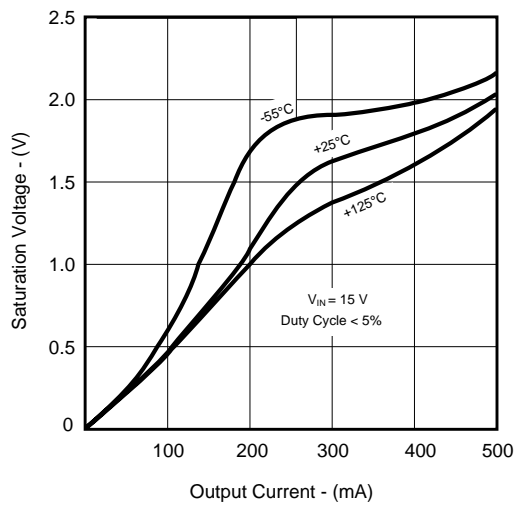


Figure 11 - Output Saturation Voltage vs. Output Current and Temperature (Sink Transistor)

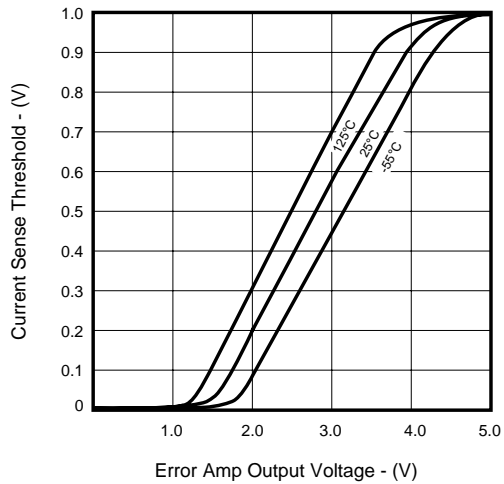


Figure 12 - Current Sense Threshold vs. Error Amplifier Output

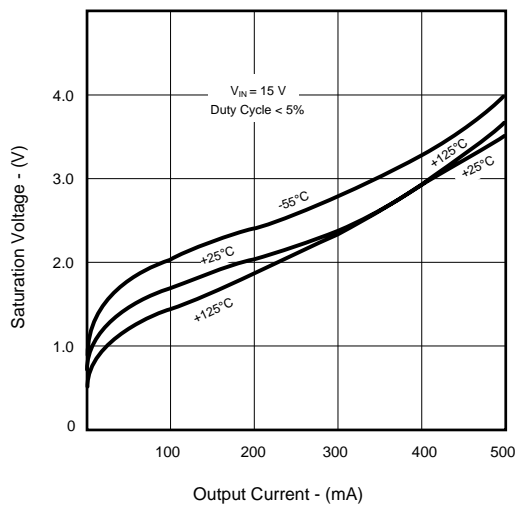


Figure 13 - Output Saturation Voltage vs. Output Current and Temperature (Source Transistor)

Application Information

The oscillator of the 1844/45 family of PWM's is programmed by the external timing components (R_T , C_T) as shown in Figure 14.

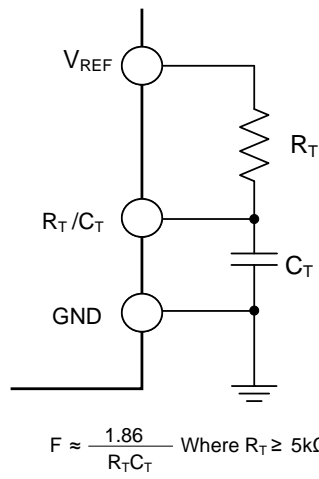


Figure 14 - Oscillator Timing Circuit

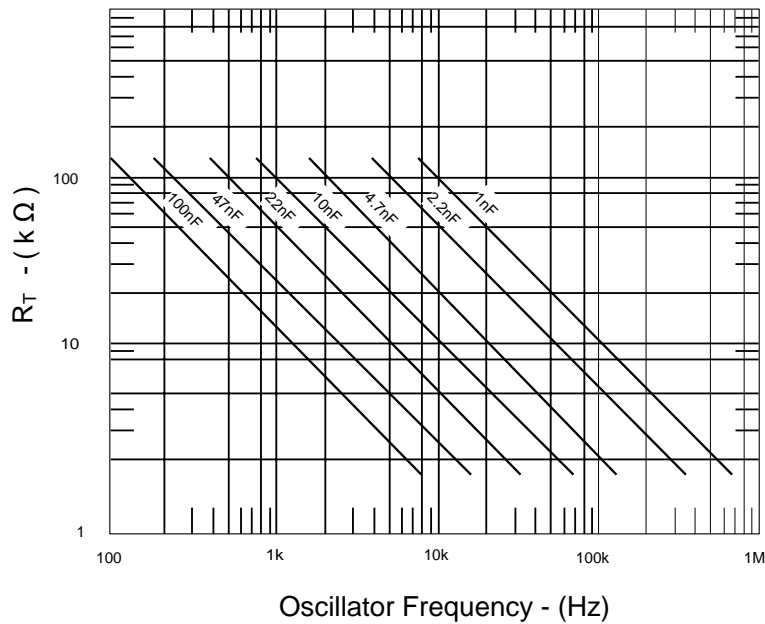


Figure 15 - Oscillator Frequency vs. R_T for various C_T

Typical Application Circuits

Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.

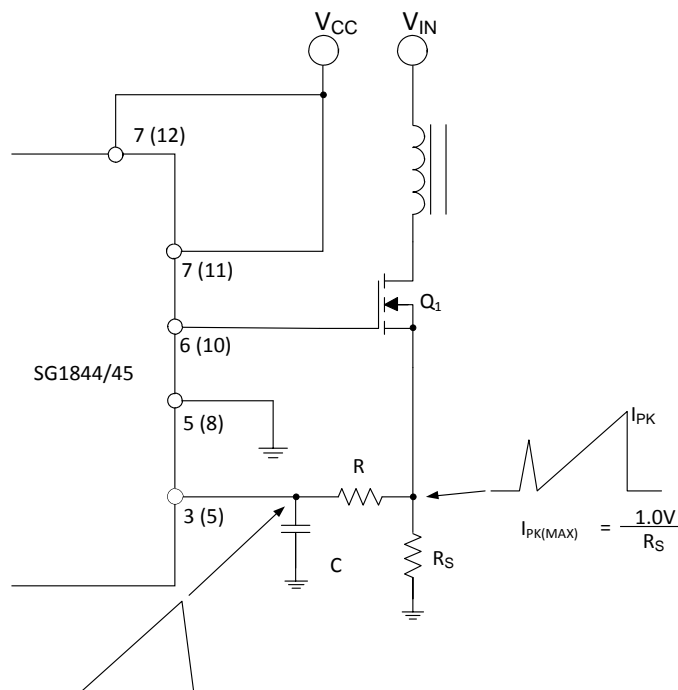


Figure 16 • Current Sense Spike Suppression

The RC low-pass filter will eliminate the leading edge current spike caused by parasitic of Power MOSFET.

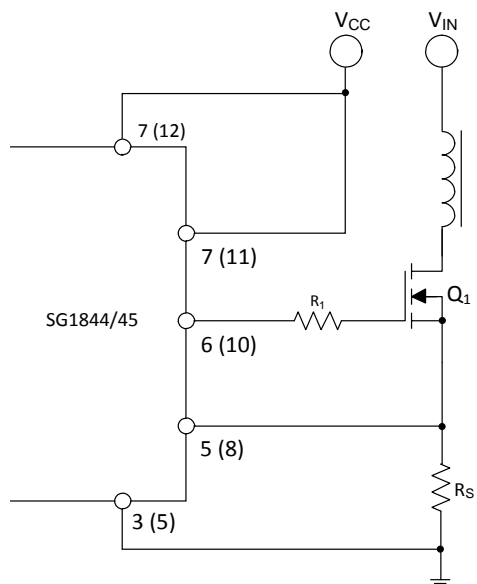


Figure 17 • MOSFET Parasitic Oscillations

A resistor (R₁) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

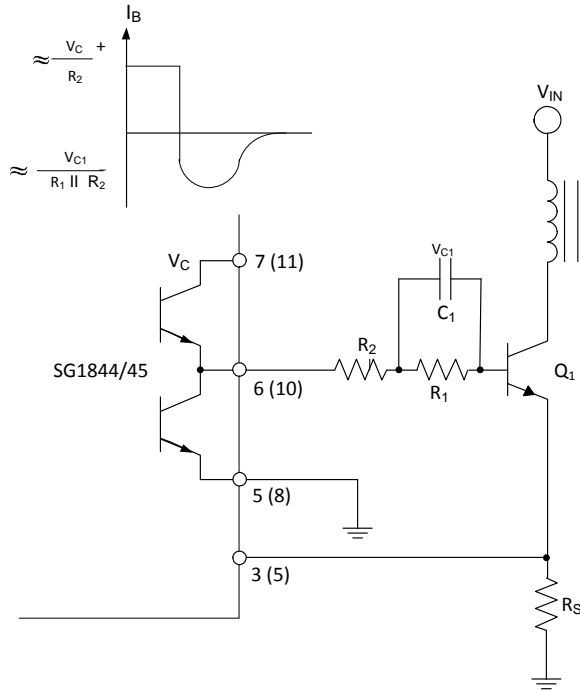


Figure 18 - Bipolar Transistor Drive

The 1844/45 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

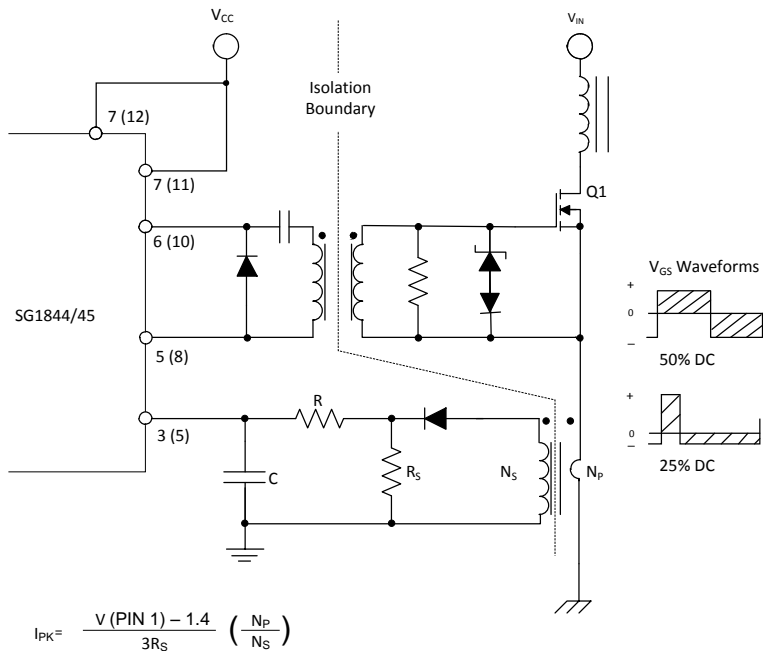
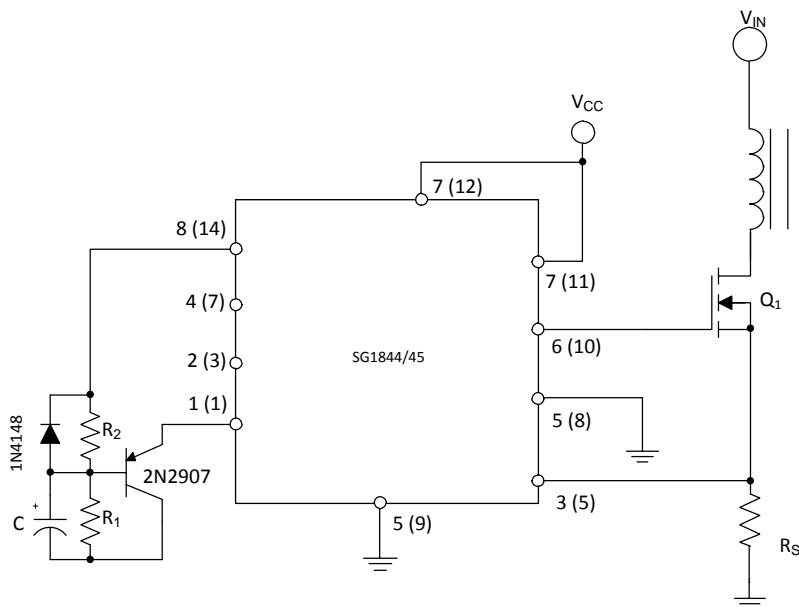


Figure 19 - Isolated MOSFET Drive

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.



$$I_{PK} = \frac{V_1}{R_S} \quad \text{Where, } 0 \leq V_1 \leq 1.0 \text{ V}$$

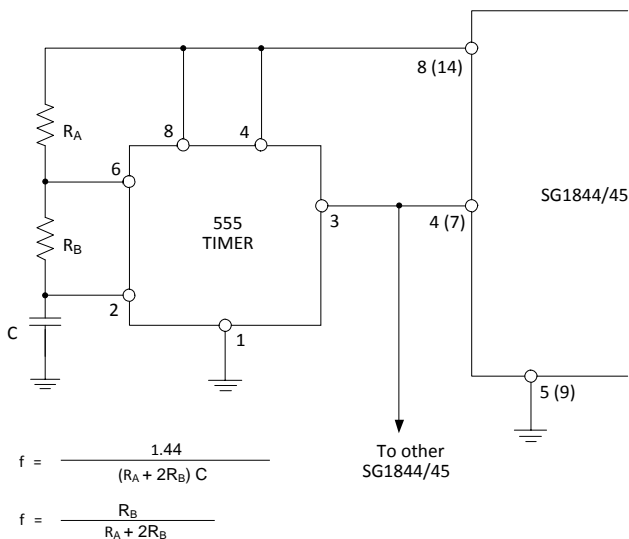
$$\text{and } V_1 = \frac{1.43 - 0.23 \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}}$$

$$t_{SOFTSTART} = -\ln\left[\frac{V_C}{R_2}\right] C \frac{R_1 R_2}{R_2 + R_2}$$

$$\text{Where, } V_2 = \frac{0.05}{1 + \frac{R_1}{R_2}}$$

Figure 20 • Adjustable Buffered Reduction of Clamp Level with Softstart

Softstart and adjustable peak current can be done with the external circuitry shown above.



$$f = \frac{1.44}{(R_A + 2R_B) C}$$

$$f = \frac{R_B}{R_A + 2R_B}$$

Figure 21 • External Duty Cycle Clamp and Multi-Unit Synchronization

Precision duty cycle limiting for a duty cycle of <50%, as well as synchronizing several 1844/45's is possible with the above circuitry.

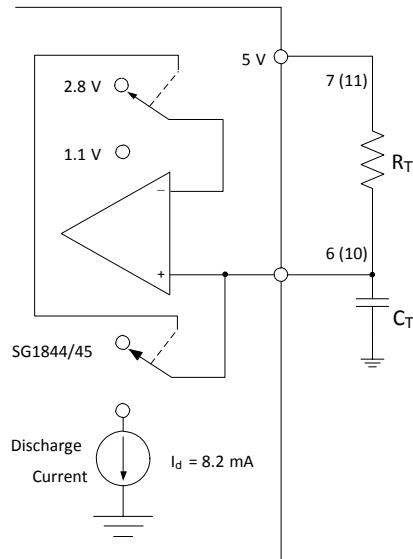


Figure 22 · Oscillator Connection

The oscillator is programmed by the values selected for the timing components R_T and C_T . Refer to application information for calculation of the component values.

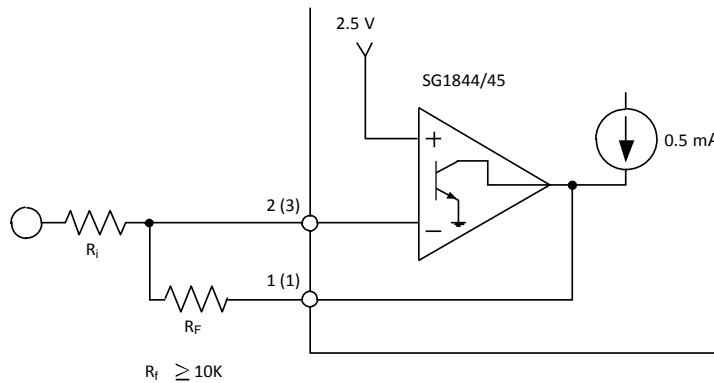
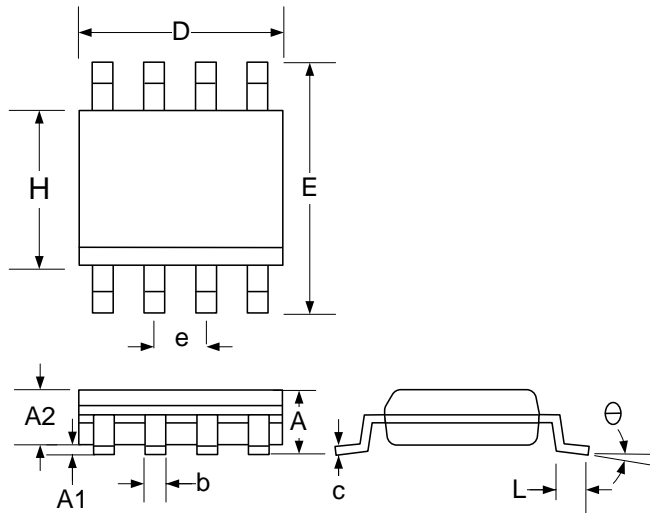


Figure 23 · Error Amplifier Connection

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.



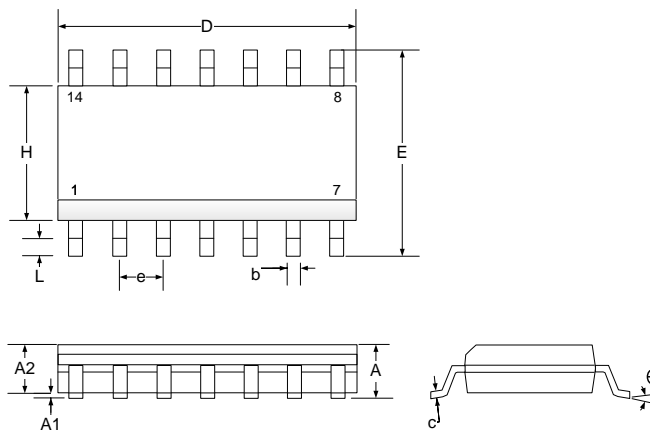
| Dim | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | 1.25 | 1.52 | 0.049 | 0.060 |
| b | 0.33 | 0.51 | 0.013 | 0.020 |
| c | 0.19 | 0.25 | 0.007 | 0.010 |
| D | 4.83 | 5.21 | 0.189 | 0.205 |
| E | 5.79 | 6.20 | 0.228 | 0.244 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 3.81 | 4.01 | 0.150 | 0.158 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| θ | 0 | 8 | 0 | 8 |
| *LC | | .010 | | 0.004 |

*Lead Coplanarity

Note:

- Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage

Figure 24 • DM 8-Pin SOIC Package Dimensions



| Dim | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | 1.25 | 1.52 | 0.049 | 0.060 |
| b | 0.33 | 0.51 | 0.013 | 0.020 |
| c | 0.19 | 0.25 | 0.007 | 0.010 |
| D | 8.54 | 8.74 | 0.336 | 0.344 |
| E | 5.79 | 6.20 | 0.228 | 0.244 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 3.81 | 4.01 | 0.150 | 0.158 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| θ | 0 | 8 | 0 | 8 |
| *LC | | .010 | | 0.004 |

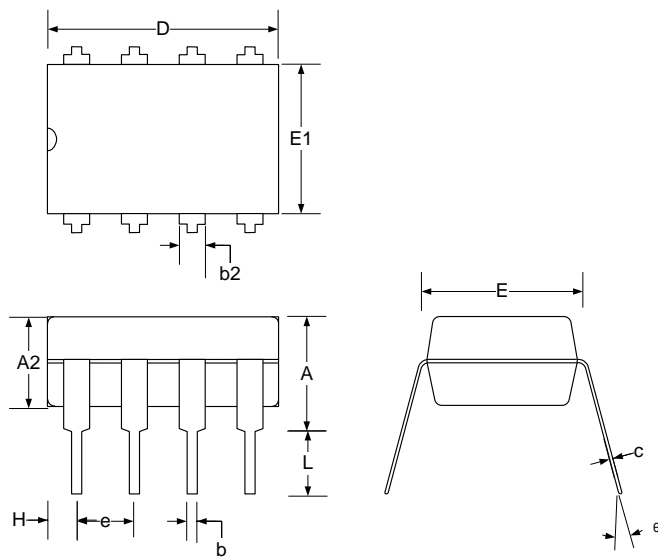
*Lead Coplanarity

Note:

- Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage

Figure 25 • D 14-Pin SOIC Package Dimensions

PACKAGE OUTLINE DIMENSIONS



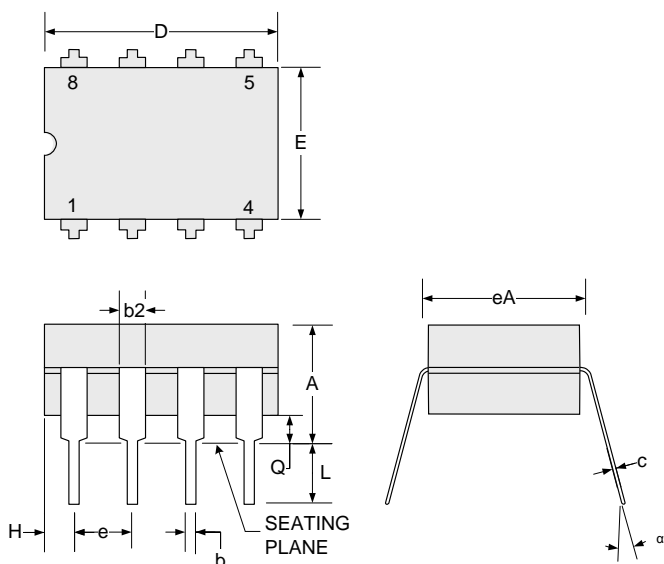
| Dim | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | | 5.08 | | 0.200 |
| A2 | 3.30 Typ. | | 1.30 Typ. | |
| b | 0.38 | 0.51 | 0.145 | 0.020 |
| b2 | 0.76 | 1.65 | 0.030 | 0.065 |
| c | 0.20 | 0.38 | 0.008 | 0.015 |
| D | | 10.16 | | 0.400 |
| E | 7.62 BSC | | 0.300 BSC | |
| e | 2.54 BSC | | 0.100 BSC | |
| E1 | 6.10 | 6.86 | 0.240 | 0.270 |
| L | 3.05 | | 0.120 | |
| θ | 0 | 15 | 0 | 15 |

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 26 • M 8-Pin PDIP Package Dimensions

PACKAGE OUTLINE DIMENSIONS

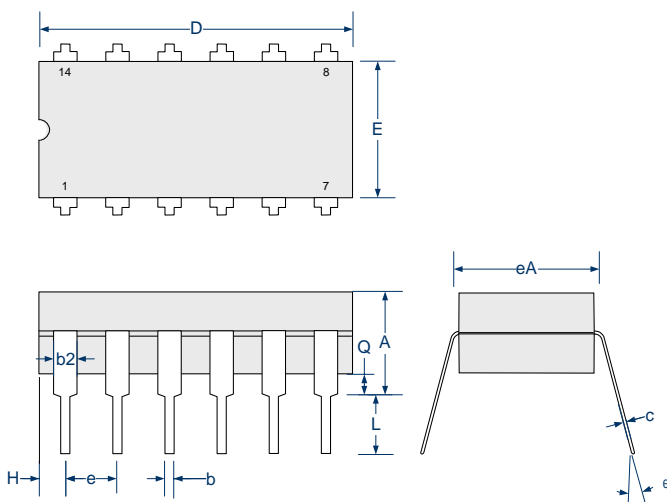


| Dim | MILLIMETERS | | INCHES | |
|----------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.32 | 5.08 | 0.170 | 0.200 |
| b | 0.38 | 0.51 | 0.015 | 0.020 |
| b2 | 1.04 | 1.65 | 0.045 | 0.065 |
| c | 0.20 | 0.38 | 0.008 | 0.015 |
| D | 9.52 | 10.29 | 0.375 | 0.405 |
| E | 5.59 | 7.11 | 0.220 | 0.280 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 7.37 | 7.87 | 0.290 | 0.310 |
| H | 0.63 | 1.78 | 0.025 | 0.070 |
| L | 3.18 | 4.06 | 0.125 | 0.160 |
| α | - | 15° | - | 15° |
| Q | 0.51 | 1.02 | 0.020 | 0.040 |

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 27 - Y 8-Pin Cerdip Package Dimensions



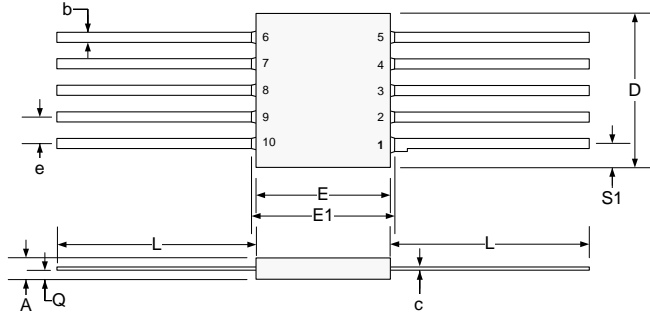
| Dim | MILLIMETERS | | INCHES | |
|----------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.32 | 5.08 | 0.170 | 0.200 |
| b | 0.38 | 0.51 | 0.015 | 0.020 |
| b2 | 1.04 | 1.65 | 0.045 | 0.065 |
| c | 0.20 | 0.38 | 0.008 | 0.015 |
| D | 19.30 | 19.94 | 0.760 | 0.785 |
| E | 5.59 | 7.11 | 0.220 | 0.280 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 7.37 | 7.87 | 0.290 | 0.310 |
| H | 0.63 | 1.78 | 0.025 | 0.070 |
| L | 3.18 | 4.06 | 0.125 | 0.160 |
| α | - | 15° | - | 15° |
| Q | 0.51 | 1.02 | 0.020 | 0.040 |

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 28 - J 14-Pin Cerdip Package Dimensions

PACKAGE OUTLINE DIMENSIONS

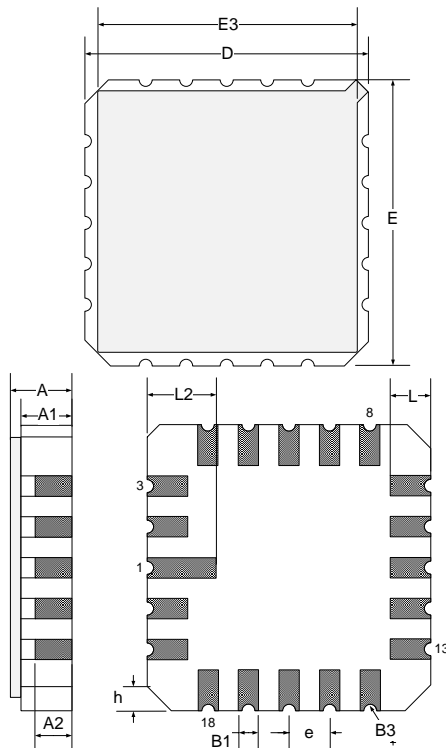


| Dim | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.45 | 1.70 | 0.057 | 0.067 |
| b | 0.25 | 0.483 | 0.010 | 0.019 |
| c | 0.102 | 0.152 | 0.004 | 0.006 |
| D | - | 7.37 | - | 0.290 |
| E | 6.04 | 6.40 | 0.238 | 0.252 |
| E1 | - | 6.91 | - | 0.272 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 6.35 | 9.40 | 0.250 | 0.370 |
| Q | 0.51 | 1.02 | 0.020 | 0.040 |
| S1 | 0.20 | 0.38 | 0.008 | 0.015 |

Note:

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13mm (.0005") radius of the true position (TP) at maximum material condition.
3. Dimension "e" determines a zone within which all body and lead irregularities lie.

Figure 29 - F 10-Pin Ceramic Flatpack Package Dimensions



| Dim | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| D/E | 8.64 | 9.14 | 0.340 | 0.360 |
| E3 | - | 8.128 | - | 0.320 |
| e | 1.270 BSC | | 0.050 BSC | |
| B1 | 0.635 TYP | | 0.025 TYP | |
| L | 1.02 | 1.52 | 0.040 | 0.060 |
| A | 1.626 | 2.286 | 0.064 | 0.090 |
| h | 1.016 TYP | | 0.040 TYP | |
| A1 | 1.372 | 1.68 | 0.054 | 0.066 |
| A2 | - | 1.168 | - | 0.046 |
| L2 | 1.91 | 2.41 | 0.075 | 0.95 |
| B3 | 0.203R | | 0.008R | |

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 30 - L 20-Pin Leadless Chip Carrier Package Dimensions



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