THE DATASHEET OF

ADM7160ACPZN3.3-R7

Ultralow Noise, 200 mA Linear Regulator

Data Sheet **ADM7160**

FEATURES

- PSRR performance of 54 dB at 100 kHz
- Ultralow noise independent of V_{OUT}
  - 3 µV rms, 0.1 Hz to 10 Hz
  - 9.5 µV rms, 0.1 Hz to 100 kHz
  - 9 µV rms, 10 Hz to 100 kHz
  - 17 µV rms, 10 Hz to 1 MHz
- Low dropout voltage: 150 mV at 200 mA load
- Maximum output current: 200 mA
- Input voltage range: 2.2 V to 5.5 V
- Low quiescent and shutdown current
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature: −2.5%/+1.5%
- 5-lead TSOT package and 6-lead LFCSP package

APPLICATIONS

- ADC/DAC power supplies
- RF, VCO, and PLL power supplies
- Post dc-to-dc regulation

APPLICATION CIRCUIT

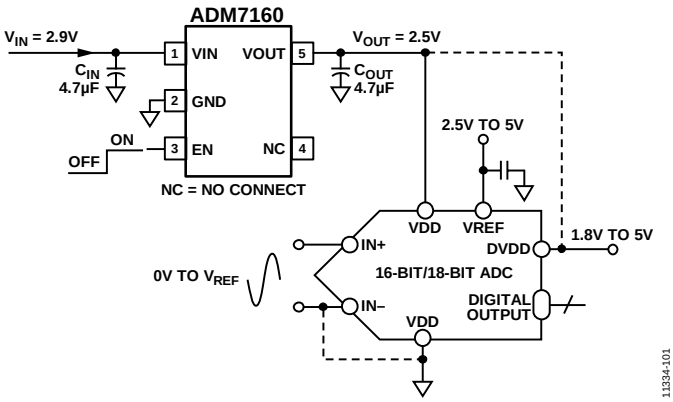

Figure 1. ADM7160 Powering a 16-Bit/18-Bit ADC

GENERAL DESCRIPTION

The ADM7160 is an ultralow noise, low dropout linear regulator that operates from 2.2 V to 5.5 V and provides up to 200 mA of output current. The low 150 mV dropout voltage at 200 mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADM7160 achieves ultralow noise performance without the need for a bypass capacitor, making the device ideal for noise-sensitive analog front-end and RF applications. The ADM7160 also achieves ultralow noise performance without compromising PSRR or transient line and load performance.

Current-limit and thermal overload protection circuits prevent damage under adverse conditions. The ADM7160 also includes an internal pull-down resistor on the EN input.

The ADM7160 is specifically designed for stable operation with tiny 1 µF, ±30% ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADM7160 is available in tiny 5-lead TSOT and 6-lead LFCSP packages with 16 fixed output voltage options, ranging from 1.1 V to 3.3 V. The LFCSP offers a very compact solution that provides excellent thermal performance for applications that require up to 200 mA of output current in a small, low profile footprint.

Rev. A
Document Feedback

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SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater; EN = V_{IN}, I_{LOAD} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.2		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{LOAD} = 0 µA		10		µA
		I_{LOAD} = 0 µA, T_J = −40°C to +125°C			20	µA
		I_{LOAD} = 100 µA		20		µA
		I_{LOAD} = 100 µA, T_J = −40°C to +125°C			40	µA
		I_{LOAD} = 10 mA		60		µA
		I_{LOAD} = 10 mA, T_J = −40°C to +125°C			90	µA
		I_{LOAD} = 200 mA		265		µA
		I_{LOAD} = 200 mA, T_J = −40°C to +125°C			350	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.2		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{LOAD} = 10 mA	−1		+1	%
		100 µA < I_{LOAD} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C				
		V_{OUT} < 1.8 V	−3		+2	%
		V_{OUT} ≥ 1.8 V	−2.5		+1.5	%
TEMPERATURE COEFFICIENT	TEMPCO	V_{OUT} = 2.5 V, T_J = 25°C to 85°C		29		ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C	−0.05		+0.05	%/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$					
V_{OUT} < 1.8 V		I_{LOAD} = 100 µA to 200 mA		0.006		%/mA
		I_{LOAD} = 100 µA to 200 mA, T_J = −40°C to +125°C			0.012	%/mA
V_{OUT} ≥ 1.8 V		I_{LOAD} = 100 µA to 200 mA		0.003		%/mA
		I_{LOAD} = 100 µA to 200 mA, T_J = −40°C to +125°C			0.008	%/mA
DROPOUT VOLTAGE[1]	$V_{DROPOUT}$	I_{LOAD} = 10 mA		10		mV
		I_{LOAD} = 10 mA, T_J = −40°C to +125°C			30	mV
		I_{LOAD} = 200 mA		150		mV
		I_{LOAD} = 200 mA, T_J = −40°C to +125°C			230	mV
START-UP TIME[2]	$t_{START-UP}$	V_{OUT} = 3.3 V		180		µs
CURRENT-LIMIT THRESHOLD[3]	I_{LIMIT}	T_J = 0°C to 125°C	220	300	400	mA
UNDERVOLTAGE LOCKOUT	UVLO	T_J = −40°C to +125°C				
Input Voltage Rising	$UVLO_{RISE}$				1.96	V
Input Voltage Falling	$UVLO_{FALL}$		1.28			V
Hysteresis	$UVLO_{HYS}$			120		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.2 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.2 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Pull-Down Resistance	R_{EN}	V_{IN} = V_{EN} = 5.5 V		2.6		MΩ
OUTPUT NOISE	OUT_{NOISE}	V_{IN} = 5 V, V_{OUT} = 2.5 V				
		0.1 Hz to 10 Hz		3		µV rms
		0.1 Hz to 100 kHz		9.5		µV rms
		10 Hz to 100 kHz		9		µV rms
		10 Hz to 1 MHz		17		µV rms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	I_{LOAD} = 100 mA				
$V_{IN} = V_{OUT} + 0.5$ V		100 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V		49		dB
		500 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V		43		dB
		1 MHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V		43		dB
		100 kHz, V_{IN} = 3.0 V, V_{OUT} = 2.5 V		46		dB
		500 kHz, V_{IN} = 3.0 V, V_{OUT} = 2.5 V		44		dB
		1 MHz, V_{IN} = 3.0 V, V_{OUT} = 2.5 V		44		dB
$V_{IN} = V_{OUT} + 1$ V		100 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V		54		dB
		500 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V		46		dB
		1 MHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V		46		dB
		100 kHz, V_{IN} = 3.5 V, V_{OUT} = 2.5 V		49		dB
		500 kHz, V_{IN} = 3.5 V, V_{OUT} = 2.5 V		47		dB
		1 MHz, V_{IN} = 3.5 V, V_{OUT} = 2.5 V		47		dB

[1] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This specification applies only to output voltages greater than 2.2 V.
[2] Start-up time is defined as the time from the rising edge of EN to when V_{OUT} is at 90% of its nominal value.
[3] Current-limit threshold is defined as the current at which the output voltage falls to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to fall to 90% of 3.0 V (that is, 2.7 V).

INPUT AND OUTPUT CAPACITORS, RECOMMENDED SPECIFICATIONS

T_A = −40°C to +125°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
Minimum Input and Output Capacitance[1]	C_{MIN}	0.7			µF
Capacitor ESR	R_{ESR}	0.001		0.2	Ω

[1] The minimum input and output capacitance should be greater than 0.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO regulator. For more information, see the Input and Output Capacitor Properties section.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +6.5 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADM7160 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits.

In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within the specification limits.

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). T_J is calculated using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions.

The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch printed circuit board (PCB). See JEDEC JESD51-7 and JESD51-9 for detailed information about board construction. For more information about the LFCSP package, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board.

JEDEC JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths, rather than through a single path as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package, as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications.

Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JEDEC JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W
6-Lead LFCSP	63.6	28.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

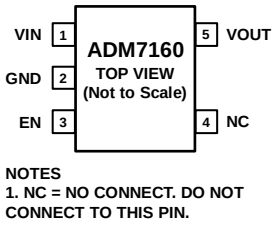

Figure 2. Pin Configuration, 5-Lead TSOT

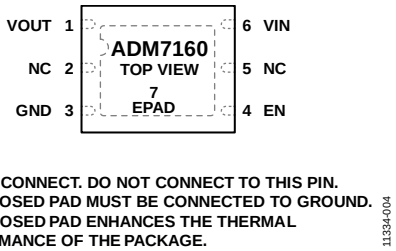

Figure 3. Pin Configuration, 6-Lead LFCSP

Table 5. Pin Function Descriptions

Pin No.			
TSOT	**LFCSP**	**Mnemonic**	**Description**
1	6	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	3	GND	Ground.
3	4	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	2, 5	NC	No Connect. Do not connect to this pin.
5	1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
N/A	7	EPAD	Exposed Pad. The exposed pad must be connected to ground. The exposed pad enhances the thermal performance of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 2.9 V, V_{OUT} = 2.5 V, I_{LOAD} = 1 mA, C_{IN} = C_{OUT} = 4.7 µF, T_A = 25°C, unless otherwise noted.

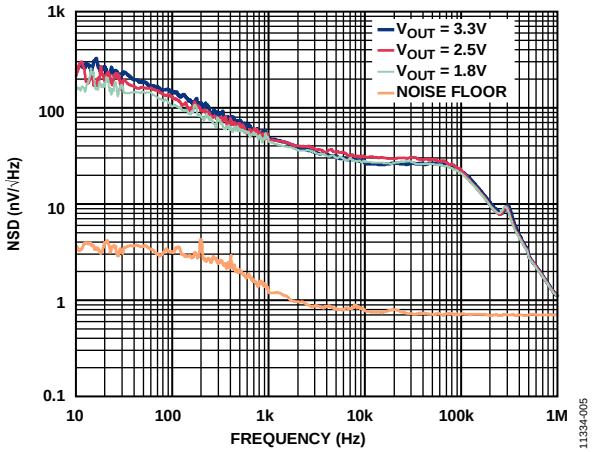

Figure 4. Noise Spectral Density at Various Output Voltages, I_{LOAD} = 10 mA

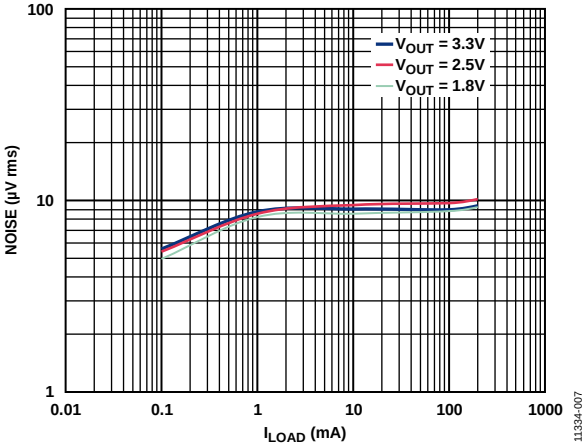

Figure 7. RMS Noise vs. Load Current, 10 Hz to 100 kHz

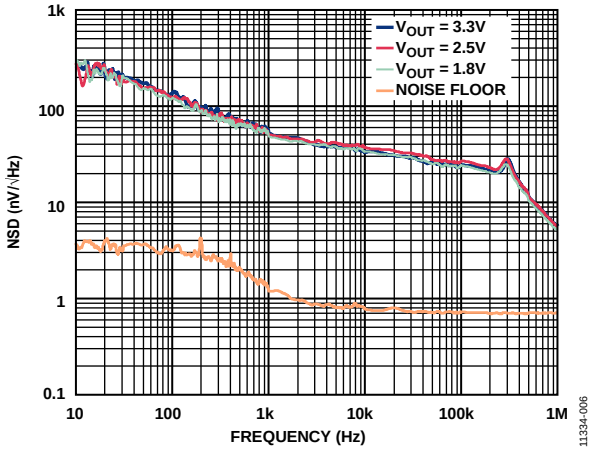

Figure 5. Noise Spectral Density at Various Output Voltages, I_{LOAD} = 200 mA

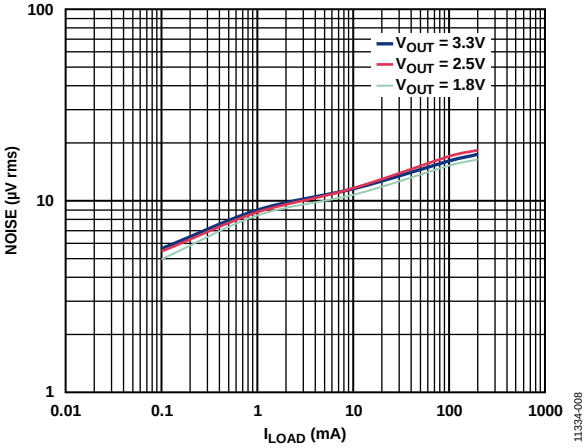

Figure 8. RMS Noise vs. Load Current, 10 Hz to 1 MHz

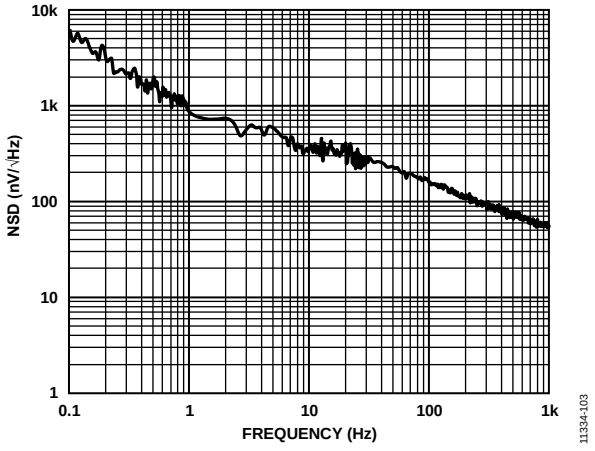

Figure 6. Noise Spectral Density, 0.1 Hz to 1 kHz

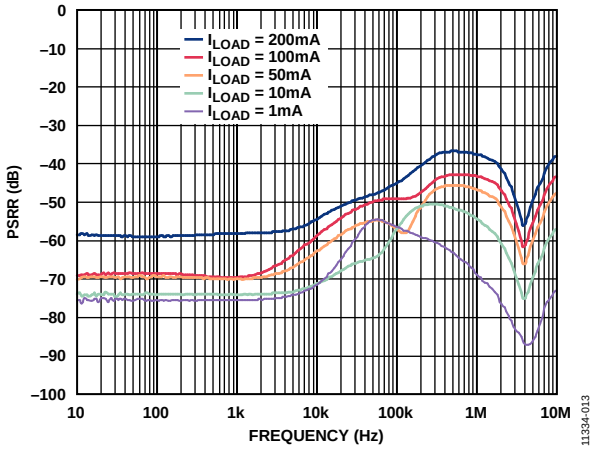

Figure 9. PSRR vs. Frequency and Load Current, 500 mV Headroom, V_{OUT} = 3.3 V

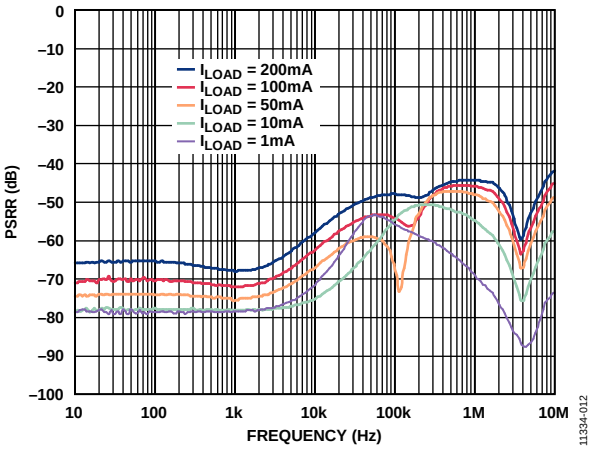

Figure 12. PSRR vs. Frequency and Load Current, 1 V Headroom, V_{OUT} = 3.3 V

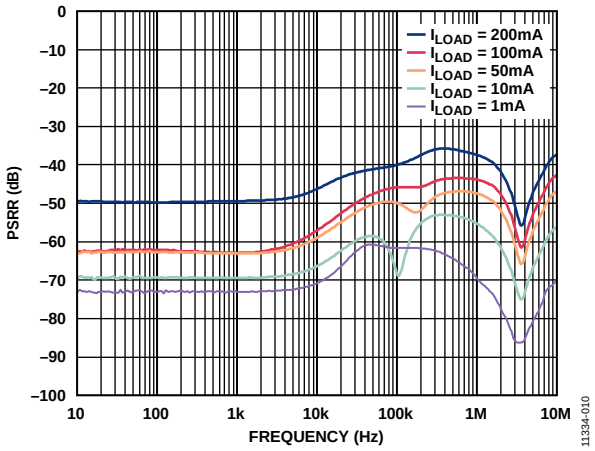

Figure 10. PSRR vs. Frequency and Load Current, 500 mV Headroom, V_{OUT} = 2.5 V

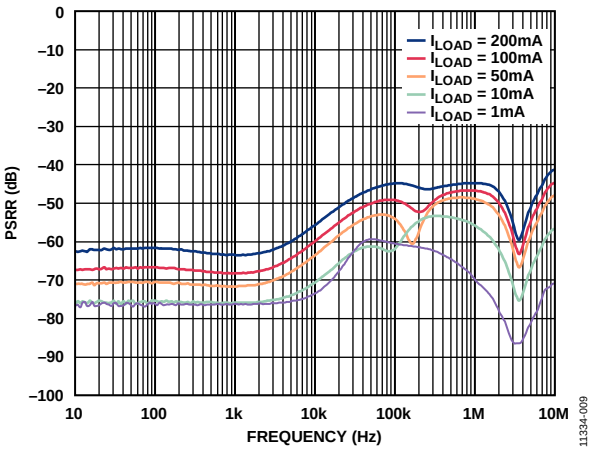

Figure 13. PSRR vs. Frequency and Load Current, 1 V Headroom, V_{OUT} = 2.5 V

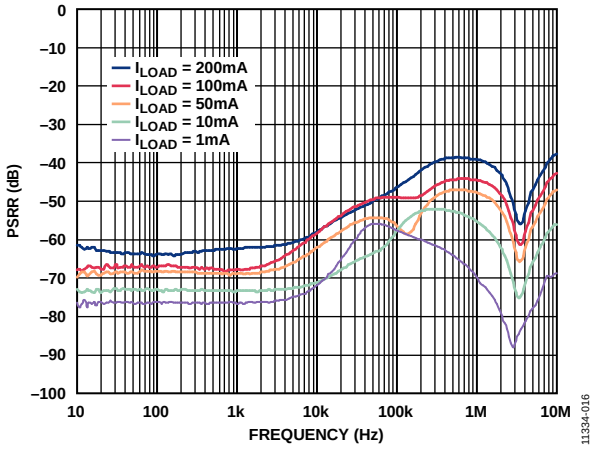

Figure 11. PSRR vs. Frequency and Load Current, 500 mV Headroom, V_{OUT} = 1.8 V

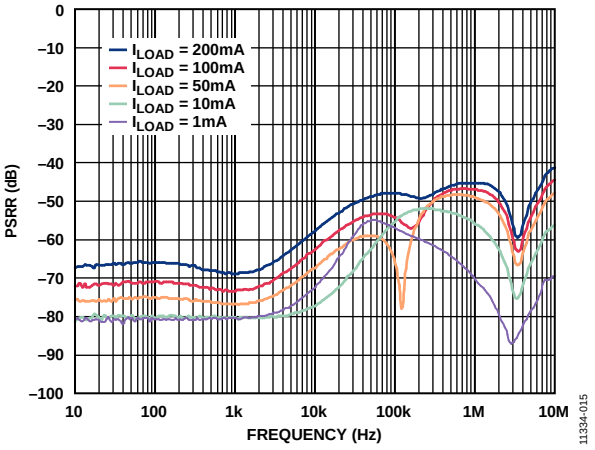

Figure 14. PSRR vs. Frequency and Load Current, 1 V Headroom, V_{OUT} = 1.8 V

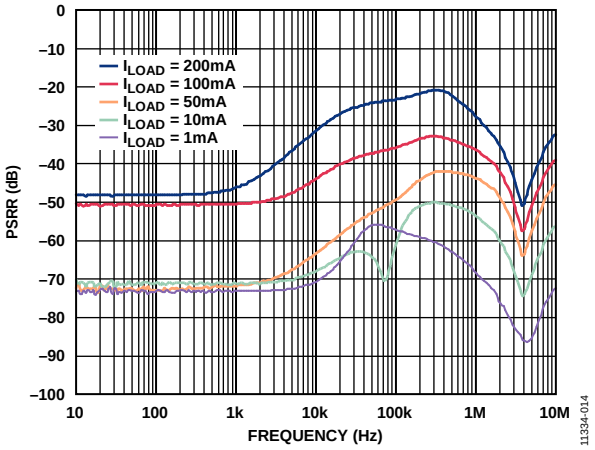

Figure 15. PSRR vs. Frequency and Load Current, 300 mV Headroom, V_{OUT} = 3.3 V

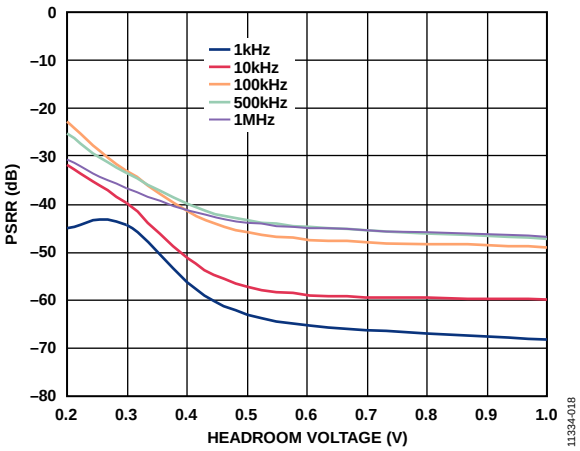

Figure 18. PSRR vs. Headroom Voltage at Various Frequencies, I_{LOAD} = 100 mA

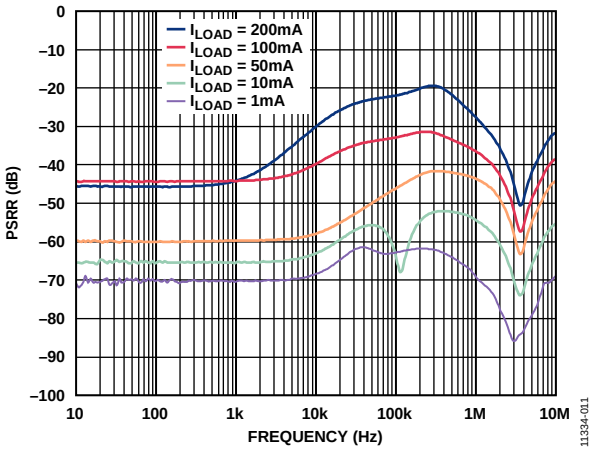

Figure 16. PSRR vs. Frequency and Load Current, 300 mV Headroom, V_{OUT} = 2.5 V

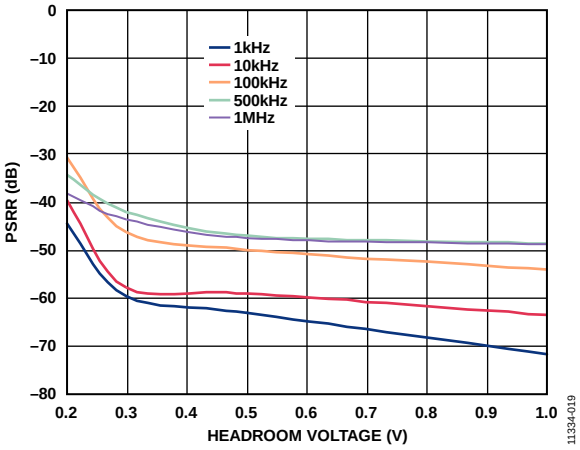

Figure 19. PSRR vs. Headroom Voltage at Various Frequencies, I_{LOAD} = 50 mA

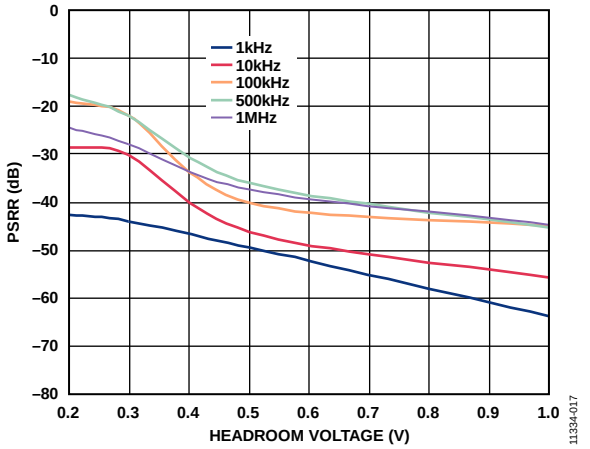

Figure 17. PSRR vs. Headroom Voltage at Various Frequencies, I_{LOAD} = 200 mA

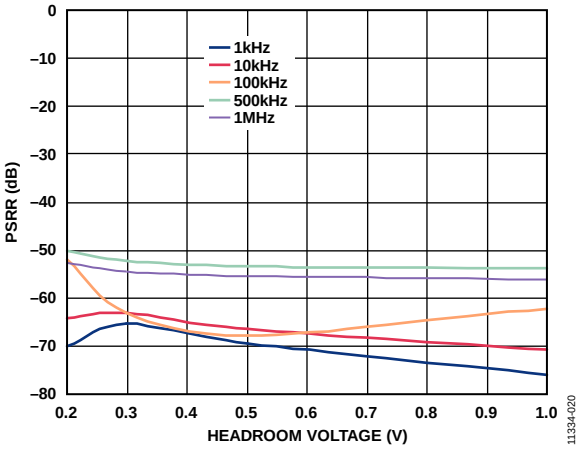

Figure 20. PSRR vs. Headroom Voltage at Various Frequencies, I_{LOAD} = 10 mA

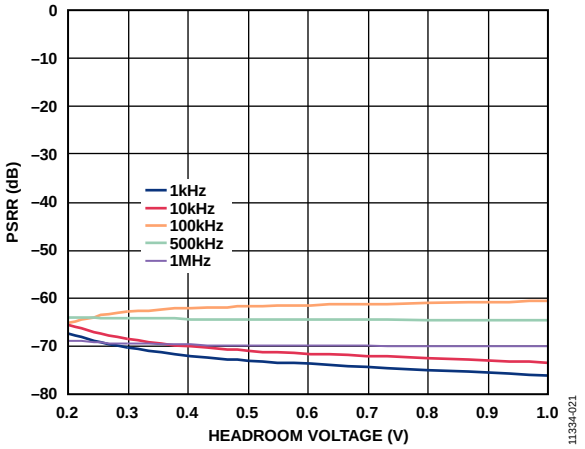

Figure 21. PSRR vs. Headroom Voltage at Various Frequencies, I_{LOAD} = 1 mA

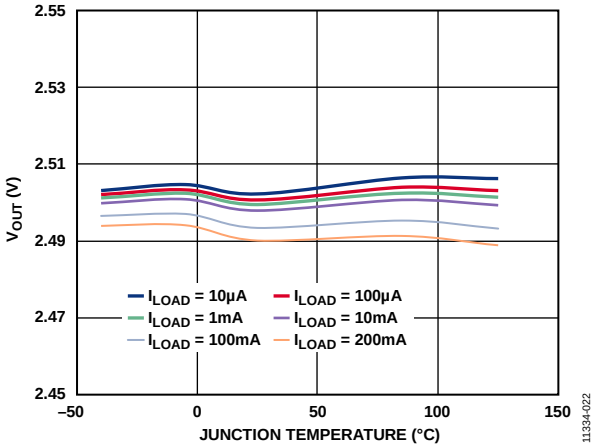

Figure 24. Output Voltage vs. Junction Temperature

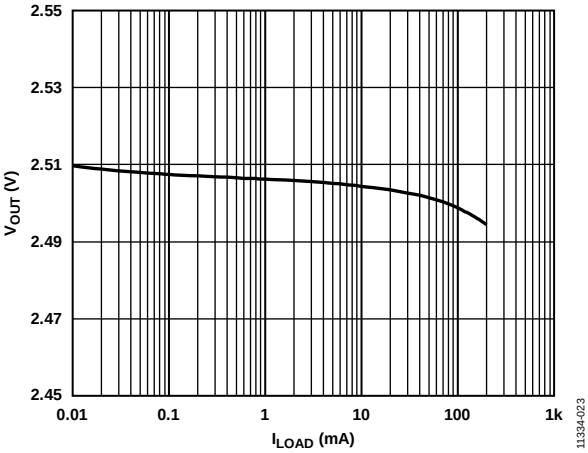

Figure 22. Output Voltage vs. Load Current

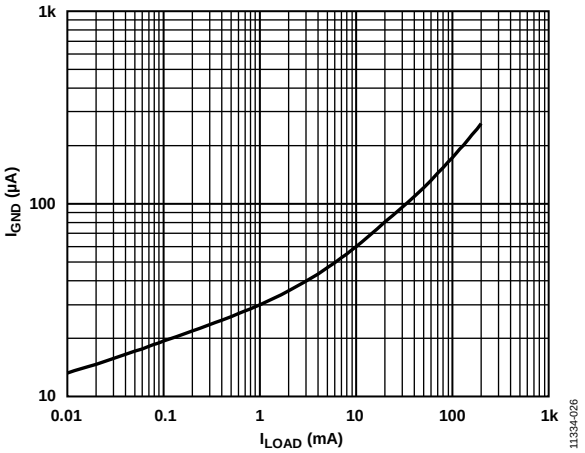

Figure 25. Ground Current vs. Load Current

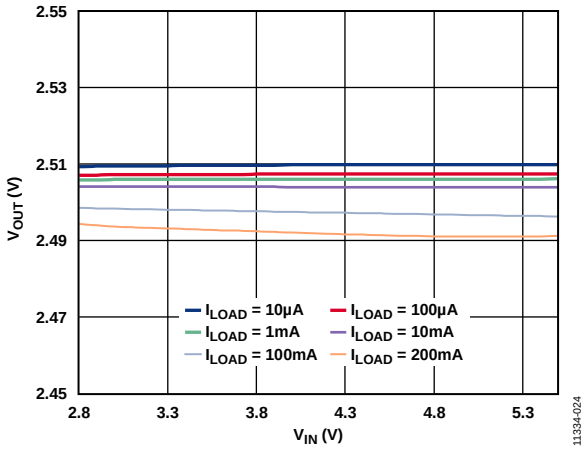

Figure 23. Output Voltage vs. Input Voltage

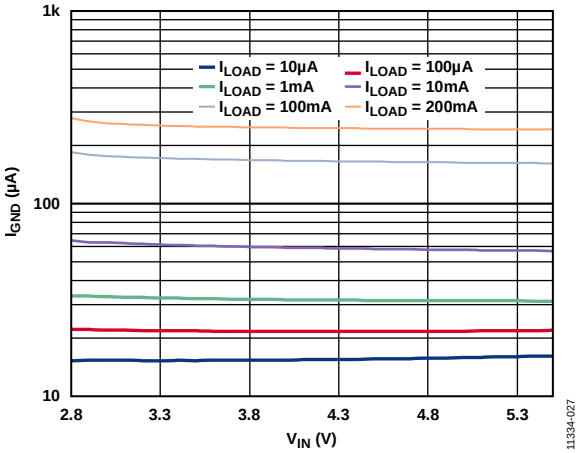

Figure 26. Ground Current vs. Input Voltage

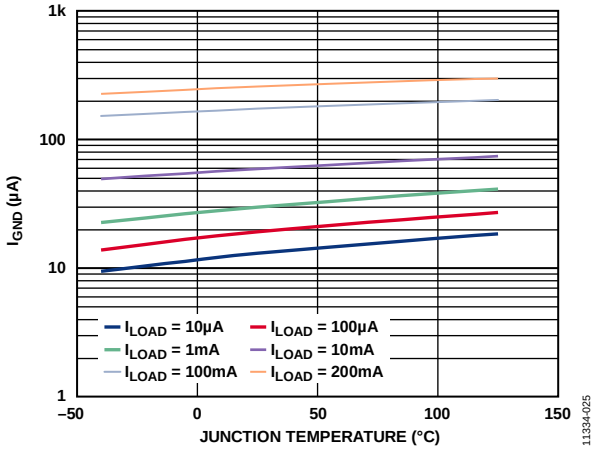

Figure 27. Ground Current vs. Junction Temperature

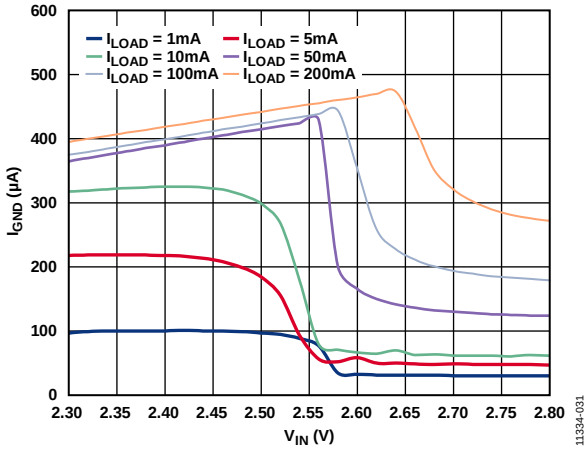

Figure 30. Ground Current vs. Input Voltage (in Dropout)

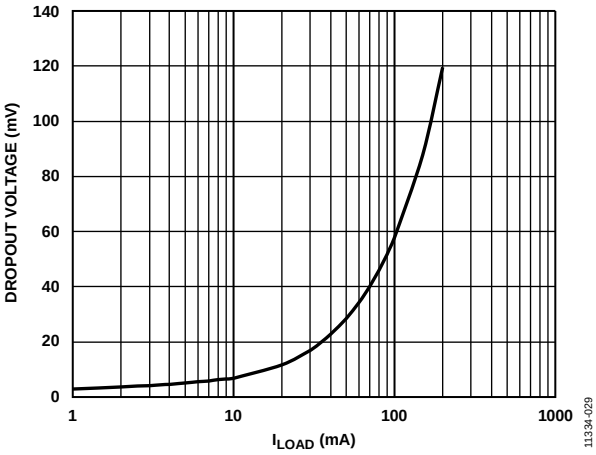

Figure 28. Dropout Voltage vs. Load Current

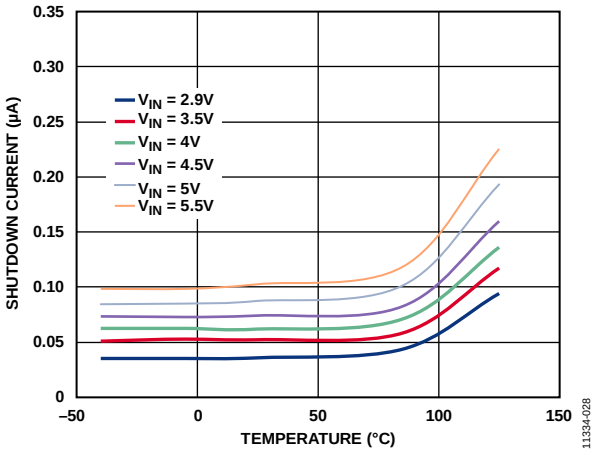

Figure 31. Shutdown Current vs. Temperature at Various Input Voltages

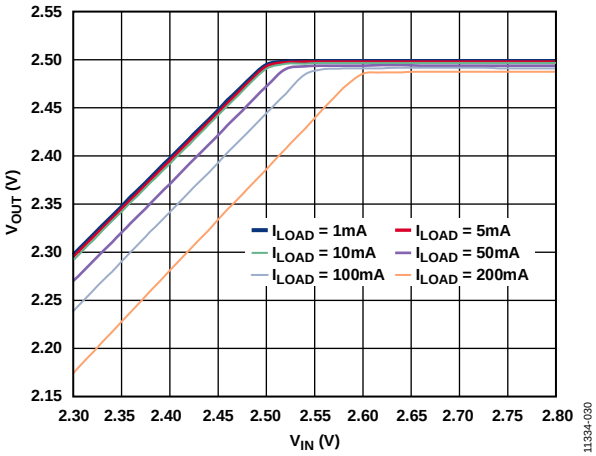

Figure 29. Output Voltage vs. Input Voltage (in Dropout)

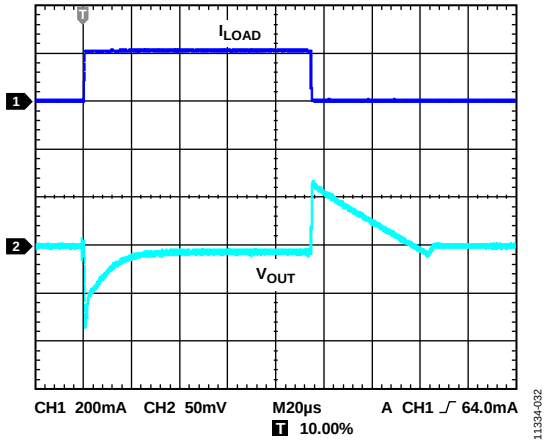

Figure 32. Load Transient Response, C_{IN} and C_{OUT} = 1 µF, I_{LOAD} = 1 mA to 200 mA

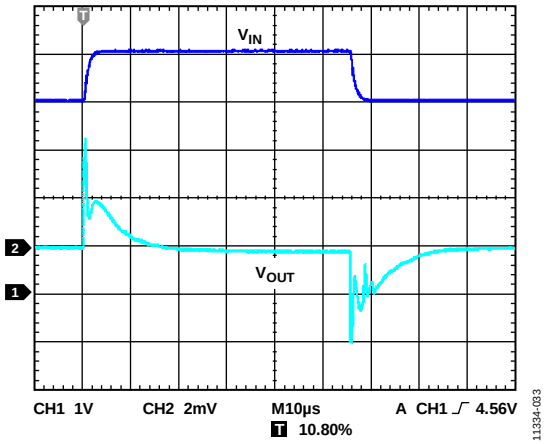

Figure 33. Line Transient Response, C_{IN} and C_{OUT} = 1 µF, I_{LOAD} = 200 mA

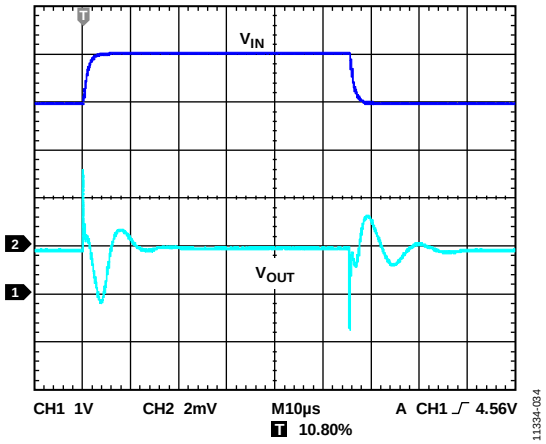

Figure 34. Line Transient Response, C_{IN} and C_{OUT} = 1 µF, I_{LOAD} = 1 mA

THEORY OF OPERATION

The ADM7160 is an ultralow noise, low quiescent current, low dropout linear regulator that operates from 2.2 V to 5.5 V and can provide up to 200 mA of output current. The ADM7160 consumes a low 265 µA of quiescent current (typical) at full load. Shutdown current consumption is typically 200 nA.

Using innovative design techniques, the ADM7160 provides superior noise performance for noise-sensitive analog front-end and RF applications without the need for a noise bypass capacitor. The ADM7160 is also optimized for use with small 1 µF ceramic capacitors.

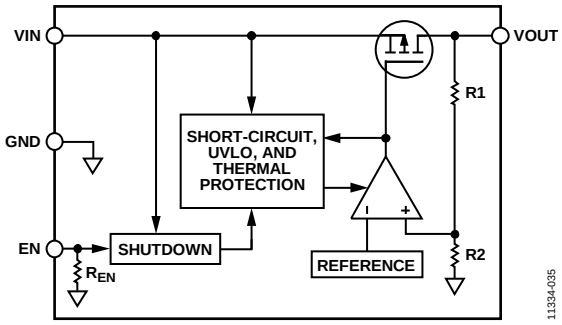

Figure 35. Internal Block Diagram

Internally, the ADM7160 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

An internal pull-down resistor on the EN input holds the input low when the EN pin is left open.

The ADM7160 is available in 16 output voltage options, ranging from 1.1 V to 3.3 V.

ENABLE FEATURE

The ADM7160 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

As shown in Figure 36, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off. The EN pin has built-in hysteresis. This hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

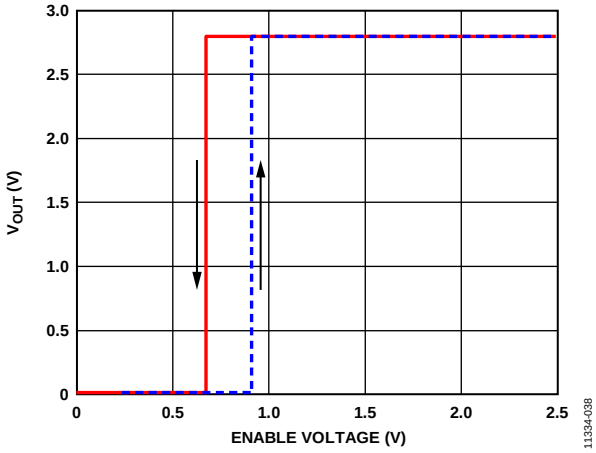

Figure 36. Typical EN Pin Operation

The EN pin active/inactive thresholds are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 37 shows typical EN active/inactive thresholds when the input voltage varies from 2.2 V to 5.5 V.

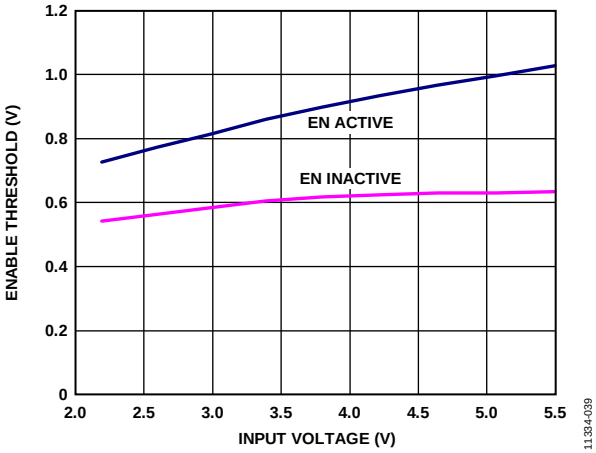

Figure 37. Typical EN Pin Thresholds vs. Input Voltage

SOFT START

The ADM7160 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 180 µs from when the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 38, the start-up time is dependent on the output voltage setting.

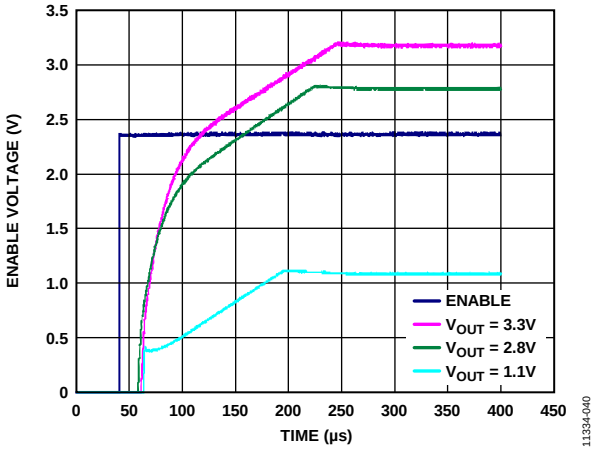

Figure 38. Typical Start-Up Behavior

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADM7160 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADM7160 is designed to reach current limit when the output load reaches 300 mA (typical). When the output load exceeds 300 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature begins to rise above 150°C, the output is turned off, reducing the output current to 0 mA. When the junction temperature falls below 135°C, the output is turned on again, and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADM7160 reaches current limit, so that only 300 mA is conducted into the short. If self-heating of the junction causes its temperature to rise above 150°C, thermal shutdown is activated, turning off the output and reducing the output current to 0 mA. As the junction temperature cools and falls below 135°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 300 mA and 0 mA that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADM7160 is designed for operation with small, space-saving ceramic capacitors, but it can function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADM7160. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADM7160 to large changes in load current. Figure 39 shows the transient response for an output capacitance value of 1 µF.

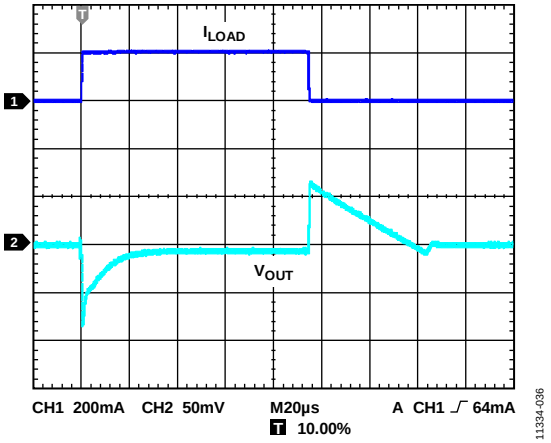

Figure 39. Output Transient Response, C_{OUT} = 1 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If output capacitance greater than 1 µF is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADM7160, as long as it meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have an adequate dielectric to ensure the minimum capacitance over the required temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 40 shows the capacitance vs. voltage bias characteristics of a 0402, 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is approximately ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

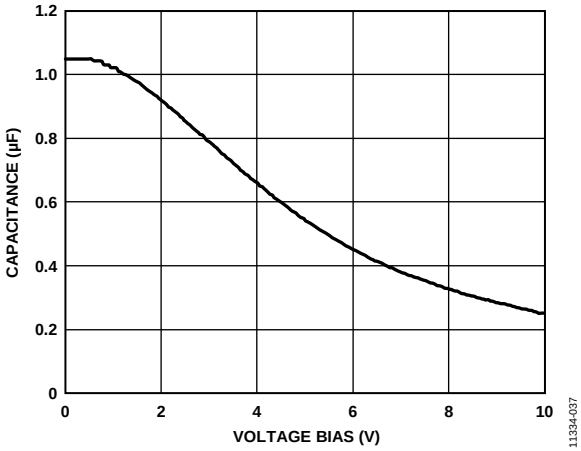

Figure 40. Capacitance vs. Voltage Bias Characteristics

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance (TOL) of the capacitor is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 40.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor selected in this example meets the minimum capacitance requirement of the LDO regulator over temperature and tolerance at the selected output voltage.

To guarantee the performance of the ADM7160, it is imperative that the effects of dc bias, temperature, and tolerance on the behavior of the capacitors be evaluated for each application.

Figure 41 and Figure 42 show the connection of 4.7 µF capacitors on the VIN and VOUT pins for the 5-lead TSOT and 6-lead LFCSP packages, respectively.

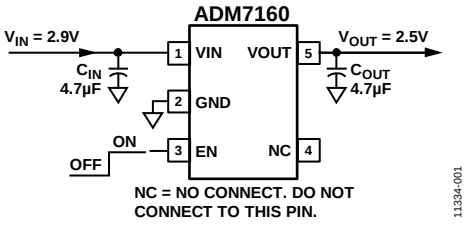

Figure 41. 5-Lead TSOT with 4.7 µF Input and Output Capacitors

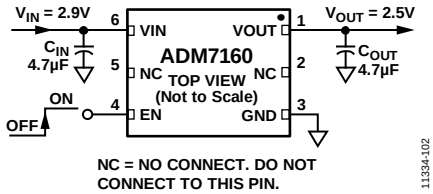

Figure 42. 6-Lead LFCSP with 4.7 µF Input and Output Capacitors

THERMAL CONSIDERATIONS

In most applications, the ADM7160 does not dissipate much heat due to its high efficiency. However, in applications with high ambient temperature and a high supply voltage-to-output voltage differential, the heat dissipated in the package can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the ADM7160 enters thermal shutdown. To prevent any permanent damage, the regulator recovers only after the junction temperature decreases below 135°C. Therefore, thermal analysis for the selected application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADM7160 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds used and the amount of copper used to solder the package GND pin and the exposed pad (in the case of the LFCSP) to the PCB.

Table 6 shows typical θ_{JA} values for the 5-lead TSOT and 6-lead LFCSP packages for various PCB copper sizes.

Table 6. Typical θ_{JA} Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**TSOT**	**LFCSP**
0[1]	170	231.2
50	152	161.8
100	146	150.1
300	134	111.5
500	131	91.8

[1] Device soldered to minimum size pin traces.

Table 7 shows the typical Ψ_{JB} values for the 5-lead TSOT and 6-lead LFCSP.

Table 7. Typical Ψ_{JB} Values

Package	Ψ_{JB} (°C/W)
TSOT	43
LFCSP	28.3

The junction temperature of the ADM7160 can be calculated using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
θ_{JA} is the junction-to-ambient thermal resistance of the package.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation can be simplified as follows:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not exceed 125°C.

Figure 43 through Figure 54 show junction temperature calculations for various ambient temperatures, load currents, input-to-output voltage differentials, and areas of PCB copper.

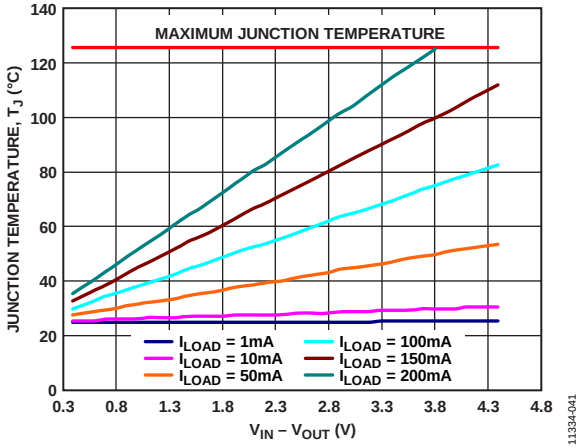

Figure 43. TSOT, 500 mm² of PCB Copper, T_A = 25°C

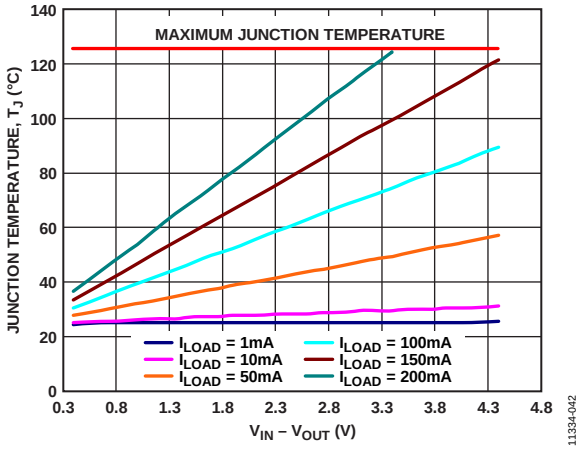

Figure 44. TSOT, 100 mm² of PCB Copper, T_A = 25°C

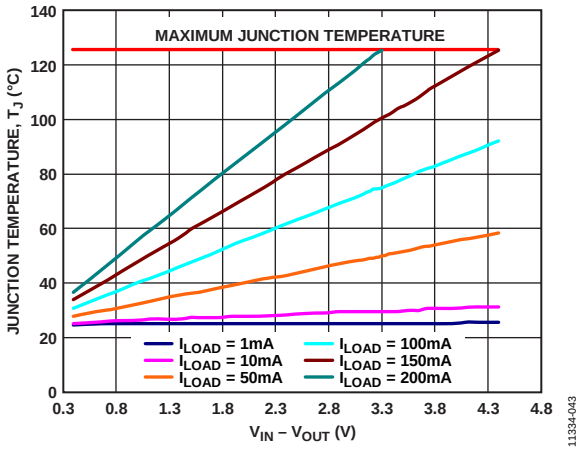

Figure 45. TSOT, 50 mm² of PCB Copper, T_A = 25°C

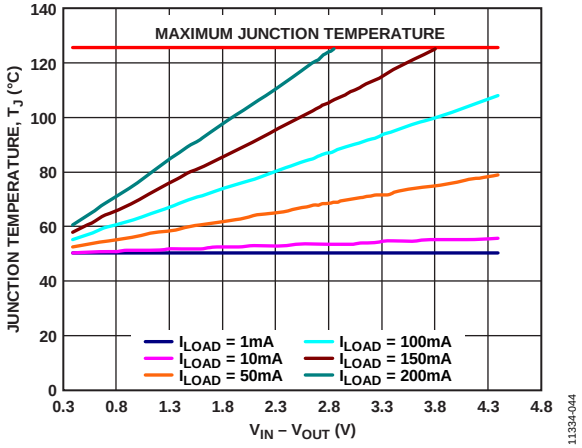

Figure 46. TSOT, 500 mm² of PCB Copper, T_A = 50°C

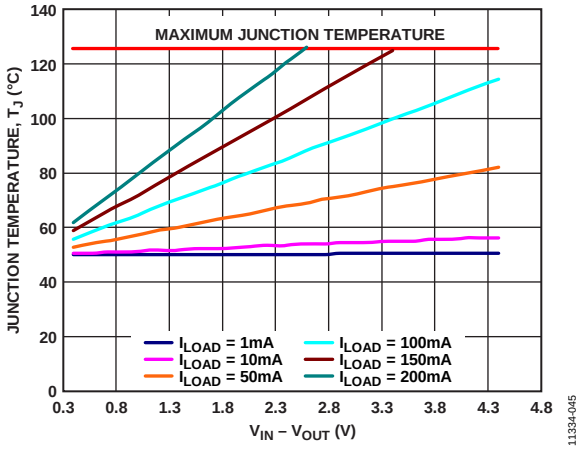

Figure 47. TSOT, 100 mm² of PCB Copper, T_A = 50°C

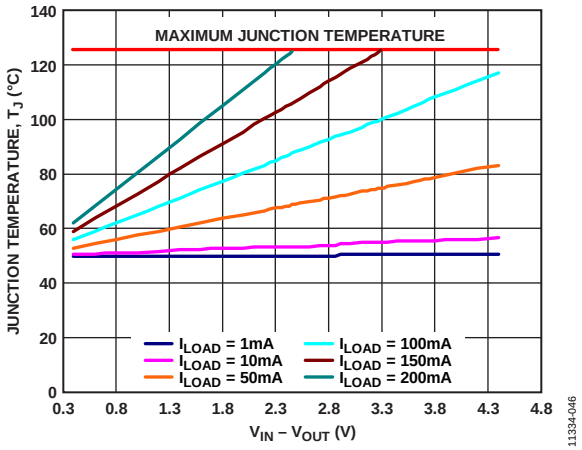

Figure 48. TSOT, 50 mm² of PCB Copper, T_A = 50°C

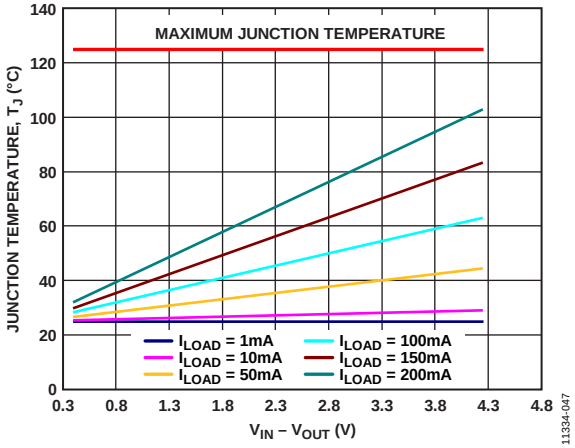

Figure 49. LFCSP, 500 mm² of PCB Copper, T_A = 25°C

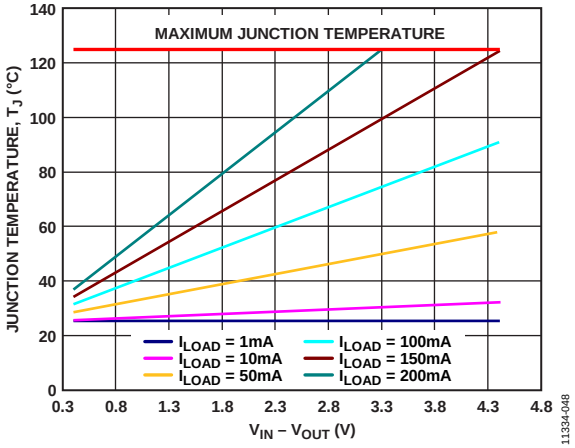

Figure 50. LFCSP, 100 mm² of PCB Copper, T_A = 25°C

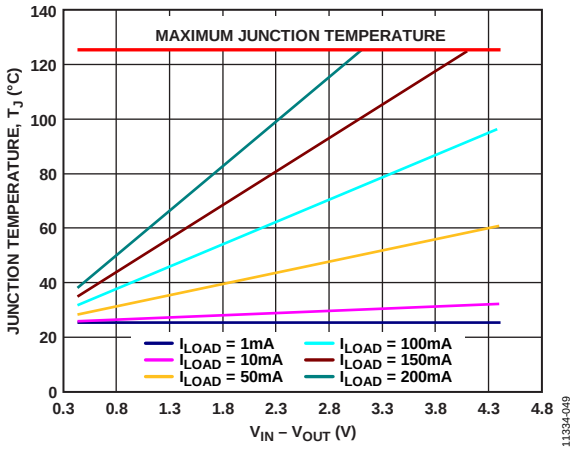

Figure 51. LFCSP, 50 mm² of PCB Copper, T_A = 25°C

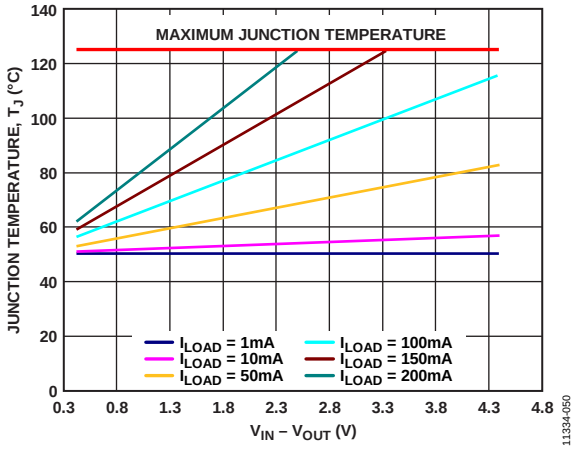

Figure 52. LFCSP, 500 mm² of PCB Copper, T_A = 50°C

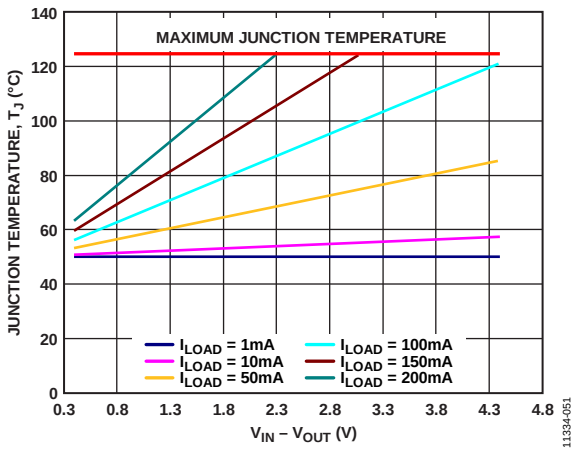

Figure 53. LFCSP, 100 mm² of PCB Copper, T_A = 50°C

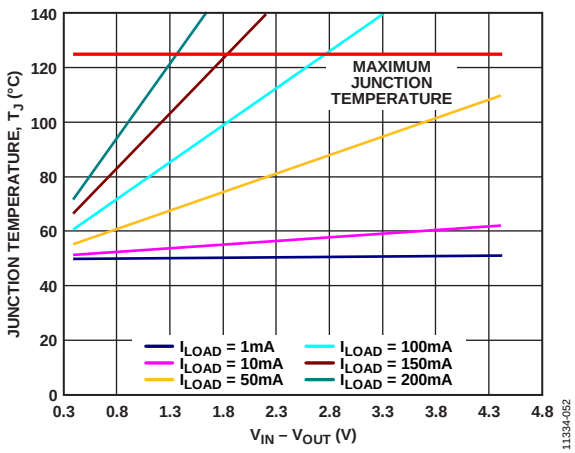

Figure 54. LFCSP, 50 mm² of PCB Copper, T_A = 50°C

In cases where the board temperature is known, use the Ψ_{JB} thermal characterization parameter to estimate the junction temperature rise (see Figure 55 and Figure 56). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 43°C/W for the 5-lead TSOT package and 28.3°C/W for the 6-lead LFCSP package.

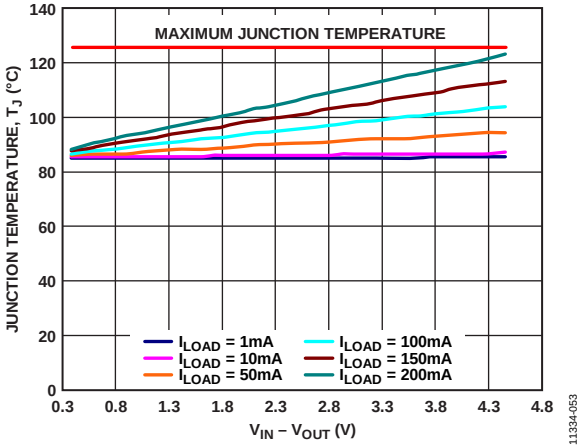

Figure 55. TSOT, T_A = 85°C

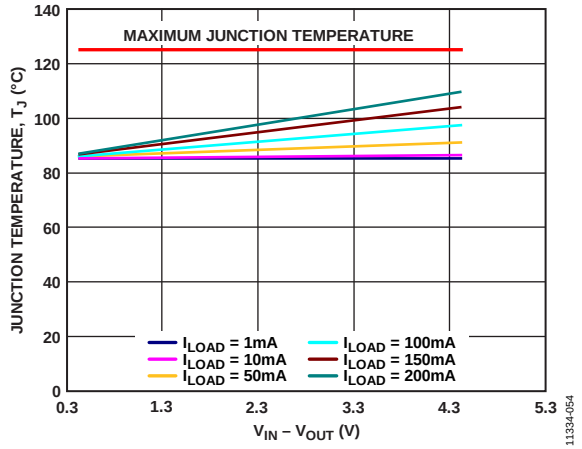

Figure 56. LFCSP, T_A = 85°C

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADM7160. However, as shown in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors achieves the smallest possible footprint solution on boards where area is limited.

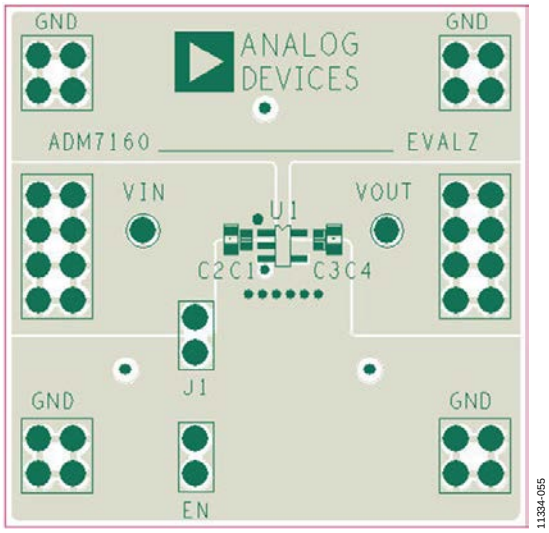

Figure 57. Example of PCB Layout, TSOT Package

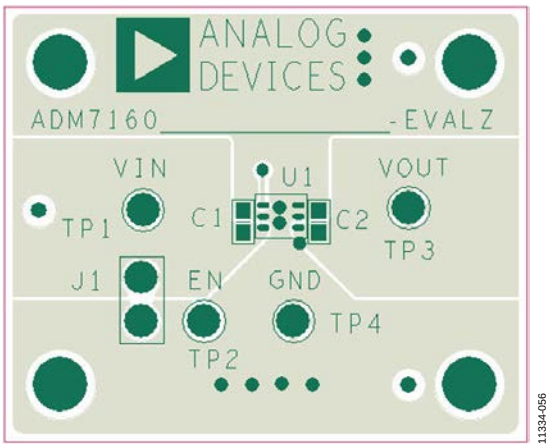

Figure 58. Example of PCB Layout, LFCSP Package

TYPICAL APPLICATION CIRCUITS

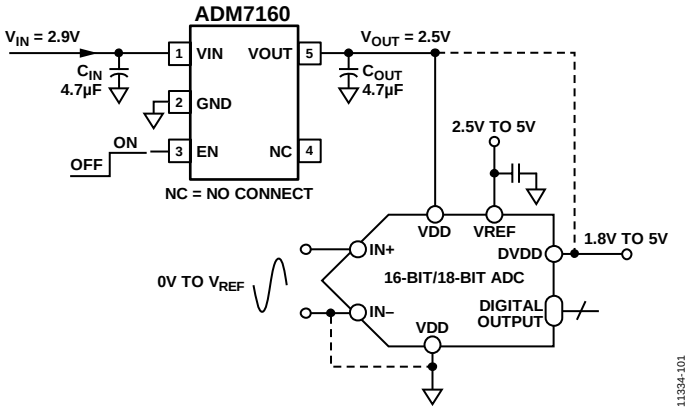

Figure 59. ADM7160 Powering a 16-Bit/18-Bit ADC

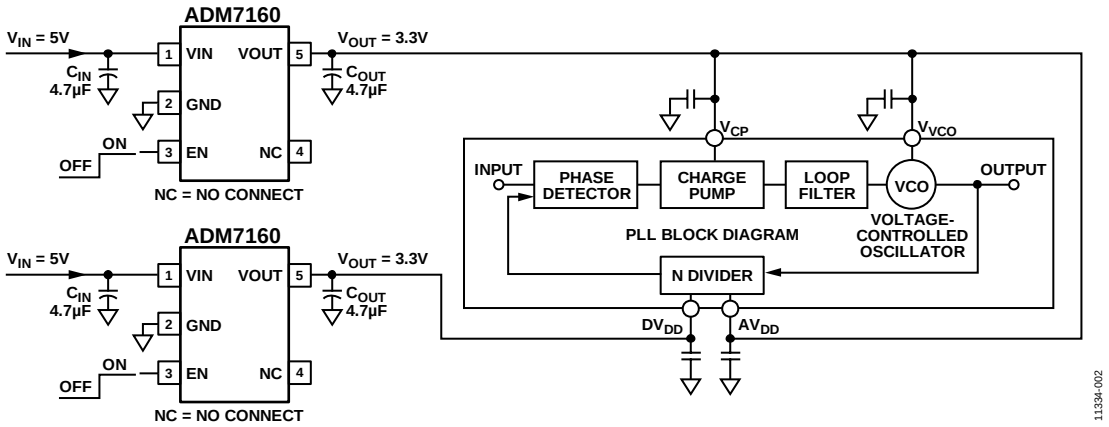

Figure 60. ADM7160 Powering a PLL/VCO

OUTLINE DIMENSIONS

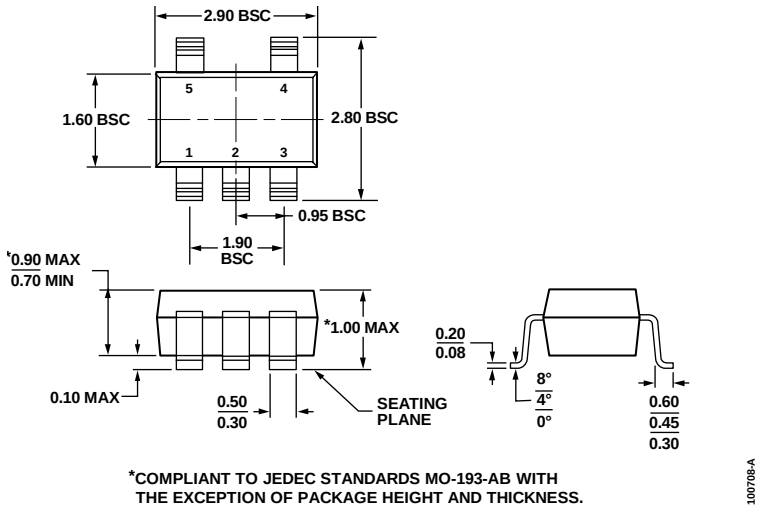

Figure 61. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

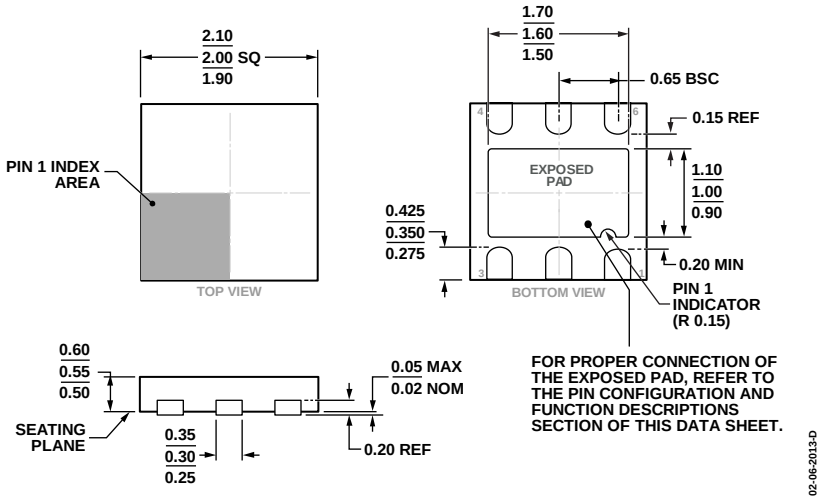

Figure 62. 6-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-6-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADM7160AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LNH
ADM7160AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LNJ
ADM7160AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LNK
ADM7160AUJZ-1.8-R2	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LNH
ADM7160AUJZ-2.5-R2	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LNJ
ADM7160AUJZ-3.3-R2	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LNK
ADM7160ACPZN1.8-R7	−40°C to +125°C	1.8	6-Lead LFCSP_UD	CP-6-3	LNH
ADM7160ACPZN2.5-R7	−40°C to +125°C	2.5	6-Lead LFCSP_UD	CP-6-3	LNJ
ADM7160ACPZN3.3-R7	−40°C to +125°C	3.3	6-Lead LFCSP_UD	CP-6-3	LNK
ADM7160ACPZN1.8-R2	−40°C to +125°C	1.8	6-Lead LFCSP_UD	CP-6-3	LNH
ADM7160ACPZN2.5-R2	−40°C to +125°C	2.5	6-Lead LFCSP_UD	CP-6-3	LNJ
ADM7160ACPZN3.3-R2	−40°C to +125°C	3.3	6-Lead LFCSP_UD	CP-6-3	LNK
ADM7160CP-EVALZ			Evaluation Board for LFCSP_UD		
ADM7160UJ-EVALZ			Evaluation Board for TSOT		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact your local Analog Devices, Inc., sales or distribution representative.

NOTES

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D11334-0-4/14(A)

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