



**THE DATASHEET OF
TPS60501DGS**



TPS6050x High-Efficiency, 250-mA Step-Down Charge Pump

1 Features

- Wide Input Voltage Range From 1.8 V to 6.5 V
- Regulated 3.3-V, 1.8-V, 1.5-V, or Adjustable Output Voltage
- Up to 250-mA Output Current
- Up to 90% Efficiency
- Output Voltage Tolerance 3% Over Line, Load, and Temperature Variation
- Device Quiescent Current Less Than 40 μ A
- Output Voltage Supervisor Included (Power Good)
- Internal Soft Start
- Load Isolated From Battery During Shutdown
- Overtemperature and Overcurrent Protected
- Micro-Small 10-Pin VSSOP Package
- EVM Available, TPS60500EVM-193

2 Applications

- Mobile Phones
- Portable Instruments
- Internet Audio Player
- PC Peripherals
- USB Powered Applications

3 Description

The TPS6050x devices are a family of switched capacitor voltage converters, designed specifically for space-critical battery-powered applications.

The TPS6050x step-down charge pumps generate a regulated, fixed 3.3-V, 1.8-V, 1.5-V, or adjustable output voltage. Only four small ceramic capacitors are required to build a complete high-efficiency DC–DC charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between three different conversion modes. The output can deliver a maximum of 250-mA output current. The power good function supervises the output voltage and goes high when the output voltage rises to 97% of the nominal value.

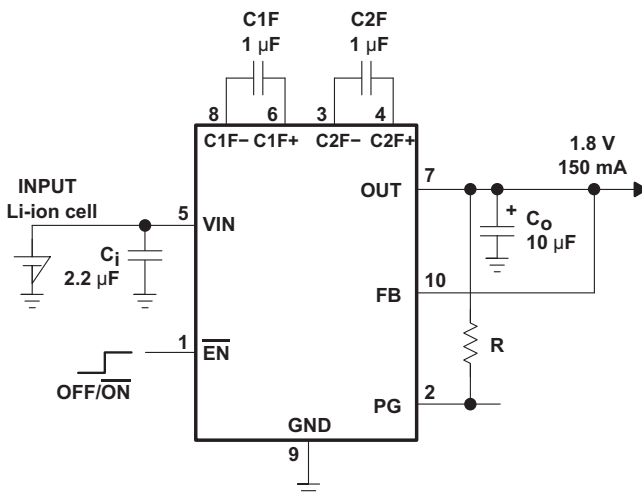
The TPS6050x devices come in a micro-small 10-pin VSSOP package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS60500	VSSOP (10)	3.05 mm x 4.98 mm
TPS60501		
TPS60502		
TPS60503		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Input Voltage

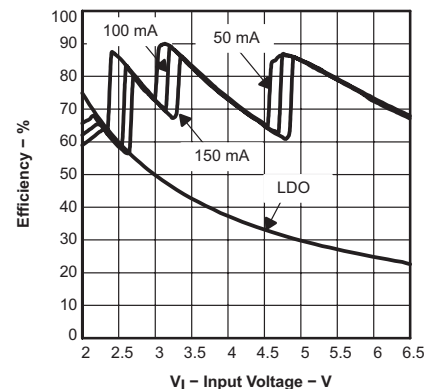


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2002) to Revision C

Page

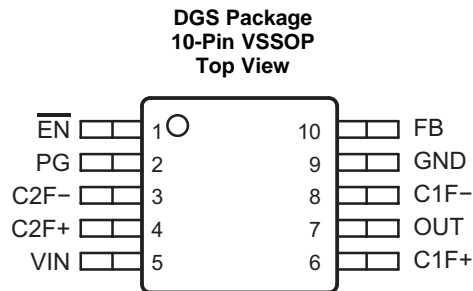
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**

5 Device Comparison Table

PART NUMBER ⁽¹⁾	OUTPUT VOLTAGE [V]	MINIMUM INPUT VOLTAGE FOR $I_{OUT} = 150\text{ mA}$
TPS60500DGS	Adjustable (0.8 V to 3.3 V)	$V_{IN} > V_{OUT} + 1$
TPS60501DGS	3.3	$V_{IN} > 4.3\text{ V}$
TPS60502DGS	1.8	$V_{IN} > 2.8\text{ V}$
TPS60503DGS	1.5	$V_{IN} > 2.5\text{ V}$

(1) The DGS package is available taped and reeled. Add R suffix to device type (for example, TPS60500DGSR) to order quantities of 2500 devices per reel.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1F+	6	–	Positive terminal of the flying capacitor C1F
C1F–	8	–	Negative terminal of the flying capacitor C1F
C2F+	4	–	Positive terminal of the flying capacitor C2F
C2F–	3	–	Negative terminal of the flying capacitor C2F
$\overline{\text{EN}}$	1	I	Device-enable Input. – $\overline{\text{EN}}$ = High disables the device. Output and input are isolated in shutdown mode. – $\overline{\text{EN}}$ = Low enables the device.
GND	9	–	Ground
FB	10	O	TPS60500: connect via voltage divider to V_O TPS60501 to TPS60503: connect directly to V_O
OUT	7	O	Regulated 3.3 V, 1.8 V, 1.5 V, or adjustable power output Bypass OUT to GND with the output filter capacitor C_O .
PG	2	O	Open drain power good detector output. As soon as the voltage on OUT reaches about 97% of its nominal value this pin goes high.
VIN	5	I	Supply Input. Connect to an input supply in the 1.8-V to 6.5-V range.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Voltage at VIN, EN, PG to GND ⁽²⁾	-0.3	7	V
Voltage at OUT, FB to GND	-0.3	3.6	V
Voltage at C1F+, C1F-, C2F+, C2F- to GND	-0.3	7	V
Output current at OUT		300	mA
T _J Maximum junction temperature		150	°C
T _{stg} Storage temperature	-55	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The voltage at EN, and PG can exceed VIN up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

7.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V _{IM} Input voltage at VIN	1.8		6.5	V
I _{OUT} Output current at OUT			250	mA
C _{IN} Input capacitor	2.2			μF
C1F, C2F Flying capacitors		1		μF
Output capacitor	C _{OUT} for I _{OUT} ≤ 150 mA	4.7		μF
	C _{OUT} for 150 mA < I _{OUT} < 250 mA	22		
T _J Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TPS6050x	UNIT
	DGS (VSSOP)	
	10 PINS	
R _{θJA} Junction-to-ambient thermal resistance	157	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	53	°C/W
R _{θJB} Junction-to-board thermal resistance	76	°C/W
Ψ _{JT} Junction-to-top characterization parameter	5.5	°C/W
Ψ _{JB} Junction-to-board characterization parameter	75	°C/W
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	—	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

at $C_{IN} = 4.7 \mu\text{F}$, $C1F = C2F = 1 \mu\text{F}$, $C_{OUT} = 10 \mu\text{F}$, $T_A = -40^\circ\text{C}$ to 85°C , $V_{IN} = 5 \text{ V}$, $V_{(EN)} = \text{GND}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{IN}	Supply voltage		1.8		6.5	V	
I_{OUT}	Maximum output current	$V_{IN} = 1.8 \text{ V}$ to 2.7 V , $V_{IN} - V_{OUT} > 1 \text{ V}$	50			mA	
		$V_{IN} \geq 2.7 \text{ V}$, $V_{IN} - V_{OUT} > 1 \text{ V}$	150				
		$V_{OUT} = 1.5 \text{ V}$, $V_{IN} \geq 3.1 \text{ V}$	250				
		$V_{IN} \geq 3.7 \text{ V}$, $1.8 \text{ V} \leq V_{OUT} \leq 2.5 \text{ V}$	250				
		$V_{OUT} > 2.5 \text{ V}$, $V_{IN} > V_{OUT} + 1.2 \text{ V}$	250				
V_{OUT}	Output voltage	TPS60500	$V_{IN} > 2.7 \text{ V}$; $V_{IN} - V_{OUT} > 1 \text{ V}$ at $I_{OUT} \leq 150 \text{ mA}$,	0.8		3.3	V
		TPS60501		3.3			
		TPS60502		1.8			
		TPS60503		1.5			
$V_{(FB)}$	Feedback voltage	TPS60500		0.8		V	
	Tolerance of output voltage	TPS60501	$I_{OUT} = 0 \text{ mA}$ to 150 mA , $C_{OUT} = 47 \mu\text{F}$	-4%		3%	
		TPS60500		3%			
		TPS60502		4%			
		TPS60503		4%			
V_{pp}	Output voltage ripple at OUT	$I_{OUT} = 150 \text{ mA}$, $V_{OUT} = 1.5 \text{ V}$		30		mV _{PP}	
I_Q	Quiescent current (no-load input current)	$I_{OUT} = 0 \text{ mA}$		40	75	μA	
$T_{(SD)}$	Thermal shutdown temperature			150		$^\circ\text{C}$	
$I_{OUT(SD)}$	Shutdown supply current	$V_{(EN)} = V_{IN}$		0.05	0.5	μA	
$f_{(OSC)}$	Internal switching frequency		600	800	1200	kHz	
V_{IL}	$\overline{\text{EN}}$ input low voltage				$0.3 \times V_{IN}$	V	
V_{IH}	$\overline{\text{EN}}$ input high voltage		$0.7 \times V_{IN}$			V	
$I_{lkg(SD)}$	$\overline{\text{EN}}$ input leakage current	$V_{(EN)} = 0 \text{ V}$ or V_{IN}		0.01	0.1	μA	
$I_{lkg(FB)}$	FB input leakage current	TPS60500			0.1	μA	
$R_{(max)}$	Maximum resistance of the external voltage divider	TPS60500	R1 + R2 at FB pin		1	M Ω	
	Short circuit current (start-up current)	$V_{IN} = 6.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	100	300		mA	
	Output current limit	$V_{OUT} > 0.6 \text{ V}$		500		mA	
	No load start-up time			80		μs	
FOR POWER GOOD COMPARATOR:							
$V_{(PG)}$	Power good trip voltage	See (1)		$V_{ml} - 2\%$		V	
$t_{d,r}$	Power good delay time	V_{OUT} ramping positive	100		200	μs	
		V_{OUT} ramping negative	50		100	μs	
V_{OL}	Power good output voltage low	$V_{OUT} = 0 \text{ V}$, $I_{(PG)} = 1 \text{ mA}$			0.3	V	
I_{lkg}	Power good leakage current	$V_{OUT} = 3.3 \text{ V}$, $V_{(PG)} = 3.3 \text{ V}$		0.01	0.1	μA	

(1) V_{ml} is the output voltage at the maximum load current. V_{ml} is not a JEDEC symbol.

7.6 Typical Characteristics

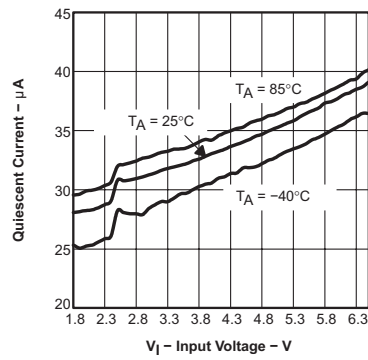


Figure 1. Quiescent Current vs Input Voltage

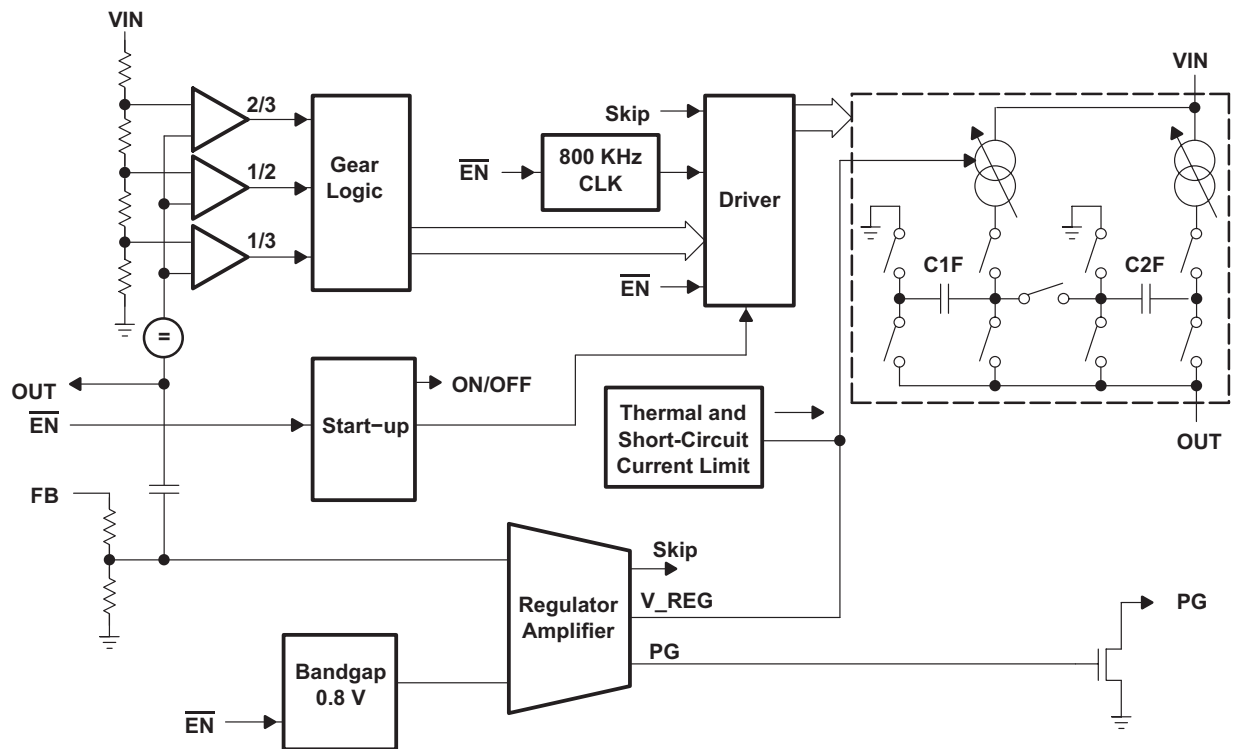
8 Detailed Description

8.1 Overview

The TPS6050x charge pumps provide a regulated output voltage in the range of 0.8 V to 3.3 V from an input voltage of 1.8 V to 6.5 V. The devices use switched capacitor fractional conversion to achieve high efficiency over the entire input and output voltage range. Regulation is achieved by sensing the output voltage and enabling the internal switches as needed to maintain the selected output voltage. This skip-mode regulation is used over a load range from 0 mA to 150 mA. At a higher output current, the device works in a linear regulation mode.

The TPS6050x circuits consist of an oscillator, a voltage reference, an internal resistive feedback circuit (fixed-voltage version only), an error amplifier, two charge pump stages with MOSFET switches, a shutdown or start-up circuit, and a control circuit.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Short-Circuit Current Limit and Thermal Protection

When the output voltage is lower than 0.6 V, the output current is limited to 300 mA typically.

The device also has a thermal protection which reduces the output current when the temperature of the chip exceeds 150°C. The output current declines to 0 mA when the chip temperature rises to 160°C.

8.3.2 Enable

Driving \overline{EN} high disables the converter. This disables all internal circuits, reducing input current to only 0.05 μ A. Leakage current drawn from the output pin OUT is a maximum of 1 μ A. The device exits shutdown once \overline{EN} is set low (see [Start-up Procedure](#)). The typical no-load start-up time is 80 μ s. When the device is disabled, the load is isolated from the input, an important feature in battery-operated products because it extends the battery shelf life.

Feature Description (continued)

8.3.3 Power Good Detector

The power good (PG) output is an open-drain output on all TPS6050x devices. The PG output pulls low when the output is out of regulation. When the output rises above 97% nominal V_{out} , the power good output is pulled high by resistor. In shutdown, power good is pulled low. In normal operation, an external pullup resistor is typically used to connect the PG pin to V_{OUT} or V_{IN} . If the PG output is not used, it should remain unconnected.

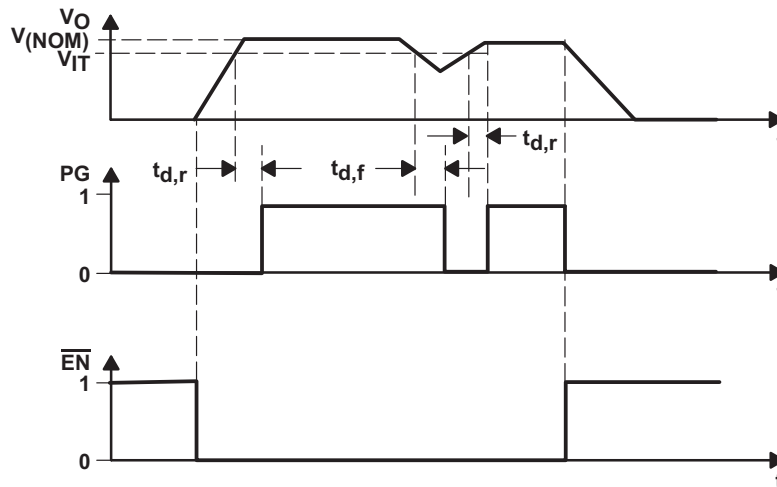


Figure 2. Power Good Timing Diagram

8.4 Device Functional Modes

8.4.1 Start-up Procedure

The device is enabled when \overline{EN} is set from logic high to logic low. The charge pump stages immediately start switching to transfer energy to the output. In start-up until the output voltage has reached 0.6 V, the input current is limited to 300 mA typically.

8.4.2 Conversion Modes

The TPS6050x devices use fractional conversion to achieve high efficiency over a wide input and output voltage range. Depending on the input to output voltage ratio and output current, internal circuitry switches between an LDO mode, a 2/3x mode, a 0.5x mode, and a 1/3x mode.

8.4.2.1 LDO Conversion Mode

In the LDO mode, the flying capacitors are no longer used for transferring energy. The switches 1, 2, 5, and 6 are closed and connect the input directly with the output. This mode is automatically selected if the input to output voltage ratio does not allow the use of another conversion mode with higher efficiency. In LDO mode, the regulation is done by switching off MOSFET 2 and 6 until the output current reaches the *linear-skip* current (150 mA typical). At a higher output current, the output voltage is regulated by controlling the resistance of the switch. The minimum input to output voltage difference required for regulation is 1 V.

Device Functional Modes (continued)

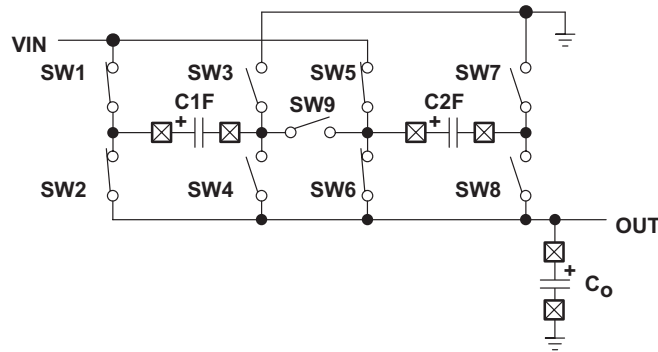


Figure 3. LDO Conversion Mode

8.4.2.2 2/3x Conversion Mode

In the first cycle, the two flying capacitors are connected in parallel and are charged up in series with the output capacitor. In the second cycle, the flying capacitors are connected in series. This mode provides higher efficiency than the LDO mode because the current into VIN is only 2/3 of the output current. The mode is automatically selected if the input voltage is higher than 3/2 of the selected output voltage.

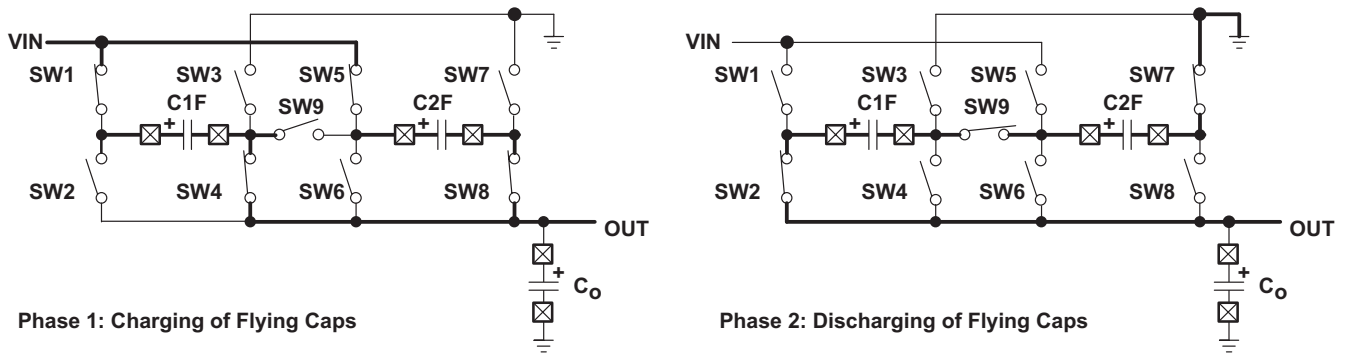


Figure 4. 2/3x Conversion Mode

Device Functional Modes (continued)

8.4.2.3 0.5x Conversion Mode

This conversion mode is internally selected if the input to output voltage ratio is greater than two (for example, 3.6-V to 1.5-V conversion). In the 0.5x mode, the flying capacitors and the switches always work in parallel, which reduces the resistance of the circuit compared to the other modes. In the first cycle, the flying capacitors are charged in series with the output capacitors. In the second cycle, the flying capacitors are connected in parallel with the output capacitor, which discharges the flying capacitors.

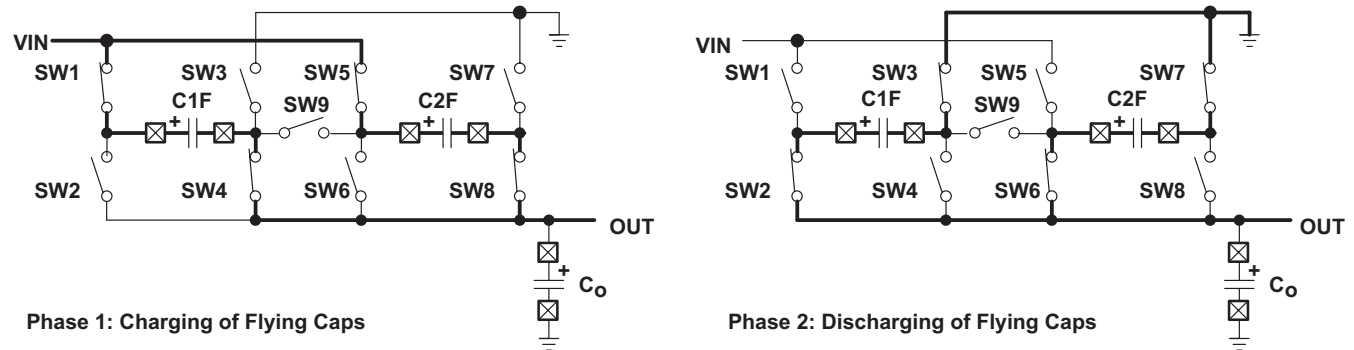


Figure 5. 0.5x Conversion Mode

8.4.2.4 1/3x Conversion Mode

This mode was implemented to provide high efficiency even with an input to output voltage ratio greater than three (for example, 5-V to 1.5-V conversion). In the first cycle, the two flying capacitors are charged in series with the output capacitor. In the next step, the flying capacitors which are charged to $V_{IN}/3$, are connected in parallel to the output capacitor.

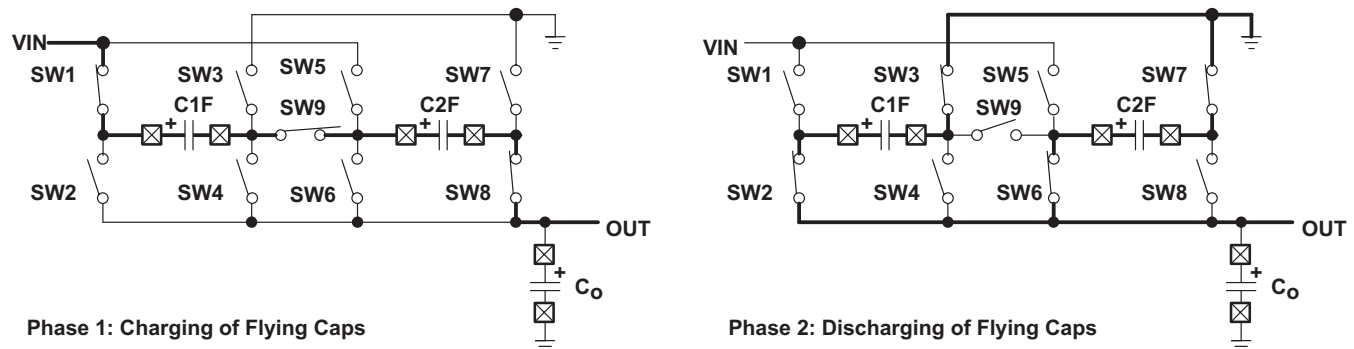


Figure 6. 1/3x Conversion Mode

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6050x devices are switched capacitor voltage converters providing fractional conversion to achieve high efficiency over a wide input and output voltage range. They support regulated output voltages of 3.3 V, 1.8 V and 1.5 V or adjustable output voltages from a 1.8-V to 6.5-V input voltage range.

9.2 Typical Applications

9.2.1 Typical Application Circuit for Fixed-Voltage and Adjustable-Voltage Versions

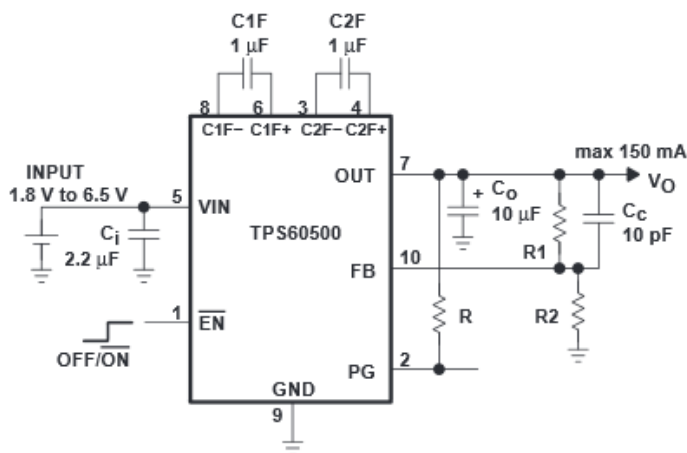


Figure 7. Typical Operating Circuit – TPS60500, Adjustable Output Voltage

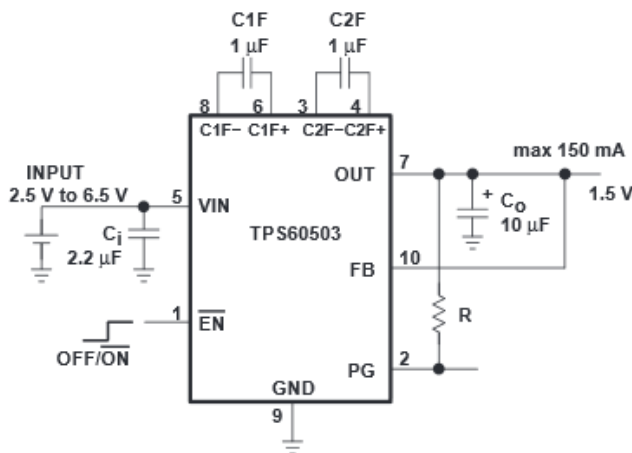


Figure 8. Typical Operating Circuit – TPS60503, Maximum 150-mA Output Current

Table 2. Recommended Capacitors

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG	805	1 μ F	Ceramic
	LMK212BJ225MG	805	2.2 μ F	Ceramic
	EMK316BJ225KL	1206	2.2 μ F	Ceramic
	LMK316BJ475KL	1206	4.7 μ F	Ceramic
	JMK316BJ106KL	1206	10 μ F	Ceramic
TDK	C2012X5R1C105M	805	1 μ F	Ceramic
	C2012X5R1A225M	805	2.2 μ F	Ceramic
	C2012X5R0J106M	805	10 μ F/6.3 V	Ceramic

Table 3 contains a list of manufacturers of ceramic capacitors. Ceramic capacitors provide the lowest output voltage ripple because they typically have the lowest ESR-rating.

Table 3. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t-yuden.com
TDK	X7R/X5R ceramic	www.component.tdk.com
Vishay	X7R/X5R ceramic	www.vishay.com
Kemet	X7R/X5R ceramic	www.kemet.com

9.2.1.2.2 Resistor Combinations

Table 4. Resistor Combinations

NOMINAL OUTPUT VOLTAGE	EQUATION	POSSIBLE E24 RESISTOR COMBINATIONS
1.2 V	$R1 = 0.5R2$	$R1 = 100 \text{ k}\Omega$, $R2 = 200 \text{ k}\Omega$, (1.20 V)
1.5 V	$R1 = 0.875R2$	$R1 = 160 \text{ k}\Omega$, $R2 = 180 \text{ k}\Omega$, (1.51 V)
1.6 V	$R1 = R2$	any
1.8 V	$R1 = 1.25R2$	$R1 = 150 \text{ k}\Omega$, $R2 = 120 \text{ k}\Omega$, (1.80 V)
2.5 V	$R1 = 2.125R2$	$R1 = 510 \text{ k}\Omega$, $R2 = 240 \text{ k}\Omega$, (2.50 V)
		$R1 = 470 \text{ k}\Omega$, $R2 = 220 \text{ k}\Omega$, (2.51 V)

Equations:

$$V_{\text{OUT}} = \frac{(R1+R2)}{R2} \times V_{\text{FB}}$$

$$V_{\text{FB}} = 0.8 \text{ V} \tag{1}$$

$$R1 - R2 \left(\frac{V_{\text{OUT}}}{V_{\text{FB}}} \right) = R2 \tag{2}$$

9.2.1.3 Application Curves

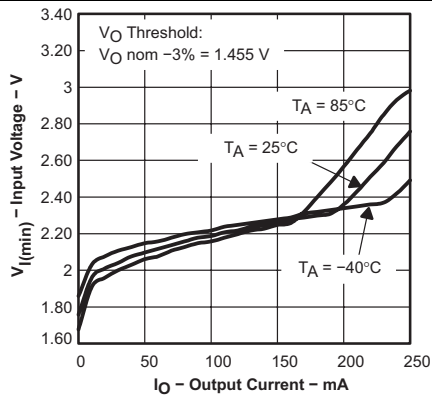


Figure 10. TPS60503
Minimum Input Voltage vs Output Current

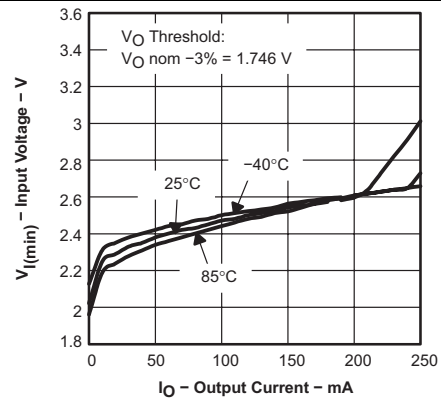


Figure 11. TPS60502
Minimum Input Voltage vs Output Current

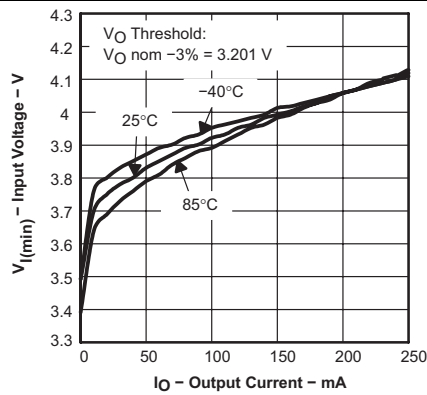


Figure 12. TPS60501
Minimum Input Voltage vs Output Current

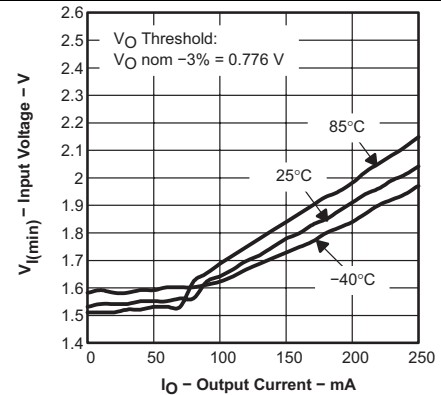


Figure 13. TPS60500
Minimum Input Voltage vs Output Current

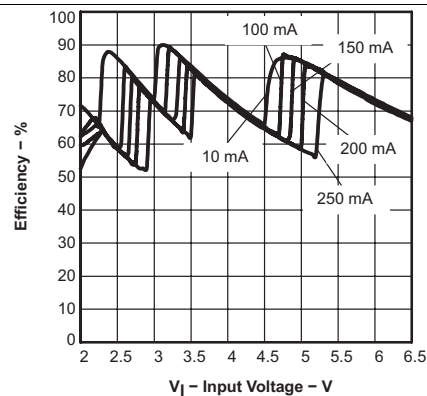


Figure 14. TPS60503
Efficiency vs Input Voltage

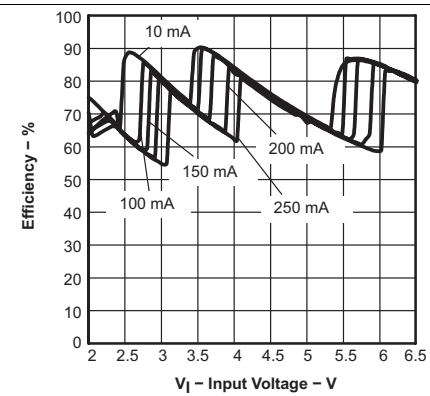


Figure 15. TPS60502
Efficiency vs Input Voltage

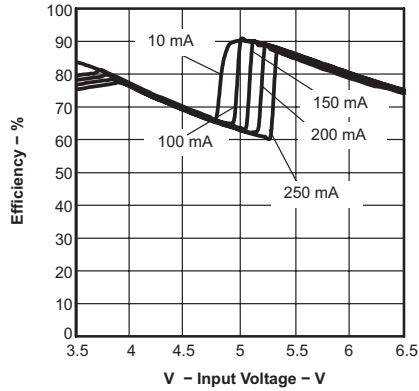


Figure 16. TPS60501
Efficiency vs Input Voltage

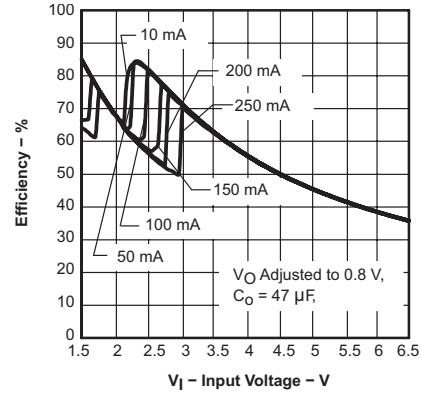


Figure 17. TPS60500
Efficiency vs Input Voltage

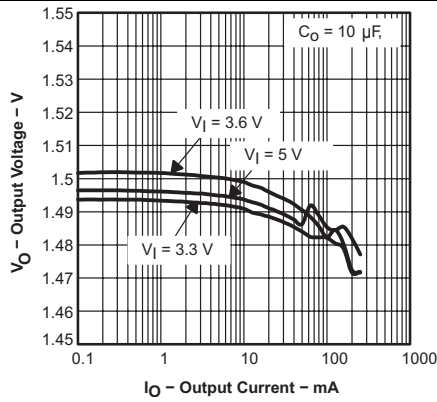


Figure 18. TPS60503
Output Voltage vs Output Current

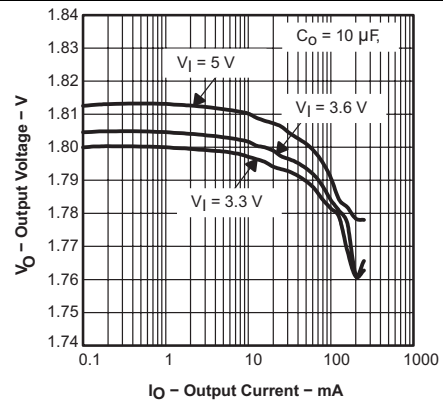


Figure 19. TPS60502
Output Voltage vs Output Current

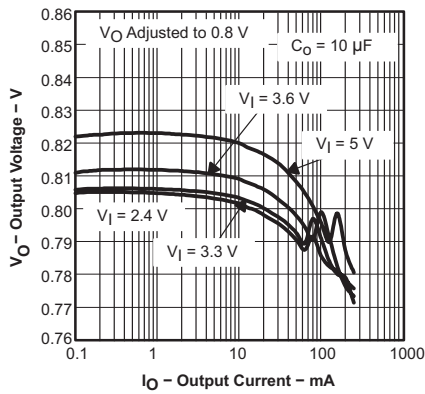


Figure 20. TPS60500
Output Voltage vs Output Current

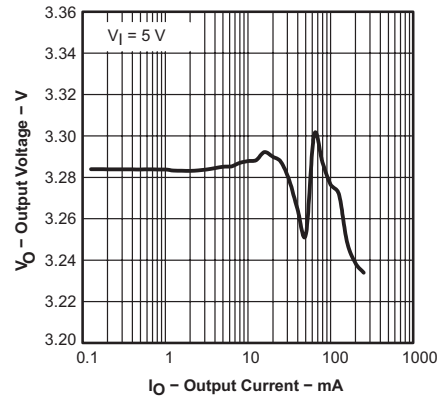


Figure 21. TPS60501
Output Voltage vs Output Current

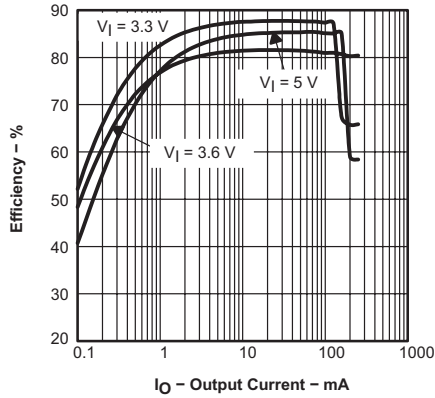


Figure 22. TPS60503
Efficiency vs Output Current

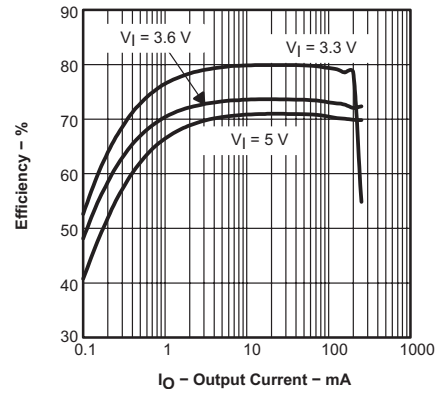


Figure 23. TPS60502
Efficiency vs Output Current

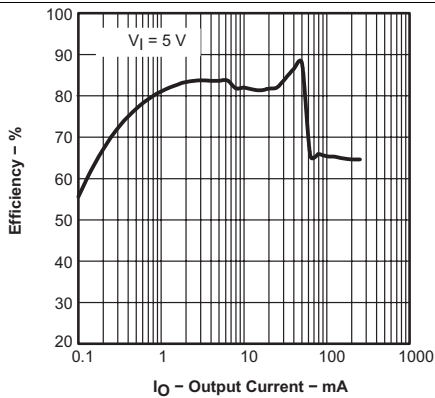


Figure 24. TPS60501
Efficiency vs Output Current

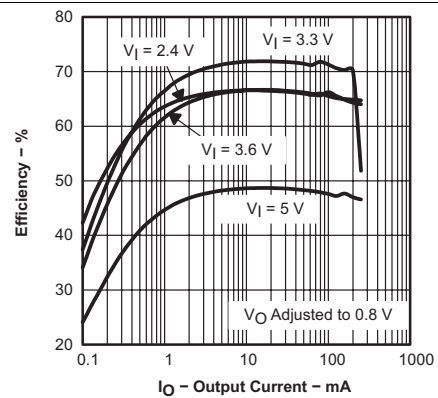


Figure 25. TPS60500
Efficiency vs Output Current

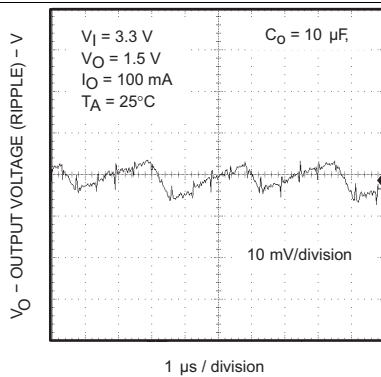


Figure 26. Output Voltage (Ripple) vs Time

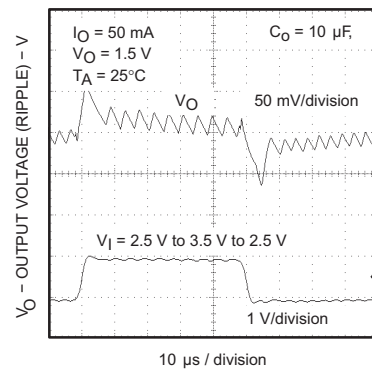


Figure 27. Line Transient Response

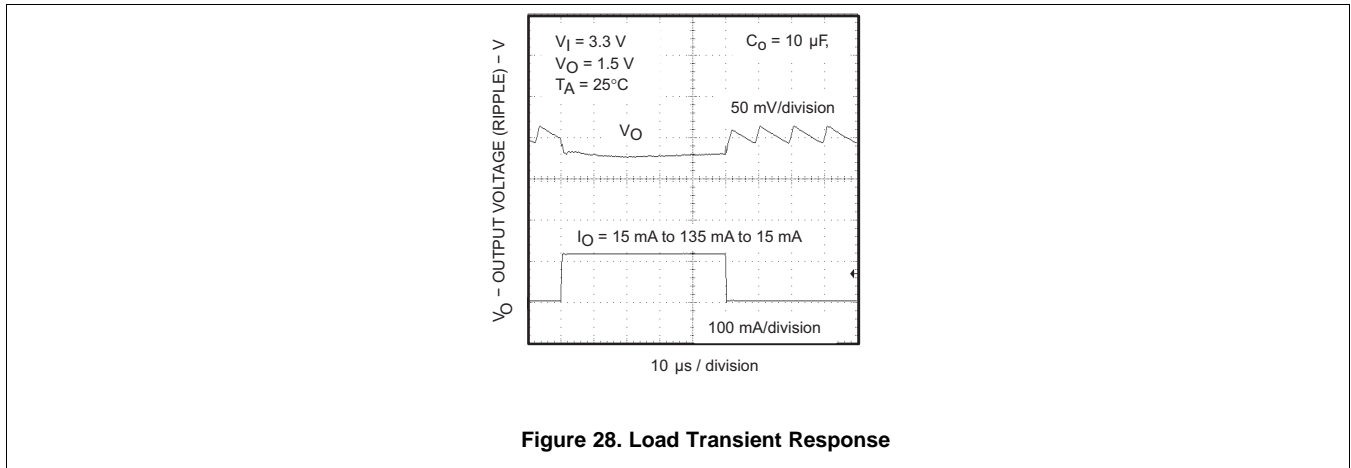


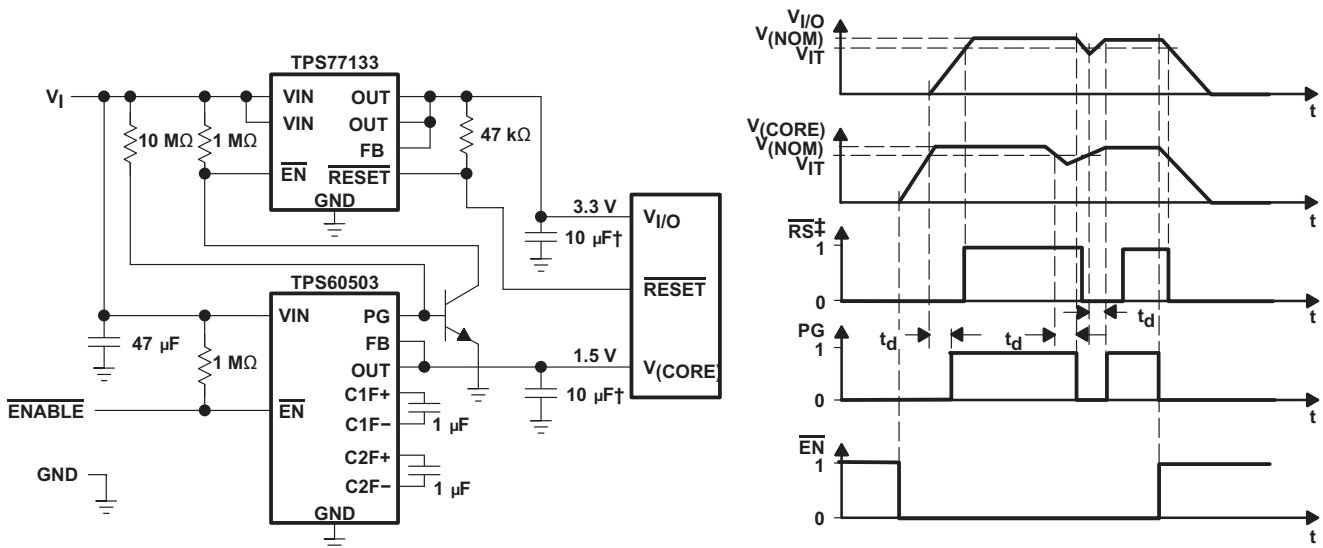
Figure 28. Load Transient Response

9.3 System Examples

9.3.1 DSP Supply With Sequencing

This application shows a power supply for a typical digital signal processor (DSP). DSPs usually have core voltages in the 1-V to 2.5-V range, whereas the voltage at the I/O-pins (I/O voltage) is typically 3.3 V to interface with external logic and converters. Therefore, a power supply with two output voltages is required. The application works with an input voltage in the range of 3.5 V to 6.5 V. The maximum output current is 150 mA on each output.

The supply is enabled by pulling the enable pin (\overline{EN} of the TPS60503) to GND. The step-down charge pump starts and its power good (PG) output goes high. This enables the LDO which powers the I/O lines and generates a reset signal for the DSP. Figure 29 shows the timing diagram of the start-up or shutdown procedure.



† Recommended value for stability, DSP may require higher capacitance.

‡ RS is the RESET output of the TPS77133.

Figure 29. DSP Supply With Sequencing

System Examples (continued)

9.3.2 LC-Post Filter

If the output voltage ripple of the step-down charge pump is too high, an LC post filter can be used.

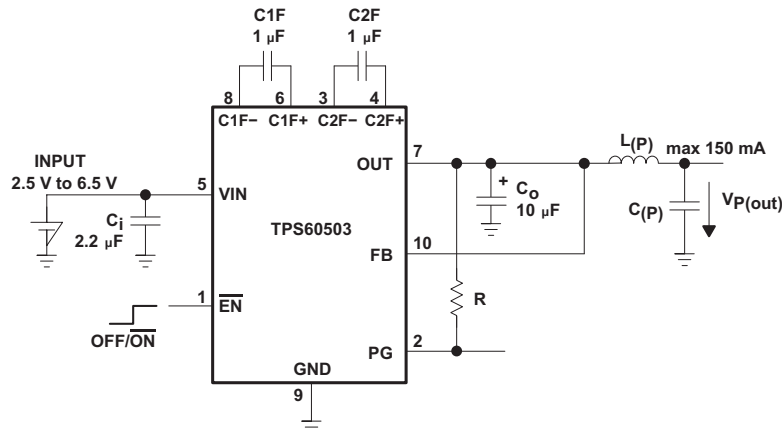


Figure 30. LC-Post Filter

Table 5. Measurement Results on Different $C_{(fly)}$, $C_{(P)}$, $L_{(P)}$ Combinations; BW = 500 MHz

V_I [V]	I_o [mA]	C_I [μ F]	$C_{(XF)}$ [μ F]	C_O [μ F]	$L_{(P)}$ [μ H]	$C_{(P)}$ [μ F]	V_o [V]	TYPICAL $V_{P(Out)}$ V_{PP} [mV]	TYPICAL $V_{O(RMS)}$ [mV]
		CERAMIC	CERAMIC	CERAMIC		CERAMIC			
5	50	2.2	0.22	4.7	—	0.1 (X7R)	3.3	50	8
5	50	2.2	0.22	4.7	—	0.1 (X7R)	1.5	30	9
5	150	4.7	1	10	—	0.1 (X7R)	1.5	50	6
5	250	4.7	1	2 x 10	—	0.1 (X7R)	1.5	45	8
5	100	4.7	1	10	0.1	0.1 (X7R)	1.5	20	4

9.3.3 Power Supply With Dynamic Voltage Scaling

Dynamic voltage scaling of the core can be used to reduce power consumption of a digital signal processor (DSP). During the periods, in which the maximum DSP performance is not required, the core voltage can be reduced when the DSP operates at a lower clock-rate. This function is called runtime power control (RPC) and is supported by modern DSPs. RPC extends battery lifetime in handheld applications, like MP3 players and digital cameras.

The supply of DSPs is separated into I/O interface and core supply. Interface is mostly powered by a 3.3-V system supply, whereas core supply achieves voltages far below 1.5 V. The TPS60500 is powered by the 3.3-V system supply. The DSP itself selects the applied core voltage.

The core voltage is switched between 1.5 V and 1.1 V by changing the feedback resistor network. A MOSFET modifies the voltage divider at the feedback (FB) pin by switching a resistor. In this application, a general-purpose MOSFET BSS138 is used with a $V_{GS(th)}$ of 1.6 V. A DSP 3.3-V I/O port drives the gate. The feedback resistor network consists of R2, R3 and R4. $C_{(ff)}$ is the fast-forward capacitor for improved line regulation.

General requirements for the application:

- Output voltage1 (DSP core): 1.5 V \pm 0.08 V
- Output voltage 2 (DSP core): 1.1 V +0.1 V –0.05 V
- Input voltage: 3 V to 3.3 V
- Output current: 150 mA (10R load)

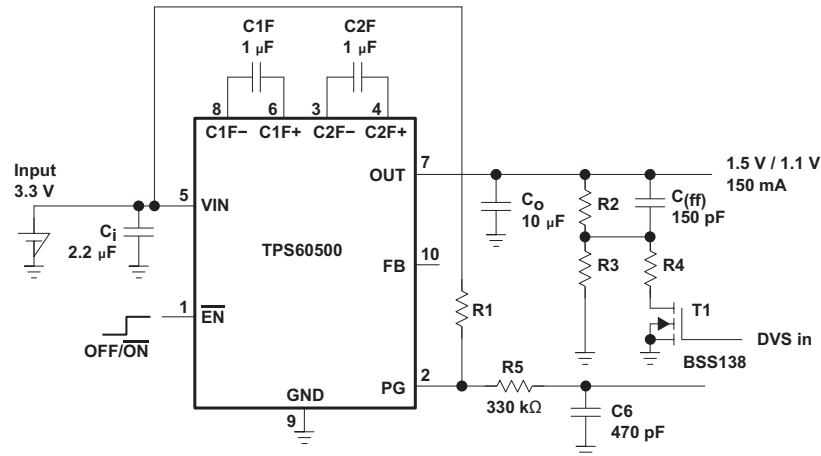


Figure 31. Dynamic Voltage Scaling Application

To keep current through the adjustment resistor network as low as possible, the resistors are calculated to:

V_{out1} adjusted by R2 and R3

$$R3 = \frac{V_{FB}}{\frac{V_{out1} - V_{FB}}{R2}} \quad \begin{array}{l} V_{out1} = 1.1V, \\ R2 = 180k\Omega, \\ V_{ref} = 0.80V, \\ \rightarrow R3 = 470k\Omega \end{array} \quad (3)$$

V_{out2} adjusted by R2 and $R_x = R3 || R4$

$$R_x = \frac{V_{FB} \times R2}{(V2 - V_{FB})} \quad \begin{array}{l} V_{out2} = 1.5V, \\ \rightarrow R_x = 206k\Omega \end{array} \quad (4)$$

$$\frac{1}{R_x} = \frac{1}{R3} + \frac{1}{R4} \quad \rightarrow R4 = \frac{1}{\frac{1}{R_x} - \frac{1}{R3}} \quad \rightarrow R4 = 360k\Omega \quad (5)$$

9.3.4 Internet Audio Power Supply

The input voltage from a single or dual NiCd, NiMH or alkaline cell is boosted to 3.3 V. This voltage is used as system supply for the application and as an input voltage for the step-down charge pump which is used to provide the core voltage for a DSP.

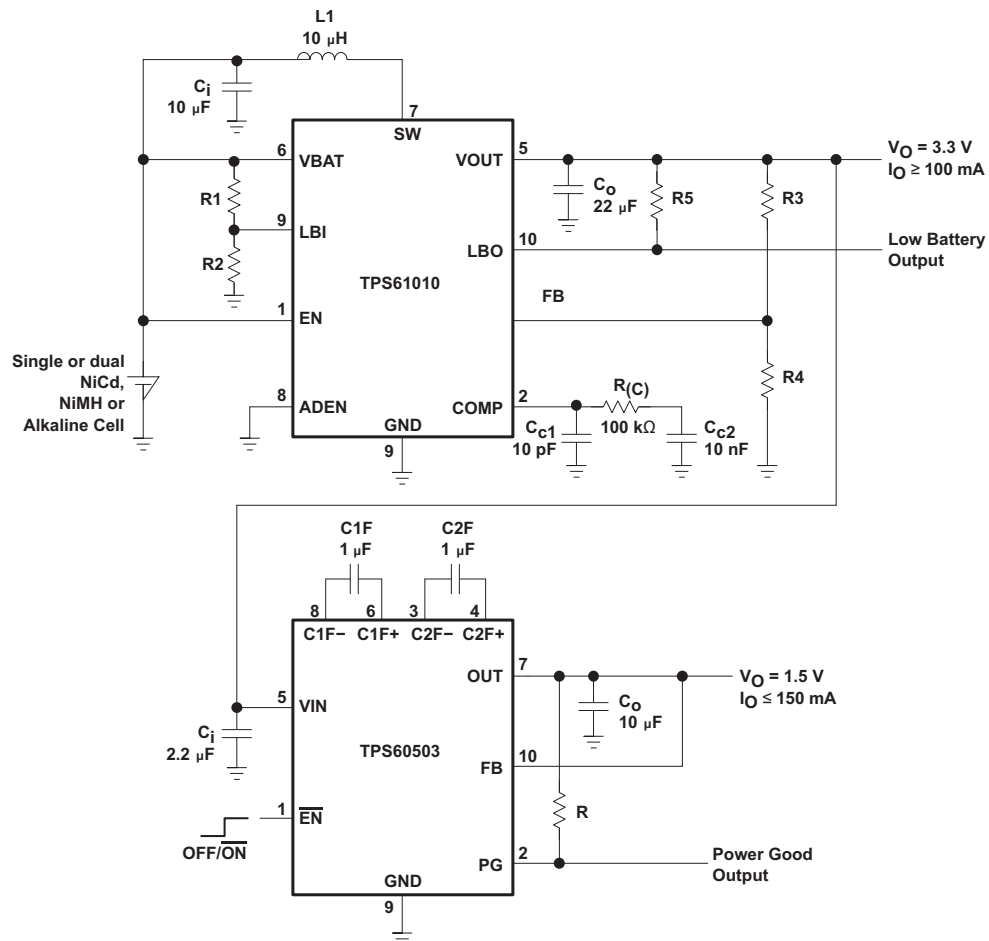


Figure 32. Internet Audio Power Supply

10 Power Supply Recommendations

The TPS6050x devices have no special requirements for its input power supply. The output currents of the input power supply need to be rated according to the supply voltage, output voltage and output current of the TPS6050x.

11 Layout

11.1 Layout Guidelines

All capacitors must be soldered as close as possible to the IC. A PCB layout proposal for a two-layer board is shown in [Figure 33](#). Connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance.

11.2 Layout Examples

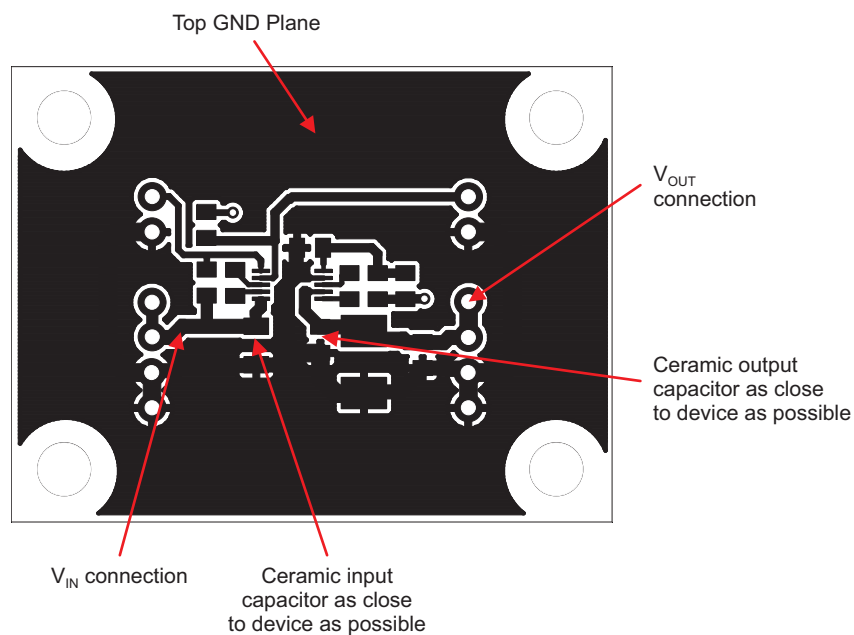


Figure 33. Recommended PCB Layout for TPS6050x (Top Layer)

Layout Examples (continued)

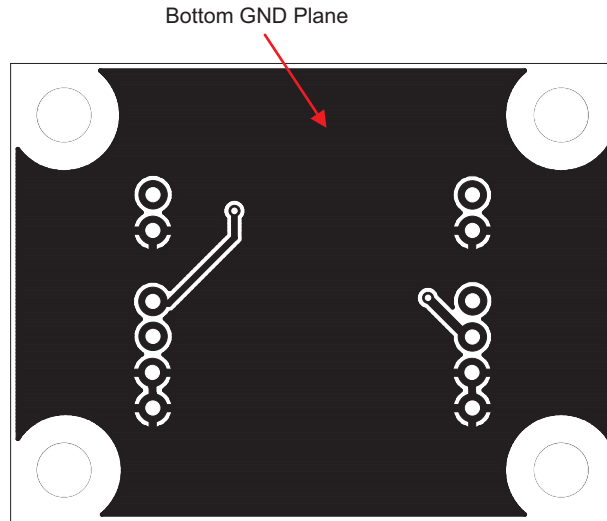


Figure 34. Recommended PCB Layout for TPS6050x (Bottom Layer)

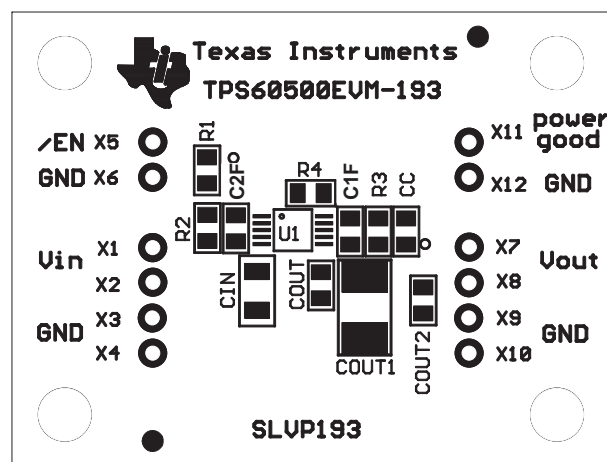


Figure 35. Top Silkscreen

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS60500	Click here	Click here	Click here	Click here	Click here
TPS60501	Click here	Click here	Click here	Click here	Click here
TPS60502	Click here	Click here	Click here	Click here	Click here
TPS60503	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60500DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60500DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60500DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60500DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60501DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC	Samples
TPS60501DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC	Samples
TPS60502DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60502DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60502DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60503DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60500DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60501DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60502DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60500DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60501DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60502DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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