



**THE DATASHEET OF  
SN74LS155ADR**

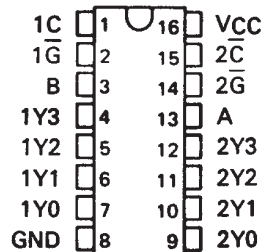


# SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SDLS057 - MARCH 1974 - REVISED MARCH 1988

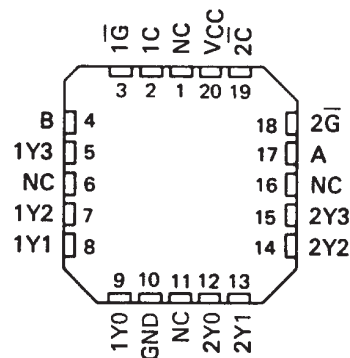
- **Applications:**
  - Dual 2-to 4-Line Decoder
  - Dual 1-to 4-Line Demultiplexer
  - 3-to 8-Line Decoder
  - 1-to 8-Line Demultiplexer
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
  - Totem Pole ('155, 'LS155A)
  - Open-Collector ('156, 'LS156)

SN54155, SN54156, SN54LS155A,  
SN54LS156 . . . J OR W PACKAGE  
SN74155, SN74156 . . . N PACKAGE  
SN74LS155A, SN74LS156 . . . D OR N PACKAGE  
(TOP VIEW)



TYPES	TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS	TYPICAL POWER DISSIPATION
'155, '156	21 ns	125 mW
'LS155A	18 ns	31 mW
'LS156	32 ns	31 mW

SN54LS155A, SN54LS156 . . . FK PACKAGE  
(TOP VIEW)

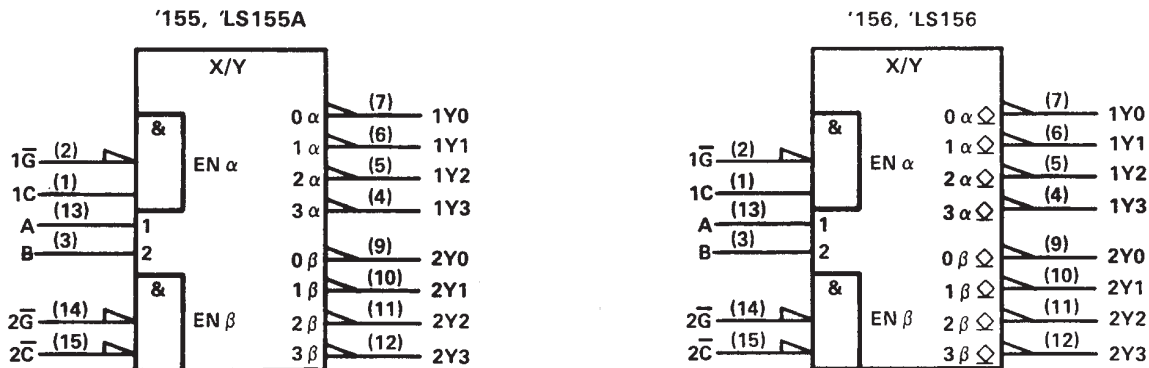


## description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

NC - No internal connection

## logic symbols (2-line to 4-line decoder)†



† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. For alternative symbols for other applications, see the following page.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

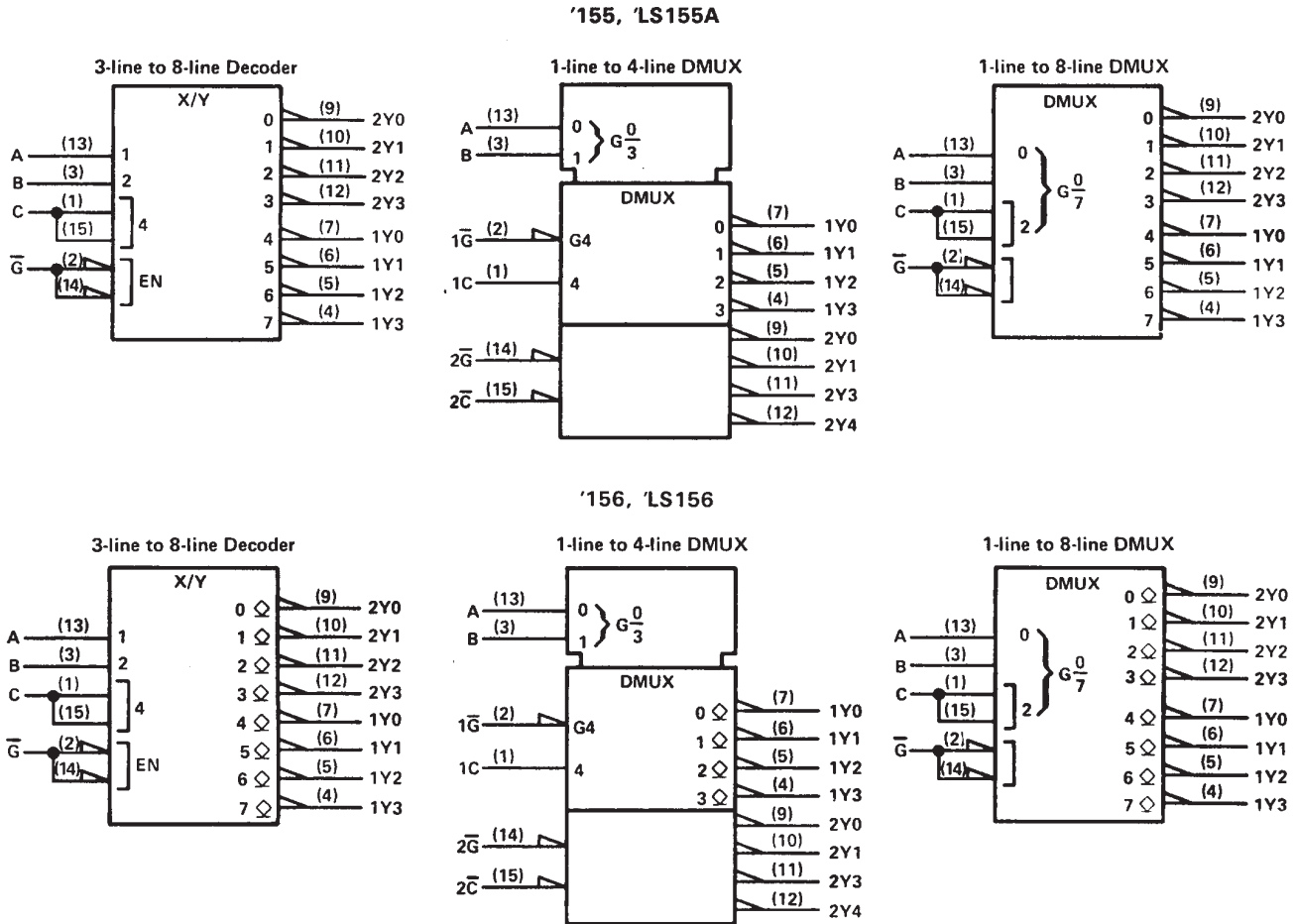
Copyright © 1988, Texas Instruments Incorporated

# SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156

## DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

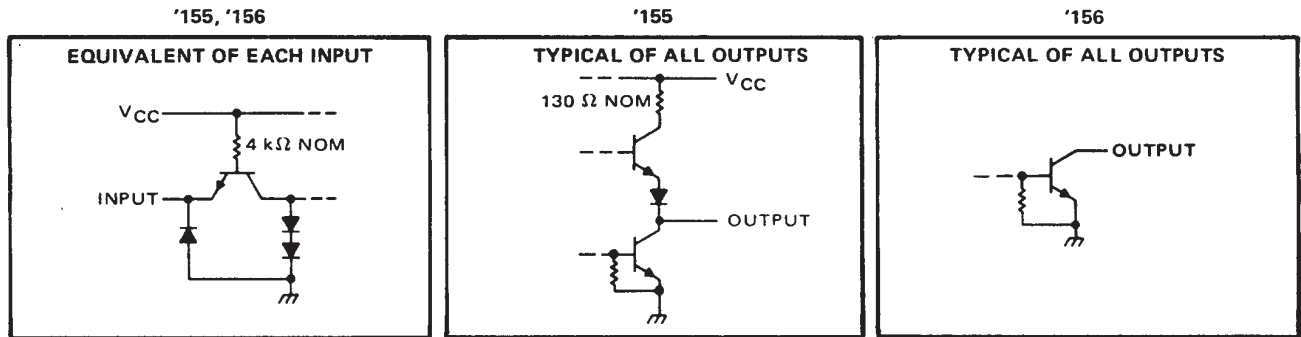
SDLS057 – MARCH 1974 – REVISED MARCH 1988

### additional logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

### schematics of inputs and outputs

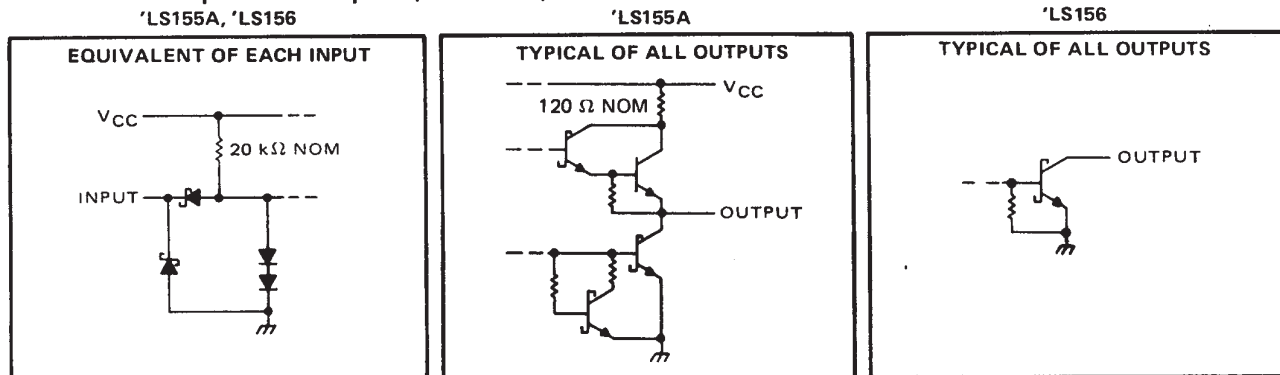


# SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156

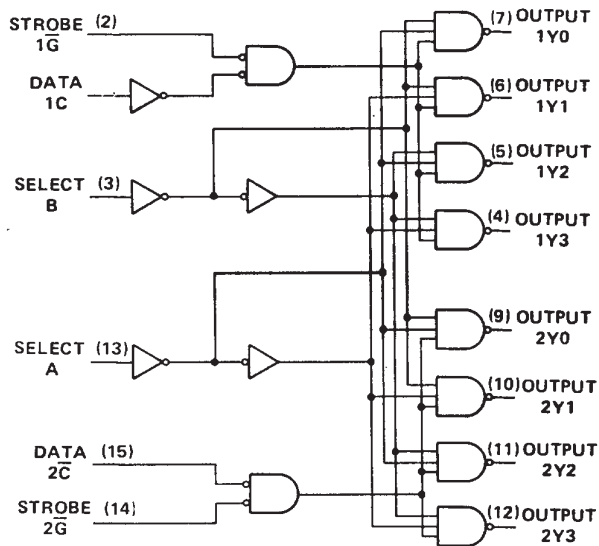
## DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SDLS057 - MARCH 1974 - REVISED MARCH 1988

### schematics of inputs and outputs (continued)



### logic diagram (positive logic)



### FUNCTION TABLES

2-LINE-TO-4-LINE DECODER  
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT	STROBE	DATA	1Y0	1Y1	1Y2	1Y3	
B A	1G	1C					
X X	H	X	H	H	H	H	
L L	L	H	L	H	H	H	
L H	L	H	H	L	H	H	
H L	L	H	H	H	L	H	
H H	L	H	H	H	H	L	
X X	X	L	H	H	H	H	

INPUTS				OUTPUTS			
SELECT	STROBE	DATA	2Y0	2Y1	2Y2	2Y3	
B A	2G	2C					
X X	H	X	H	H	H	H	
L L	L	L	L	H	H	H	
L H	L	L	H	L	H	H	
H L	L	L	H	H	L	H	
H H	L	L	H	H	H	L	
X X	X	H	H	H	H	H	

FUNCTION TABLE  
3-LINE-TO-8-LINE DECODER  
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT	STROBE	OR DATA		(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C† B A	OR G‡			2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X X X	H			H	H	H	H	H	H	H	H
L L L	L			L	H	H	H	H	H	H	H
L L H	L			H	L	H	H	H	H	H	H
L H L	L			H	H	L	H	H	H	H	H
L H H	L			H	H	H	L	H	H	H	H
H L L	L			H	H	H	H	L	H	H	H
H L H	L			H	H	H	H	H	L	H	H
H H L	L			H	H	H	H	H	H	L	H
H H H	L			H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together

‡G = inputs 1G and 2G connected together

H = high level, L = low level, X = irrelevant



# SN54155A, SN74155A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SDLS057 – MARCH 1974 – REVISED MARCH 1988

## recommended operating conditions

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, $V_{OH}$	5.5			5.5			V
Low-level output current, $I_{OL}$	16			16			mA
Operating free-air temperature, $T_A$	-55			125			°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54156 SN74156		UNIT	
		MIN	TYP‡		MAX
$V_{IH}$ High-level input voltage		2		V	
$V_{IL}$ Low-level input voltage		0.8		V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$	-1.5		V	
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$	250		$\mu\text{A}$	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4	V	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1		mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	40		$\mu\text{A}$	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-1.6		mA	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54156	25	35	mA
		SN74156	25	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54156 SN74156			UNIT
					MIN	TYP	MAX	
$t_{PLH}$	A, B, $2\bar{C}$ , $1\bar{G}$ , or $2\bar{G}$	Y	2	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3	15	23	ns	
$t_{PHL}$	A, B, $2\bar{C}$ , $1\bar{G}$ , or $2\bar{G}$	Y	2		20	30	ns	
$t_{PLH}$	A or B	y	3		23	34	ns	
$t_{PHL}$	A or B	Y	3		23	34	ns	
$t_{PLH}$	1C	Y	3		18	27	ns	
$t_{PHL}$	1C	Y	3		22	33	ns	

§  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN54LS155A, SN74LS155A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SDLS057 – MARCH 1974 – REVISED MARCH 1988

## recommended operating conditions

	SN54LS155A			SN74LS155A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS155A			SN74LS155A			UNIT	
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX		
$V_{IH}$ High-level input voltage		2			2			V	
$V_{IL}$ Low-level input voltage				0.7			0.8	V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V	
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$			0.25	0.4		0.25	0.4	V
							0.35	0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu$ A	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA	
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		6.1	10		6.1	10	mA	

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER <sup>¶</sup>	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155A SN74LS155A			UNIT
					MIN	TYP	MAX	
$t_{PLH}$	A, B, $2\bar{C}$ , $1\bar{G}$ , or $2\bar{G}$	Y	2	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 3	10	15	ns	
$t_{PHL}$	A, B, $2\bar{C}$ , $1\bar{G}$ , or $2\bar{G}$	Y	2		19	30	ns	
$t_{PLH}$	A or B	Y	3		17	26	ns	
$t_{PHL}$	A or B	Y	3		19	30	ns	
$t_{PLH}$	1C	Y	3		18	27	ns	
$t_{PHL}$	1C	Y	3		18	27	ns	

<sup>¶</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN54LS156A, SN74LS156A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SDLS057 – MARCH 1974 – REVISED MARCH 1988

## recommended operating conditions

	SN54LS156			SN74LS156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, $V_{OH}$				5.5			V
Low-level output current, $I_{OL}$				4			8 mA
Operating free-air temperature, $T_A$	-55			125			0 70 °C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS156			SN74LS156			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage					0.7			V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5			V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$				100			$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$		0.25 0.4		0.25 0.4		V
		$I_{OL} = 8 \text{ mA}$				0.35 0.5		
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.1			0.1 mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				20			20 $\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.4			-0.4 mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.1 10				6.1 10		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS156 SN74LS156			UNIT
					MIN	TYP	MAX	
$t_{PLH}$	A, B, 2C 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 3	25	40	ns	
$t_{PHL}$	A, B, 2C, 1G, or 2G	Y	2		34	51	ns	
$t_{PLH}$	A or B	Y	3		31	46	ns	
$t_{PHL}$	A or B	Y	3		34	51	ns	
$t_{PLH}$	1C	Y	3		32	48	ns	
$t_{PHL}$	1C	Y	3		32	48	ns	

§  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9750801QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QE A SNJ54LS155AJ	<a href="#">Samples</a>
5962-9750801QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QF A SNJ54LS155AW	<a href="#">Samples</a>
5962-9750801QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QF A SNJ54LS155AW	<a href="#">Samples</a>
SN54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS155AJ	<a href="#">Samples</a>
SN54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS155AJ	<a href="#">Samples</a>
SN54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS156J	<a href="#">Samples</a>
SN54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS156J	<a href="#">Samples</a>
SN74LS155AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS155A	<a href="#">Samples</a>
SN74LS155AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS155AN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS155AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS155AN	<a href="#">Samples</a>
SN74LS155ANE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS155AN	<a href="#">Samples</a>
SN74LS155ANE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS155AN	<a href="#">Samples</a>
SN74LS155ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS155A	<a href="#">Samples</a>
SN74LS155ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS155A	<a href="#">Samples</a>
SN74LS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS156	<a href="#">Samples</a>
SN74LS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS156	<a href="#">Samples</a>
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS156	<a href="#">Samples</a>
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS156	<a href="#">Samples</a>
SN74LS156DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS156	<a href="#">Samples</a>
SN74LS156DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS156	<a href="#">Samples</a>
SN74LS156N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS156N	<a href="#">Samples</a>
SN74LS156N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS156N	<a href="#">Samples</a>
SN74LS156NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS156N	<a href="#">Samples</a>
SN74LS156NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS156N	<a href="#">Samples</a>
SN74LS156NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS156	<a href="#">Samples</a>
SN74LS156NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS156	<a href="#">Samples</a>
SNJ54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QE A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54LS155AJ	
SNJ54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QE A SNJ54LS155AJ	<a href="#">Samples</a>
SNJ54LS155AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QF A SNJ54LS155AW	<a href="#">Samples</a>
SNJ54LS155AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9750801QF A SNJ54LS155AW	<a href="#">Samples</a>
SNJ54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS156J	<a href="#">Samples</a>
SNJ54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS156J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS155A, SN54LS156, SN74LS155A, SN74LS156 :**

- Catalog: [SN74LS155A](#), [SN74LS156](#)
- Military: [SN54LS155A](#), [SN54LS156](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS155ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS156DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS156NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

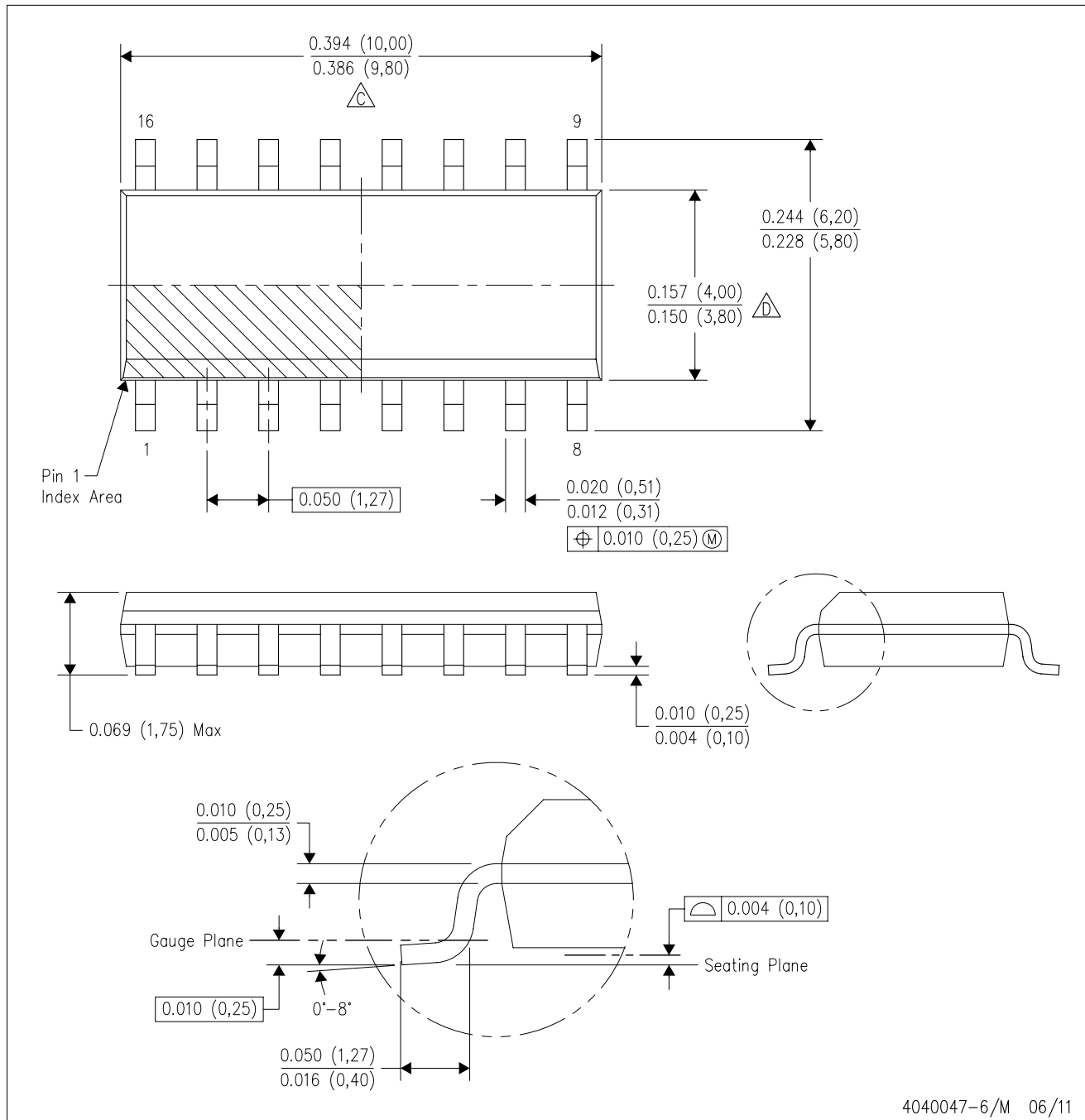
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS155ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS156DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS156NSR	SO	NS	16	2000	367.0	367.0	38.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

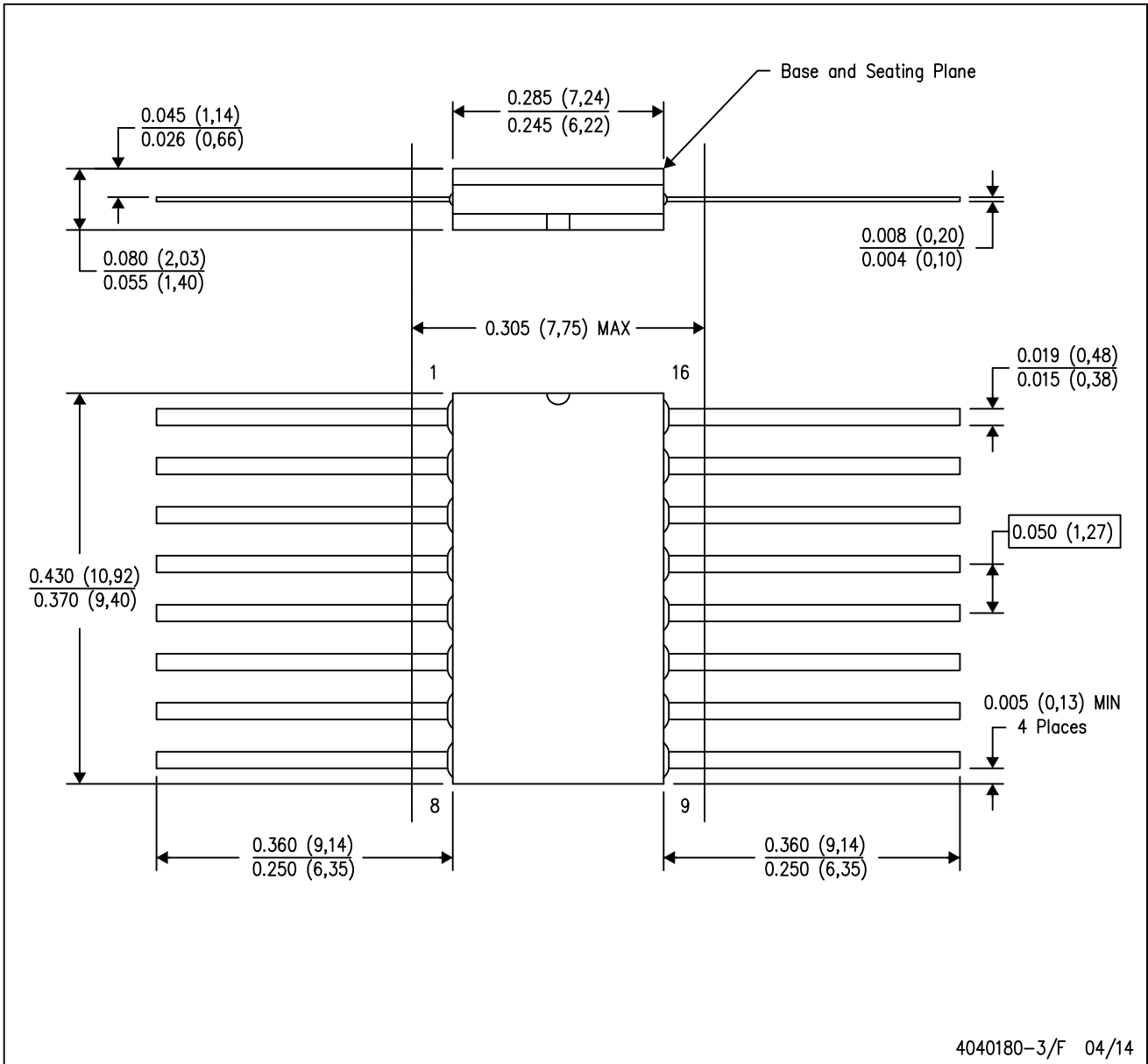
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74LS155ADR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management