



**THE DATASHEET OF
TPS3838K33DRVTG4**



NanoPower Supervisory Circuits

Check for Samples: [TPS3836](#), [TPS3837](#), [TPS3838](#)

FEATURES

- Supply Current: 220 nA (typical)
- Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3.0 V, and 3.3 V
- Power-On Reset Generator With Selectable Delay Time: 10 ms or 200 ms
- Push/Pull $\overline{\text{RESET}}$ Output (TPS3836), Push/Pull RESET Output (TPS3837), or Open-Drain $\overline{\text{RESET}}$ Output (TPS3838)
- Manual Reset
- SOT23-5 and 2x2 SON-6 Packages
- Temperature Range: -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors
- Portable- and Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook Computers
- Automotive Systems
- Applications Using the MSP430™

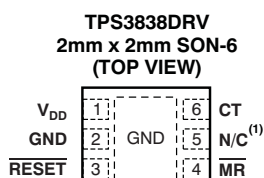
DESCRIPTION

The TPS3836, TPS3837, and TPS3838 families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

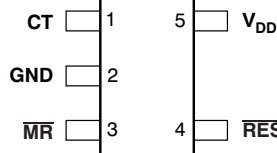
During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage of V_{IT} . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT} .

When CT is connected to GND, a fixed delay time of typical 10 ms is asserted. When connected to V_{DD} , the delay time is typically 200 ms. When the supply voltage drops below the threshold voltage V_{IT} , the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

The TPS3836 has an active-low, push-pull $\overline{\text{RESET}}$ output. The TPS3837 has an active-high, push-pull RESET, and the TPS3838 integrates an active-low, open-drain $\overline{\text{RESET}}$ output. The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3.0 V, and 3.3 V. The circuits are available in either a SOT23-5 or 2x2 SON-6 package. The TPS3836, TPS3837, and TPS3838 families are characterized for operation over a temperature range of -40°C to $+85^{\circ}\text{C}$.

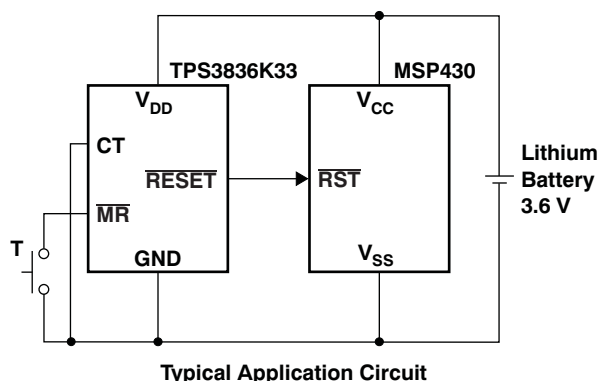
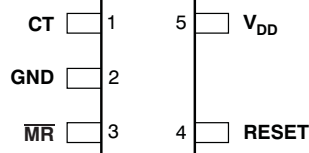


TPS3836, TPS3838
DBV PACKAGE
(TOP VIEW)



(1) N/C: Not connected.

TPS3837
DBV PACKAGE
(TOP VIEW)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION⁽¹⁾

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V _{IT}) ⁽²⁾
TPS383xE18	1.8 V	1.71 V
TPS383xJ25	2.5 V	2.25 V
TPS383xH30	3.0 V	2.79 V
TPS383xL30	3.0 V	2.64 V
TPS383xK33	3.3 V	2.93 V

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Custom threshold voltages are available. Minimum order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

	TPS383xx	UNIT
Supply voltage, V _{DD} ⁽²⁾	7	V
All other pins ^{(2) (3)}	-0.3 to 7	V
Maximum low output current, I _{OL}	5	mA
Maximum high output current, I _{OH}	-5	mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±10	mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±10	mA
Continuous total power dissipation	See Dissipation Ratings Table	
Operating temperature range, T _A	-40 to +85	°C
Storage temperature range, T _{STG}	-65 to +150	°C
Soldering temperature	+260	°C

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) If RESET or RESET are pulled above V_{DD}, the internal ESD structure will present an effective 1.5 kΩ resistor between these pins, causing leakage current to flow into the RESET or RESET pin.

DISSIPATION RATINGS

PACKAGE	T _A < +25°C POWER RATING	DERATING FACTOR ABOVE T _A = +25°C	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW
DRV Low-K ⁽¹⁾	715 mW	7.1 mW/°C	395 mW	285 mW
DRV High-K ⁽²⁾	1540 mW	15.4 mW/°C	845 mW	615 mW

- (1) The JEDEC low-K (1s) board used to derive this data was a 3in x 3in, two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.6	6	V
Voltage range, CT, \overline{MR} , RESET, and \overline{RESET} pins	0	$V_{DD} + 0.3$	V
High-level input voltage, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at \overline{MR} , $\Delta t/\Delta V$		100	ns/V
Operating temperature range, T_A	-40	+85	°C
Pull-up resistor value, \overline{RESET} pin (TPS3838 only)	$\frac{V_{PULL-UP}}{50 \mu A}$		Ω

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{OH}	High-level output voltage	\overline{RESET} (TPS3836)	$V_{DD} = 3.3 \text{ V}, I_{OH} = -2 \text{ mA}$	$0.8 \times V_{DD}$		V	
			$V_{DD} = 6 \text{ V}, I_{OH} = -3 \text{ mA}$				
		RESET (TPS3837)	$V_{DD} = 1.8 \text{ V}, I_{OH} = -1 \text{ mA}$				
			$V_{DD} = 3.3 \text{ V}, I_{OL} = -2 \text{ mA}$				
V_{OL}	Low-level output voltage	\overline{RESET} (TPS3836, TPS3838)	$V_{DD} = 1.8 \text{ V}, I_{OL} = 1 \text{ mA}$		0.4	V	
			$V_{DD} = 3.3 \text{ V}, I_{OL} = 2 \text{ mA}$				
		RESET (TPS3837)	$V_{DD} = 3.3 \text{ V}, I_{OL} = 2 \text{ mA}$				
			$V_{DD} = 6 \text{ V}, I_{OL} = 3 \text{ mA}$				
	Power-up reset voltage ⁽¹⁾	TPS3836, TPS3838	$V_{DD} \geq 1.1 \text{ V}, I_{OL} = 50 \mu A$		0.2	V	
		TPS3837	$V_{DD} \geq 1.1 \text{ V}, I_{OL} = -50 \mu A$	$0.8 \times V_{DD}$		V	
V_{IT}	Negative-going input threshold voltage ⁽²⁾	TPS383xE18	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.66	1.71	1.74	V
		TPS383xJ25		2.18	2.25	2.29	
		TPS383xH30		2.70	2.79	2.85	
		TPS383xL30		2.56	2.64	2.69	
		TPS383xK33		2.84	2.93	2.99	
V_{HYS}	Hysteresis at V_{DD} input		$1.7 \text{ V} < V_{IT} < 2.5 \text{ V}$	30		mV	
			$2.5 \text{ V} < V_{IT} < 3.5 \text{ V}$	40			
			$3.5 \text{ V} < V_{IT} < 5 \text{ V}$	50			
I_{IH}	High-level input current	\overline{MR} ⁽³⁾	$\overline{MR} = 0.7 \times V_{DD}, V_{DD} = 6 \text{ V}$	-40	-60	-100	μA
		CT	$CT = V_{DD} = 6 \text{ V}$	-25		+25	nA
I_{IL}	Low-level input current	\overline{MR} ⁽³⁾	$\overline{MR} = 0 \text{ V}, V_{DD} = 6 \text{ V}$	-130	-200	-340	μA
		CT	$CT = 0 \text{ V}, V_{DD} = 6 \text{ V}$	-25		+25	nA
I_{OH}	High-level output current	TPS3838	$V_{DD} = V_{IT} + 0.2 \text{ V}, V_{OH} = V_{DD}$			25	nA
I_{DD}	Supply current		$V_{DD} > V_{IT}, V_{DD} < 3 \text{ V}$	220	400	nA	
			$V_{DD} > V_{IT}, V_{DD} > 3 \text{ V}$	250	450		
			$V_{DD} < V_{IT}$	10	15	μA	
	Internal pull-up resistor at \overline{MR}			30		k Ω	
C_I	Input capacitance at \overline{MR} and CT		$V_I = 0 \text{ V to } V_{DD}$	5		pF	

(1) The lowest voltage at which the \overline{RESET} output becomes active. $t_R, V_{DD} \geq 15 \mu s/V$.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminal.

(3) If manual reset is unused, \overline{MR} should be connected to V_{DD} to minimize current consumption.

SWITCHING CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $R_L = 1\text{ M}\Omega$, and $C_L = 50\text{ pF}$, unless otherwise noted.

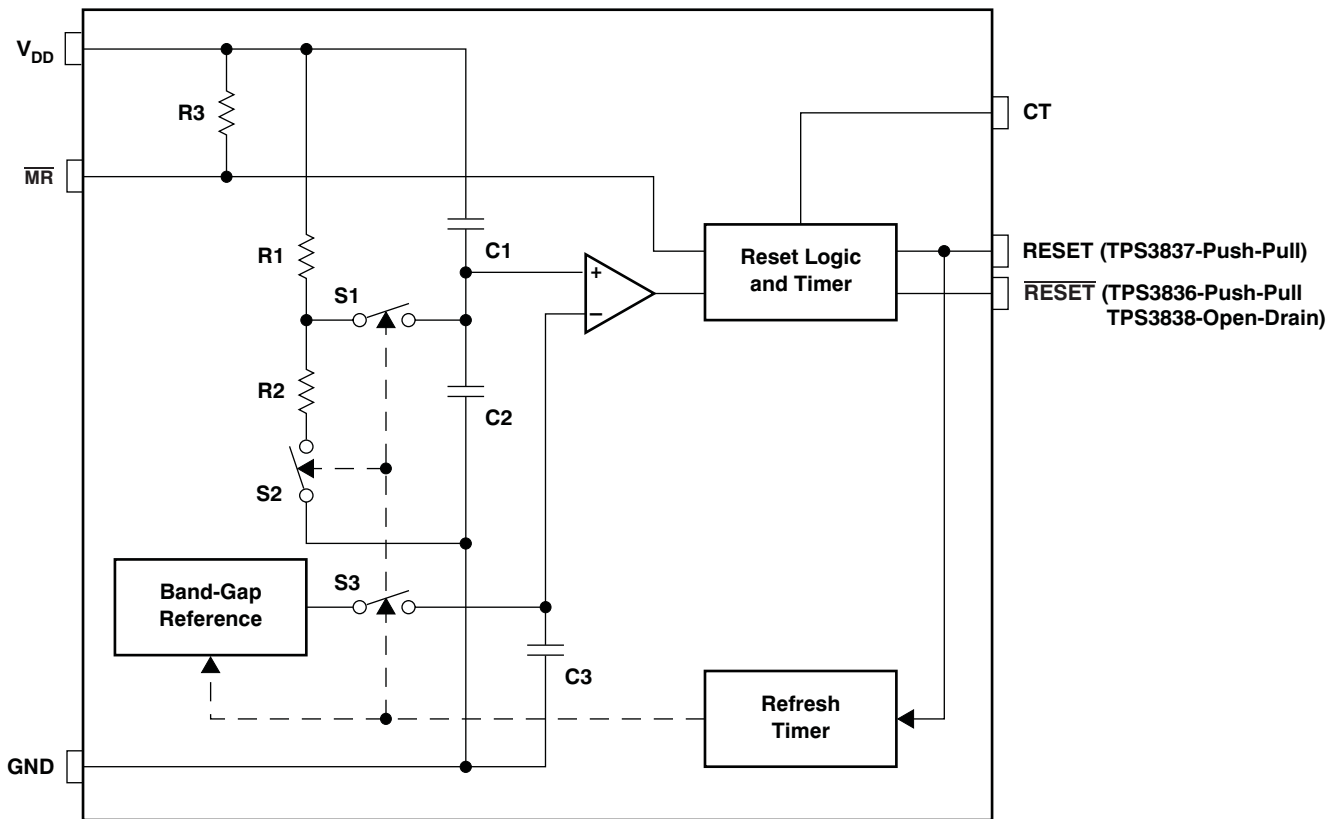
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Delay time	$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $\overline{MR} = 0.7 \times V_{DD}$, CT = GND, (See Timing Diagram)	5	10	15	ms
		$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $\overline{MR} = 0.7 \times V_{DD}$, CT = V_{DD} , (See Timing Diagram)	100	200	300	
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to \overline{RESET} delay (TPS3836, TPS3838)	$V_{IL} = V_{IT} - 0.2\text{ V}$, $V_{IH} = V_{IT} + 0.2\text{ V}$		10	μs
			$V_{IL} = 1.6\text{ V}$		50	
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to \overline{RESET} delay (TPS3837)	$V_{IL} = V_{IT} - 0.2\text{ V}$, $V_{IH} = V_{IT} + 0.2\text{ V}$		10	μs
			$V_{IL} = 1.6\text{ V}$		50	
t_{PHL}	Propagation (delay) time, high-to-low-level output	\overline{MR} to \overline{RESET} delay (TPS3836, TPS3838)	$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IL} = 0.7 \times V_{DD}$		0.1	μs
t_{PLH}	Propagation (delay) time, low-to-high-level output	\overline{MR} to \overline{RESET} delay (TPS3837)	$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IL} = 0.7 \times V_{DD}$		0.1	μs

TIMING REQUIREMENTS

At $T_A = +25^\circ\text{C}$, $R_L = 1\text{ M}\Omega$, and $C_L = 50\text{ pF}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_W	Pulse width	at V_{DD}	$V_{IH} = V_{IT} + 0.2\text{ V}$, $V_{IL} = V_{IT} - 0.2\text{ V}$		6	μs
		at \overline{MR}	$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		1	

FUNCTIONAL BLOCK DIAGRAM

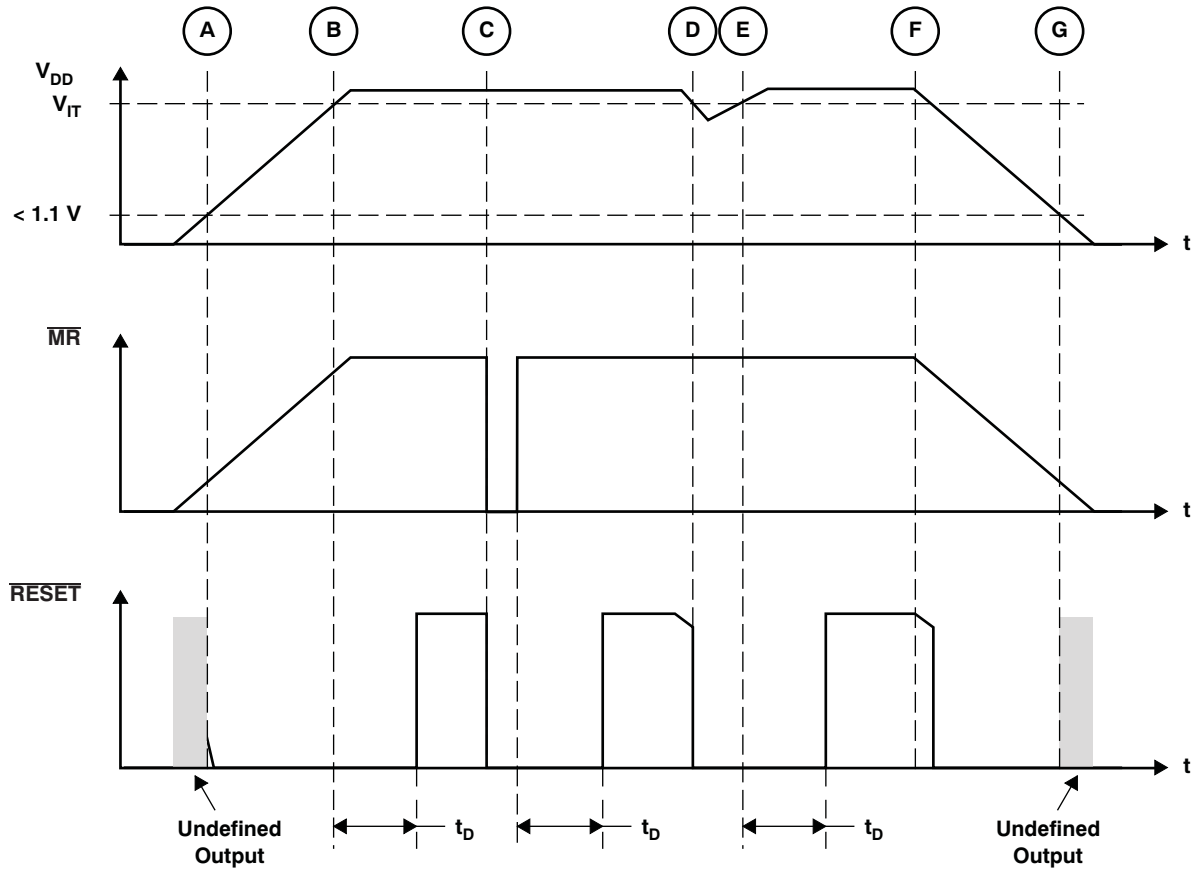


FUNCTION TABLE

\overline{MR}	$V_{DD} > V_{IT}$	$\overline{RESET}^{(1)}$	$RESET^{(2)}$
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3836 and TPS3838.
(2) TPS3837.

TIMING DIAGRAM



TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
 vs
 SUPPLY VOLTAGE**

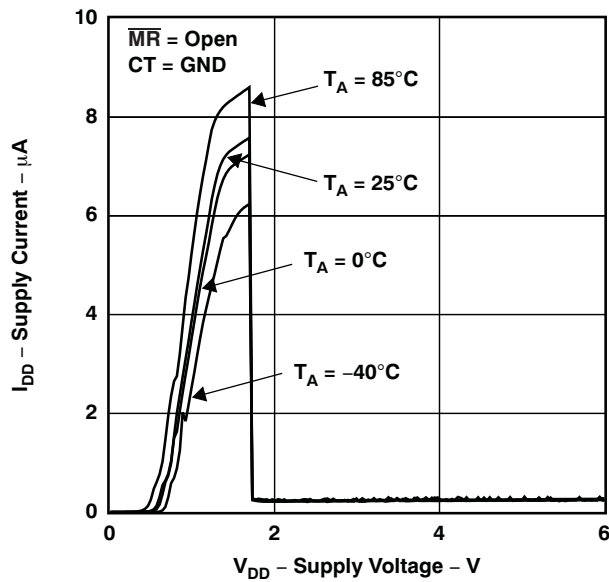


Figure 1.

**MANUAL RESET CURRENT
 vs
 MANUAL RESET VOLTAGE**

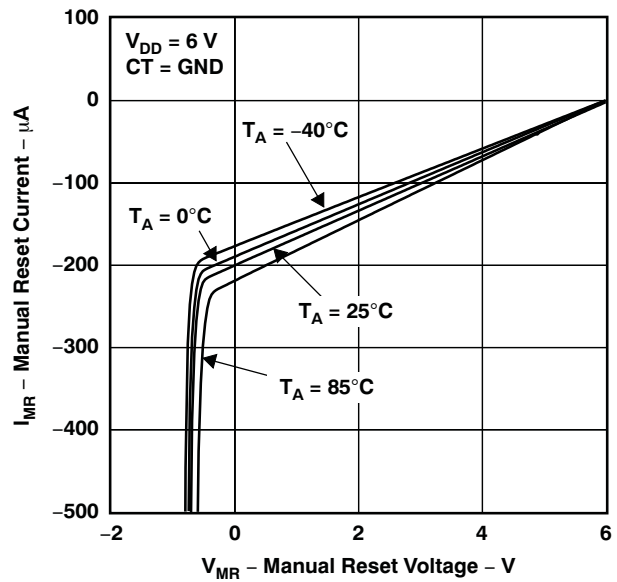


Figure 2.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

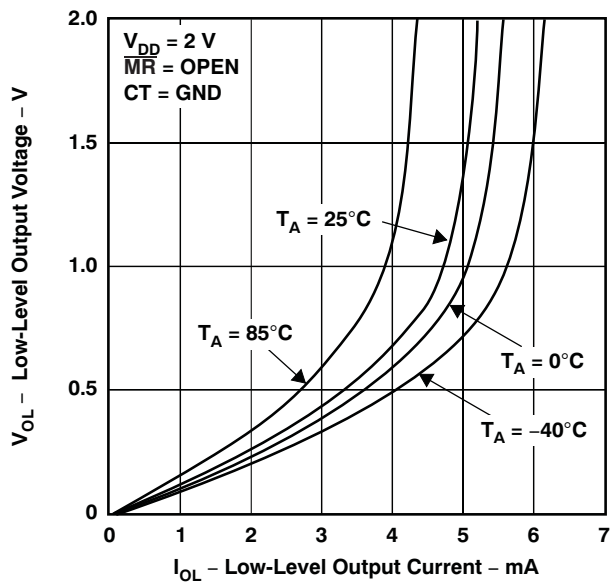


Figure 3.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

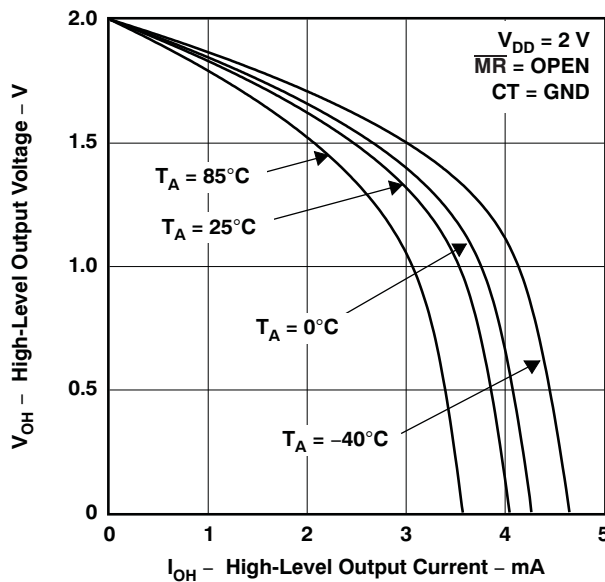


Figure 4.

NORMALIZED RESET THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

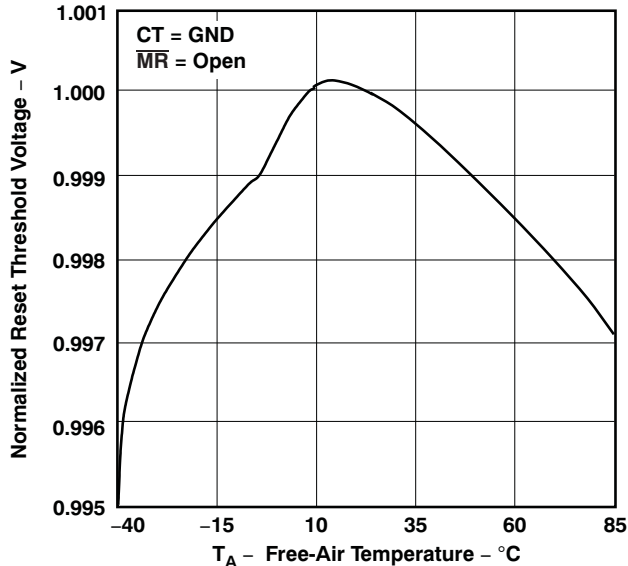


Figure 5.

MINIMUM PULSE DURATION AT V_{DD}
vs
 V_{DD} THRESHOLD OVERDRIVE

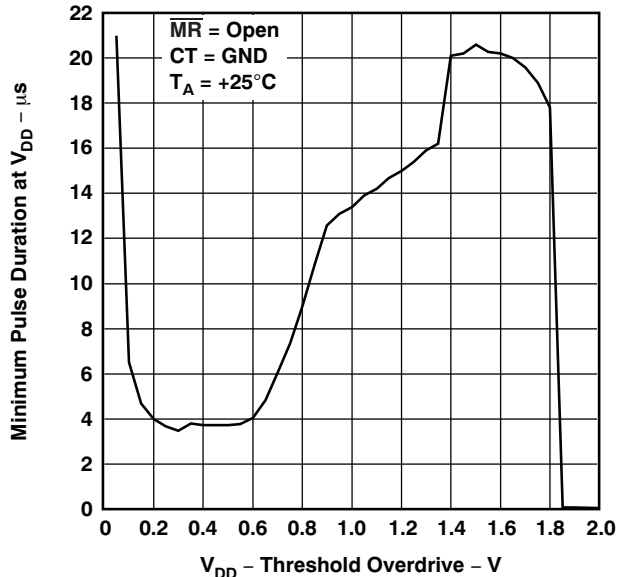


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3836E18DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDNI	Samples
TPS3836E18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDNI	Samples
TPS3836E18DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDNI	Samples
TPS3836H30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHRI	Samples
TPS3836H30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHRI	Samples
TPS3836J25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDSI	Samples
TPS3836J25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDSI	Samples
TPS3836K33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDTI	Samples
TPS3836K33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDTI	Samples
TPS3836K33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDTI	Samples
TPS3836K33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDTI	Samples
TPS3836L30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCAI	Samples
TPS3836L30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCAI	Samples
TPS3836L30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCAI	Samples
TPS3836L30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCAI	Samples
TPS3837E18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDOI	Samples
TPS3837E18DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDOI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3837J25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDRI	Samples
TPS3837J25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDRI	Samples
TPS3837K33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDUI	Samples
TPS3837K33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDUI	Samples
TPS3837K33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDUI	Samples
TPS3837L30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCBI	Samples
TPS3837L30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCBI	Samples
TPS3837L30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCBI	Samples
TPS3838E18DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDQI	Samples
TPS3838E18DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDQI	Samples
TPS3838E18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDQI	Samples
TPS3838E18DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDQI	Samples
TPS3838J25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDPI	Samples
TPS3838J25DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDPI	Samples
TPS3838J25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDPI	Samples
TPS3838J25DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDPI	Samples
TPS3838K33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDVI	Samples
TPS3838K33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDVI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3838K33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDVI	Samples
TPS3838K33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDVI	Samples
TPS3838K33DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCS	Samples
TPS3838K33DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCS	Samples
TPS3838L30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCCI	Samples
TPS3838L30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCCI	Samples
TPS3838L30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCCI	Samples
TPS3838L30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCCI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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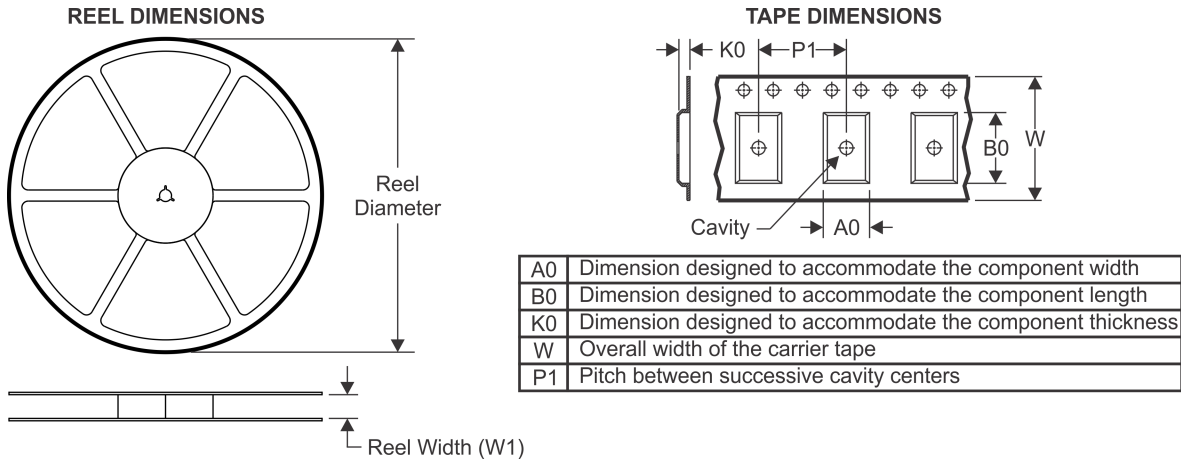
OTHER QUALIFIED VERSIONS OF TPS3836, TPS3838 :

- Automotive: [TPS3836-Q1](#), [TPS3838-Q1](#)
- Enhanced Product: [TPS3836-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



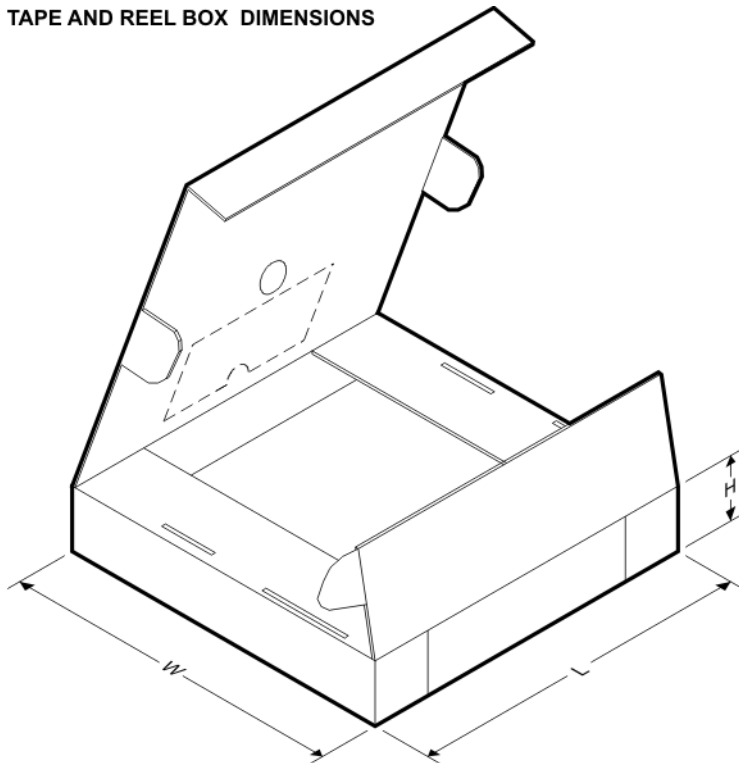
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3836E18DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836E18DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836H30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836H30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836J25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836J25DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836K33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836K33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3836L30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3836L30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3837E18DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3837J25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3837J25DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3837K33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3837K33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3837L30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3837L30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3838E18DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3838E18DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838J25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838J25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3838J25DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3838J25DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838K33DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838K33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3838K33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3838K33DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838K33DRVVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3838K33DRVVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3838L30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838L30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3838L30DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838L30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3836E18DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3836E18DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3836H30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3836H30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3836J25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3836J25DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3836K33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3836K33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3836L30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3836L30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3837E18DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3837J25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3837J25DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3837K33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3837K33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3837L30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3837L30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3838E18DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3838E18DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3838J25DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3838J25DBVT	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3838J25DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3838J25DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3838K33DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3838K33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3838K33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3838K33DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3838K33DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3838K33DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3838L30DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3838L30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3838L30DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3838L30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

GENERIC PACKAGE VIEW

DRV 6

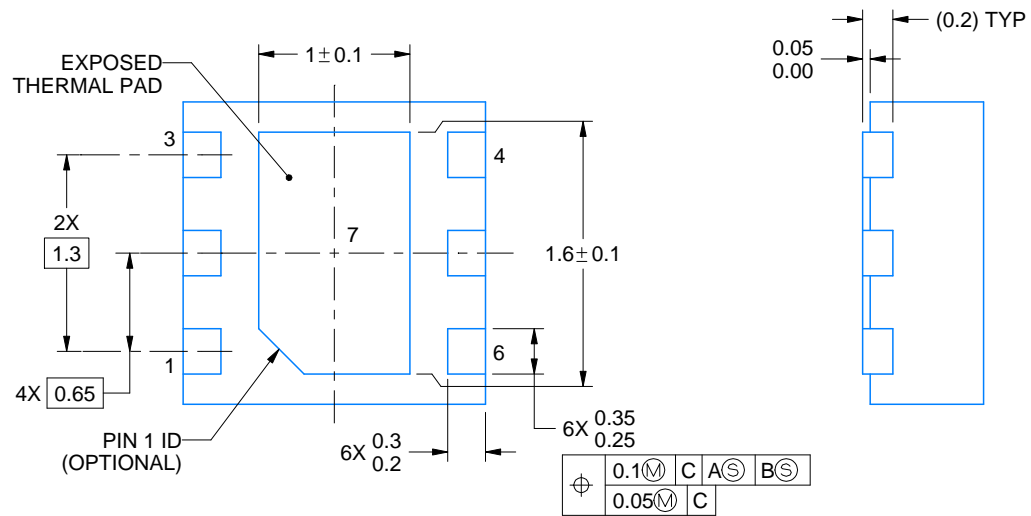
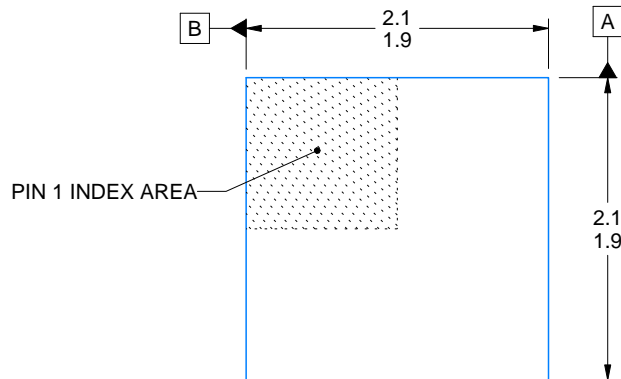
WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206925/F



4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

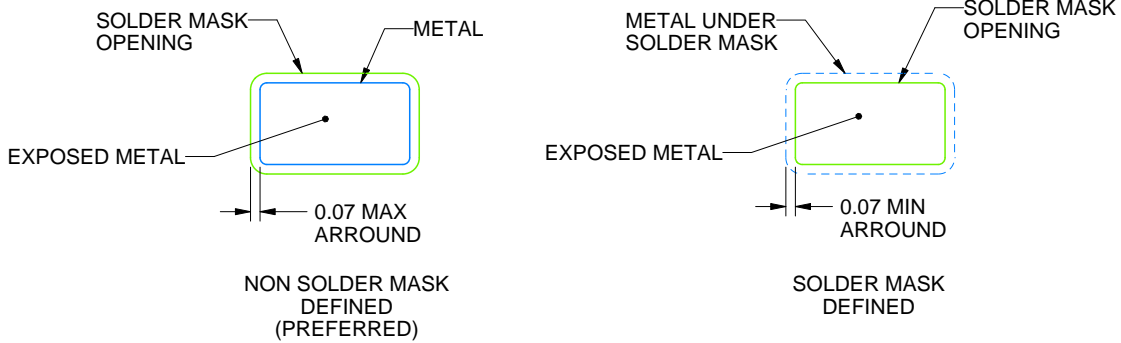
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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