CS53L21

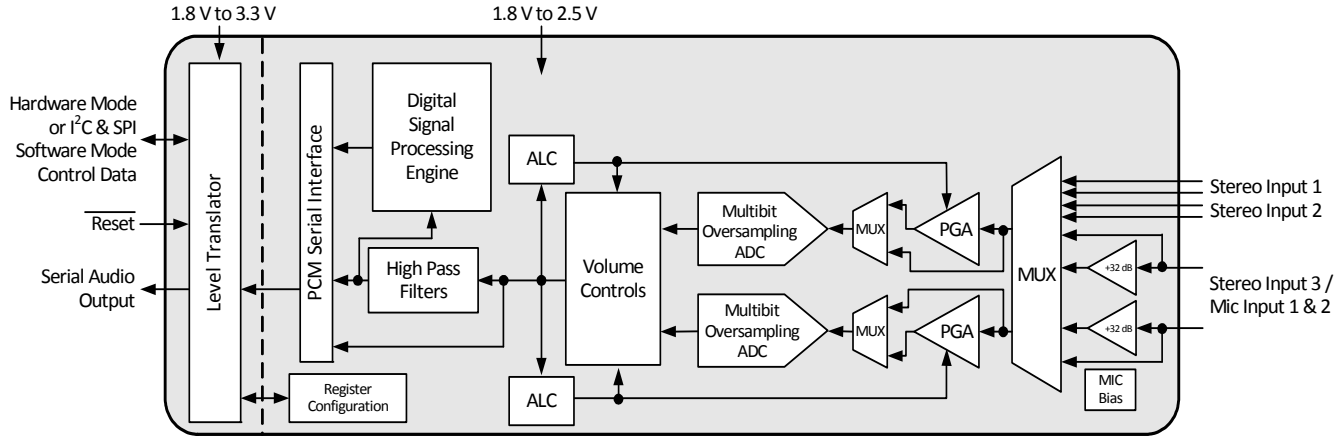
# Low-Power, Stereo Analog-to-Digital Converter

## FEATURES

- 98-dB dynamic range (A-weighted)
- –88-dB THD+N
- Analog gain controls
  - +32-dB or +16-dB mic preamps
  - Analog programmable gain amplifier (PGA)
- +20-dB digital boost
- Programmable automatic level control (ALC)
  - Noise gate for noise suppression
  - Programmable threshold and attack/release rates
- Independent left/right channel control
- Digital volume control
- High-pass filter disable for DC measurements
- Stereo 3:1 analog input MUX
- Dual mic inputs
  - Programmable, low noise mic bias levels
  - Differential mic mix for common mode noise rejection
- Very low 64 Fs oversampling clock reduces power consumption

## SYSTEM FEATURES

- 24-bit conversion
- 4–96 kHz sample rate
- Multibit delta–sigma architecture
- Low power operation
  - Stereo record (ADC): 8.72 mW @ 1.8 V
  - Stereo record (mic to PGA and ADC): 13.73 mW @ 1.8 V
- Variable power supplies
  - 1.8–2.5-V digital and analog
  - 1.8–3.3-V interface logic
- Power down management
  - ADC, mic preamplifier, PGA
- Software Mode (I²C™ and SPI™ control)
- Hardware Mode (standalone control)
- Flexible clocking options
  - Master or slave operation
- Digital routing mixes
  - Mono mixes



## APPLICATIONS

- Portable audio players
- Digital microphones
- Digital voice recorders
- Voice recognition systems
- Audio/video capture cards

## GENERAL DESCRIPTION

The CS53L21 is a highly integrated, 24-bit, 96-kHz, low power stereo A/D. Based on multibit, delta–sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. The ADC offers many features suitable for low power, portable system applications.

The ADC input path allows independent channel control of a number of features. An input multiplexer selects between line-level or microphone-level inputs for each channel. The microphone input path includes a selectable programmable-gain preamp stage and a low noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft ramp and zero cross transitions. The ADC also features a digital volume attenuator with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately.

The Signal Processing Engine (SPE) controls left/right channel volume mixing, channel swap and channel mute functions. All volume-level changes may be configured to occur on soft ramp and zero cross transitions.

The CS53L21 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CDB53L21 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see “Ordering Information” on page 56 for complete details.

In addition to its many features, the CS53L21 operates from a low-voltage analog and digital core, making this A/D ideal for portable systems that require extremely low power consumption in a minimal amount of space.

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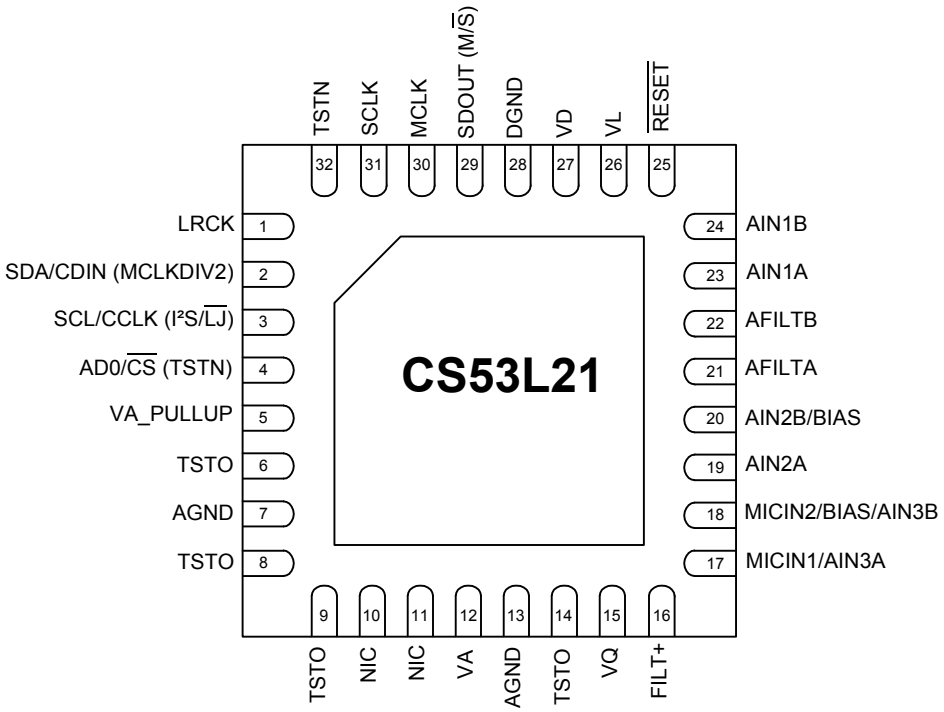
# 1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE




| Pin Name | # | Pin Description |
|---|---|---|
| LRCK | 1 | **Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line. |
| SDA/CDIN (MCLKDIV2) | 2 | **Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode. |
| | | **MCLK Divide by 2** (*Input*) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry. |
| SCL/CCLK (I²S/LJ) | 3 | **Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. |
| | | **Interface Format Selection** (*Input*) - Hardware Mode: Selects between I²S and left-Justified interface formats for the ADC. |
| AD0/CS (TSTN) | 4 | **Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format. |
| | | **Test In** (*Input*) - Hardware Mode: This pin is an input used for test purposes only and should be tied to DGND for normal operation. |
| VA_PULLUP | 5 | **Reference Pull-up** (*Input*) - This pin is an input used for test purposes only and must be pulled-up to VA using a 47 kΩ resistor. |
| TSTO | 6 | **Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin). |
| AGND | 7 | **Analog Ground** (*Input*) - Ground reference for the internal analog section. |
| TSTO | 8 | **Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin). |

| | | |
|---|---|---|
| TSTO | 9 | **Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin). |
| NIC<br>NIC | 10<br>11 | .**Not Internally Connected** - This pin is not connected internal to the device and may be connected to ground or left “floating”. No other external connection should be made to this pin. |
| VA | 12 | **Analog Power** (*Input*) - Positive power for the internal analog section. |
| AGND | 13 | **Analog Ground** (*Input*) - Ground reference for the internal analog section. |
| TSTO | 14 | **Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin). |
| VQ | 15 | **Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. |
| FILT+ | 16 | **Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits. |
| MICIN1/<br>AIN3A | 17 | **Microphone Input 1** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table. |
| MICIN2/<br>BIAS/AIN3B | 18 | **Microphone Input 2** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table. |
| AIN2A | 19 | **Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table. |
| AIN2B/BIAS | 20 | **Analog Input** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table. |
| AFILTA<br>AFILTB | 21<br>22 | **Filter Connection** (*Output*) - Filter connection for the ADC inputs. |
| AIN1A<br>AIN1B | 23<br>24 | **Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table. |
| $\overline{\text{RESET}}$ | 25 | **Reset** (*Input*) - The device enters a low power mode when this pin is driven low. |
| VL | 26 | **Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages. |
| VD | 27 | **Digital Power** (*Input*) - Positive power for the internal digital section. |
| DGND | 28 | **Digital Ground** (*Input*) - Ground reference for the internal digital section. |
| SDOUT<br>(M/$\overline{\text{S}}$) | 29 | **Serial Audio Data Output** (*Output*) - Output for two’s complement serial audio data.<br>**Serial Port Master/Slave** (*Input/Output*) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port. |
| MCLK | 30 | **Master Clock** (*Input*) - Clock source for the delta-sigma modulators. |
| SCLK | 31 | **Serial Clock** *(Input/Output*) -- Serial clock for the serial audio interface. |
| TSTN | 32 | **Test In** (*Input*) - This pin is an input used for test purposes only and should be tied to DGND for normal operation. |
| Thermal Pad | - | Thermal relief pad for optimized heat dissipation. See “QFN Thermal Pad” on page 53. |

## 1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

| Pin Name SW/(HW) | I/O | Driver | Receiver |
|---|---|---|---|
| $\overline{\text{RESET}}$ | Input | - | 1.8 V - 3.3 V |
| SCL/CCLK (I²S/$\overline{\text{LJ}}$) | Input | - | 1.8 V - 3.3 V, with Hysteresis |
| SDA/CDIN (MCLKDIV2) | Input/Output | 1.8 V - 3.3 V, CMOS/Open Drain | 1.8 V - 3.3 V, with Hysteresis |
| AD0/$\overline{\text{CS}}$ (DEM) | Input | - | 1.8 V - 3.3 V |
| MCLK | Input | - | 1.8 V - 3.3 V |
| LRCK | Input/Output | 1.8 V - 3.3 V, CMOS | 1.8 V - 3.3 V |
| SCLK | Input/Output | 1.8 V - 3.3 V, CMOS | 1.8 V - 3.3 V |
| SDOUT (M/$\overline{\text{S}}$) | Input/Output | 1.8 V - 3.3 V, CMOS | 1.8 V - 3.3 V |

**Table 1. I/O Power Rails**

## 2. TYPICAL CONNECTION DIAGRAMS

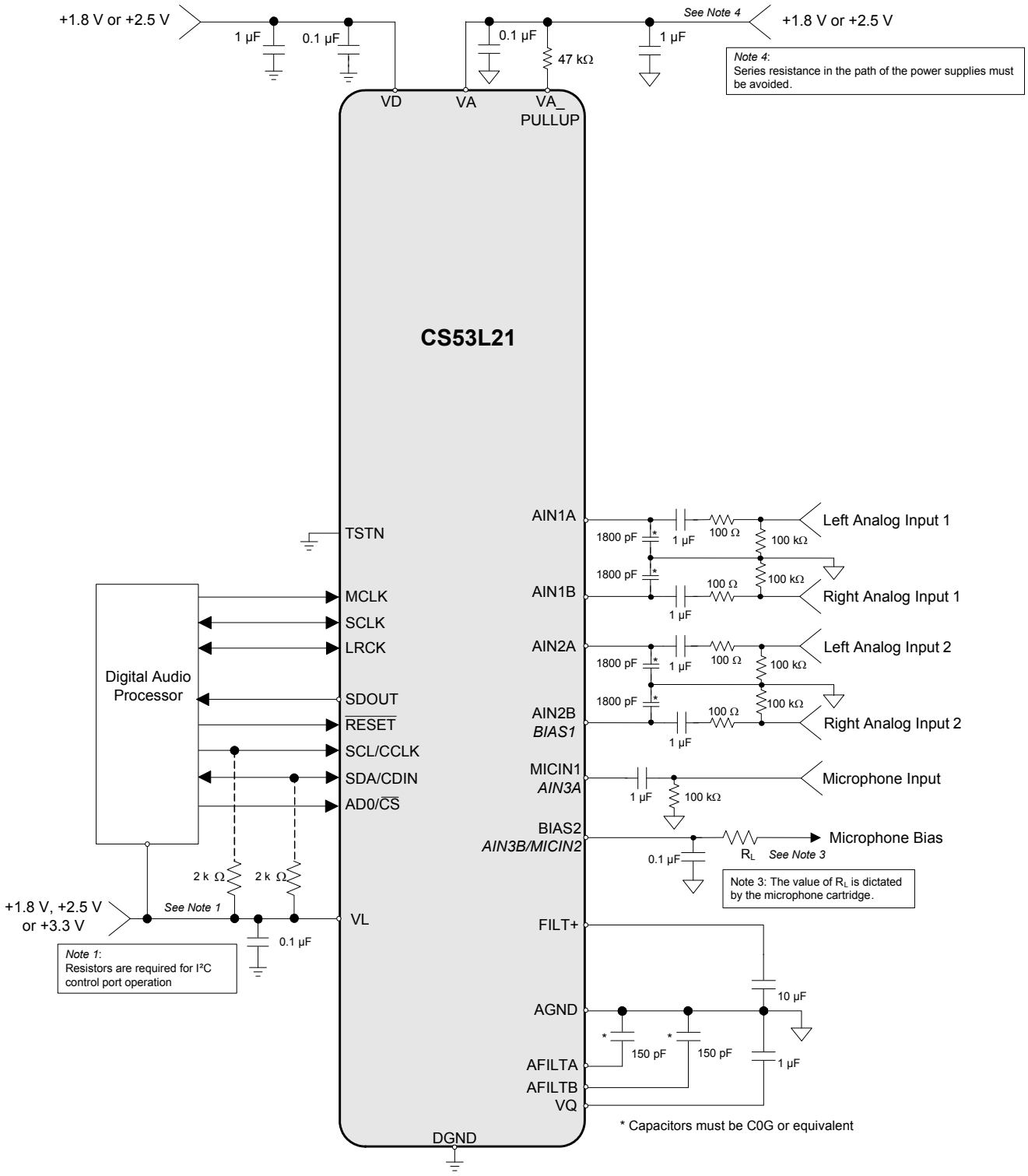



**Figure 1. Typical Connection Diagram (Software Mode)**

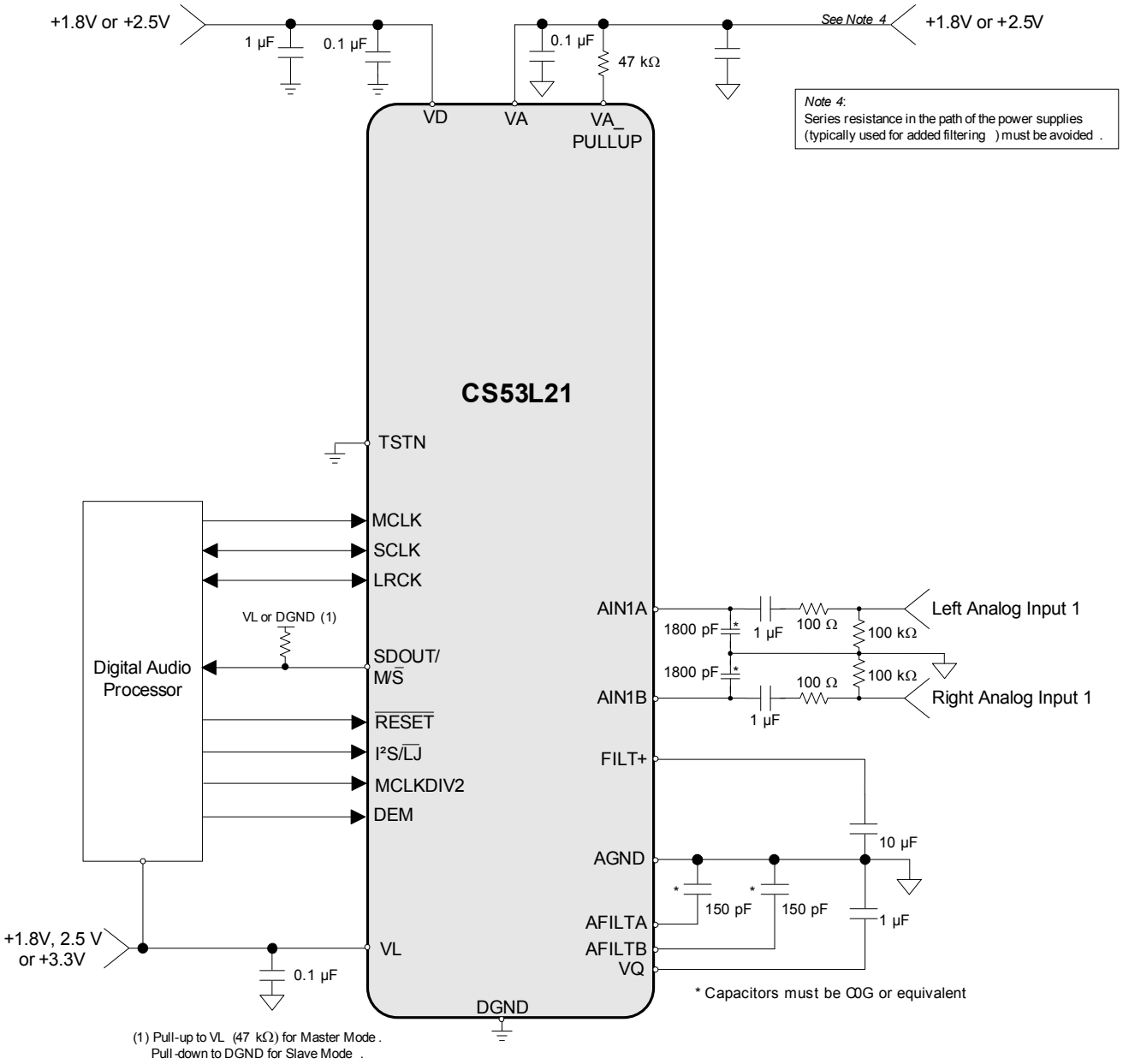



**Figure 2. Typical Connection Diagram (Hardware Mode)**

# 3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A$ = 25° C.)

## SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

| Parameters | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| DC Power Supply (Note 1) | | | | | |
| Analog Core | | VA | 1.65 | 2.63 | V |
| Digital Core | | VD | 1.65 | 2.63 | V |
| Serial/Control Port Interface | | VL | 1.65 | 3.47 | V |
| Ambient Temperature | Commercial - CNZ<br>Automotive - DNZ | $T_A$ | -10<br>-40 | +70<br>+85 | °C<br>°C |

**Note:**

1. The device will operate properly over the full range of the analog, digital core and serial/control port interface supplies.

## ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

| Parameters | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| DC Power Supply | Analog<br>Digital<br>Serial/Control Port Interface | VA<br>VD<br>VL | -0.3<br>-0.3<br>-0.3 | 3.0<br>3.0<br>4.0 | V<br>V<br>V |
| Input Current | (Note 2) | $I_{in}$ | - | ±10 | mA |
| Analog Input Voltage | (Note 3) | $V_{IN}$ | AGND-0.7 | VA+0.7 | V |
| Digital Input Voltage (Note 3) | | $V_{IND}$ | -0.3 | VL+ 0.4 | V |
| Ambient Operating Temperature (power applied) | | $T_A$ | -50 | +115 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | +150 | °C |

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

**Notes:**

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

## ANALOG CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

| Parameter (Note 4) | | VA = 2.5 V (nominal) Min | Typ | Max | VA = 1.8 V (nominal) Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ***Analog In to ADC (PGA bypassed)*** | | | | | | | | |
| Dynamic Range | A-weighted | 93 | 99 | - | 90 | 96 | - | dB |
| | unweighted | 90 | 96 | - | 87 | 93 | - | dB |
| Total Harmonic Distortion + Noise | -1 dBFS | - | -86 | -80 | - | -84 | -78 | dB |
| | -20 dBFS | - | -76 | - | - | -73 | - | dB |
| | -60 dBFS | - | -36 | - | - | -33 | - | dB |
| ***Analog In to PGA to ADC*** | | | | | | | | |
| ***Dynamic Range*** | | | | | | | | |
| PGA Setting: 0 dB | A-weighted | 92 | 98 | - | 89 | 95 | - | dB |
| | unweighted | 89 | 95 | - | 86 | 92 | - | dB |
| PGA Setting: +12 dB | A-weighted | 85 | 91 | - | 82 | 88 | - | dB |
| | unweighted | 82 | 88 | - | 79 | 85 | - | dB |
| Total Harmonic Distortion + Noise | | | | | | | | |
| PGA Setting: 0 dB | -1 dBFS | - | -88 | -81 | - | -86 | -80 | dB |
| | -60 dBFS | - | -35 | - | - | -32 | - | dB |
| PGA Setting: +12 dB | -1 dBFS | - | -85 | -79 | - | -83 | -77 | dB |
| ***Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC*** | | | | | | | | |
| ***Dynamic Range*** | | | | | | | | |
| PGA Setting: 0 dB | A-weighted | - | 86 | - | - | 83 | - | dB |
| | unweighted | - | 83 | - | - | 80 | - | dB |
| Total Harmonic Distortion + Noise | | | | | | | | |
| PGA Setting: 0 dB | -1 dBFS | - | -76 | - | - | -74 | - | dB |
| ***Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC*** | | | | | | | | |
| ***Dynamic Range*** | | | | | | | | |
| PGA Setting: 0 dB | A-weighted | - | 78 | - | - | 75 | - | dB |
| | unweighted | - | 74 | - | - | 71 | - | dB |
| Total Harmonic Distortion + Noise | | | | | | | | |
| PGA Setting: 0 dB | -1 dBFS | - | -74 | - | - | -71 | - | dB |
| ***Other Characteristics*** | | | | | | | | |
| DC Accuracy | | | | | | | | |
| Interchannel Gain Mismatch | | - | 0.2 | - | - | 0.2 | - | dB |
| Gain Drift | | - | ±100 | - | - | ±100 | - | ppm/°C |
| Offset Error | SDOUT Code with HPF On | - | 352 | - | - | 352 | - | LSB |
| Input | | | | | | | | |
| Interchannel Isolation | | - | 90 | - | - | 90 | - | dB |
| Full-scale Input Voltage | ADC | 0.74•VA | 0.78•VA | 0.82•VA | 0.74•VA | 0.78•VA | 0.82•VA | Vpp |
| | PGA (0 dB) | 0.75•VA | 0.794•VA | 0.83•VA | 0.75•VA | 0.794•VA | 0.83•VA | Vpp |
| | MIC (+16 dB) | | 0.129•VA | | | 0.129•VA | | Vpp |
| | MIC (+32 dB) | | 0.022•VA | | | 0.022•VA | | Vpp |
| Input Impedance (Note 5) | ADC | - | 20 | - | - | 20 | - | kΩ |
| | PGA | - | 39 | - | - | 39 | - | kΩ |
| | MIC | - | 50 | - | - | 50 | - | kΩ |

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. Measured between AINxx and AGND.

## ANALOG CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

| Parameter (Note 4) | | VA = 2.5 V (nominal) Min | Typ | Max | VA = 1.8 V (nominal) Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ***Analog In to ADC*** | | | | | | | | |
| Dynamic Range | A-weighted | 91 | 99 | - | 88 | 96 | - | dB |
| | unweighted | 78 | 96 | - | 85 | 93 | - | dB |
| Total Harmonic Distortion + Noise | -1 dBFS | - | -86 | -78 | - | -84 | -76 | dB |
| | -20 dBFS | - | -76 | - | - | -73 | - | dB |
| | -60 dBFS | - | -36 | - | - | -33 | - | dB |
| ***Analog In to PGA to ADC*** | | | | | | | | |
| ***Dynamic Range*** | | | | | | | | |
| PGA Setting: 0 dB | A-weighted | 90 | 98 | - | 87 | 95 | - | dB |
| | unweighted | 87 | 95 | - | 84 | 92 | - | dB |
| PGA Setting: +12 dB | A-weighted | 83 | 91 | - | 80 | 88 | - | dB |
| | unweighted | 80 | 88 | - | 77 | 85 | - | dB |
| Total Harmonic Distortion + Noise | | | | | | | | |
| PGA Setting: 0 dB | -1 dBFS | - | -88 | -80 | - | -86 | -78 | dB |
| | -60 dBFS | - | -35 | - | - | -32 | - | dB |
| PGA Setting: +12 dB | -1 dBFS | - | -85 | -77 | - | -83 | -75 | dB |
| ***Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC*** | | | | | | | | |
| ***Dynamic Range*** | | | | | | | | |
| PGA Setting: 0 dB | A-weighted | - | 86 | - | - | 83 | - | dB |
| | unweighted | - | 83 | - | - | 80 | - | dB |
| Total Harmonic Distortion + Noise | | | | | | | | |
| PGA Setting: 0 dB | -1 dBFS | - | -76 | - | - | -74 | - | dB |
| ***Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC*** | | | | | | | | |
| ***Dynamic Range*** | | | | | | | | |
| PGA Setting: 0 dB | A-weighted | - | 78 | - | - | 75 | - | dB |
| | unweighted | - | 74 | - | - | 71 | - | dB |
| Total Harmonic Distortion + Noise | | | | | | | | |
| PGA Setting: 0 dB | -1 dBFS | - | -74 | - | - | -71 | - | dB |
| ***Other Characteristics*** | | | | | | | | |
| DC Accuracy | | | | | | | | |
| Interchannel Gain Mismatch | | - | 0.1 | - | - | 0.1 | - | dB |
| Gain Drift | | - | ±100 | - | - | ±100 | - | ppm/°C |
| Offset Error | SDOUT Code with HPF On | - | 352 | - | - | 352 | - | LSB |
| Input | | | | | | | | |
| Interchannel Isolation | | - | 90 | - | - | 90 | - | dB |
| Full-scale Input Voltage | ADC | 0.74•VA | 0.78•VA | 0.82•VA | 0.74•VA | 0.78•VA | 0.82•VA | Vpp |
| | PGA (0 dB) | 0.75•VA | 0.794•VA | 0.83•VA | 0.75•VA | 0.794•VA | 0.83•VA | Vpp |
| | MIC (+16 dB) | | 0.129•VA | | | 0.129•VA | | Vpp |
| | MIC (+32 dB) | | 0.022•VA | | | 0.022•VA | | Vpp |
| Input Impedance (Note 5) | ADC | 18 | - | - | 18 | - | - | kΩ |
| | PGA | 40 | - | - | 40 | - | - | kΩ |
| | MIC | 50 | - | - | 50 | - | - | kΩ |

## ADC DIGITAL FILTER CHARACTERISTICS

| Parameter (Note 6) | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Passband (Frequency Response) | to -0.1 dB corner | 0 | - | 0.46 | Fs |
| Passband Ripple | | -0.09 | - | 0.17 | dB |
| Stopband | | 0.6 | - | - | Fs |
| Stopband Attenuation | | 33 | - | - | dB |
| Total Group Delay | | - | 7.6/Fs | - | s |
| ***High-Pass Filter Characteristics (48 kHz Fs)*** | | | | | |
| Frequency Response | -3.0 dB<br>-0.13 dB | -<br>- | 3.7<br>24.2 | -<br>- | Hz<br>Hz |
| Phase Deviation | @ 20 Hz | - | 10 | - | Deg |
| Passband Ripple | | - | - | 0.17 | dB |
| Filter Settling Time | | - | $10^5$/Fs | 0 | s |

6. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 23 to 26) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

## SWITCHING SPECIFICATIONS - SERIAL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT $C_{LOAD}$ = 15 pF.)

| Parameters | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ pin Low Pulse Width | (Note 7) | | 1 | - | ms |
| MCLK Frequency | | | 1.024 | 38.4 | MHz |
| MCLK Duty Cycle | (Note 8) | | 45 | 55 | % |
| ***Slave Mode*** | | | | | |
| Input Sample Rate (LRCK) | Quarter-Speed Mode<br>Half-Speed Mode<br>Single-Speed Mode<br>Double-Speed Mode | $F_s$<br>$F_s$<br>$F_s$<br>$F_s$ | 4<br>8<br>4<br>50 | 12.5<br>25<br>50<br>100 | kHz<br>kHz<br>kHz<br>kHz |
| LRCK Duty Cycle | | | 45 | 55 | % |
| SCLK Frequency | | $1/t_P$ | - | $64 \cdot F_s$ | Hz |
| SCLK Duty Cycle | | | 45 | 55 | % |
| LRCK Setup Time Before SCLK Rising Edge | | $t_{s(LK-SK)}$ | 40 | - | ns |
| LRCK Edge to SDOUT MSB Output Delay | | $t_{d(MSB)}$ | - | 52 | ns |
| SDOUT Setup Time Before SCLK Rising Edge | | $t_{s(SDO-SK)}$ | 20 | - | ns |
| SDOUT Hold Time After SCLK Rising Edge | | $t_{h(SK-SDO)}$ | 30 | - | ns |

| Parameters | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| ***Master Mode*** (Note 9) | | | | | |
| Output Sample Rate (LRCK) | All Speed Modes (Note 10) | $F_s$ | - | $\frac{MCLK}{128}$ | Hz |
| LRCK Duty Cycle | | | 45 | 55 | % |
| SCLK Frequency | | $1/t_P$ | - | $64 \cdot F_s$ | Hz |
| SCLK Duty Cycle | | | 45 | 55 | % |
| LRCK Edge to SDOUT MSB Output Delay | | $t_{d(MSB)}$ | - | 52 | ns |
| SDOUT Setup Time Before SCLK Rising Edge | | $t_{s(SDO-SK)}$ | 20 | - | ns |
| SDOUT Hold Time After SCLK Rising Edge | | $t_{h(SK-SDO)}$ | 30 | - | ns |

7. After powering up the CS53L21, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
8. See "Example System Clock Frequencies" on page 51 for typical MCLK frequencies.
9. See"Master" on page 29.
10. "MCLK" refers to the external master clock applied.

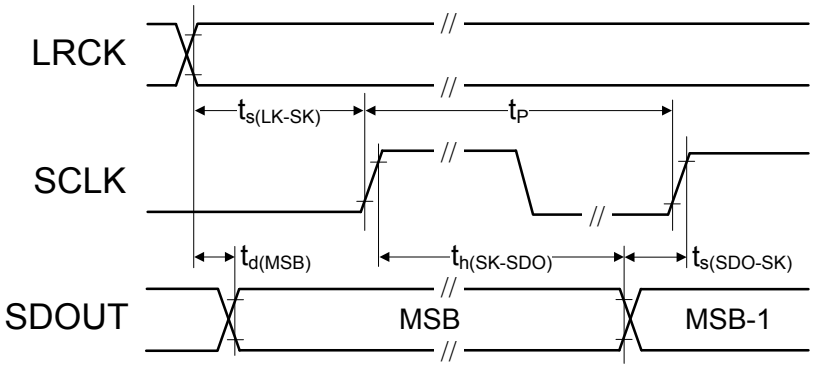



**Figure 3. Serial Audio Interface Slave Mode Timing**

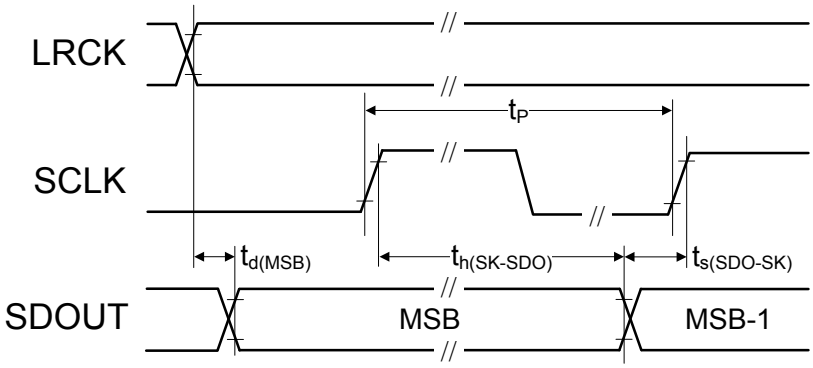



**Figure 4. Serial Audio Interface Master Mode Timing**

## SWITCHING SPECIFICATIONS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA $C_L$ = 30 pF)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| SCL Clock Frequency | $f_{scl}$ | - | 100 | kHz |
| $\overline{\text{RESET}}$ Rising Edge to Start | $t_{irs}$ | 500 | - | ns |
| Bus Free Time Between Transmissions | $t_{buf}$ | 4.7 | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | $t_{hdst}$ | 4.0 | - | µs |
| Clock Low time | $t_{low}$ | 4.7 | - | µs |
| Clock High Time | $t_{high}$ | 4.0 | - | µs |
| Setup Time for Repeated Start Condition | $t_{sust}$ | 4.7 | - | µs |
| SDA Hold Time from SCL Falling (Note 11) | $t_{hdd}$ | 0 | - | µs |
| SDA Setup time to SCL Rising | $t_{sud}$ | 250 | - | ns |
| Rise Time of SCL and SDA | $t_{rc}$ | - | 1 | µs |
| Fall Time SCL and SDA | $t_{fc}$ | - | 300 | ns |
| Setup Time for Stop Condition | $t_{susp}$ | 4.7 | - | µs |
| Acknowledge Delay from SCL Falling | $t_{ack}$ | 300 | 3450 | ns |

11. Data must be held for sufficient time to bridge the transition time, $t_{fc}$, of SCL.

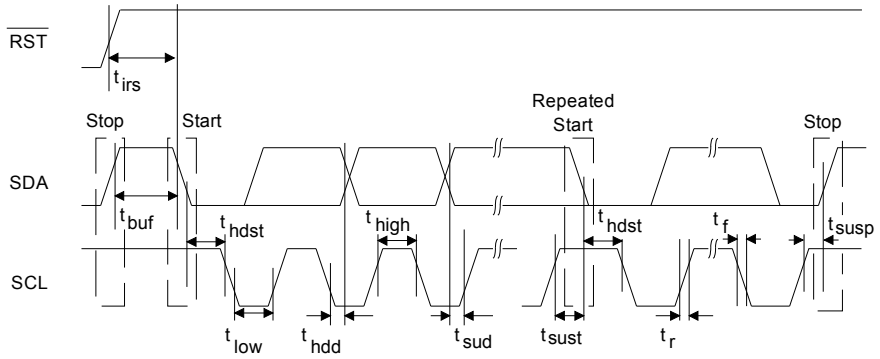



**Figure 5. Control Port Timing - I²C**

## SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

| Parameter | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| CCLK Clock Frequency | | $f_{sck}$ | 0 | 6.0 | MHz |
| $\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling | | $t_{srs}$ | 20 | - | ns |
| $\overline{\text{CS}}$ Falling to CCLK Edge | | $t_{css}$ | 20 | - | ns |
| $\overline{\text{CS}}$ High Time Between Transmissions | | $t_{csh}$ | 1.0 | - | µs |
| CCLK Low Time | | $t_{scl}$ | 66 | - | ns |
| CCLK High Time | | $t_{sch}$ | 66 | - | ns |
| CDIN to CCLK Rising Setup Time | | $t_{dsu}$ | 40 | - | ns |
| CCLK Rising to DATA Hold Time | (Note 12) | $t_{dh}$ | 15 | - | ns |
| Rise Time of CCLK and CDIN | (Note 13) | $t_{r2}$ | - | 100 | ns |
| Fall Time of CCLK and CDIN | (Note 13) | $t_{f2}$ | - | 100 | ns |

12. Data must be held for sufficient time to bridge the transition time of CCLK.
13. For $f_{sck}$ <1 MHz.

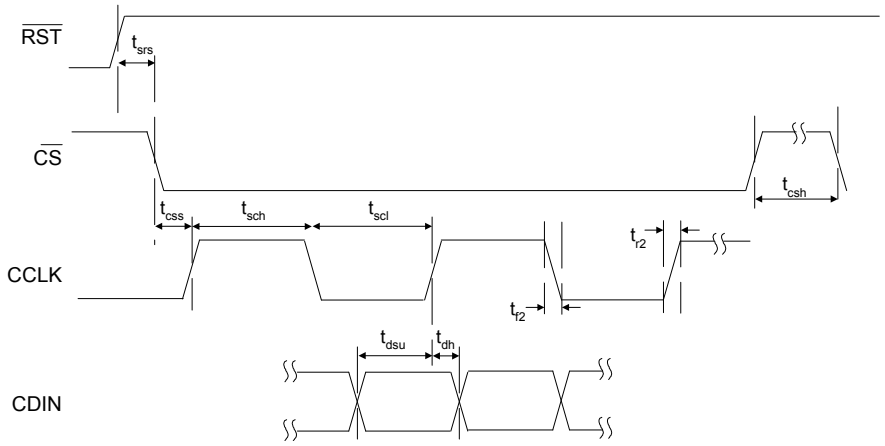



**Figure 6. Control Port Timing - SPI Format**

## DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

| Parameters | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***VQ Characteristics*** | | | | | |
| Nominal Voltage | | - | 0.5•VA | - | V |
| Output Impedance | | - | 23 | - | kΩ |
| DC Current Source/Sink (Note 14) | | - | - | 10 | µA |
| FILT+ | | - | VA | - | V |
| ***MIC BIAS Characteristics*** | | | | | |
| Nominal Voltage | MICBIAS_LVL[1:0] = 00 | - | 0.8•VA | - | V |
| | MICBIAS_LVL[1:0] = 01 | - | 0.7•VA | - | V |
| | MICBIAS_LVL[1:0] = 10 | - | 0.6•VA | - | V |
| | MICBIAS_LVL[1:0] = 11 | - | 0.5•VA | - | V |
| DC Current Source | | - | - | 1 | mA |
| Power Supply Rejection Ratio (PSRR) | 1 kHz | - | 50 | - | dB |
| Power Consumption (Normal Operation Worse Case) | 1 kHz | - | - | 30 | mW |
| **Power Supply Rejection Ratio (PSRR)** (Note 15) | 1 kHz | - | 60 | - | dB |

14. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.
15. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

## DIGITAL INTERFACE SPECIFICATIONS AND CHARACTERISTICS

| Parameters (Note 16) | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input Leakage Current | $I_{in}$ | - | ±10 | µA |
| Input Capacitance | | - | 10 | pF |
| 1.8 V - 3.3 V Logic | | | | |
| High-Level Output Voltage ($I_{OH}$ = -100 µA) | $V_{OH}$ | VL - 0.2 | - | V |
| Low-Level Output Voltage ($I_{OL}$ = 100 µA) | $V_{OL}$ | - | 0.2 | V |
| High-Level Input Voltage | $V_{IH}$ | 0.68•VL | - | V |
| Low-Level Input Voltage | $V_{IL}$ | - | 0.32•VL | V |

16. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

## POWER CONSUMPTION

See (Note 17)

| | Operation | Power Control. Registers 02h Reserved bit 6 | Reserved bit 5 | PDN_PGAB | PDN_PGAA | PDN_ADCB | PDN_ADCA | PDN | 03h PDN_MICB | PDN_MICA | PDN_MICBIAS | V | | Typical Current (mA) $i_{VA}$ | $i_{VD}$ | $i_{VL}$ (Note 18) | Total Power ($mW_{rms}$) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Off (Note 19) | x | x | x | x | x | x | x | x | x | x | 1.8 | | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | | 2.5 | | 0 | 0 | 0 | 0 |
| 2 | Standby (Note 20) | x | x | x | x | x | x | 1 | x | x | x | 1.8 | | 0.01 | 0.02 | 0 | 0.05 |
| | | | | | | | | | | | | 2.5 | | 0.01 | 0.03 | 0 | 0.10 |
| 3 | Mono Record ADC | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1.8 | | 1.85 | 2.03 | 0.03 | 7.05 |
| | | | | | | | | | | | | 2.5 | | 2.07 | 3.05 | 0.05 | 12.94 |
| | PGA to ADC | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.8 | | 2.35 | 2.03 | 0.03 | 7.95 |
| | | | | | | | | | | | | 2.5 | | 2.58 | 3.08 | 0.05 | 14.29 |
| | MIC to PGA to ADC (with Bias) | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.8 | | 3.67 | 2.05 | 0.03 | 10.36 |
| | | | | | | | | | | | | 2.5 | | 3.95 | 3.09 | 0.05 | 17.71 |
| | MIC to PGA to ADC (no Bias) | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.8 | | 3.27 | 2.03 | 0.03 | 9.61 |
| | | | | | | | | | | | | 2.5 | | 3.52 | 3.08 | 0.05 | 16.62 |
| 4 | Stereo Record ADC | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.8 | | 2.69 | 2.12 | 0.03 | 8.72 |
| | | | | | | | | | | | | 2.5 | | 2.93 | 3.18 | 0.04 | 15.40 |
| | PGA to ADC | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.8 | | 3.65 | 2.12 | 0.03 | 10.45 |
| | | | | | | | | | | | | 2.5 | | 3.91 | 3.17 | 0.04 | 17.84 |
| | MIC to PGA to ADC (no Bias) | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.8 | | 5.48 | 2.11 | 0.03 | 13.73 |
| | | | | | | | | | | | | 2.5 | | 5.76 | 3.17 | 0.04 | 22.45 |

17. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.
18. VL current will slightly increase in master mode.
19. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
20. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.

# 4. APPLICATIONS

## 4.1 Overview

### *4.1.1 Architecture*

The CS53L21 is a highly integrated, low power, 24-bit audio A/D. The ADC operates at 64Fs, where Fs is equal to the system sample rate. The different clock rates maximize power savings while maintaining high performance. The A/D operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

### *4.1.2 Line and MIC Inputs*

The analog input portion of the A/D allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Six line inputs with configuration for two MIC inputs (or one MIC input with common mode rejection), two MIC bias outputs and independent channel control (including a high-pass filter disable function) are available. A Programmable Gain Amplifier (PGA), MIC boost, and Automatic Level Control (ALC), with noise gate settings, provide analog gain and adjustment. Digital volume controls, including gain, boost, attenuation and inversion are also available.

### *4.1.3 Signal Processing Engine*

The ADC data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps.

### *4.1.4 Device Control (Hardware or Software Mode)*

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

### *4.1.5 Power Management*

Two Software Mode control registers provide independent power-down control of the ADC, PGA, MIC preamp and MIC bias, allowing operation in select applications with minimal power consumption.

## 4.2 Hardware Mode

A limited feature set is available when the A/D powers up in Hardware Mode (see "Recommended Power-Up Sequence" on page 30) and may be controlled via stand-alone control pins. Table 2 shows a list of functions/features, the default configuration and the associated stand-alone control available.

| Hardware Mode Feature/Function Summary | | | | |
|---|---|---|---|---|
| **Feature/Function** | | **Default Configuration** | **Stand-Alone Control** | **Note** |
| Power Control | Device<br>PGAx<br>ADCx<br>MIC Bias<br>MICx Preamp | Powered Up<br>Powered Up<br>Powered Up<br>Powered Down<br>Powered Down | - | - |
| Auto-Detect | | Enabled | - | - |
| Speed Mode | Serial Port Slave<br>Serial Port Master | Auto-Detect Speed Mode<br>Single-Speed Mode | - | - |
| MCLK Divide | | (Selectable) | "MCLKDIV2" pin 2 | see Section 4.5 on page 28 |
| Serial Port Master / Slave Selection | | (Selectable) | "M/$\overline{S}$" pin 29 | see Section 4.5 on page 28 |
| Interface Control | ADC | (Selectable) | "I²S/$\overline{LJ}$" pin 3 | see Section 4.6 on page 30 |
| ADC Volume and Gain | Digital Boost<br>Soft Ramp<br>Zero Cross<br>Invert<br>PGAx<br>Attenuator<br>ALC<br>Noise Gate | Disabled<br>Disabled<br>Disabled<br>Disabled<br>0 dB<br>0 dB<br>Disabled<br>Disabled | - | - |
| ADCx High-Pass Filter<br>ADCx High-Pass Filter Freeze | | Enabled<br>Continuous DC Subtraction | - | - |
| Line/MIC Input Select | | AIN1A to PGAA<br>AIN1B to PGAB | - | - |
| ADC mix Volume and Gain | Invert<br>Soft Ramp<br>Zero Cross | Disabled<br>Enabled<br>Enabled | - | - |
| Signal Processing Engine (SPE) | MIX | Disabled | - | - |
| Data Selection (SPE Enable) | | ADC Data to SPE | - | - |
| Channel Swap | ADC | ADCA = L; ADCB = R | - | - |

**Table 2. Hardware Mode Feature Summary**

## 4.3 Analog Inputs

AINxA and AINxB are the analog inputs, internally biased to VQ, that accepts line-level and MIC-level signals, allowing various gain and signal adjustments for each channel.

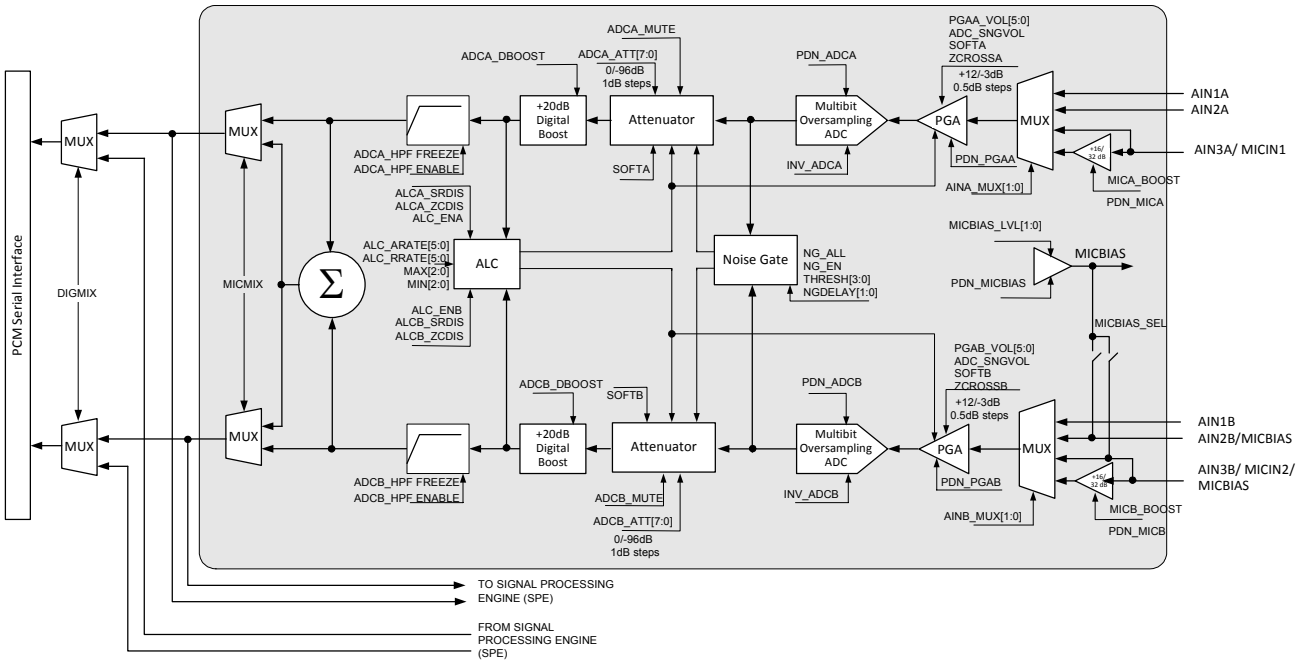



**Figure 7. Analog Input Architecture**

### 4.3.1 Digital Code, Offset and DC Measurement

The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively and cause the ADC overflow bit to be set to a '1'.

Given the two's complement format, low-level signals may cause the MSB of the serial data to periodically toggle between '1' and '0', possibly introducing noise into the system as the bit switches back and forth. To prevent this phenomena, a constant DC offset is added to the serial data bringing the low-level signal just above the point at which the MSB would normally toggle, thus reducing the noise introduced. Note that this offset is not removed (refer to "Analog Characteristics (Commercial - CNZ)" on page 12 and/or "Analog Characteristics (Automotive - DNZ)" on page 13 for the specified offset level).

The A/D may be used to measure DC voltages by disabling the high-pass filter for the designated channel. DC levels are measured relative to VQ and will be decoded as positive two's complement binary numbers above VQ and negative two's complement binary numbers below VQ.

| | |
|---|---|
| Software Controls: | "Status (Address 20h) (Read Only)" on page 50, "ADC Control (Address 06h)" on page 41. |

### 4.3.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is “frozen” during normal operation, the current value of the DC offset for the corresponding channel is held. It is this DC offset that will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the A/D with the high-pass filter enabled and the DC offset not “frozen” until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Freezing the DC offset.

The high-pass filters are controlled using the ADCx_HPFRZ and ADCx_HPFEN bits.

If a particular ADC channel is used to measure DC voltages, the high-pass filter may be disabled using the ADCx_HPFEN bit.

| | |
|---|---|
| Software Controls: | “ADC Control (Address 06h)” on page 41. |

### 4.3.3 Digital Routing

The digital output of the ADC may be internally routed to the Signal Processing Engine (SPE). ADC output volume may be controlled using the ADCMIX [6:0] bits, and channel swaps can be done using the ADCA[1:0] and ADCB[1:0] bits. This “processed” ADC data can be selected for output in place of the ADC output data using the DIGMIX bit.

| | |
|---|---|
| Software Controls: | “ADCx Mixer Volume Control: ADCA (Address 0Eh) and ADCB (Address 0Fh)” on page 46, “Interface Control (Address 04h)” on page 39. |

### 4.3.4 Differential Inputs

The stereo pair inputs act as a single differential input when the MICMIX bit is enabled. This provides common mode rejection of noise in digitally intense PCBs, where the microphone signal traverses long traces, or across long microphone cables as illustrated in Figure 8.

Since the mixer provides a differential combination of the two signals, the potential input mix may exceed the maximum full-scale input and result in clipping. The level out of the mixer, therefore, is automatically attenuated 6 dB. Gain may be applied using either the analog PGA or MIC preamp or the digital ADCMIX volume control to readjust a small signal to desired levels.

The analog inputs may also be used as a differential input pair as illustrated in Figure 9. The two channels are differentially combined when the MICMIX bit is enabled.

#### 4.3.4.1 External Passive Components

The microphone input is internally biased to VQ. Input signals must be AC coupled using external capacitors with values consistent with the desired high-pass filter design. The MICINx input resistance of 50 kW may be combined with an external capacitor of 1 mF to achieve the cutoff frequency defined by the equation,

$$fc = \frac{1}{2\pi(50\ k\Omega)(1\ \mu F)} = 3.18\ Hz$$

An electrolytic capacitor must be placed such that the positive terminal is positioned relative to the side with the greater bias voltage. The MICBIAS voltage level is controlled by the MICBIAS_LVL[1:0] bits.

The MICBIAS series resistor must be selected based on the requirements of the particular microphone used. The MICBIAS output pin is selected using the MICBIAS_SEL bit.

| | |
|---|---|
| Software Controls: | "Interface Control (Address 04h)" on page 39, "MIC Control (Address 05h)" on page 40. |

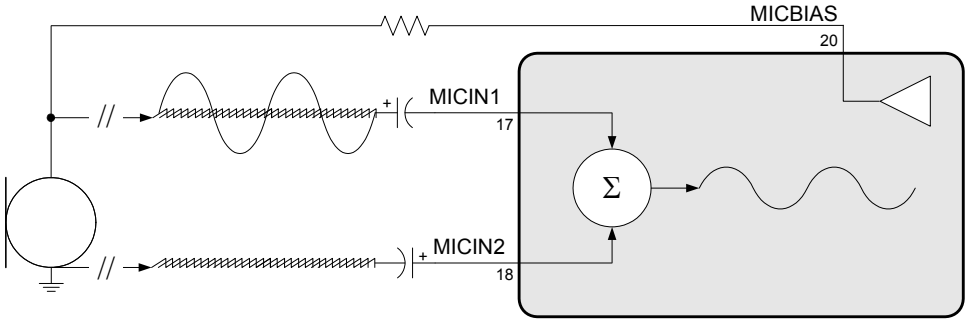



**Figure 8. MIC Input Mix w/Common Mode Rejection**

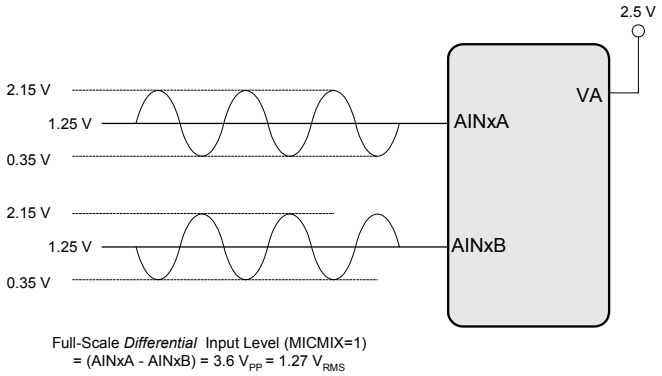



**Figure 9. Differential Input**

### 4.3.5 *Analog Input Multiplexer*

A stereo 4-to-1 analog input multiplexer selects between a line-level input source, or a mic-level input source, depending on the PDN_PGAx and AINx_MUX[1:0] bit settings. Signals may be routed to or by-passed around the PGA. To conserve power, the PGAs may be powered down allowing the user to select from multiple line-level sources and route the stereo signal directly to the ADC. When using the MIC pre-amp, however, the PGA must be powered up.

Analog input channel B may also be used as an output for the MIC bias voltage. The MICBIAS_SEL bit routes the bias voltage to either of two pins. The multiplexer must then select from the remainder of the two input channels.

Each ADC, PGA and MIC preamp has an associated input resistance. When selecting between these paths, the input resistance to the A/D will change accordingly. Refer to the input resistance characteristics in the Characteristic and Specification Tables for the input resistance of each path.

| | |
|---|---|
| Software Controls: | "Power Control 1 (Address 02h)" on page 36, "MIC Control (Address 05h)" on page 40 "ADCx Input Select, Invert and Mute (Address 07h)" on page 42. |

### 4.3.6 MIC and PGA Gain

The MIC-level input passes through a +16 dB or +32 dB analog gain stage prior to the input multiplexer, allowing it to be used for microphone level signals without the need for any external gain. The PGA must be powered up when using the MIC preamp.

The PGA stage provides an additional +12 dB to -3 dB of analog gain in 0.5 dB steps.

| | |
|---|---|
| Software Controls: | "Power Control 1 (Address 02h)" on page 36, "ADCx Input Select, Invert and Mute (Address 07h)" on page 42, "ALCX and PGAX Control: ALCA, PGAA (Address 0Ah) and ALCB, PGAB (Address 0Bh)" on page 45, "MIC Control (Address 05h)" on page 40. |

### 4.3.7 Automatic Level Control (ALC)

When enabled, the ALC monitors the analog input signal after the digital attenuator, detects when peak levels exceed the maximum threshold settings and lowers, first, the PGA gain settings and then increases the digital attenuation levels at a programmable attack rate and maintains the resulting level below the maximum threshold.

When input signal levels fall below the minimum threshold, digital attenuation levels are decreased first and the PGA gain is then increased at a programmable release rate and maintains the resulting level above the minimum threshold.

Attack and release rates are affected by the ADC soft ramp/zero cross settings and sample rate, Fs. ALC soft ramp and zero cross dependency may be independently enabled/disabled.

*Recommended settings*: Best level control may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. **Note: 1.)** The maximum realized gain must be set in the PGAx_VOL register. The ALC will only apply the gain set in the PGAx_VOL. **2.)** The ALC maintains the output signal between the MIN and MAX thresholds. As the input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

| | |
|---|---|
| Software Controls: | "ALC Enable and Attack Rate (Address 1Ch)" on page 47, "ALC Release Rate (Address 1Dh)" on page 48, "ALC Threshold (Address 1Eh)" on page 48, "ALCX and PGAX Control: ALCA, PGAA (Address 0Ah) and ALCB, PGAB (Address 0Bh)" on page 45. |

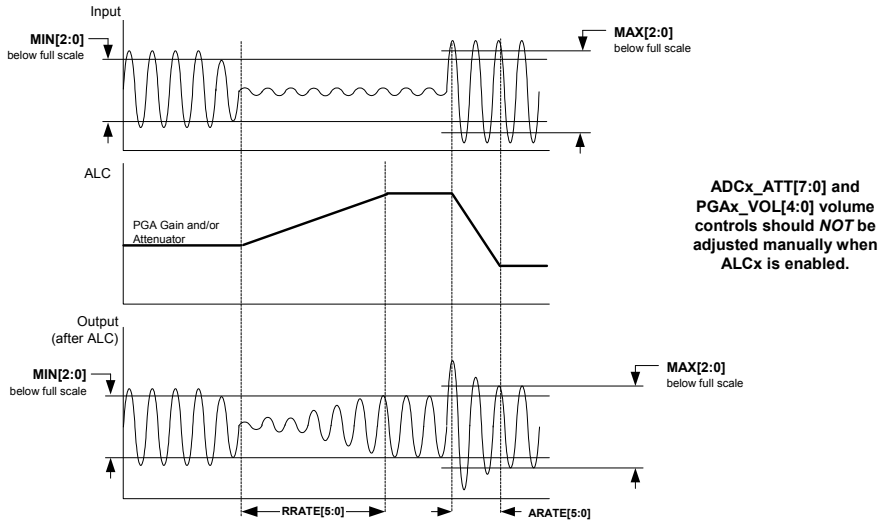



**Figure 10. ALC**

### 4.3.8 Noise Gate

The noise gate may be used to mute signal levels that fall below a programmable threshold. This prevents the ALC from applying gain to noise. A programmable delay may be used to set the minimum time before the noise gate attacks the signal.

Maximum noise gate attenuation levels will depend on the gain applied in either the PGA or MIC preamp. For example: If both +32 dB preamplification and +12 dB programmable gain is applied, the maximum attenuation that the noise gate achieves will be 52 dB (-96 + 32 + 12) below full-scale.

Ramp-down time to the maximum setting is affected by the SOFTx bit.

*Recommended settings*: For best results, enable soft ramp for the digital attenuator. When the analog inputs are configured for differential signals (see "Differential Inputs" on page 23"Differential Inputs" on page 23), enable the NG_ALL bit to trigger the noise gate only when *both* inputs fall below the threshold.

| | |
|---|---|
| Software Controls: | "Noise Gate Configuration and Misc. (Address 1Fh)" on page 49, "ADC Control (Address 06h)" on page 41. |

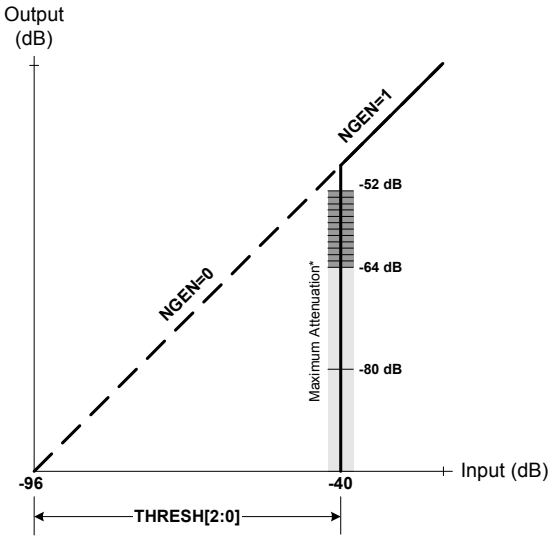



**Figure 11. Noise Gate Attenuation**

## 4.4 Signal Processing Engine

The SPE provides various signal processing functions that apply to the ADC data.

| | |
|---|---|
| Software Controls: | "SPE Control (Address 09h)" on page 43 |

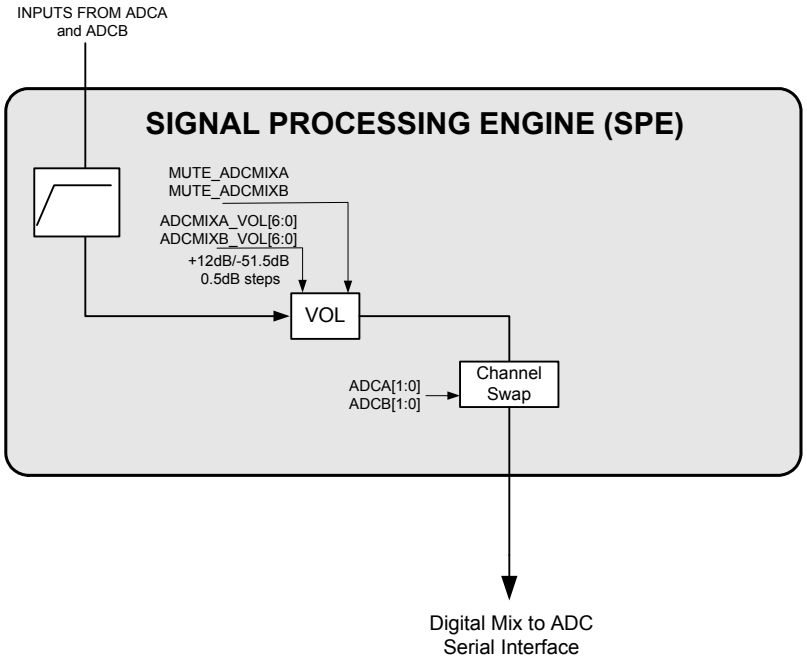



**Figure 12. Signal Processing Engine**

### *4.4.1 Volume Controls*

The digital volume control functions offer independent control over the ADC signal path into the mixer. The volume controls are programmable to ramp in increments of 0.125 dB at a rate controlled by the soft ramp/zero cross settings.

The signal paths may also be muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the SPE_SZC[1:0] bits.

| | |
|---|---|
| Software Controls: | "ADCx Mixer Volume Control: ADCA (Address 0Eh) and ADCB (Address 0Fh)" on page 46 |

### *4.4.2 Mono Channel Mixer*

A channel mixer may be used to create a mix of the left and right channels for the ADC data. This mix allows the user to produce a MONO signal from a stereo source. The mixer may also be used to implement a left/right channel swap.

| | |
|---|---|
| Software Controls: | "Channel Mixer (Address 18h)" on page 47. |

## 4.5 Serial Port Clocking

The A/D serial audio interface port operates either as a slave or master. It accepts externally generated clocks in slave mode and will generate synchronous clocks derived from an input master clock (MCLK) in master mode.

The frequency of the MCLK must be an integer multiple of, and synchronous with, the system sample rate, Fs. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device.

The SPEED and MCLKDIV2 software control bits or the SDOUT/(M/$\overline{S}$) and MCLKDIV2 stand-alone control pins, configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. The value on the SDOUT pin is latched immediately after powering up in Hardware Mode.

| | | | |
|---|---|---|---|
| **Software Control:** | "MIC Power Control and Speed Control (Address 03h)" on page 37, "SPE Control (Address 09h)" on page 43. | | |
| **Hardware Control:** | **Pin** | **Setting** | **Selection** |
| | "SDOUT, M/$\overline{S}$" pin 29 | 47 kΩ Pull-down | Slave |
| | | 47 kΩ Pull-up | Master |
| | "MCLKDIV2" pin 2 | LO | No Divide |
| | | HI | MCLK is divided by 2 prior to all internal circuitry. |

### *4.5.1 Slave*

LRCK and SCLK are inputs in Slave Mode. The speed of the A/D is automatically determined based on the input MCLK/LRCK ratio when the Auto-Detect function is enabled. Certain input clock ratios will then require an internal divide-by-two of MCLK* using either the MCLKDIV2 bit or the MCLKDIV2 stand-alone control pin.

Additional clock ratios are allowed when the Auto-Detect function is disabled; but the appropriate speed mode must be selected using the SPEED[1:0] bits.

| Auto-Detect | QSM | HSM | SSM | DSM |
|---|---|---|---|---|
| Disabled (Software Mode only) | 512, 768, 1024, 1536, 2048, 3072 | 256, 384, 512, 768, 1024, 1536 | 128, 192, 256, 384, 512, 768 | 128, 192, 256, 384 |
| Enabled | 1024, 1536, 2048*, 3072* | 512, 768, 1024*, 1536* | 256, 384, 512*, 768* | 128, 192, 256*, 384* |

*MCLKDIV2 must be enabled.

**Table 3. MCLK/LRCK Ratios**

### 4.5.2 Master

LRCK and SCLK are internally derived from the internal MCLK (after the divide, if MCLKDIV2 is enabled). In Hardware Mode the A/D operates in single-speed only. In Software Mode, the A/D operates in either quarter-, half-, single- or double-speed depending on the setting of the SPEED[1:0] bits.

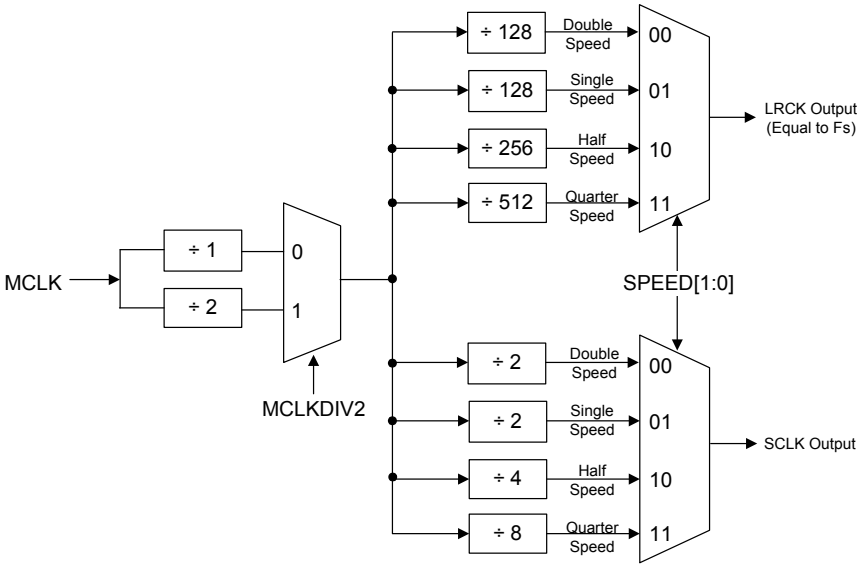



**Figure 13. Master Mode Timing**

### 4.5.3 High-Impedance Digital Output

The serial port may be placed on a clock/data bus that allows multiple masters for the serial port I/O without the need for external buffers. The 3ST_SP bit places the internal buffers for these I/O in a high-impedance state, allowing another device to transmit serial port data without bus contention.

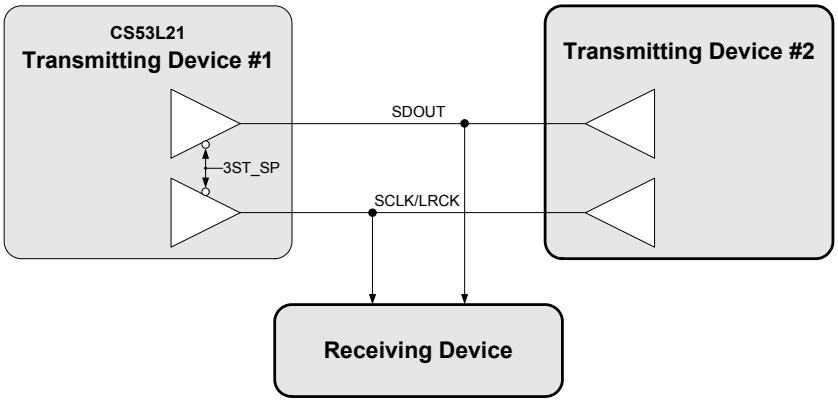



**Figure 14. Tri-State Serial Port**

### 4.5.4 Quarter- and Half-Speed Mode

Quarter-Speed Mode (QSM) and Half-Speed Mode (HSM) allow lower sample rates while maintaining a relatively flat noise floor in the typical audio band of 20 Hz - 20 kHz. Single-Speed Mode (SSM) will allow lower frequency sample rates.

## 4.6 Digital Interface Formats

The serial port operates in standard I²S or Left-Justified digital interface formats with varying bit depths from 16 to 24. Data is clocked out of the ADC or into the SPE on the rising edge of SCLK. Figures 15-16 illustrate the general structure of each format. Refer to "Switching Specifications - Serial Port" on page 14 for exact timing relationship between clocks and data.

| | | | |
|---|---|---|---|
| **Software Control:** | "Interface Control (Address 04h)" on page 39. | | |
| **Hardware Control:** | **Pin** | **Setting** | **Selection** |
| | "I²S/$\overline{LJ}$" pin 3 | LO | Left-Justified Interface |
| | | HI | I²S Interface |

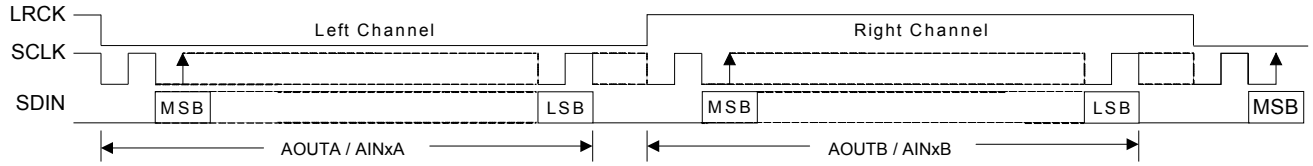



**Figure 15. I²S Format**

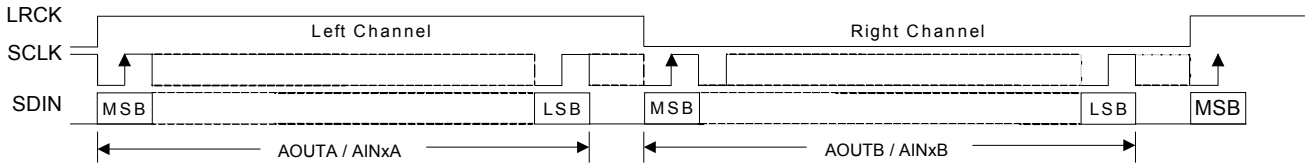



**Figure 16. Left-Justified Format**

## 4.7 Initialization

Figure 17 shows the initialization and power-down sequence. The A/D enters a Power-Down state on initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, ADC and switched-capacitor low-pass filters are powered down.

The device remains in the Power-Down state until $\overline{RESET}$ is brought high, at which point, the control port is accessible and the desired register settings can be loaded per the descriptions in Section 4.10. If a valid write sequence to the control port is not made within approximately 10 ms, the A/D enters Hardware Mode.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+ will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

## 4.8 Recommended Power-Up Sequence

1. Hold $\overline{RESET}$ low until the power supplies are stable.
2. Bring $\overline{RESET}$ high. After approximately 10 ms, the device will enter Hardware Mode.
3. For Software Mode operation, set the PDN bit to '1'b in under 10 ms. This places the device in "standby".
4. Load the desired register settings while keeping the PDN bit set to '1'b.
5. Start MCLK to the appropriate frequency, as discussed in Section 4.5. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the PDN bit to '0'b.
7. Bring $\overline{RESET}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

## 4.9 Recommended Power-Down Sequence

To minimize audible pops when turning off or placing the A/D in standby,

1. Mute the ADCs.
2. Set the PDN bit in the power control register to '1'b. The A/D will not power down until it reaches a fully muted sate. Do not remove MCLK until after the part has fully muted. Note that it may be necessary to disable the soft ramp and/or zero cross volume transitions to achieve faster muting/power down.
3. Bring $\overline{\text{RESET}}$ low.

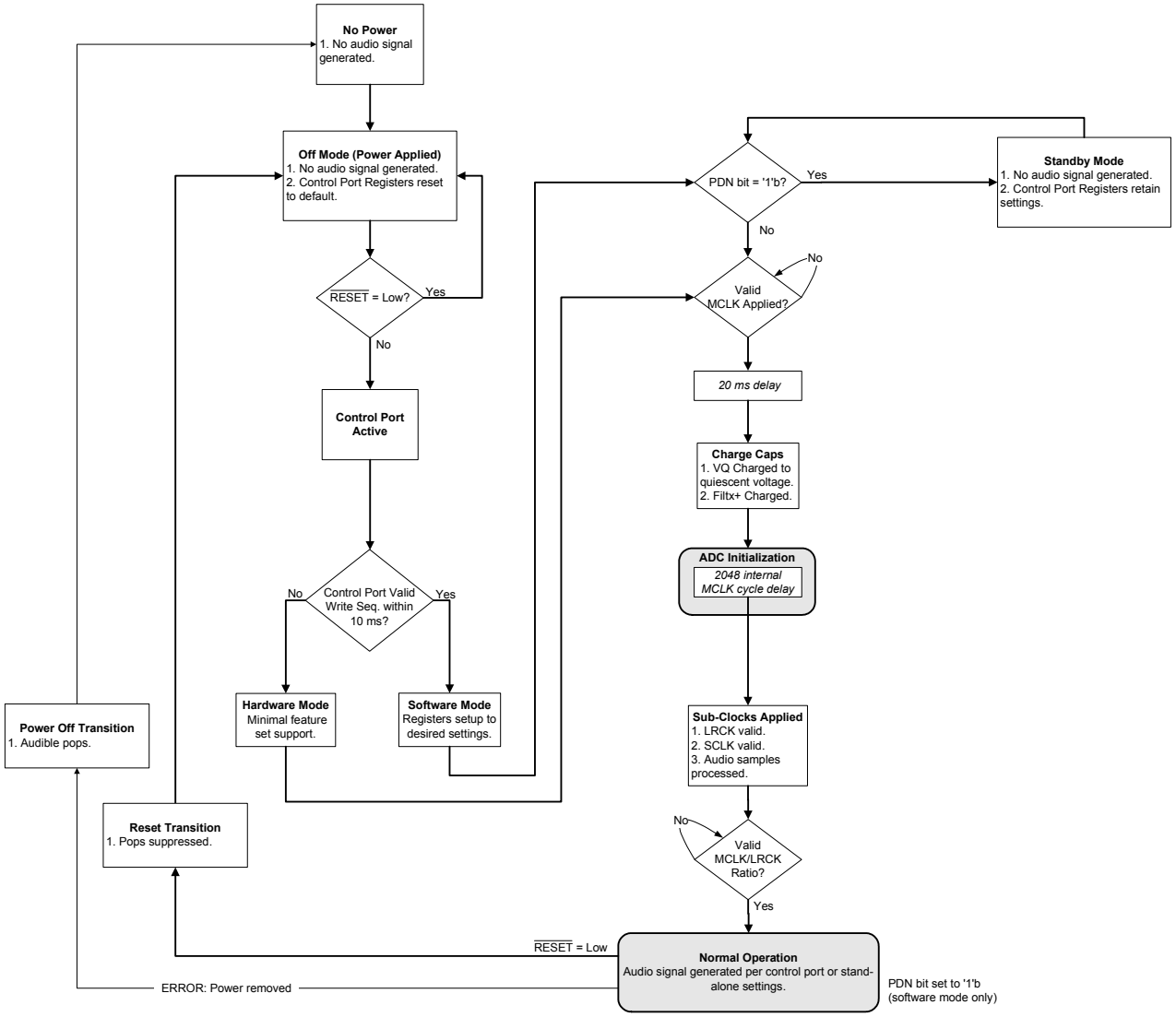



**Figure 17. Initialization Flow Chart**

## 4.10 Software Mode

The control port is used to access the registers allowing the A/D to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The device enters software mode only after a successful write command using either SPI or I²C protocol, with the device acting as a slave. The SPI protocol is permanently selected whenever there is a high-to-low transition on the AD0/CS pin after reset. If using the I²C protocol, pin AD0/CS should be permanently connected to either VL or GND; this option allows the user to slightly alter the chip address as desired.

### 4.10.1 SPI Control

In Software Mode, $\overline{CS}$ is the CS53L21 chip-select signal, CCLK is the control port bit clock (input into the CS53L21 from the microcontroller), CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The A/D will only support write operations. Read request will be ignored.

Figure 18 shows the operation of the control port in Software Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001010. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP autoincrement capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

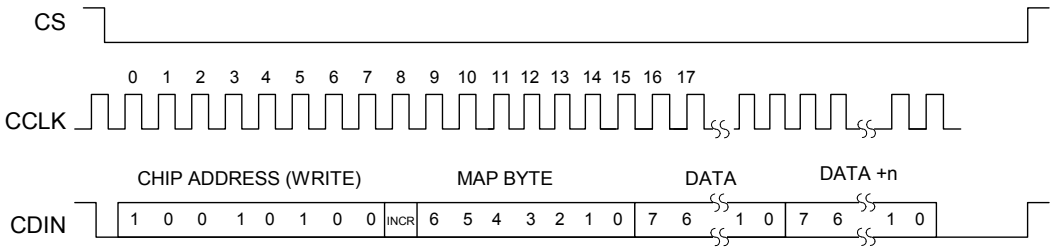



**Figure 18. Control Port Timing in SPI Mode**

### 4.10.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pin AD0 forms the least significant bit of the chip address and should be connected through a resistor to VL or DGND as desired. The pin's state is sensed while the CS53L21 is being reset.

The signal timings for a read and write cycle are shown in Figure 19 and Figure 20. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS53L21 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100101. To communicate with a CS53L21, the chip address field, which is the first byte sent to the CS53L21, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the autoincrement bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS53L21 after each input byte is read and is input to the CS53L21 from the microcontroller after each transmitted byte.

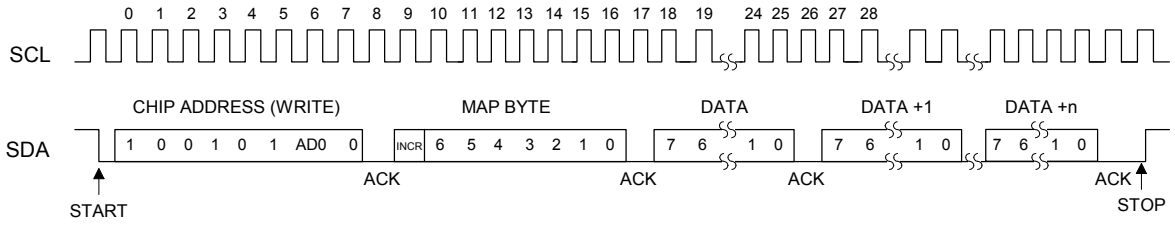



**Figure 19. Control Port Timing, I²C Write**

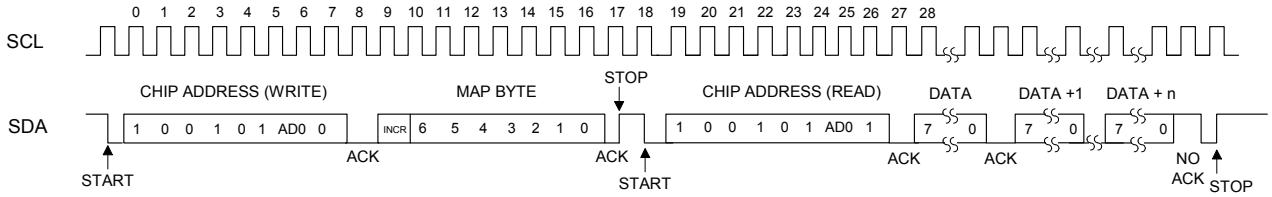



**Figure 20. Control Port Timing, I²C Read**

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 20, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 100101x0 (chip address and write operation).

Receive acknowledge bit.

Send MAP byte, autoincrement off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 100101x1 (chip address and read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the autoincrement bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

### *4.10.3 Memory Address Pointer (MAP)*

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

#### *4.10.3.1 Map Increment (INCR)*

The device has MAP autoincrement capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

# 5. REGISTER QUICK REFERENCE

Software mode register defaults are as shown. “Reserved” registers must maintain their default state.

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01h | ID | Chip_ID4 | Chip_ID3 | Chip_ID2 | Chip_ID1 | Chip_ID0 | Rev_ID2 | Rev_ID1 | Rev_ID0 |
| | p 36 default | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 02h | Power Ctl. 1 | Reserved | Reserved | Reserved | PDN_PGAB | PDN_PGAA | PDN_ADCB | PDN_ADCA | PDN |
| | p 36 default | 0 | 1(See Note 2 on page 36) | 1(See Note 2 on page 36) | 0 | 0 | 0 | 0 | 0 |
| 03h | Speed Ctl. & Power Ctl. 2 | AUTO | SPEED1 | SPEED0 | 3-ST_SP | PDN_MICB | PDN_MICA | PDN_ MICBIAS | MCLKDIV2 |
| | p 37 default | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 04h | Interface Ctl. | Reserved | M/S | Reserved | Reserved | Reserved | ADC_I²S/LJ | DIGMIX | MICMIX |
| | p 39 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05h | MIC Control & Misc. | ADC_SNGVOL | ADCB_ DBOOST | ADCA_ DBOOST | MICBIAS_ SEL | MICBIAS_ LVL1 | MICBIAS_ LVL0 | MICB_ BOOST | MICA_ BOOST |
| | p 40 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06h | ADC Control | ADCB_HPF EN | ADCB_HP FRZ | ADCA_HPF EN | ADCA_HP FRZ | SOFTB | ZCROSSB | SOFTA | ZCROSSA |
| | p 41 default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 07h | ADC Input Select, Invert, Mute | AINB_MUX1 | AINB_MUX0 | AINA_MUX1 | AINA_MUX0 | INV_ADCB | INV_ADCA | ADCB_ MUTE | ADCA_ MUTE |
| | p 42 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 09h | SPE Control | Reserved | SPE_ ENABLE | FREEZE | Reserved | Reserved | Reserved | SPE_SZC1 | SPE_SZC0 |
| | p 43 default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0Ah | ALCA SZC & PGAA Vol-ume | ALCA_SR DIS | ALCA_ZC DIS | Reserved | PGAA VOL4 | PGAA VOL3 | PGAA VOL2 | PGAA VOL1 | PGAA VOL0 |
| | p 45 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | ALCB SZC & PGAB Vol-ume | ALCB_SR DIS | ALCB_ZC DIS | Reserved | PGAB VOL4 | PGAB VOL3 | PGAB VOL2 | PGAB VOL1 | PGAB VOL0 |
| | p 45 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | ADCA Atten-uator | ADCA_ ATT7 | ADCA_ ATT6 | ADCA_ ATT5 | ADCA_ ATT4 | ADCA_ ATT3 | ADCA_ ATT2 | ADCA_ ATT1 | ADCA_ ATT0 |
| | p 46 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | ADCB Atten-uator | ADCB_ ATT7 | ADCB_ ATT6 | ADCB_ ATT5 | ADCB_ ATT4 | ADCB_ ATT3 | ADCB_ ATT2 | ADCB_ ATT1 | ADCB_ ATT0 |
| | p 46 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Eh | Vol. Control ADCMIXA | MUTE_ADC MIXA | ADCMIXA VOL6 | ADCMIXA VOL5 | ADCMIXA VOL4 | ADCMIXA VOL3 | ADCMIXA VOL2 | ADCMIXA VOL1 | ADCMIXA VOL0 |
| | p 46 default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Fh | Vol. Control ADCMIXB | MUTE_ADC MIXB | ADCMIXB VOL6 | ADCMIXB VOL5 | ADCMIXB VOL4 | ADCMIXB VOL3 | ADCMIXB VOL2 | ADCMIXB VOL1 | ADCMIXB VOL0 |
| | p 46 default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 10h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 16h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18h | ADC Channel Mixer | Reserved | Reserved | Reserved | Reserved | ADCA1 | ADCA0 | ADCB1 | ADCB0 |
| | p 47 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ah | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1Bh | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ch | ALC Enable & Attack Rate | ALC_ENB | ALC_ENA | ALC_ARATE5 | AALC_RATE4 | ALC_ARATE3 | ALC_ARATE2 | ALC_ARATE1 | ALC_ARATE0 |
| | p 47 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Dh | ALC Release Rate | Reserved | Reserved | ALC_RRATE5 | ALC_RRATE4 | ALC_RRATE3 | ALC_RRATE2 | ALC_RRATE1 | ALC_RRATE0 |
| | p 48 default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1Eh | ALC Threshold | MAX2 | MAX1 | MAX0 | MIN2 | MIN1 | MIN0 | Reserved | Reserved |
| | p 48 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Fh | Noise Gate Config | NG_ALL | NG_EN | NG_BOOST | THRESH2 | THRESH1 | THRESH0 | NGDELAY1 | NGDELAY0 |
| | p 49 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20h | Status | Reserved | SP_CLK ERR | SPEB_OVFL | SPEA_OVFL | PCMA_OVFL | PCMB_OVFL | ADCA_OVFL | ADCB_OVFL |
| | p 50 default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21h | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

# 6. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.
All “Reserved” registers must maintain their default state.

## 6.1 Chip I.D. and Revision Register (Address 01h) (Read Only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Chip_ID4 | Chip_ID3 | Chip_ID2 | Chip_ID1 | Chip_ID0 | Rev_ID2 | Rev_ID1 | Rev_ID0 |

**Chip I.D. (Chip_ID[4:0])**

Default: 11011

Function:

I.D. code for the CS53L21. Permanently set to 11011.

**Chip Revision (Rev_ID[2:0])**

Default: 001

Function:

CS53L21 revision level. Revision B is coded as 001. Revision A is coded as 000.

## 6.2 Power Control 1 (Address 02h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | PDN_PGAB | PDN_PGAA | PDN_ADCB | PDN_ADCA | PDN |

**Notes:**

1. To activate the power-down sequence for individual channels (A or B,) *both* channels must first be powered down either by enabling the PDN bit or by enabling the power-down bits for both channels. Enabling the power-down bit on an individual channel basis after the A/D has fully powered up will mute the selected channel without achieving any power savings.
2. Reserved bits 5 and 6 should always be set “high” by the user to minimize power consumption during normal operation.

*Recommended channel power-down sequence*: 1.) Enable the PDN bit, 2.) enable power-down for the select channels, 3.) disable the PDN bit.

**Power Down PGA X (PDN_PGAX)**

Default: 0

0 - Disable
1 - Enable

Function:

PGA channel x will either enter a power-down or muted state when this bit is enabled. See Power Control 1 (Address 02h) Note 1 above.

This bit is used in conjunction with AINx_MUX bits to determine the analog input path to the ADC. Refer to "ADCX Input Select Bits (AINX_MUX[1:0])" on page 42 for the required settings.

**Power Down ADC X (PDN_ADCX)**

Default: 0

0 - Disable
1 - Enable

Function:

ADC channel x will either enter a power-down or muted state when this bit is enabled. See Note 1 on page 36.

**Power Down (PDN)**

Default: 0

0 - Disable
1 - Enable

Function:

The entire A/D will enter a low-power state when this function is enabled. The contents of the control port registers are retained in this mode.

## 6.3 MIC Power Control and Speed Control (Address 03h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AUTO | SPEED1 | SPEED0 | 3-ST_SP | PDN_MICB | PDN_MICA | PDN_MICBIAS | MCLKDIV2 |

**Auto-Detect Speed Mode (AUTO)**

Default: 1

0 - Disable
1 - Enable

Function:

Enables the autodetect circuitry for detecting the speed mode of the A/D when operating as a slave. When AUTO is enabled, the MCLK/LRCK ratio must be implemented according to Table 3 on page 28. The SPEED[1:0] bits are ignored when this bit is enabled. Speed is determined by the MCLK/LRCK ratio.

**Speed Mode (SPEED[1:0])**

Default: 01

11 - Quarter-Speed Mode (QSM) - 4 to 12.5 kHz sample rates
10 - Half-Speed Mode (HSM) - 12.5 to 25 kHz sample rates
01 - Single-Speed Mode (SSM) - 4 to 50 kHz sample rates
00 - Double-Speed Mode (DSM) - 50 to 100 kHz sample rates

Function:

Sets the appropriate speed mode for the A/D in Master or Slave Mode. QSM is optimized for 8 kHz sample rate and HSM is optimized for 16 kHz sample rate. These bits are ignored when the AUTO bit is enabled (see Auto-Detect Speed Mode (AUTO) above).

**Tri-State Serial Port Interface (3ST_SP)**

Default: 0

0 - Disable
1 - Enable

Function:

When enabled and the device is configured as a master, all serial port outputs (clocks and data) are placed in a high impedance state. If the serial port is configured as a slave, only the SDOUT pin will be placed in a high-impedance state. The other signals will remain as inputs.

**Power Down MIC X (PDN_MICX)**

Default: 1

0 - Disable
1 - Enable

Function:

When enabled, the microphone preamp for channel x will be in a power-down state.

**Power Down MIC BIAS (PDN_MICBIAS)**

Default: 1

0 - Disable
1 - Enable

Function:

When enabled, the microphone bias circuit will be in a power-down state.

**MCLK Divide By 2 (MCLKDIV2)**

Default: 0

0 - Disabled
1 - Divide by 2

Function:

Divides the input MCLK by 2 prior to all internal circuitry. This bit is ignored when the AUTO bit is disabled in Slave Mode.

## 6.4 Interface Control (Address 04h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | M/S | Reserved | Reserved | Reserved | ADC_I²S/LJ | DIGMIX | MICMIX |

**Master/Slave Mode (M/S)**

Default: 0

0 - Slave
1 - Master

Function:

Selects either master or slave operation for the serial port.

**ADC I²S or Left-Justified (ADC_I²S/LJ)**

Default: 0

0 - Left-Justified
1 - I²S

Function:

Selects either the I²S or Left-Justified digital interface format for the data on SDOUT. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in this section “Digital Interface Formats” on page 30.

**Digital Mix (DIGMIX)**

Default: 0

| DIGMIX | SPE_ENABLE | Mix Selected |
|---|---|---|
| 0 | x | ADC data to ADC serial port, SDOUT data. |
| 1 | 0 | Reserved |
| | 1 | SPE Processed ADC data to ADC serial port, SDOUT data. |

Function:

Routes the ADC outputs to the serial port SDOUT pin. DIGMIX selects either “raw” ADC data or SPE processed ADC data to SDOUT. Note: If DIGMIX = 1, SPE_ENABLE must be 1 for the SPE to be functional.

**Microphone Mix (MICMIX)**

Default: 0

0 - Disabled; No Mix: Left/Right Channel to ADC serial port, SDOUT.
1 - Enabled; Mix: Differential mix ((A-B)/2)to ADC serial port, SDOUT.

Function:

Selects between the ADC stereo mix or a differential mix of analog inputs A and B.

## 6.5 MIC Control (Address 05h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_SNGVOL | ADCB_DBOOST | ADCA_DBOOST | MICBIAS_SEL | MICBIAS_LVL1 | MICBIAS_LVL0 | MICB_BOOST | MICA_BOOST |

**ADC Single Volume Control (ADC_SNGVOL)**

Default: 0

0 - Disabled
1 - Enabled

Function:

The individual PGA Volume (PGAx_VOLx) and ADC channel attenuation (ADCx_ATTx) levels as well as the ALC A and B enable (ALC_ENx) are independently controlled by their respective control registers when this function is disabled. When enabled, the volume on both channels is determined by the ADCA Attenuator Control register, or the PGAA Control register, and the ADCB Attenuator and PGAB Control registers are ignored. The ALC enable control for channel B is controlled by the ALC A enable when the ADC_SNGVOL bit is enabled and the ALC_ENB control register is ignored.

**ADCx 20 dB Digital Boost (ADCx_DBOOST)**

Default: 0

0 - Disabled
1 - Enabled

Function:

Applies a 20 dB digital gain to the input signal on ADC channel x, regardless of the input path.

**MIC Bias Select (MICBIAS_SEL)**

Default: 0

0 - MICBIAS on AIN3B/MICIN2 pin
1 - MICBIAS on AIN2B pin

Function:

Determines the output pin for the internally generated MICBIAS signal. If set to ‘0’b, the MICBIAS is output on the AIN3B/MICIN2 pin. If set to ‘1’b, the MICBIAS is output on the AIN2B pin.

**MIC Bias Level (MICBIAS_LVL[1:0])**

Default: 00

00 - 0.8 x VA
01 - 0.7 x VA
10 - 0.6 x VA
11 - 0.5 x VA

Function:

Determines the output voltage level of the MICBIAS output.

**MIC X Preamplifier Boost (MICX_BOOST)**

Default: 0

0 - +16 dB Gain
1 - +32 dB Gain

Function:

Determines the amount of gain applied to the microphone preamplifier for channel x.

## 6.6 ADC Control (Address 06h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADCB_HPFEN | ADCB_HPFRZ | ADCA_HPFEN | ADCA_HPFRZ | SOFTB | ZCROSSB | SOFTA | ZCROSSA |

**ADCX High-Pass Filter Enable (ADCX_HPFEN)**

Default: 1

0 - High-pass filter is disabled
1 - High-pass filter is enabled

Function:

When this bit is set, the internal high-pass filter will be enabled for ADCx. When set to '0', the high-pass filter will be disabled. For DC measurements, this bit must be cleared to '0'. "ADC Digital Filter Characteristics" on page 14.

**ADCX High-Pass Filter Freeze (ADCX_HPFRZ)**

Default: 0

0 - Continuous DC Subtraction
1 - Frozen DC Subtraction

Function:

The high-pass filter works by continuously subtracting a measure of the DC offset from the output of the decimation filter. If the ADCx_HPFRZ bit is taken high during normal operation, the current value of the DC offset is frozen, and this DC offset will continue to be subtracted from the conversion result. For DC measurements, this bit must be set to '1'. See "ADC Digital Filter Characteristics" on page 14.

**Soft Ramp CHX Control (SOFTX)**

Default: 0

0 - Disabled
1 - Enabled

Function:

Soft Ramp allows level changes to be implemented via an incremental ramp. ADCx_ATT[7:0] digital attenuation changes are ramped from the current level to the new level at a rate of 0.125 dB per LRCK period. PGAx_VOL[4:0] gain changes are ramped in 0.5 dB steps every 16 LRCK periods.

Soft Ramp and Zero Cross Enabled
When used in conjunction with the ZCROSSx bit, the PGAx_VOL[4:0] gain changes will occur in 0.5 dB steps and be implemented on a signal zero crossing.

**Zero Cross CHX Control (ZCROSSX)**

Default: 0

0 - Disabled
1 - Enabled

Function:

Zero Cross Enable dictates that signal level changes will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 1024 sample periods (approximately 10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enabled
When used in conjunction with the SOFTx bit, the PGAx_VOL[4:0] gain changes will occur in 0.5 dB steps and be implemented on a signal zero crossing.

The ADC Attenuator ADCx_ATT[7:0] is not affected by the ZCROSSx bit.

| **SOFTx** | **ZCROSSx** | **Analog PGA Volume** (PGAx_VOL[4:0]) | **Digital Attenuator** (ADCx_ATT[7:0]) |
|---|---|---|---|
| 0 | 0 | Volume changes immediately. | Volume changes immediately. |
| 0 | 1 | Volume changes at next zero cross time. | Volume changes immediately. |
| 1 | 0 | Volume changes in 0.5 dB steps. | Change volume in 0.125 dB steps. |
| 1 | 1 | Volume changes in 0.5 dB steps at every signal zero-cross. | Change volume in 0.125 dB steps. |

## 6.7 ADCx Input Select, Invert and Mute (Address 07h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AINB_MUX1 | AINB_MUX0 | AINA_MUX1 | AINA_MUX0 | INV_ADCB | INV_ADCA | ADCB_MUTE | ADCA_MUTE |

**ADCX Input Select Bits (AINX_MUX[1:0])**

Default: 00

| **PDN_PGAx** | **AINx_MUX[1:0]** | **Selected Path to ADC** |
|---|---|---|
| 0 | 00 | AIN1x-->PGAx |
| 0 | 01 | AIN2x-->PGAx |
| 0 | 10 | AIN3x/MICINx-->PGAx |
| 0 | 11 | AIN3x/MICINx-->Pre-Amp*(+16/+32 dB Gain)*-->PGAx |
| 1 | 00 | AIN1x |
| 1 | 01 | AIN2x |
| 1 | 10 | AIN3x/MICINx |
| 1 | 11 | Reserved |

Function:

Selects the specified analog input signal into ADCx. The microphone preamp is only available when PDN_PGAx is disabled. See Figure 21.

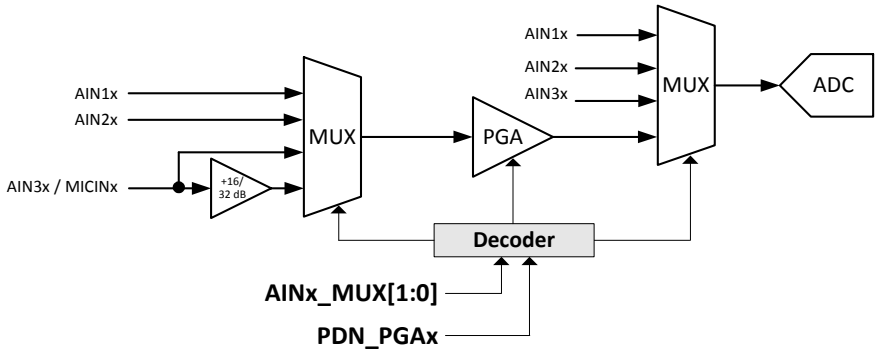



**Figure 21. AIN and PGA Selection**

**ADCX Invert Signal Polarity (INV_ADCX)**

Default: 0

0 - Disabled
1 - Enabled

Function:

When enabled, this bit will invert the signal polarity of the ADC x channel.

**ADCX Channel Mute (ADCX_MUTE)**

Default: 0

0 - Disabled
1 - Enabled

Function:

The output of channel x ADC will mute when enabled. The muting function is affected by the ADCx Soft bit (SOFT).

## 6.8 SPE Control (Address 09h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SPE_ENABLE | FREEZE | Reserved | Reserved | Reserved | SPE_SZC1 | SPE_SZC0 |

**SPE_ENABLE**

Default: 0

0 - Reserved
1 - ADC Serial Port to SPE

Function:

Selects the digital signal source for the SPE. Note: If DIGMIX = 1, SPE_ENABLE must be 1 for the SPE to be functional.

**Freeze Controls (FREEZE)**

Default: 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to all control port registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in the control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

**Note:**

1. This bit should only be used to synchronize run-time controls, such as volume and mute, during normal operation. Using this bit before the relevant circuitry begins normal operation could cause the change to take effect immediately, ignoring the FREEZE bit.

**SPE Soft Ramp and Zero Cross Control (SPE_SZC[1:0])**

Default = 10

00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

**Note:** The SPE_ENABLE bits in reg09h must be set to 1 to enable function control

Immediate Change

When Immediate Change is selected all volume-level changes will take effect immediately in one step.

Zero Cross

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 1024 and 2048 sample periods (21.3 ms to 42.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 0.5 dB per 4 left/right clock periods.

Soft Ramp on Zero Crossing

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

## 6.9 ALCX and PGAX Control: ALCA, PGAA (Address 0Ah) and ALCB, PGAB (Address 0Bh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALCX_SRDIS | ALCX_ZCDIS | Reserved | PGAX_VOL4 | PGAX_VOL3 | PGAX_VOL2 | PGAX_VOL1 | PGAX_VOL0 |

**ALCX Soft Ramp Disable (ALCX_SRDIS)**

Default: 0

0 - Off
1 - On

Function:

Overrides the SOFTx bit setting for the ADC. When this bit is set, the ALC attack rate in the PGA will not be dictated by the soft ramp setting. ALC volume-level changes will take effect in one step.

**ALCX Zero Cross Disable (ALCX_ZCDIS)**

Default: 0

0 - Off
1 - On

Function:

Overrides the ZCROSSx bit setting for the ADC. When this bit is set, the ALC attack rate in the PGA will not be dictated by the zero cross setting. ALC volume-level changes will take effect immediately in one step.

**PGA X Gain Control (PGAX_VOL[4:0])**

Default: 00000

| Binary Code | Volume Setting |
|---|---|
| 11000 | +12 dB |
| … | … |
| 01010 | +5 dB |
| … | … |
| 00000 | 0 dB |
| 11111 | -0.5 dB |
| 11110 | -1 dB |
| … | … |
| 11001 | -3 dB |
| 11010 | -3 dB |

Function:

The PGAx Gain Control register allows independent setting of the signal levels in 0.5 dB increments as dictated by the ADCx Soft and Zero Cross bits (SOFTx and ZCROSSx) from +12 dB to -3 dB. Gain settings are decoded as shown in the table above. The gain changes are implemented as dictated by the ALCX Soft and Zero Cross bits (ALCX_SRDIS and ALCX_ZCDIS).

**Note:** When the ALC is enabled, the PGA is automatically controlled and should not be adjusted manually.

## 6.10 ADCx Attenuator: ADCA (Address 0Ch) and ADCB (Address 0Dh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADCx_ATT7 | ADCx_ATT6 | ADCx_ATT5 | ADCx_ATT4 | ADCx_ATT3 | ADCx_ATT2 | ADCx_ATT1 | ADCx_ATT0 |

**ADCX Attenuation Control (ADCX_ATT[7:0])**

Default: 00h

| Binary Code | Volume Setting |
|---|---|
| 0111 1111 | 0 dB |
| … | … |
| 0000 0000 | 0 dB |
| 1111 1111 | -1 dB |
| 1111 1110 | -2 dB |
| … | … |
| 1010 0000 | -96 dB |
| … | … |
| 1000 0000 | -96 dB |

Function:

The level of ADCX can be adjusted in 1.0 dB increments as dictated by the ADCx Soft and Zero Cross bits (SOFTx and ZCROSSx) from 0 to -96 dB. Levels are decoded in two's complement, as shown in the table above.

**Note:** When the ALC is enabled, the Attenuator and PGA volume is automatically controlled and should not be adjusted manually.

## 6.11 ADCx Mixer Volume Control: ADCA (Address 0Eh) and ADCB (Address 0Fh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MUTE_ADCMIXx | ADCMIXx_VOL6 | ADCMIXx_VOL5 | ADCMIXx_VOL4 | ADCMIXx_VOL3 | ADCMIXx_VOL2 | ADCMIXx_VOL1 | ADCMIXx_VOL0 |

**Note:** The SPE_ENABLE bit in reg09h must be set to 1 to enable function control in this register.

**ADCX Mixer Channel Mute (MUTE_ADCMIXX)**

Default: 1

0 - Disabled
1 - Enabled

Function:

The ADC channel X input to the output mixer will mute when enabled. The muting function is affected by the SPEX Soft and Zero Cross bits (SPEX_SZC[1:0]).

**ADCX Mixer Volume Control (ADCMIXX_VOL[6:0])**

Default = 000 0000

| Binary Code | Volume Setting |
|---|---|
| 001 1000 | +12.0 dB |
| … | … |
| 000 0000 | 0 dB |
| 111 1111 | -0.5 dB |
| 111 1110 | -1.0 dB |
| … | … |

| Binary Code | Volume Setting |
|---|---|
| 001 1001 | -51.5 dB |

Function:

The level of the ADCX input to the output mixer can be adjusted in 0.5 dB increments as dictated by the SPEX Soft and Zero Cross bits (SPE_SZC[1:0]) from +12 to -51.5 dB. Levels are decoded as shown in the table above.

## 6.12 Channel Mixer (Address 18h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | ADCA1 | ADCA0 | ADCB1 | ADCB0 |

**Note:** The SPE_ENABLE bits in reg09h must be set to 1 to enable function control in this register.

**Channel Mixer (ADCx[1:0])**

Default: 00

| ADCA[1:0] | SDOUT | ADCB[1:0] | SDOUT |
|---|---|---|---|
| 00 | L | 00 | R |
| 01 | $\frac{L+R}{2}$ | 01 | $\frac{L+R}{2}$ |
| 10 | | 10 | |
| 11 | R | 11 | L |

Function:

Implements mono mixes of the left and right channels as well as a left/right channel swap.

## 6.13 ALC Enable and Attack Rate (Address 1Ch)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALC_ENB | ALC_ENA | ALC_ARATE5 | ALC_ARATE4 | ALC_ARATE3 | ALC_ARATE2 | ALC_ARATE1 | ALC_ARATE0 |

**ALC Enable (ALC_ENX)**

Default: 0

0 - Disabled
1 - Enabled

Function:

Enables automatic level control for ADC channel x.

**Notes:**

1. When the ALC is enabled, the Attenuator and PGA volume is automatically controlled and should not be adjusted manually.
2. The ALC should only be configured while the power down bit is enabled.

**ALC Attack Rate (ARATE[5:0])**

Default: 000000

| Binary Code | Attack Time |
|---|---|
| 000000 | Fastest Attack |
| … | … |
| 111111 | Slowest Attack |

Function:

Sets the rate at which the ALC attenuates the analog input from levels above the maximum setting in the ALC threshold register.

The limiter attack rate is user-selectable but is also a function of the sampling frequency, Fs, and the SOFTx and ZCROSSx bit settings unless the disable bit for each function is enabled.

## 6.14 ALC Release Rate (Address 1Dh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | ALC_RRATE5 | ALC_RRATE4 | ALC_RRATE3 | ALC_RRATE2 | ALC_RRATE1 | ALC_RRATE0 |

**ALC Release Rate (RRATE[5:0])**

Default: 111111

| Binary Code | Release Time |
|---|---|
| 000000 | Fastest Release |
| … | … |
| 111111 | Slowest Release |

Function:

Sets the rate at which the ALC releases the PGA and digital attenuation from levels below the minimum setting in the ALC threshold register, and returns the input level to the PGA_VOL[4:0] and ADCx_ATT[7:0] setting. The ALC release rate is user selectable, but is also a function of the sampling frequency, Fs, and the SOFTx and ZCROSS bit settings unless the disable bit for each function is enabled.

## 6.15 ALC Threshold (Address 1Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MAX2 | MAX1 | MAX0 | MIN2 | MIN1 | MIN0 | Reserved | Reserved |

**Maximum Threshold (MAX[2:0])**

Default: 000

| MAX[2:0] | Threshold Setting (dB) |
|---|---|
| 000 | 0 |
| 001 | -3 |
| 010 | -6 |
| 011 | -9 |
| 100 | -12 |
| 101 | -18 |
| 110 | -24 |
| 111 | -30 |

Function:

Sets the maximum level, relative to full scale, at which to limit and attenuate the input signal at the attack rate.

**Minimum Threshold (MIN[2:0])**

Default: 000

| MIN[2:0] | Threshold Setting (dB) |
|---|---|
| 000 | 0 |
| 001 | -3 |
| 010 | -6 |
| 011 | -9 |
| 100 | -12 |
| 101 | -18 |
| 110 | -24 |
| 111 | -30 |

Function:

Sets the minimum level at which to disengage the ALC's attenuation or amplify the input signal at a rate set in the release rate register until levels again reach this minimum threshold. The ALC uses this minimum as a hysteresis point for the input signal as it maintains the signal below the maximum as well as below the minimum setting. This provides a more natural sound as the ALC attacks and releases.

## 6.16 Noise Gate Configuration and Misc. (Address 1Fh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NG_ALL | NG_EN | NG_BOOST | THRESH2 | THRESH1 | THRESH0 | NGDELAY1 | NGDELAY0 |

**Noise Gate Channel Gang (NG_ALL)**

Default: 0

0 - Disabled
1 - Enabled

Function:

Gangs the noise gate function for channel A and B. When enabled, both channels must fall below the threshold setting for the noise gate attenuation to take effect.

**Noise Gate Enable (NG_EN)**

Default: 0

0 - Disabled
1 - Enabled

Function:

Enables the noise gate. Maximum attenuation is relative to all gain settings applied.

**Noise Gate Boost (NG_BOOST) and Threshold (THRESH[3:0])**

Default: 000

| THRESH[2:0] | Minimum Setting (NG_BOOST = '0'b) | Minimum Setting (NG_BOOST = '1'b) |
|---|---|---|
| 000 | -64 dB | -34 dB |
| 001 | -67 dB | -37 dB |
| 010 | -70 dB | -40 dB |
| 011 | -73 dB | -43 dB |
| 100 | -76 dB | -46 dB |
| 101 | -82 dB | -52 dB |
| 110 | Reserved | -58 dB |
| 111 | Reserved | -64 dB |

Function:
Sets the threshold level of the noise gate. Input signals below the threshold level will be attenuated to -96 dB. NG_BOOST = '1'b adds 30 dB to the threshold settings.

**Noise Gate Delay Timing (NGDELAY[1:0])**

Default: 00

00 - 50 ms
01 - 100 ms
10 - 150 ms
11 - 200 ms

Function:

Sets the delay time before the noise gate attacks. Noise gate attenuation is dictated by the SOFTx and ZCROSS bit settings unless the disable bit for each function is enabled.

## 6.17 Status (Address 20h) (Read Only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SP_CLKERR | Reserved | Reserved | Reserved | Reserved | ADCA_OVFL | ADCB_OVFL |

For all bits in this register, a "1" means the associated error condition has occurred at least once since the register was last read. A "0" means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0.

**Serial Port Clock Error (SP_CLK Error)**

Default: 0

Function:

Indicates an invalid MCLK to LRCK ratio. See "Serial Port Clocking" on page 28"Serial Port Clocking" on page 28 for valid clock ratios.

**Note:** On initial power up and application of clocks, this bit will be high as the serial port re-synchronizes.

**ADC Overflow (ADCX_OVFL)**

Default = 0

Function:

Indicates that there is an over-range condition anywhere in the CS53L21 ADC signal path of each of the associated ADCs.

# 7. ANALOG PERFORMANCE PLOTS

## 7.1 ADC_FILT+ Capacitor Effects on THD+N

The value of the capacitor on the ADC_FILT+ pin, 16, affects the low frequency total harmonic distortion + noise (THD+N) performance of the ADC. Larger capacitor values yield significant improvement in THD+N at low frequencies. Figure 22 shows the THD+N versus frequency for the ADC analog input. Plots were taken from the CDB53L21 using an Audio Precision analyzer.

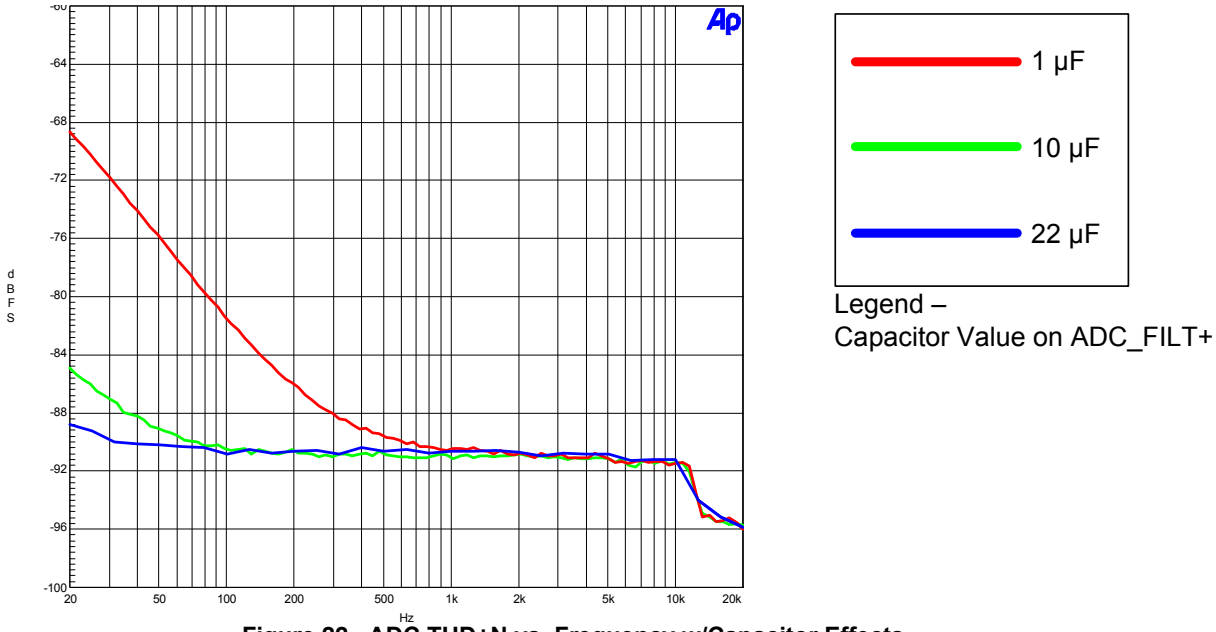



**Figure 22. ADC THD+N vs. Frequency w/Capacitor Effects**

# 8. EXAMPLE SYSTEM CLOCK FREQUENCIES

## 8.1 Auto Detect Enabled

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | |
|---|---|---|---|---|
| | **1024x** | **1536x** | **2048x*** | **3072x*** |
| 8 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 11.025 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 12 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | |
|---|---|---|---|---|
| | **512x** | **768x** | **1024x*** | **1536x*** |
| 16 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 22.05 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 24 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | |
|---|---|---|---|---|
| | **256x** | **384x** | **512x*** | **768x*** |
| 32 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | |
|---|---|---|---|---|
| | 128x | 192x | 256x* | 384x* |
| 64 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

*The"MCLKDIV2" pin 4 must be set HI.

### 8.2 Auto Detect Disabled

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | | | |
|---|---|---|---|---|---|---|
| | 512x | 768x | 1024x | 1536x | 2048x | 3072x |
| 8 | - | 6.1440 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 11.025 | - | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 12 | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | | | |
|---|---|---|---|---|---|---|
| | 256x | 384x | 512x | 768x | 1024x | 1536x |
| 16 | - | 6.1440 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 22.05 | - | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 24 | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | |
|---|---|---|---|---|
| | 256x | 384x | 512x | 768x |
| 32 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate LRCK (kHz) | MCLK (MHz) | | | |
|---|---|---|---|---|
| | 128x | 192x | 256x | 384x |
| 64 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

## 9. PCB LAYOUT CONSIDERATIONS

### 9.1 Power Supply, Grounding

As with any high-resolution converter, the CS53L21 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 9 shows the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS53L21 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS53L21 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and AGND. The CS53L21 evaluation board demonstrates the optimum layout and power supply arrangements.

## 9.2 QFN Thermal Pad

The CS53L21 is available in a compact QFN package. The under side of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS53L21 evaluation board demonstrates the optimum thermal pad and via configuration.

# 10.DIGITAL FILTERS

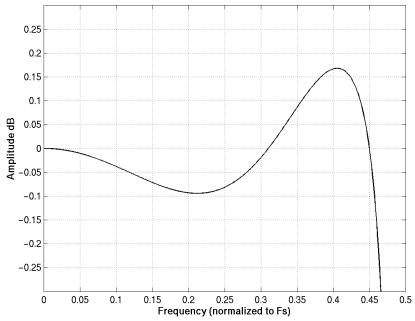



**Figure 23. ADC Passband Ripple**

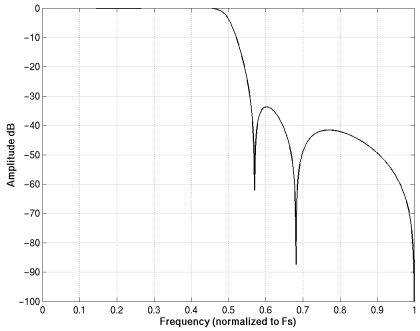



**Figure 24. ADC Stopband Rejection**

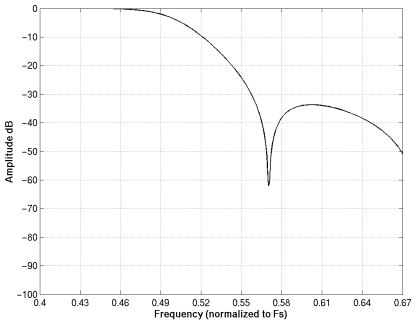



**Figure 25. ADC Transition Band**

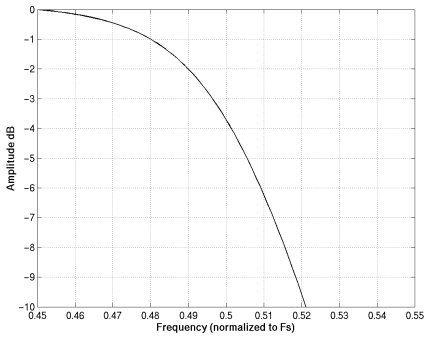



**Figure 26. ADC Transition Band Detail**

# 11.PARAMETER DEFINITIONS

**Dynamic Range**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

**Total Harmonic Distortion + Noise**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

**Frequency Response**

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

**Interchannel Isolation**

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch**

The gain difference between left and right channel pairs. Units in decibels.

**Gain Error**

The deviation from the nominal full-scale analog output for a full-scale digital input.

**Gain Drift**

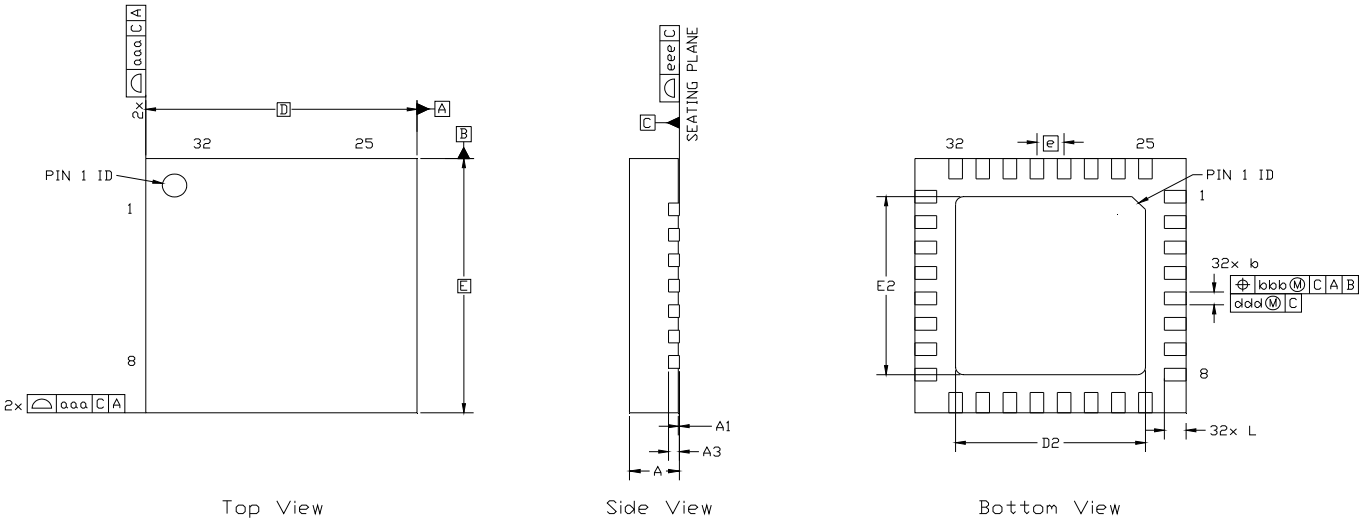
The change in gain value with temperature. Units in ppm/°C.

**Offset Error**

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

# 12.PACKAGE DIMENSIONS

## 32L QFN (5 X 5 mm BODY) PACKAGE DRAWING




| | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| **Dimension** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | | 0.20 REF | | | 0.008 REF | |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | | 5.00 BSC | | | 0.197 BSC | |
| D2 | 3.50 | 3.65 | 3.80 | 0.138 | 0.144 | 0.150 |
| e | | 0.50 BSC | | | 0.020 BSC | |
| E | | 5.00 BSC | | | 0.197 BSC | |
| E2 | 3.50 | 3.65 | 3.80 | 0.138 | 0.144 | 0.150 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| aaa | | 0.15 | | | 0.006 | |
| bbb | | 0.10 | | | 0.004 | |
| ddd | | 0.05 | | | 0.002 | |
| eee | | 0.08 | | | 0.003 | |

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M.
3. This drawing conforms to JEDEC outline MO-220, variation VHHD-4.
4. Recommended reflow profile is per JEDEC/IPC J-STD-020

# THERMAL CHARACTERISTICS

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Junction to Ambient Thermal Impedance | 2 Layer Board<br>4 Layer Board | $\theta_{JA}$ | -<br>- | 52<br>38 | -<br>- | °C/Watt |

# 13.ORDERING INFORMATION

| Product | Description | Package | Pb-Free | Grade | Temp Range | Container | Order # |
|---|---|---|---|---|---|---|---|
| CS53L21 | Low-Power Stereo A/D | 32L-QFN | Yes | Commercial | -10 to +70° C | Rail | CS53L21-CNZ |
| | | | | | | Tape and Reel | CS53L21-CNZR |
| | | | | Automotive | -40 to +85° C | Rail | CS53L21-DNZ |
| | | | | | | Tape and Reel | CS53L21-DNZR |
| CDB53L21 | CS53L21 Evaluation Board | - | No | - | - | - | CDB53L21 |

# 14.REFERENCES

1. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000. http://www.semiconductors.philips.com

# 15.REVISION HISTORY

| Revision | Changes |
|---|---|
| F1<br>JUL '15 | Updated voltage range in "Specified Operating Conditions" on page 11.<br>Corrected Max passband frequency in "ADC Digital Filter Characteristics" on page 14.<br>Updated Section 4.8 "Recommended Power-Up Sequence" on page 30.<br>Updated Section 4.10 "Software Mode" on page 31.<br>Added note 1 in the FREEZE control register in "SPE Control (Address 09h)" on page 43.<br>Added note 2 in the ALC Enable register in "ALC Enable and Attack Rate (Address 1Ch)" on page 47.<br>Replaced the package drawing, notes, and dimensions table in Section 12. "Package Dimensions" on page 55. |

## Contacting Cirrus Logic Support

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