

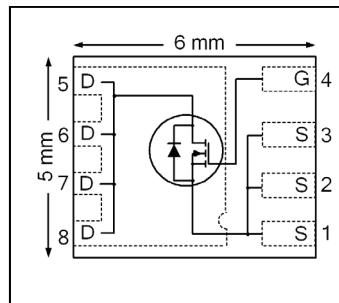


**THE DATASHEET OF  
IRLH7134TRPBF**



HEXFET® Power MOSFET

$V_{DSS}$	<b>40</b>	<b>V</b>
$R_{DS(on) \max}$ (@ $V_{GS} = 10V$ )	<b>3.3</b>	<b>mΩ</b>
$Q_g$ (typical)	<b>39</b>	<b>nC</b>
$I_D$ (@ $T_{C(Bottom)} = 25^\circ C$ )	<b>50</b>	<b>A</b>


**Applications**

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

**Features**

Low $R_{DS(ON)}$ (< 4.7mΩ @ $V_{GS} = 4.5V$ )
Low Thermal Resistance to PCB (<1.2°C/W)
Low Profile (<0.9mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

 results in  
⇒

**Benefits**

Lower Conduction Losses
Enables better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable Part Number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLH7134TRPbF	PQFN 5mm x 6 mm	Tape and Reel	4000	
IRLH7134TR2PbF	PQFN 5mm x 6 mm	Tape and Reel	400	EOL notice # 259

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	± 16	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	26	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	21	
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	134⑥⑦	
$I_D @ T_{C(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	85⑥⑦	
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	50⑦	
$I_{DM}$	Pulsed Drain Current ①	640	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑤	3.6	W
$P_D @ T_{C(Bottom)} = 25^\circ C$	Power Dissipation ⑤	104	
	Linear Derating Factor ⑤	0.029	W/°C
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

Notes ① through ⑦ are on page 9

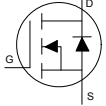
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	37	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.8	3.3	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A ③
		—	3.9	4.9		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 40A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-5.6	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V
g <sub>fs</sub>	Forward Transconductance	120	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 50A
Q <sub>g</sub>	Total Gate Charge	—	39	58	nC	V <sub>DS</sub> = 20V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 50A
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	9.0	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	4.5	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	16	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	9.5	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	20.5	—		
Q <sub>oss</sub>	Output Charge	—	23	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	0.6	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	21	—	ns	V <sub>DD</sub> = 20V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 50A R <sub>G</sub> = 1.7Ω
t <sub>r</sub>	Rise Time	—	75	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	18	—		
t <sub>f</sub>	Fall Time	—	13	—		
C <sub>iss</sub>	Input Capacitance	—	3720	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	610	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	350	—		

**Avalanche Characteristics**

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	125	mJ
I <sub>AR</sub>	Avalanche Current ①	—	50	A

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	50⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	640		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 50A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	25	38	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 50A, V <sub>DD</sub> = 20V
Q <sub>rr</sub>	Reverse Recovery Charge	—	74	110	nC	di/dt = 400A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic Inductance				

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	1.2	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	30	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	35	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	22	

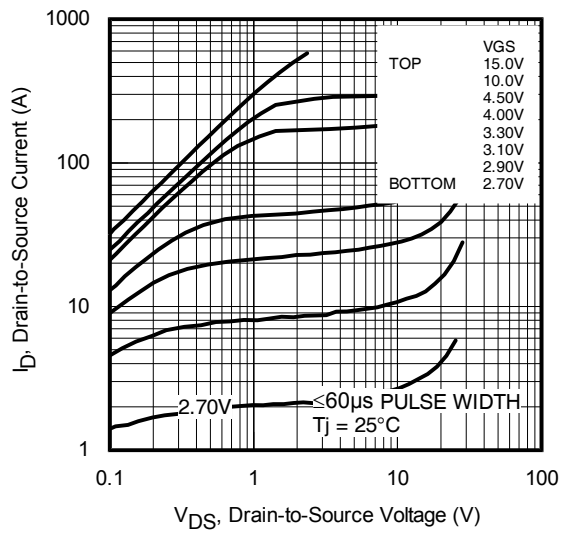


Fig 1. Typical Output Characteristics

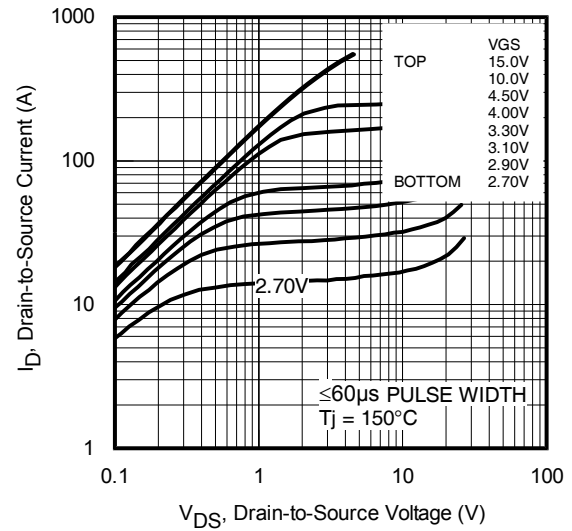


Fig 2. Typical Output Characteristics

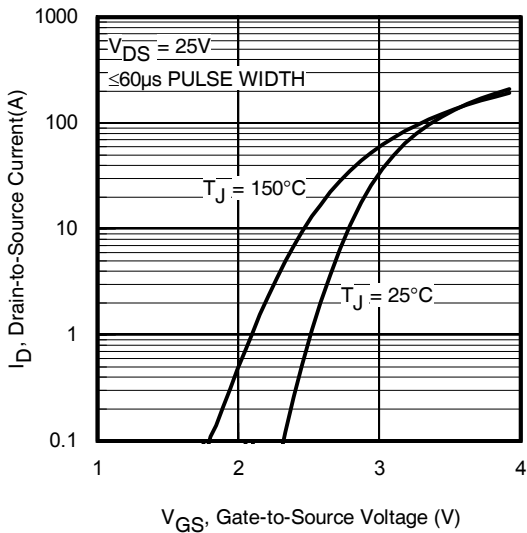


Fig 3. Typical Transfer Characteristics

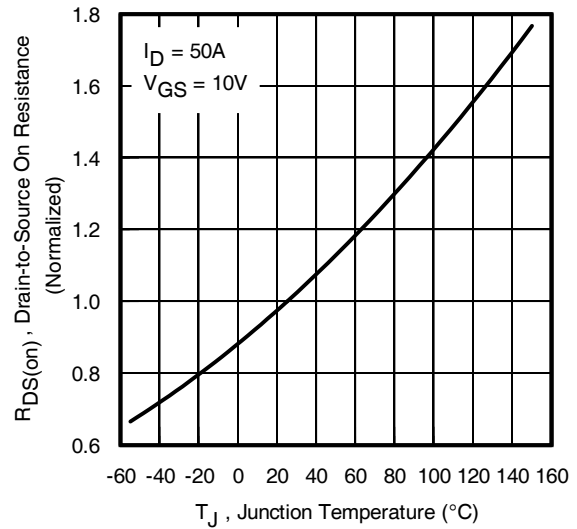


Fig 4. Normalized On-Resistance vs. Temperature

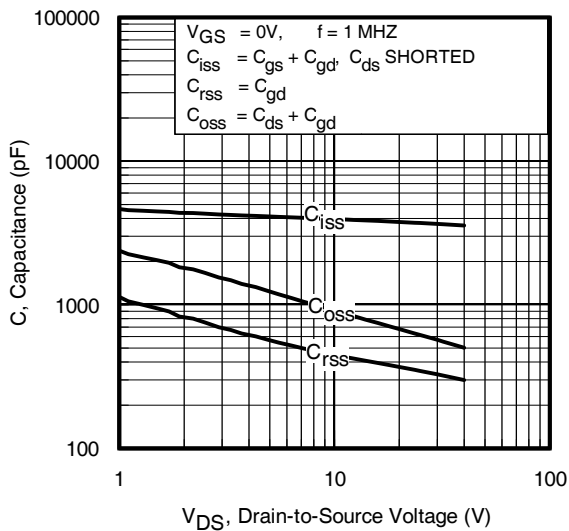


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

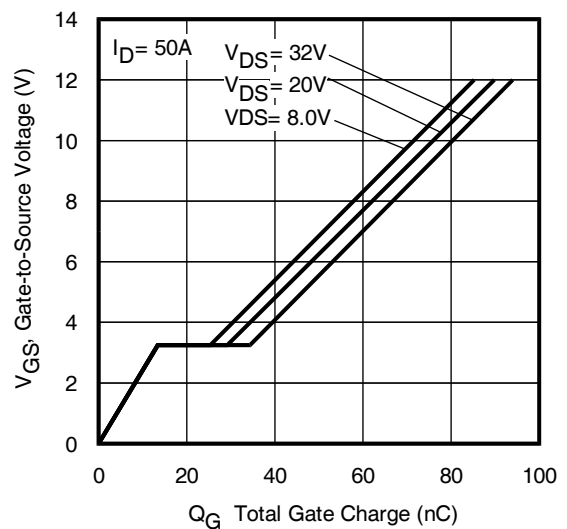
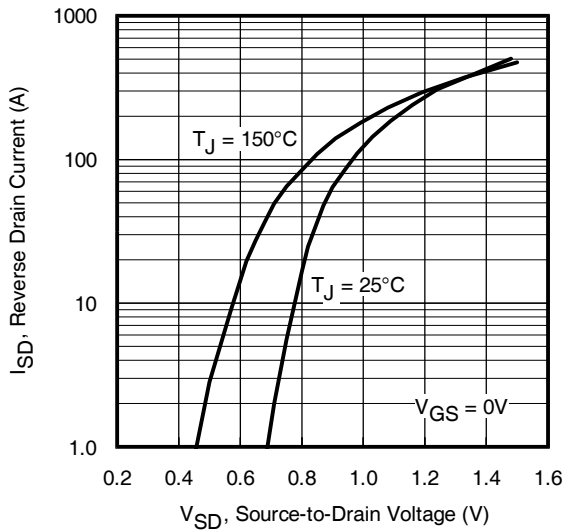
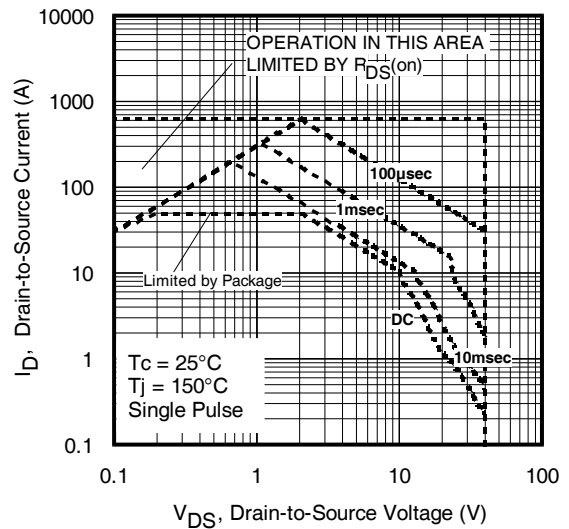
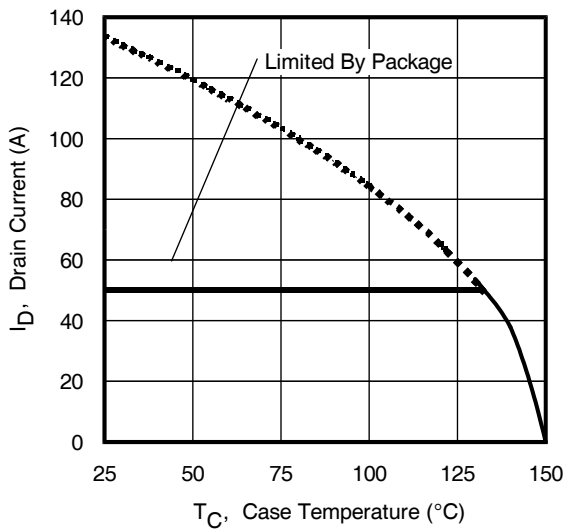
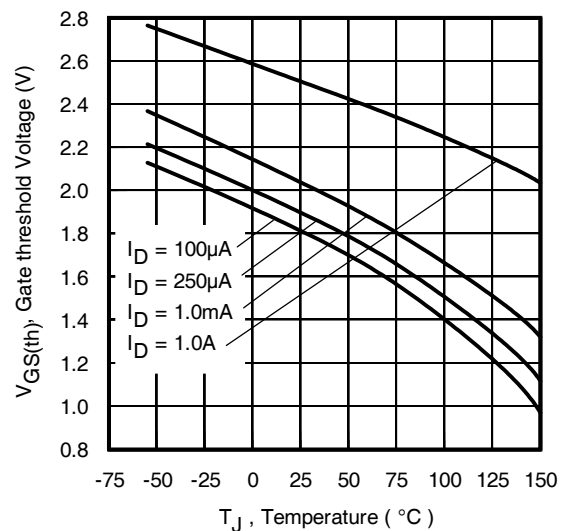
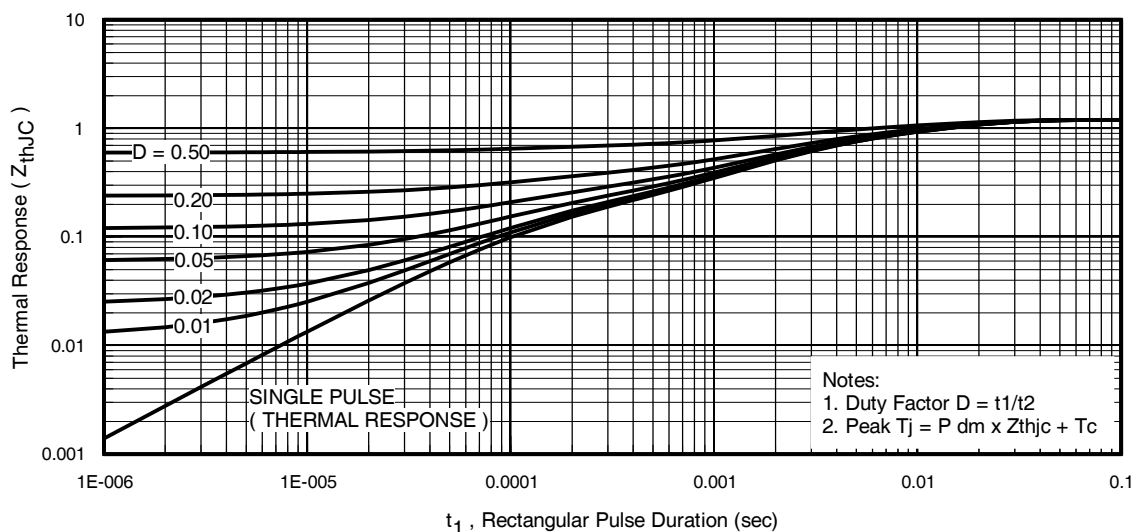


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Threshold Voltage vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

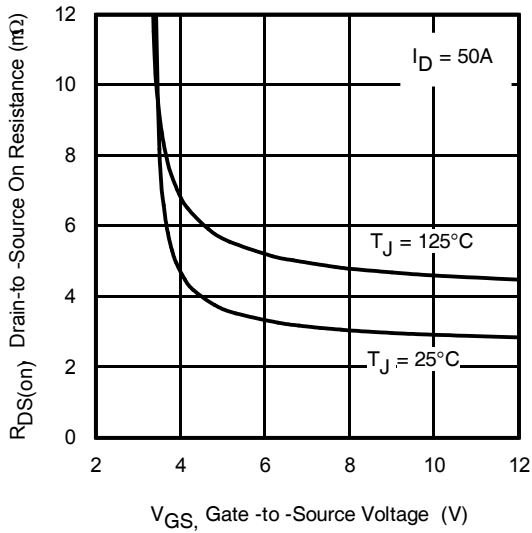


Fig 12. On-Resistance vs. Gate Voltage

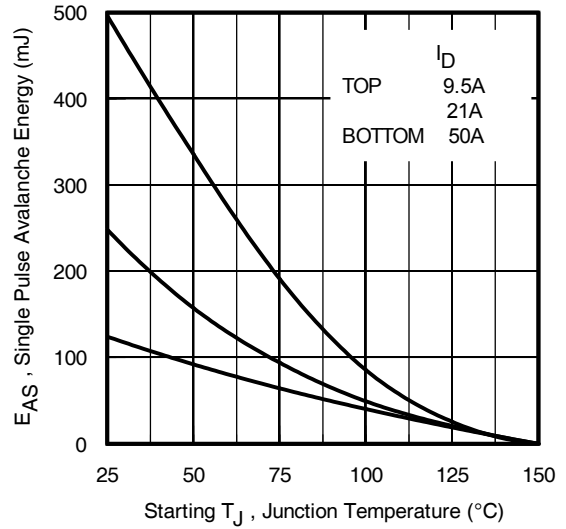


Fig 13. Maximum Avalanche Energy vs. Drain Current

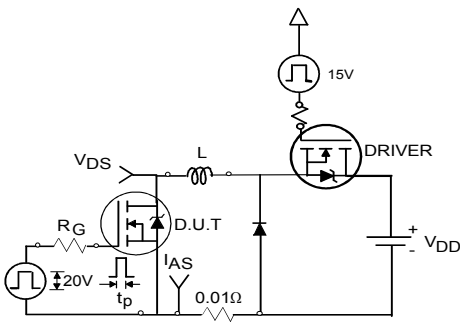


Fig 14a. Unclamped Inductive Test Circuit

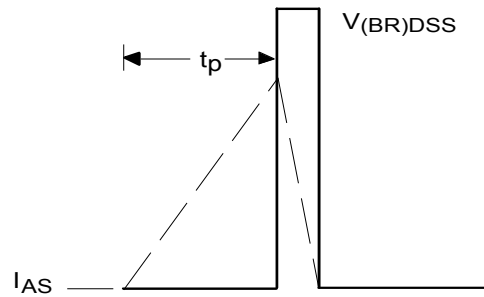


Fig 14b. Unclamped Inductive Waveforms

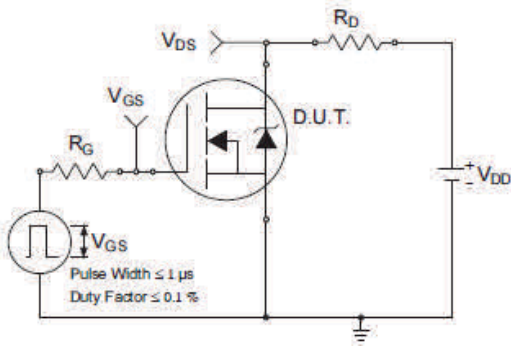


Fig 15a. Switching Time Test Circuit

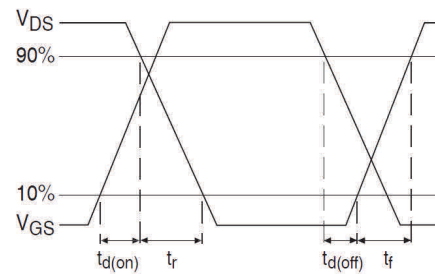
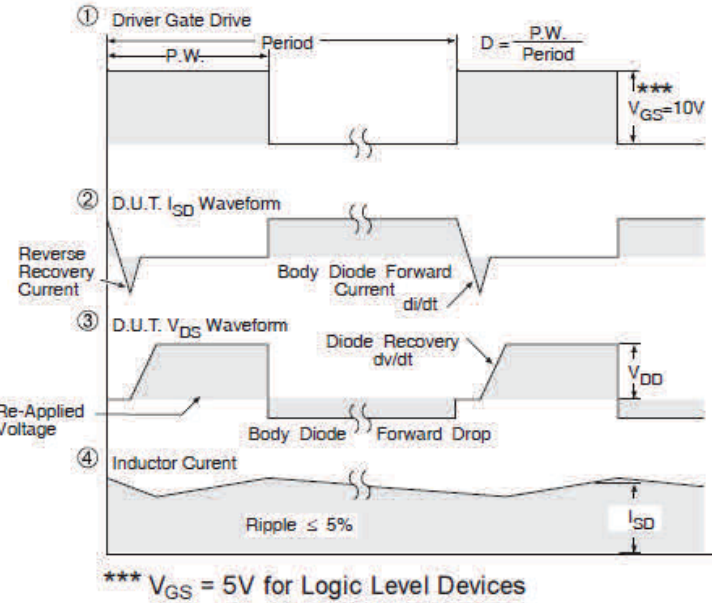
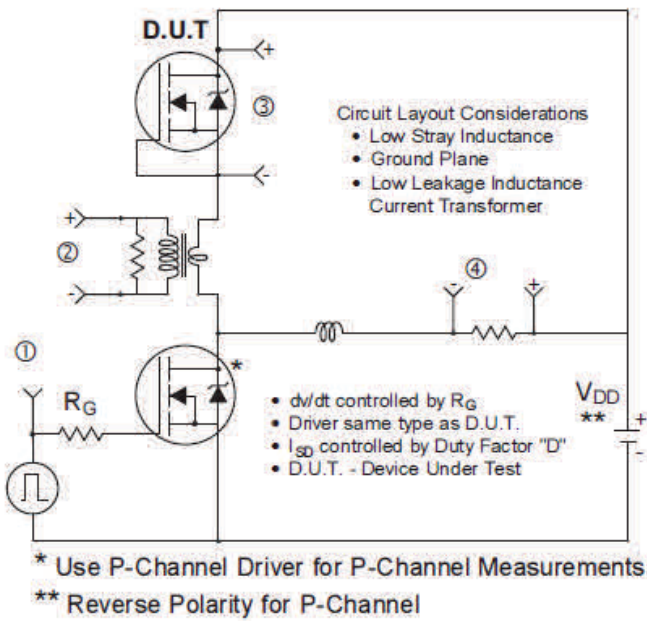
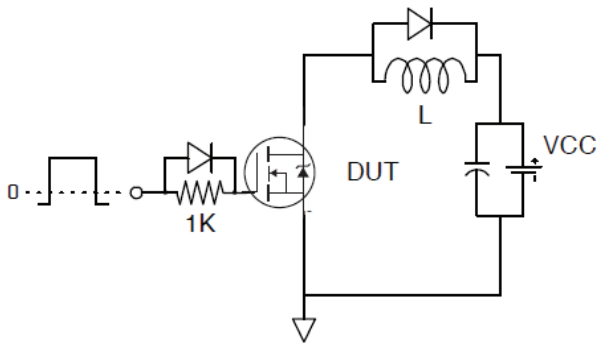


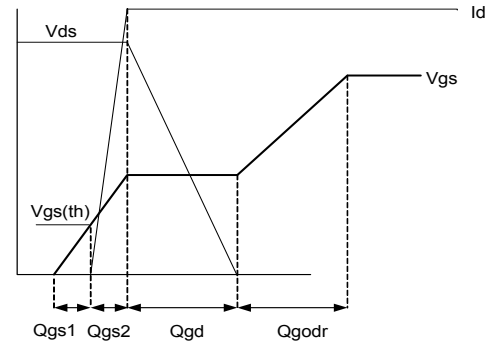
Fig 15b. Switching Time Waveforms



**Fig 16.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs

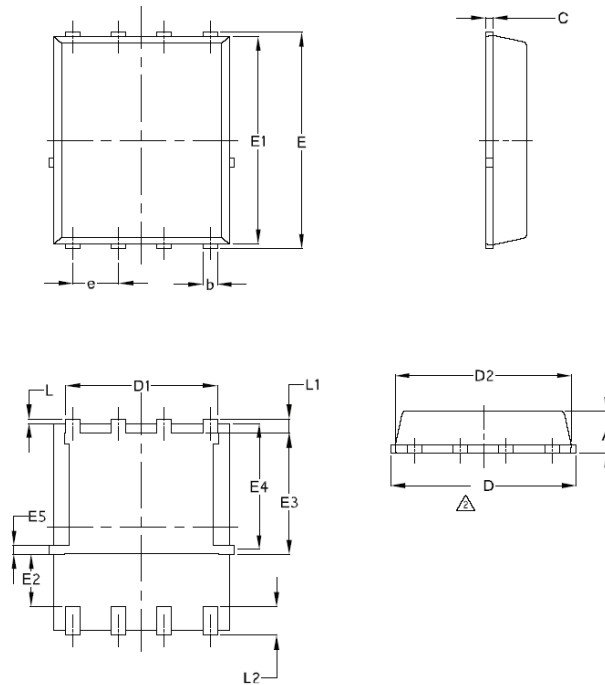


**Fig 17.** Gate Charge Test Circuit

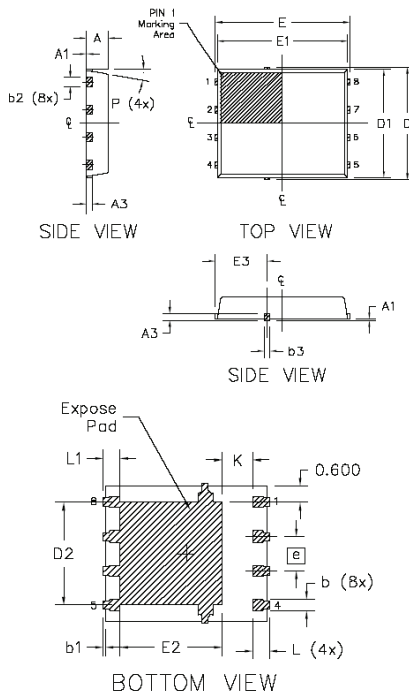


**Fig 18.** Gate Charge Waveform

VDD

**PQFN 5x6 Outline "E" Package Details**


SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.17	0.0354	0.0461
b	0.33	0.48	0.0130	0.0189
C	0.195	0.300	0.0077	0.0118
D	4.80	5.15	0.1890	0.2028
D1	3.91	4.31	0.1539	0.1697
D2	4.80	5.00	0.1890	0.1968
E	5.90	6.15	0.2323	0.2421
E1	5.65	6.00	0.2224	0.2362
E2	1.51	—	0.0594	—
E3	3.32	3.78	0.1307	0.1480
E4	3.42	3.58	0.1346	0.1409
E5	0.18	0.32	0.0071	0.0126
e	1.27 BSC		0.050 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.66	0.0150	0.0260
L2	0.51	0.86	0.0201	0.0339
I	0	0.18	0	0.0071

**PQFN 5x6 Outline "G" Package Details**


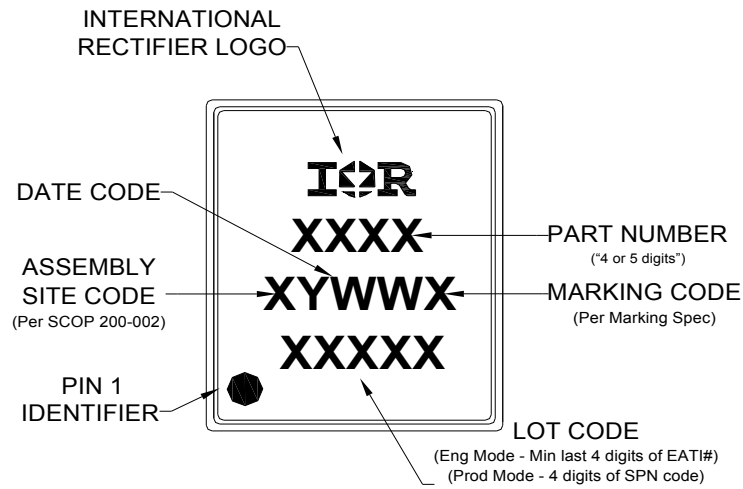
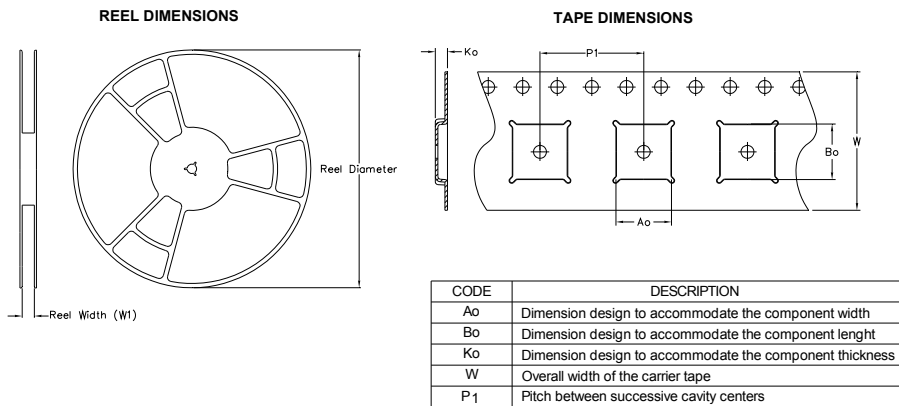
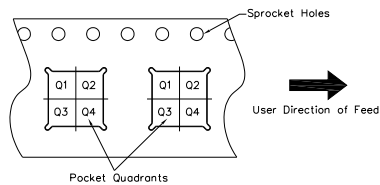
DIM SYMBOL	MILLIMETERS		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254 REF		0.0100 REF	
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150 BSC		0.2028 BSC	
D1	5.000 BSC		0.1969 BSC	
D2	3.700	3.900	0.1457	0.1535
E	6.150 BSC		0.2421 BSC	
E1	6.000 BSC		0.2362 BSC	
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27 REF		0.050 REF	
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

**Note:**

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

**PQFN 5x6 Part Marking**

**PQFN 5x6 Tape and Reel**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F <sup>†</sup> guidelines)	
<b>Moisture Sensitivity Level</b>	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>†</sup> )
<b>RoHS Compliant</b>	Yes	

<sup>†</sup> Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.099\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 50\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Package is limited to 50A by die-source to lead-frame bonding technology.

**Revision History**

Date	Comment
5/13/2014	<ul style="list-style-type: none"> <li>• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259)</li> <li>• Updated Tape and Reel on page 8.</li> <li>• Updated data sheet based on corporate template.</li> </ul>
6/2/2015	<ul style="list-style-type: none"> <li>• Updated package outline for “option E” and added package outline for “option G” on page 7.</li> <li>• Updated "IFX" logo on page 1 &amp; 9.</li> <li>• Updated tape and reel on page 8.</li> </ul>
7/7/2015	<ul style="list-style-type: none"> <li>• Corrected package outline for “option E” on page 7.</li> </ul>
8/01/2016	<ul style="list-style-type: none"> <li>• Updated “Infineon” logo –all pages.</li> <li>• Updated disclaimer on last page.</li> <li>• Corrected typo on switch time test condition from “V<sub>GS</sub> =10V” to “V<sub>GS</sub>= 4.5V” on page 2.</li> </ul>

**Published by**  
**Infineon Technologies AG**  
**81726 München, Germany**

**© Infineon Technologies AG 2015**  
**All Rights Reserved.**

**IMPORTANT NOTICE**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office ([www.infineon.com](http://www.infineon.com)).

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View IRLH7134TRPBF on WIN SOURCE](#)

 [Infineon Technologies](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management