# THE DATASHEET OF

# AD7682BCPZ

www.win-source.net 0086-755-83957316

Data Sheet

# AD7682/AD7689

## 16-Bit, 4-Channel/8-Channel, 250 kSPS PulSAR ADCs

## FEATURES

- 16-bit resolution with no missing codes
- 4-channel (AD7682)/8-channel (AD7689) multiplexer with choice of inputs
- Unipolar single-ended
- Differential (GND sense)
- Pseudobipolar
- Throughput: 250 kSPS
- INL: ±0.4 LSB typical, ±1.5 LSB maximum (±23 ppm or FSR)
- Dynamic range: 93.8 dB
- SINAD: 92.5 dB at 20 kHz
- THD: −100 dB at 20 kHz
- Analog input range: 0 V to $V_{REF}$ with $V_{REF}$ up to VDD
- Multiple reference types
  - Internal selectable 2.5 V or 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor (TEMP)
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 2.3 V to 5.5 V operation with 1.8 V to 5.5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 3.5 mW at 2.5 V/200 kSPS
  - 12.5 mW at 5 V/250 kSPS
- Standby current: 50 nA
- Low cost grade available
- 20-lead 4 mm × 4 mm LFCSP package
- 20-lead 2.4 mm × 2.4 mm WLCSP package

## APPLICATIONS

- Multichannel system monitoring
- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

## FUNCTIONAL BLOCK DIAGRAM

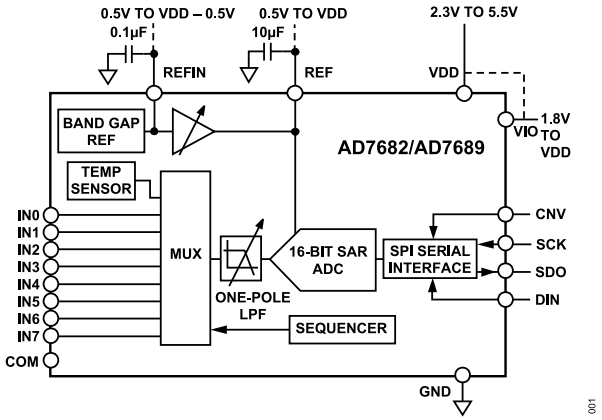


*Figure 1.*

## GENERAL DESCRIPTION

The AD7682/AD7689 are 4-channel/8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a single power supply, VDD.

The AD7682/AD7689 contain all components for use in a multichannel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; a 4-channel (AD7682) or 8-channel (AD7689) low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7682/AD7689 use a simple serial port interface (SPI) for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7682/AD7689 are housed in a tiny 20-lead lead frame chip scale package (LFCSP) and 20-lead wafer level chip scale package (WLCSP) with operation specified from −40°C to +85°C. The AD7689 includes an extended temperature range model with specifications guaranteed to a maximum temperature ($T_{MAX}$) of +125°C.

*Table 1. Multichannel 14-Bit/16-Bit PulSAR® ADCs*

| Type | Channels | 250 kSPS | 500 kSPS | ADC Driver |
|---|---|---|---|---|
| 14-Bit | 8 | AD7949 | | ADA4805-1/ADA4807-1 |
| 16-Bit | 4 | AD7682 | | ADA4805-1/ADA4807-1 |
| 16-Bit | 8 | AD7689 | AD7699 | ADA4805-1/ADA4807-1 |



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## REVISION HISTORY

**10/2023—Rev. J to Rev. K**

Added Table 12 Title; Renumbered Sequentially ... 28
Changes to Figure 43 ... 33
Updated Outline Dimensions ... 36
Changes to Ordering Guide ... 37

## SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, reference voltage ($V_{REF}$) = VDD, all specifications, $T_A$ = −40°C to +85°C, unless otherwise noted.

***Table 2.***

| Parameter | Test Conditions/ Comments | AD7689A | | | AD7682B/AD7689B | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | 16 | | | 16 | | | Bits |
| ANALOG INPUT | | | | | | | | |
| Voltage Range | Unipolar mode | 0 | | $+V_{REF}$ | 0 | | $+V_{REF}$ | V |
| | Bipolar mode | $-V_{REF}/2$ | | $+V_{REF}/2$ | $-V_{REF}/2$ | | $+V_{REF}/2$ | V |
| Absolute Input Voltage | Positive input, unipolar and bipolar modes | −0.1 | | $V_{REF}$ + 0.1 | −0.1 | | $V_{REF}$ + 0.1 | V |
| | Negative or COM input, unipolar mode | −0.1 | | +0.1 | −0.1 | | +0.1 | V |
| | Negative or COM input, bipolar mode | $V_{REF}/2$ − 0.1 | $V_{REF}/2$ | $V_{REF}/2$ + 0.1 | $V_{REF}/2$ − 0.1 | $V_{REF}/2$ | $V_{REF}/2$ + 0.1 | V |
| Analog Input CMRR[1] | Input frequency ($f_{IN}$) = 250 kHz | | 68 | | | 68 | | dB |
| Leakage Current at 25°C | Acquisition phase | | 1 | | | 1 | | nA |
| Input Impedance[2] | | | | | | | | |
| THROUGHPUT | | | | | | | | |
| Conversion Rate | | | | | | | | |
| Full Bandwidth[3] | VDD = 4.5 V to 5.5 V | 0 | | 250 | 0 | | 250 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 200 | 0 | | 200 | kSPS |
| ¼ Bandwidth[3] | VDD = 4.5 V to 5.5 V | 0 | | 62.5 | 0 | | 62.5 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 50 | 0 | | 50 | kSPS |
| Transient Response | Full-scale step, full bandwidth | | | 1.8 | | | 1.8 | µs |
| | Full-scale step, ¼ bandwidth | | | 14.5 | | | 14.5 | µs |
| ACCURACY | | | | | | | | |
| No Missing Codes | | 15 | | | 16 | | | Bits |
| Integral Linearity Error | | −4 | | +4 | −1.5 | ±0.4 | +1.5 | LSB[4] |
| Differential Linearity Error | | | | | −1 | ±0.25 | +1.5 | LSB |
| Transition Noise | REF = VDD = 5 V | | 0.6 | | | 0.5 | | LSB |
| Gain Error[5] | | −32 | | +32 | −8 | ±1 | +8 | LSB |
| Gain Error Match | | | ±2 | | −4 | ±0.5 | +4 | LSB |
| Gain Error Temperature Drift | | | ±1 | | | ±1 | | ppm/°C |
| Offset Error[5] | VDD = 4.5 V to 5.5 V | −32 | | +32 | −8 | ±1 | +8 | LSB |
| | VDD = 2.3 V to 4.5 V | | ±32 | | | ±5 | | LSB |
| Offset Error Match | | | ±2 | | −4 | ±0.5 | +4 | LSB |
| Offset Error Temperature Drift | | | ±1 | | | ±1 | | ppm/°C |
| Power Supply Sensitivity | VDD = 5 V ± 5% | | ±1.5 | | | ±1.5 | | LSB |
| AC ACCURACY[6] | | | | | | | | |
| Dynamic Range | | | 90.5 | | | 93.8 | | dB[7] |
| Signal-to-Noise (SNR) | | | | | | | | |
| LFCSP | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | | 90 | | 92.5 | 93.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 4.096 V, internal REF | | 89 | | 91 | 92.3 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V, internal REF | | 86 | | 87.5 | 88.8 | | dB |

## SPECIFICATIONS

*Table 2. (Continued)*

| Parameter | Test Conditions/ Comments | AD7689A | | | AD7682B/AD7689B | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| WLCSP | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | | | | 91 | 92 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 4.096 V, internal REF | | | | 89.5 | 91 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V, internal REF | | | | 86 | 87.5 | | dB |
| SINAD[8] | | | | | | | | |
| LFCSP | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | | 89 | | 91 | 92.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V, −60 dB input | | 30.5 | | | 33.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 4.096 V, internal REF | | 88 | | 90 | 91 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V, internal REF | | 86 | | 87 | 88.4 | | dB |
| WLCSP | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | | | | 89.5 | 91 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V, −60 dB input | | | | | 32 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 4.096 V, internal REF | | | | 88.5 | 89.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V, internal REF | | | | 85.5 | 87 | | dB |
| Total Harmonic Distortion (THD) | $f_{IN}$ = 20 kHz | | −97 | | | −100 | | dB |
| Spurious-Free Dynamic Range (SFDR) | $f_{IN}$ = 20 kHz | | 105 | | | 110 | | dB |
| Channel to Channel Crosstalk | $f_{IN}$ = 100 kHz on adjacent channel(s) | | −120 | | | −125 | | dB |
| SAMPLING DYNAMICS | | | | | | | | |
| −3 dB Input Bandwidth | Full bandwidth | | 1.7 | | | 1.7 | | MHz |
| | ¼ bandwidth | | 0.425 | | | 0.425 | | MHz |
| Aperture Delay | VDD = 5 V | | 2.5 | | | 2.5 | | ns |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | Minimum temperature ($T_{MIN}$) to $T_{MAX}$ | −40 | | +85 | −40 | | +85 | °C |

1 CMRR means common-mode rejection ratio.

2 See the Analog Inputs section.

3 The bandwidth is set in the configuration register.

4 With the 5 V input range, one LSB is 76.3 µV.

5 See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.

6 With VDD = 5 V, unless otherwise noted.

7 All specifications expressed in decibels are referred to a full-scale input range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

8 See the Terminology section.

## SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, $V_{REF}$ = VDD, all specifications, $T_A$ = −40°C to +125°C, unless otherwise noted.

***Table 3.***

| | | AD7689C | | | |
|---|---|---|---|---|---|
| **Parameter** | **Test Conditions/Comments** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | | 16 | | | Bits |
| ANALOG INPUT | | | | | |
| Voltage Range | Unipolar mode | 0 | | $+V_{REF}$ | V |
| | Bipolar mode | $-V_{REF}/2$ | | $+V_{REF}/2$ | V |
| Absolute Input Voltage | Positive input, unipolar and bipolar modes | −0.1 | | $V_{REF}$ + 0.1 | V |
| | Negative or COM input, unipolar mode | −0.1 | | +0.1 | V |
| | Negative or COM input, bipolar mode | $V_{REF}/2$ − 0.1 | $V_{REF}/2$ | $V_{REF}/2$ + 0.1 | V |
| Analog Input CMRR | $f_{IN}$ = 250 kHz | | 68 | | dB |
| Leakage Current at 25°C | Acquisition phase | | 1 | | nA |
| Input Impedance[1] | | | | | |
| THROUGHPUT | | | | | |
| Conversion Rate | | | | | |
| Full Bandwidth[2] | VDD = 4.5 V to 5.5 V | 0 | | 250 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 200 | kSPS |
| ¼ Bandwidth[3] | VDD = 4.5 V to 5.5 V | 0 | | 62.5 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 50 | kSPS |
| Transient Response | Full-scale step, full bandwidth | | | 1.8 | µs |
| | Full-scale step, ¼ bandwidth | | | 14.5 | µs |
| ACCURACY | | | | | |
| No Missing Codes | | 16 | | | Bits |
| Integral Linearity Error | | −2.0 | ±0.4 | +2.0 | LSB[3] |
| Differential Linearity Error | | −1 | ±0.25 | +1.8 | LSB |
| Transition Noise | REF = VDD = 5 V | | 0.5 | | LSB |
| Gain Error[4] | | −8 | ±1 | +8 | LSB |
| Gain Error Match | | −4 | ±0.5 | +4 | LSB |
| Gain Error Temperature Drift | | | ±1 | | ppm/°C |
| Offset Error[5] | VDD = 4.5 V to 5.5 V | −8 | ±1 | +8 | LSB |
| | VDD = 2.3 V to 4.5 V | | ±5 | | LSB |
| Offset Error Match | | −6 | ±0.5 | +6 | LSB |
| Offset Error Temperature Drift | | | ±1 | | ppm/°C |
| Power Supply Sensitivity | VDD = 5 V ± 5% | | ±1.5 | | LSB |
| AC ACCURACY[5] | | | | | |
| Dynamic Range | | | 93.8 | | dB[6] |
| Signal-to-Noise | | | | | |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | 92 | 93.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 4.096 V, internal REF | 89.5 | 92.3 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V, internal REF | 86.5 | 88.8 | | dB |
| Total Harmonic Distortion (THD) | $f_{IN}$ = 20 kHz | | −100 | | dB |
| Spurious-Free Dynamic Range | $f_{IN}$ = 20 kHz | | 110 | | dB |
| Channel-to-Channel Crosstalk | $f_{IN}$ = 100 kHz on adjacent channel(s) | | −125 | | dB |

## SPECIFICATIONS

*Table 3. (Continued)*

| Parameter | Test Conditions/Comments | AD7689C Min | AD7689C Typ | AD7689C Max | Unit |
|---|---|---|---|---|---|
| SAMPLING DYNAMICS | | | | | |
| −3 dB Input Bandwidth | Full bandwidth | | 1.7 | | MHz |
| | ¼ bandwidth | | 0.425 | | MHz |
| Aperture Delay | VDD = 5 V | | 2.5 | | ns |
| TEMPERATURE RANGE | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$ | −40 | | +125 | °C |

[1] See the Analog Inputs section.

[2] The bandwidth is set in the configuration register.

[3] With the 5 V input range, one LSB is 76.3 µV.

[4] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.

[5] With VDD = 5 V, unless otherwise noted.

[6] All specifications expressed in decibels are referred to an FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, $V_{REF}$ = VDD, all specifications, $T_A$ = −40°C to +85°C or $T_A$ = −40°C to +125°C (AD7689C), unless otherwise noted.

*Table 4.*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| INTERNAL REFERENCE | | | | | |
| REF Output Voltage | 2.5 V at 25°C | 2.490 | 2.500 | 2.510 | V |
| | 4.096 V at 25°C | 4.086 | 4.096 | 4.106 | V |
| REFIN Output Voltage[1] | 2.5 V at 25°C | | 1.2 | | V |
| | 4.096 V at 25°C | | 2.3 | | V |
| REF Output Current | | | ±300 | | µA |
| Temperature Drift | | | ±10 | | ppm/°C |
| Line Regulation | VDD = 5 V ± 5% | | ±15 | | ppm/V |
| Long-Term Drift | 1000 hours | | 50 | | ppm |
| Turn-On Settling Time | Reference capacitor ($C_{REF}$) = 10 µF | | 5 | | ms |
| EXTERNAL REFERENCE | | | | | |
| Voltage Range | REF input | 0.5 | | VDD + 0.3 | V |
| | REFIN input (buffered) | 0.5 | | VDD − 0.5 | V |
| Current Drain[2] | 250 kSPS, REF = 5 V | | 50 | | µA |
| TEMPERATURE SENSOR | | | | | |
| Output Voltage[3] | 25°C | | 283 | | mV |
| Temperature Sensitivity | | | 1 | | mV/°C |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| Input Voltage | | | | | |
| Low ($V_{IL}$) | | −0.3 | | +0.3 × VIO | V |
| High ($V_{IH}$) | | 0.7 × VIO | | VIO + 0.3 | V |
| Input Current | | | | | |
| Low ($I_{IL}$) | | −1 | | +1 | µA |
| High ($I_{IH}$) | | −1 | | +1 | µA |
| DIGITAL OUTPUTS | | | | | |
| Data Format[4] | | | | | |
| Pipeline Delay[5] | | | | | |

## SPECIFICATIONS

*Table 4. (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage | | | | | |
| Low ($V_{OL}$) | Sink current ($I_{SINK}$) = 500 µA | | | 0.4 | V |
| High ($V_{OH}$) | Source current ($I_{SOURCE}$) = −500 µA | VIO − 0.3 | | | V |
| POWER SUPPLIES | | | | | |
| VDD[6] | Specified performance | 2.3 | | 5.5 | V |
| VIO | Specified performance | 1.8 | | VDD + 0.3 | V |
| Standby Current[7, 8] | VDD and VIO = 5 V at 25°C | | 50 | | nA |
| Power Dissipation | VDD = 2.5 V, 100 kSPS throughput | | 1.7 | | µW |
| | VDD = 2.5 V, 200 kSPS throughput | | 3.5 | | mW |
| | VDD = 5 V, 250 kSPS throughput | | 12.5 | 18 | mW |
| | VDD = 5 V, 250 kSPS throughput with internal reference | | 15.5 | 21 | mW |
| Energy per Conversion | VDD = 5 V | | 60 | | nJ |
| TEMPERATURE RANGE[9] | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$, AD7682B/AD7689B, AD7689A | −40 | | +85 | °C |
| | $T_{MIN}$ to $T_{MAX}$, AD7689C | −40 | | +125 | °C |

1 This is the output from the internal band gap.

2 This is an average current and scales with throughput.

3 The output voltage is internal and present on a dedicated multiplexer input.

4 Unipolar mode is serial 16-bit straight binary. Bipolar mode is serial, 16-bit twos complement.

5 Conversion results available immediately after completed conversion.

6 The minimum VDD supply must be 3 V when the 2.5 V internal reference is enabled, and 4.5 V when the 4.096 V internal reference is enabled. See Figure 23 for more information.

7 With all digital inputs forced to VIO or GND as required.

8 During acquisition phase.

9 Contact an Analog Devices, Inc., sales representative for the extended temperature range.

## TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 1.8 V to VDD, all specifications, $T_A$ = −40°C to +85°C or $T_A$ = −40°C to +125°C (AD7689C), unless otherwise noted. See Figure 2 and Figure 3 for load conditions.

*Table 5.*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CONVERSION TIME | | | | | |
| CNV Rising Edge to Data Available | $t_{CONV}$ | | | 2.2 | µs |
| ACQUISITION TIME | $t_{ACQ}$ | 1.8 | | | µs |
| TIME BETWEEN CONVERSIONS | $t_{CYC}$ | 4.0 | | | µs |
| DATA WRITE/READ DURING CONVERSION | $t_{DATA}$ | | | 1.2 | µs |
| SCK | | | | | |
| Period | $t_{SCK}$ | $t_{DSDO}$ + 2 | | | ns |
| Low Time | $t_{SCKL}$ | 11 | | | ns |
| High Time | $t_{SCKH}$ | 11 | | | ns |
| Falling Edge to Data Remains Valid | $t_{HSDO}$ | 4 | | | ns |
| Falling Edge to Data Valid Delay | $t_{DSDO}$ | | | | |
| VIO Above 2.7 V | | | | 18 | ns |
| VIO Above 2.3 V | | | | 23 | ns |
| VIO Above 1.8 V | | | | 28 | ns |

## SPECIFICATIONS

*Table 5. (Continued)*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CNV | | | | | |
| Pulse Width | $t_{CNVH}$ | 10 | | | ns |
| Low to SDO D15 MSB Valid | $t_{EN}$ | | | | |
| VIO Above 2.7 V | | | | 18 | ns |
| VIO Above 2.3 V | | | | 22 | ns |
| VIO Above 1.8 V | | | | 25 | ns |
| High or Last SCK Falling Edge to SDO High Impedance | $t_{DIS}$ | | | 32 | ns |
| Low to SCK Rising Edge | $t_{CLSCK}$ | 10 | | | ns |
| DIN | | | | | |
| Valid Setup Time from SCK Rising Edge | $t_{SDIN}$ | 5 | | | ns |
| Valid Hold Time from SCK Rising Edge | $t_{HDIN}$ | 5 | | | ns |

VDD = 2.3 V to 4.5 V, VIO = 1.8 V to VDD, all specifications, $T_A$ = −40°C to +85°C or $T_A$ = −40°C to +125°C (AD7689C), unless otherwise noted. See Figure 2 and Figure 3 for load conditions.

*Table 6.*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CONVERSION TIME | | | | | |
| CNV Rising Edge to Data Available, $T_A \le 85°C$ | $t_{CONV}$ | | | 3.2 | µs |
| CNV Rising Edge to Data Available, $T_A \le 125°C$ (AD7689C Only) | $t_{CONV}$ | | | 3.3 | µs |
| ACQUISITION TIME | | | | | |
| $T_A \le 85°C$ | $t_{ACQ}$ | 1.8 | | | µs |
| $T_A \le 125°C$ (AD7689C Only) | $t_{ACQ}$ | 1.7 | | | µs |
| TIME BETWEEN CONVERSIONS | $t_{CYC}$ | 5 | | | µs |
| DATA WRITE/READ DURING CONVERSION | $t_{DATA}$ | | | 1.2 | µs |
| SCK | | | | | |
| Period | $t_{SCK}$ | $t_{DSDO}$ + 2 | | | ns |
| Low Time | $t_{SCKL}$ | 12 | | | ns |
| High Time | $t_{SCKH}$ | 12 | | | ns |
| Falling Edge to Data Remains Valid | $t_{HSDO}$ | 5 | | | ns |
| Falling Edge to Data Valid Delay | $t_{DSDO}$ | | | | |
| VIO Above 3 V, $T_A \le 85°C$ | | | | 24 | ns |
| VIO Above 3 V, $T_A \le 125°C$, (AD7689C Only) | | | | 30 | ns |
| VIO Above 2.7 V, $T_A \le 85°C$ | | | | 30 | ns |
| VIO Above 2.7 V, $T_A \le 125°C$, (AD7689C Only) | | | | 36 | ns |
| VIO Above 2.3 V, $T_A \le 85°C$ | | | | 38 | ns |
| VIO Above 2.3 V, $T_A \le 125°C$, (AD7689C Only) | | | | 44 | ns |
| VIO Above 1.8 V, $T_A \le 85°C$ | | | | 48 | ns |
| VIO Above 1.8 V, $T_A \le 125°C$, (AD7689C Only) | | | | 54 | ns |
| CNV | $t_{EN}$ | | | | |
| Pulse Width | $t_{CNVH}$ | 10 | | | ns |
| Low to SDO D15 MSB Valid | | | | | |
| VIO Above 3 V, $T_A \le 85°C$ | | | | 21 | ns |
| VIO Above 3 V, $T_A \le 125°C$, (AD7689C Only) | | | | 27 | ns |
| VIO Above 2.7 V, $T_A \le 85°C$ | | | | 27 | ns |
| VIO Above 2.7 V, $T_A \le 125°C$, (AD7689C Only) | | | | 33 | ns |
| VIO Above 2.3 V, $T_A \le 85°C$ | | | | 35 | ns |
| VIO Above 2.3 V, $T_A \le 125°C$, (AD7689C Only) | | | | 41 | ns |

## SPECIFICATIONS

*Table 6. (Continued)*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIO Above 1.8 V, $T_A \leq 85°C$ | | | | 45 | ns |
| VIO Above 1.8 V, $T_A \leq 125°C$, (AD7689C Only) | | | | 51 | ns |
| High or Last SCK Falling Edge to SDO High Impedance | $t_{DIS}$ | | | 50 | ns |
| Low to SCK Rising Edge | $t_{CLSCK}$ | 10 | | | ns |
| DIN | | | | | |
| Valid Setup Time from SCK Rising Edge | $t_{SDIN}$ | 5 | | | ns |
| Valid Hold Time from SCK Rising Edge | $t_{HDIN}$ | 5 | | | ns |

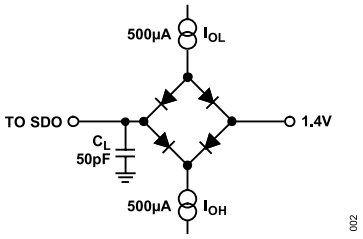



*Figure 2. Load Circuit for Digital Interface Timing*

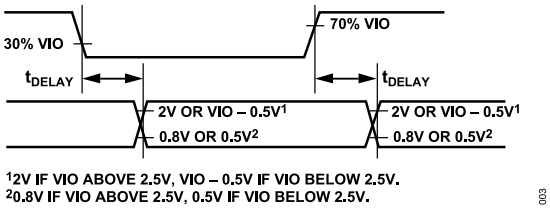



*Figure 3. Voltage Levels for Timing*

## ABSOLUTE MAXIMUM RATINGS

*Table 7.*

| Parameter | Rating |
|---|---|
| Analog Inputs | |
| INx,[1] COM | GND − 0.3 V to VDD + 0.3 V or VDD ± 130 mA |
| REF, REFIN | GND − 0.3 V to VDD + 0.3 V |
| Supply Voltages | |
| VDD, VIO to GND | −0.3 V to +7 V |
| VIO to VDD | −0.3 V to VDD + 0.3 V |
| DIN, CNV, SCK to GND | −0.3 V to VIO + 0.3 V |
| SDO to GND | −0.3 V to VIO + 0.3 V |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Thermal Impedance (LFCSP) | |
| $\theta_{JA}$ | 48°C/W |
| $\theta_{JC}$ | 4.4°C/W |

[1] See the Analog Inputs section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

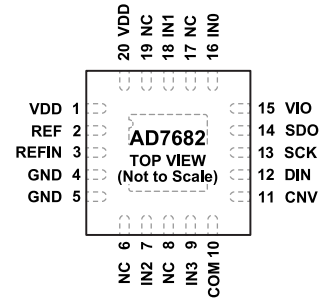



*Figure 4. AD7682 LFCSP Pin Configuration*

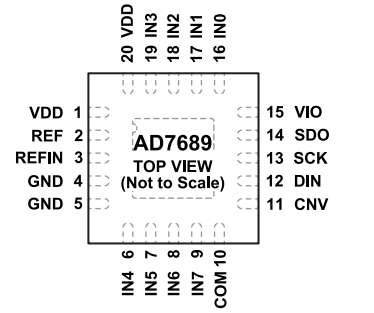



*Figure 5. AD7689 LFCSP Pin Configuration*

*Table 8. AD7682 LFCSP and AD7689 LFCSP Pin Function Descriptions*

| | LFCSP Mnemonic | | | |
|---|---|---|---|---|
| Pin No. | AD7682 | AD7689 | Type[1] | Description |
| 1, 20 | VDD | VDD | P | Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for a 2.5 V output, the minimum must be 3.0 V. When using the internal reference for 4.096 V output, the minimum must be 4.5 V. |
| 2 | REF | REF | AI/O | Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference of 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (VDD − 0.5 V, maximum), which is useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section. |
| 3 | REFIN | REFIN | AI/O | Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and requires decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and (VDD − 0.5 V) that is buffered to the REF pin, as described in the REF pin description. |
| 4, 5 | GND | GND | P | Power Supply Ground. |
| 6 | NC | IN4 | AI | No Connection (AD7682).<br>Analog Input Channel 4 (AD7689). |
| 7 | IN2 | IN5 | AI | Analog Input Channel 2 (AD7682).<br>Analog Input Channel 5 (AD7689). |
| 8 | NC | IN6 | AI | No Connection (AD7682).<br>Analog Input Channel 6 (AD7689). |
| 9 | IN3 | IN7 | AI | Analog Input Channel 3 (AD7682).<br>Analog Input Channel 7 (AD7689). |
| 10 | COM | COM | AI | Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V. |
| 11 | CNV | CNV | DI | Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indictor is enabled. |
| 12 | DIN | DIN | DI | Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion. |
| 13 | SCK | SCK | DI | Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion. |
| 14 | SDO | SDO | DO | Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary. In bipolar modes, conversion results are twos complement. |
| 15 | VIO | VIO | P | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). |

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

*Table 8. AD7682 LFCSP and AD7689 LFCSP Pin Function Descriptions (Continued)*

| | LFCSP Mnemonic | | | |
|---|---|---|---|---|
| Pin No. | AD7682 | AD7689 | Type[1] | Description |
| 16 | IN0 | IN0 | AI | Analog Input Channel 0. |
| 17 | NC | IN1 | AI | No Connection (AD7682).<br>Analog Input Channel 1 (AD7689). |
| 18 | IN1 | IN2 | AI | Analog Input Channel 1 (AD7682).<br>Analog Input Channel 2 (AD7689). |
| 19 | NC | IN3 | AI | No Connection (AD7682).<br>Analog Input Channel 3 (AD7689). |
| 21 | EPAD | EPAD | NC | Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane. |

[1] AI means analog input, AI/O means analog input/output, DI means digital input, DO means digital output, P means power, and NC means no internal connection.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

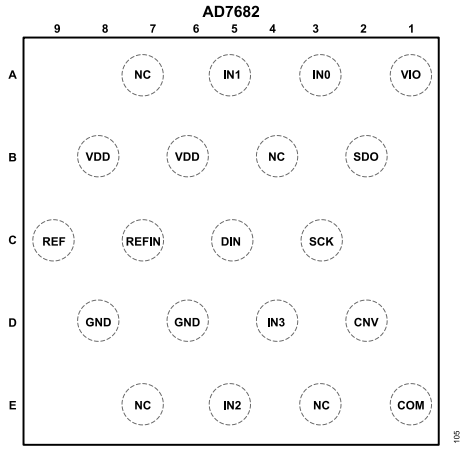



*Figure 6. AD7682 WLCSP Pin Configuration*

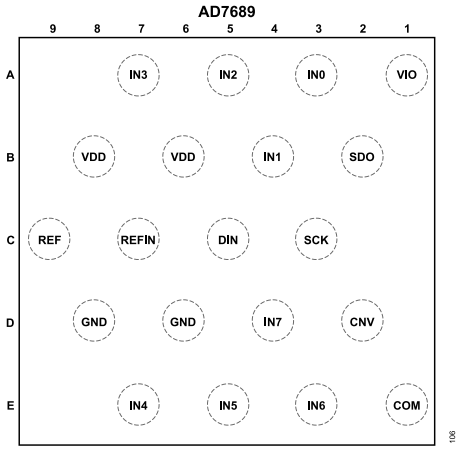



*Figure 7. AD7689 WLCSP Pin Configuration*

*Table 9. AD7682 WLCSP and AD7689 WLCSP Pin Function Descriptions*

| | WLCSP Mnemonic | | | |
|---|---|---|---|---|
| **Pin No.** | **AD7682** | **AD7689** | **Type[1]** | **Description** |
| B6, B8 | VDD | VDD | P | Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for a 2.5 V output, the minimum must be 3.0 V. When using the internal reference for 4.096 V output, the minimum must be 4.5 V. |
| C9 | REF | REF | AI/O | Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference of 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (VDD − 0.5 V, maximum), which is useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section. |
| C7 | REFIN | REFIN | AI/O | Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and requires decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and (VDD − 0.5 V) that is buffered to the REF pin, as described in the REF pin description. |
| D6, D8 | GND | GND | P | Power Supply Ground. |
| A7 | NC | IN3 | AI | No Connection (AD7682).<br>Analog Input Channel 3 (AD7689). |
| E5 | IN2 | IN5 | AI | Analog Input Channel 2 (AD7682).<br>Analog Input Channel 5 (AD7689). |
| E3 | NC | IN6 | AI | No Connection (AD7682).<br>Analog Input Channel 6 (AD7689). |
| D4 | IN3 | IN7 | AI | Analog Input Channel 3 (AD7682).<br>Analog Input Channel 7 (AD7689). |
| E1 | COM | COM | AI | Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V. |
| D2 | CNV | CNV | DI | Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indictor is enabled. |
| C5 | DIN | DIN | DI | Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion. |
| C3 | SCK | SCK | DI | Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion. |
| B2 | SDO | SDO | DO | Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary. In bipolar modes, conversion results are twos complement. |
| A1 | VIO | VIO | P | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). |

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

*Table 9. AD7682 WLCSP and AD7689 WLCSP Pin Function Descriptions (Continued)*

| | WLCSP Mnemonic | | | |
|---|---|---|---|---|
| Pin No. | AD7682 | AD7689 | Type[1] | Description |
| A3 | IN0 | IN0 | AI | Analog Input Channel 0. |
| B4 | NC | IN1 | AI | No connection (AD7682).<br>Analog Input Channel 1 (AD7689). |
| A5 | IN1 | IN2 | AI | Analog Input Channel 1 (AD7682).<br>Analog Input Channel 2 (AD7689). |
| E7 | NC | IN4 | AI | No Connection (AD7682).<br>Analog Input Channel 4 (AD7689). |

[1] AI means analog input, AI/O means analog input/output, DI means digital input, DO means digital output, P means power, and NC means no internal connection.

## TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V to 5.5 V, $V_{REF}$ = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

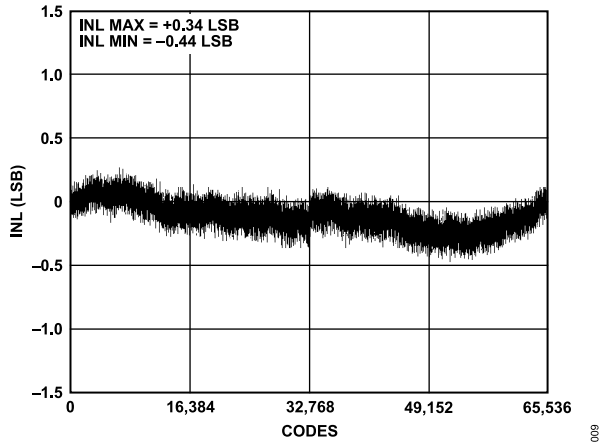



Figure 8. Integral Nonlinearity vs. Code, $V_{REF}$ = VDD = 5 V

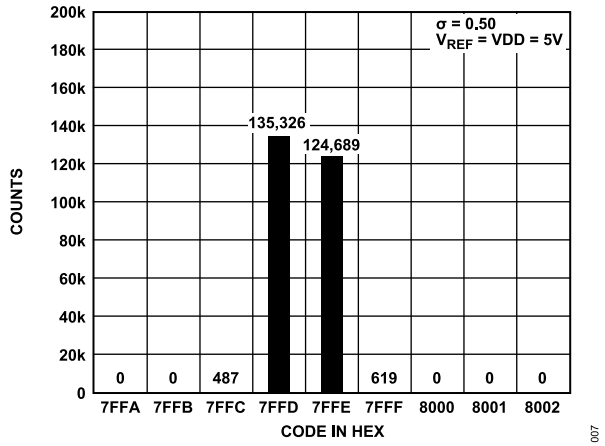



Figure 9. Histogram of a DC Input at Code Center

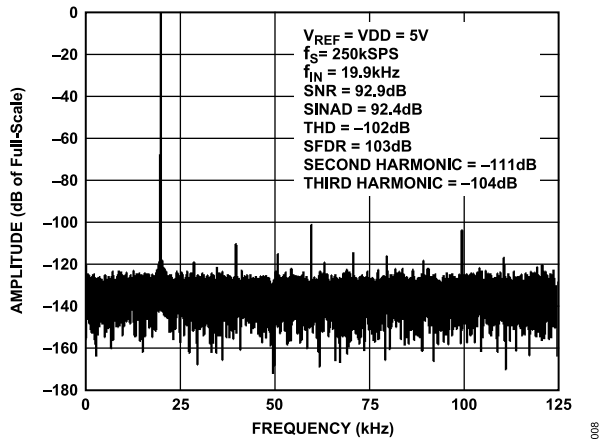



Figure 10. 20 kHz Fast Fourier Transform (FFT), $V_{REF}$ = VDD = 5 V

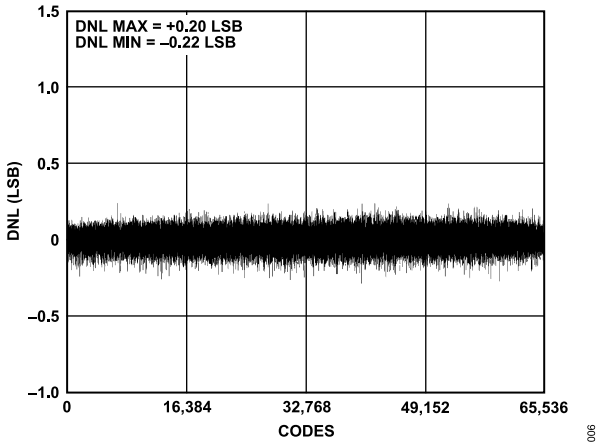



Figure 11. Differential Nonlinearity vs. Code, $V_{REF}$ = VDD = 5 V

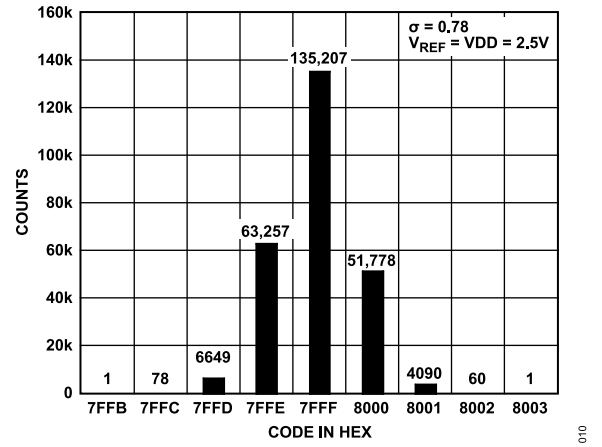



Figure 12. Histogram of a DC Input at Code Center

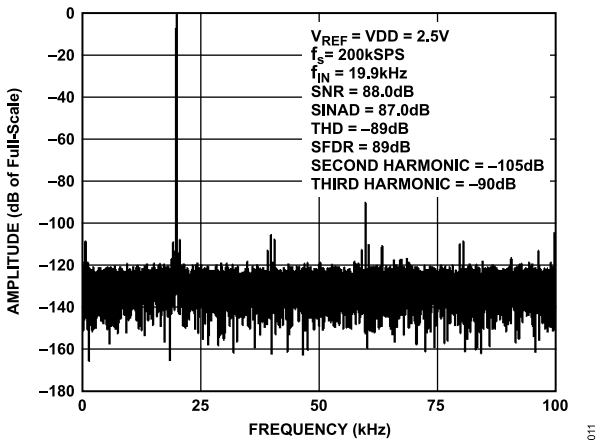



Figure 13. 20 kHz FFT, $V_{REF}$ = VDD = 2.5 V

## TYPICAL PERFORMANCE CHARACTERISTICS

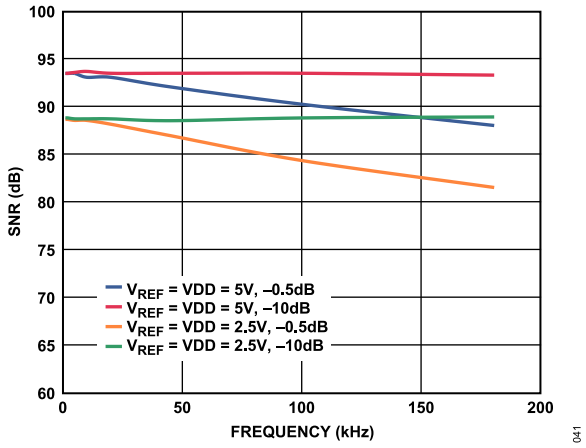



Figure 14. SNR vs. Frequency

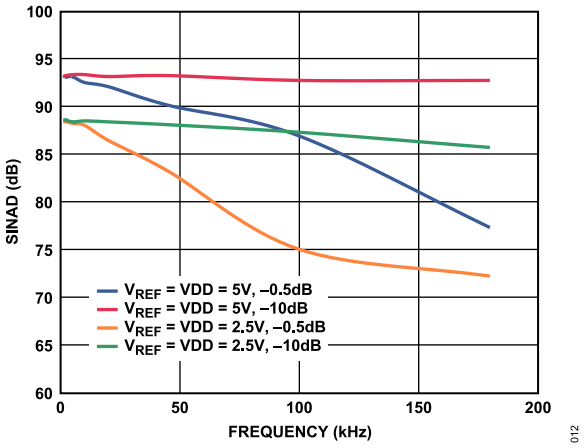



Figure 17. SINAD vs. Frequency

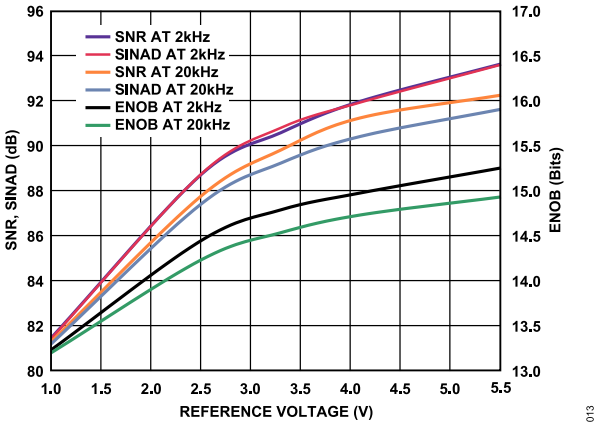



Figure 15. SNR, SINAD, and Effective Number of Bits (ENOB) vs. Reference Voltage

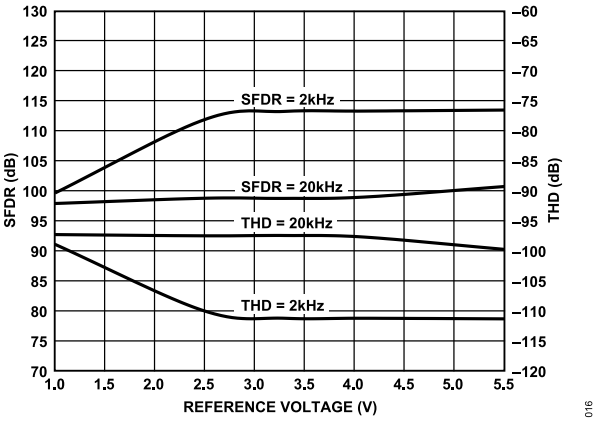



Figure 18. Spurious-Free Dynamic Range (SFDR) and THD vs. Reference Voltage

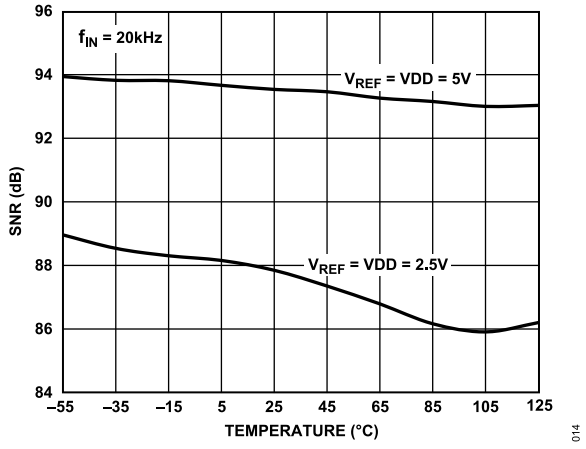



Figure 16. SNR vs. Temperature

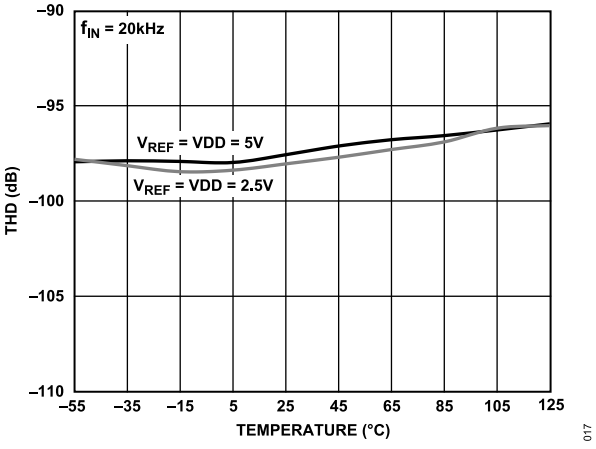



Figure 19. THD vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS

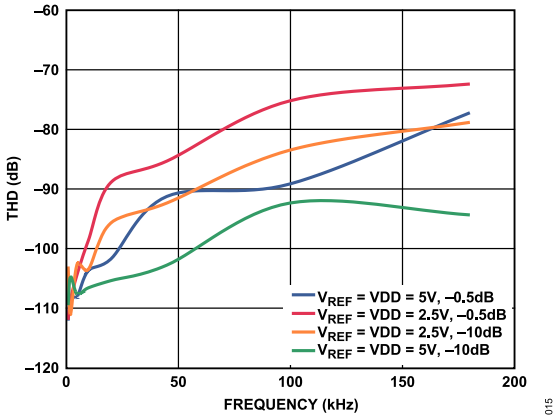



Figure 20. THD vs. Frequency

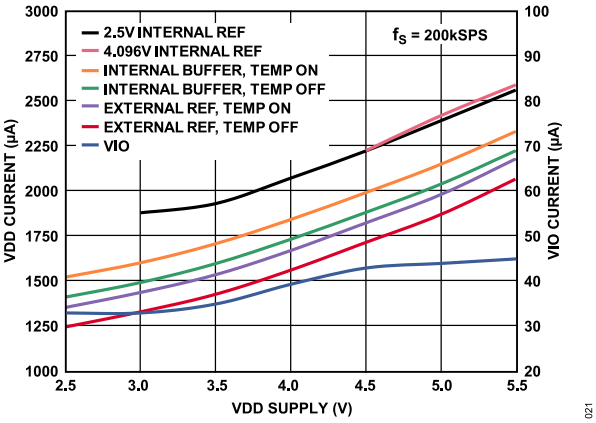



Figure 23. Operating Currents vs. Supply

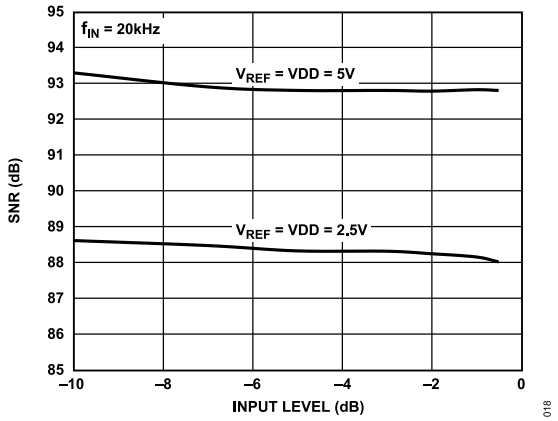



Figure 21. SNR vs. Input Level

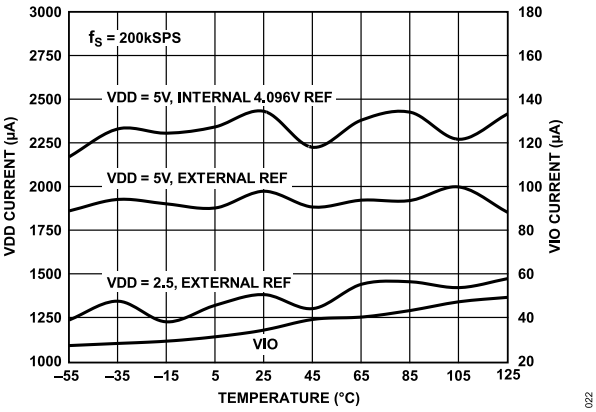



Figure 24. Operating Currents vs. Temperature

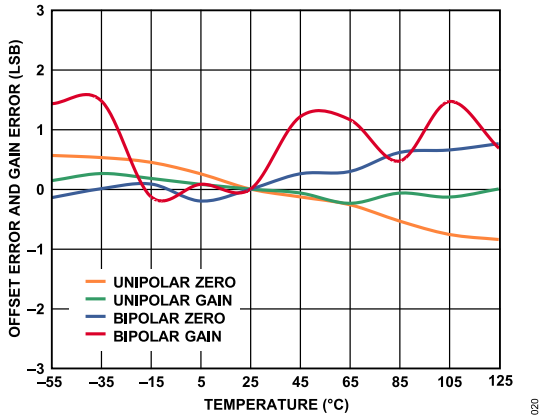



Figure 22. Offset and Gain Error vs. Temperature

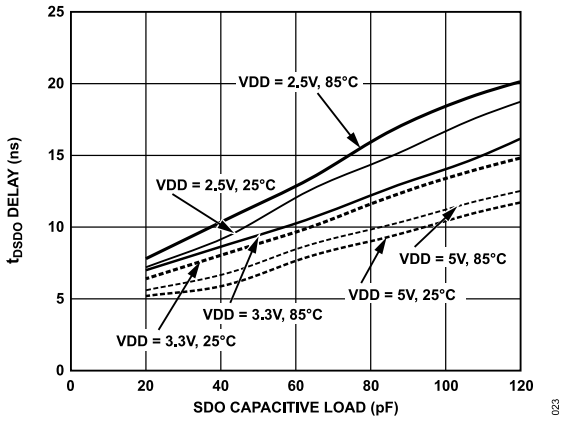



Figure 25. $t_{DSDO}$ Delay vs. SDO Capacitance Load and Supply

## TERMINOLOGY

### Least Significant Bit (LSB)

The LSB is the smallest increment represented by a converter. For an ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (V) = V_{REF}/2^N \quad (1)$$

### Integral Nonlinearity Error (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 27).

### Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

### Offset Error

The first transition must occur at a level ½ LSB above analog ground. The offset error is the deviation of the actual transition from that point.

### Gain Error

The last transition (from 111…10 to 111…11) must occur for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation in LSB (or percentage of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or percentage of full-scale range), which includes the effects of the offset error.

### Aperture Delay

Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

### Transient Response

Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

### Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

### Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

### Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

### Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the formula

$$ENOB = (SINAD_{dB} - 1.76)/6.02 \quad (2)$$

and is expressed in bits.

### Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a dc to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel, and is expressed in decibels.

### Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage ($V_{REF}$) measured at $T_{MIN}$, T (25°C), and $T_{MAX}$. It is expressed in ppm/°C as

$$TVC_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6 \quad (3)$$

where:
$V_{REF}$ *(Max)* = maximum $V_{REF}$ at $T_{MIN}$, T (25°C), or $T_{MAX}$.
$V_{REF}$ *(Min)* = minimum $V_{REF}$ at $T_{MIN}$, T (25°C), or $T_{MAX}$.
$V_{REF}$ *(25°C)* = $V_{REF}$ at 25°C.
$T_{MAX}$ = 85°C.
$T_{MIN}$ = –40°C.

## THEORY OF OPERATION

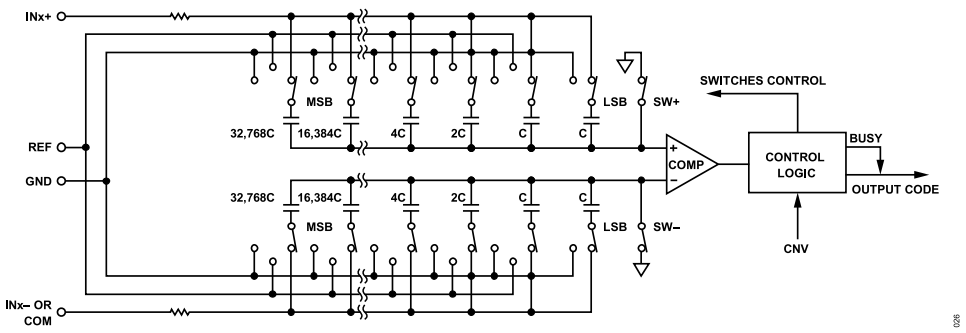



*Figure 26. ADC Simplified Schematic*

### OVERVIEW

The AD7682/AD7689 are 4-channel/8-channel, 16-bit, charge redistribution SAR ADCs. These devices are capable of converting 250,000 samples per second (250 kSPS) and power down between conversions. For example, when operating with an external reference at 1 kSPS, they consume 17 µW typically, ideal for battery-powered applications.

The AD7682/AD7689 contain all of the components for use in a multichannel, low power data acquisition system, including the following:

- 16-bit SAR ADC with no missing codes
- 4-channel/8-channel, low crosstalk multiplexer
- Internal low drift reference and buffer
- Temperature sensor
- Selectable one-pole filter
- Channel sequencer

These components are configured through an SPI-compatible, 14-bit register. Conversion results, also SPI compatible, can be read after or during conversions with the option for reading back the configuration associated with the conversion.

The AD7682/AD7689 provide the user with an on-chip track-and-hold and do not exhibit pipeline delay or latency.

The AD7682/AD7689 are specified from 2.3 V to 5.5 V and can be interfaced to any 1.8 V to 5 V digital logic family. They are housed in a 20-lead, 4 mm × 4 mm LFCSP and a 20-lead, 2.4 mm × 2.4 mm WLCSP that combine space savings and allow flexible configurations. They are pin-for-pin compatible with the 16-bit AD7699 and 14-bit AD7949.

### CONVERTER OPERATION

The AD7682/AD7689 are successive approximation ADCs based on a charge redistribution DAC. Figure 26 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs.

The capacitor arrays are used as sampling capacitors and acquire the analog signal on the INx+ and INx− (or COM) inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− open first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the INx+ and INx− (or COM) inputs captured at the end of the acquisition phase applies to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 ... V_{REF}/32,768$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7682/AD7689 have an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

## THEORY OF OPERATION

### TRANSFER FUNCTIONS

With the inputs configured for unipolar range (single-ended, COM with ground sense, or paired differentially with INx− as ground sense), the data output is straight binary.

With the inputs configured for bipolar range (COM = $V_{REF}/2$ or paired differentially with INx− = $V_{REF}/2$), the data outputs are twos complement.

The ideal transfer characteristic for the AD7682/AD7689 is shown in Figure 27 and for both unipolar and bipolar ranges with the internal 4.096 V reference.

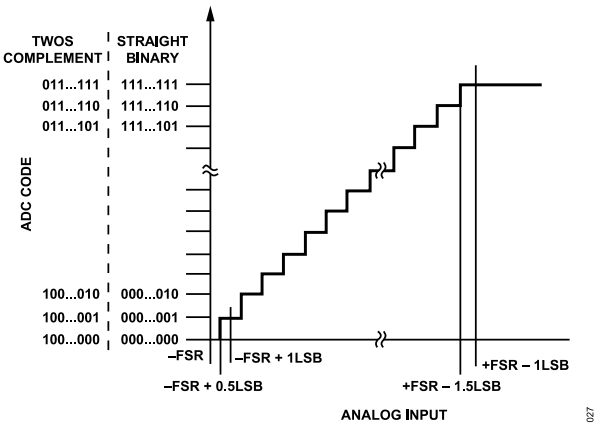



*Figure 27. ADC Ideal Transfer Function*

*Table 10. Output Codes and Ideal Input Voltages*

| Description | Unipolar Analog Input[1] ($V_{REF}$ = 4.096 V) | Digital Output Code (Straight Binary Hex) | Bipolar Analog Input[2] ($V_{REF}$ = 4.096 V) | Digital Output Code (Twos Complement Hex) |
|---|---|---|---|---|
| FSR − 1 LSB | 4.095938 V | 0xFFFF[3] | 2.047938 V | 0x7FFF[3] |
| Midscale + 1 LSB | 2.048063 V | 0x8001 | 62.5 µV | 0x0001 |
| Midscale | 2.048 V | 0x8000 | 0 V | 0x0000 |
| Midscale − 1 LSB | 2.047938 V | 0x7FFF | −62.5 µV | 0xFFFF |
| −FSR + 1 LSB | 62.5 µV | 0x0001 | −2.047938 V | 0x8001 |
| −FSR | 0 V | 0x0000[4] | −2.048 V | 0x8000[4] |

1 With COM or INx− = 0 V or all INx referenced to GND.

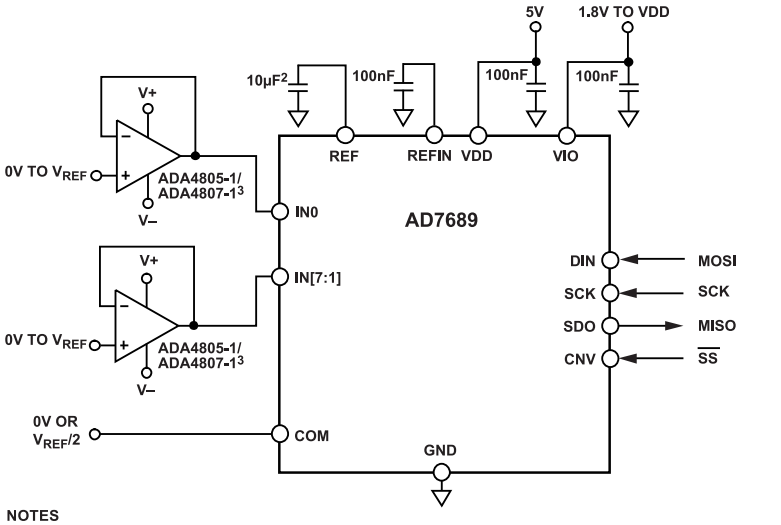
2 With COM or INx− = $V_{REF}/2$.

3 This is also the code for an overranged analog input ((INx+) − (INx−), or COM, above $V_{REF}$ − GND).

4 This is also the code for an underranged analog input ((INx+) − (INx−), or COM, below GND).

## THEORY OF OPERATION

### TYPICAL CONNECTION DIAGRAMS




NOTES
1. INTERNAL REFERENCE SHOWN. SEE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2. $C_{REF}$ IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

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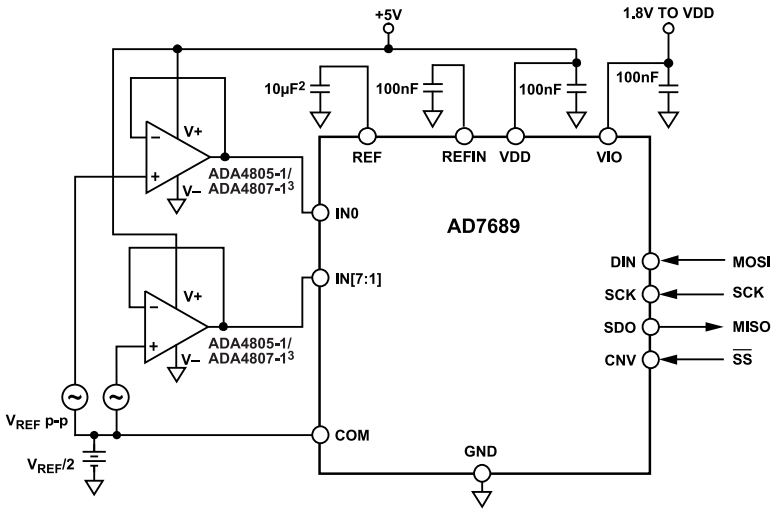
*Figure 28. Typical Application Diagram with Multiple Supplies*




NOTES
1. INTERNAL REFERENCE SHOWN. SEE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2. $C_{REF}$ IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

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*Figure 29. Typical Application Diagram Using Bipolar Input*

## THEORY OF OPERATION

### Unipolar or Bipolar

Figure 28 shows an example of the recommended connection diagram for the AD7682/AD7689 when multiple supplies are available.

### Bipolar Single Supply

Figure 29 shows an example of a system with a bipolar input using single supplies with the internal reference (optional different VIO supply). This circuit is also useful when the amplifier/signal conditioning circuit is remotely located with some common mode present. Note that for any input configuration, the INx inputs are unipolar and are always referenced to GND (no negative voltages even in bipolar range).

For this circuit, a rail-to-rail input/output amplifier can be used. However, take the offset voltage vs. input common-mode range into consideration (1 LSB = 62.5 µV with $V_{REF}$ = 4.096 V). Note that the conversion results are in twos complement format when using the bipolar input configuration. Refer to the AN-581 Application Note, *Biasing and Decoupling Op Amps in Single Supply Applications,* for additional details about using single-supply amplifiers.

## ANALOG INPUTS

### Input Structure

Figure 30 shows an equivalent circuit of the input structure of the AD7682/AD7689. The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN[7:0] and COM. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V because this causes the diodes to become forward biased and to start conducting current.

These diodes can handle a maximum forward-biased current of 130 mA. For instance, these conditions may eventually occur when the input buffer supplies are different from VDD. In such a case, for example, an input buffer with a short circuit, the current limitation can be used to protect the device.

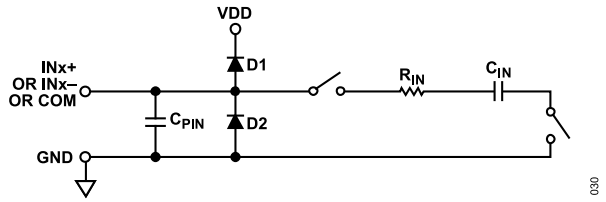



*Figure 30. Equivalent Analog Input Circuit*

This analog input structure allows the sampling of the true differential signal between INx+ and COM or INx+ and INx−. (COM or INx− = GND ± 0.1 V or $V_{REF}$ ± 0.1 V). By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 31.

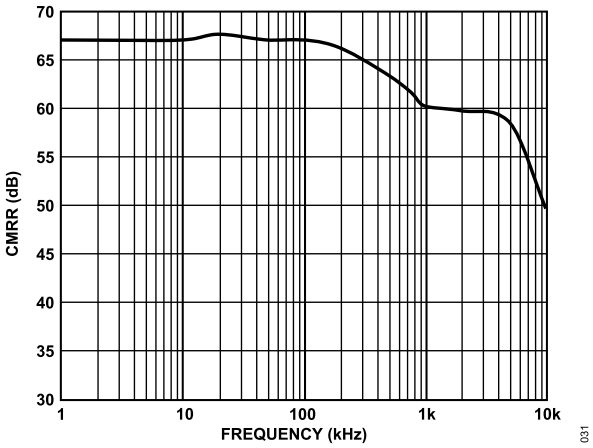



*Figure 31. Analog Input CMRR vs. Frequency*

During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, $C_{PIN}$, and the network formed by the series connection of $R_{IN}$ and $C_{IN}$. $C_{PIN}$ is primarily the pin capacitance. $R_{IN}$ is typically 2.2 kΩ and is a lumped component composed of serial resistors and the on resistance of the switches. $C_{IN}$ is typically 27 pF and is mainly the ADC sampling capacitor.

### Selectable Low-Pass Filter

During the conversion phase, when the switches are opened, the input impedance is limited to $C_{PIN}$. While the AD7682/AD7689 are acquiring, $R_{IN}$ and $C_{IN}$ make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise from the driving circuitry. The low-pass filter can be programmed for the full bandwidth or ¼ of the bandwidth with CFG[6], as shown in Table 13. This setting changes $R_{IN}$ to 19 kΩ. Note that the converter throughput must also be reduced by ¼ when using the filter. If the maximum throughput is used with the bandwidth (BW) set to ¼, the converter acquisition time, $t_{ACQ}$, is violated, resulting in increased THD.

## THEORY OF OPERATION

### Input Configurations

Figure 32 shows the different methods for configuring the analog inputs with the configuration register, CFG[12:10]. Refer to the Configuration Register, CFG section for more details.

The analog inputs can be configured as shown in the following figures:

- Figure 32 (A), single-ended referenced to system ground, CFG[12:10] = $111_2$. In this configuration, all inputs (IN[7:0]) have a range of GND to $V_{REF}$.
- Figure 32 (B), bipolar differential with a common reference point, COM = $V_{REF}/2$, CFG[12:10] = $010_2$. Unipolar differential with COM connected to a ground sense; CFG[12:10] = $110_2$. In this configuration, all inputs IN[7:0] have a range of GND to $V_{REF}$.
- Figure 32 (C), bipolar differential pairs with the negative input channel referenced to $V_{REF}/2$, CFG[12:10] = $00X_2$. Unipolar differential pairs with the negative input channel referenced to a ground sense, CFG[12:10] = $10X_2$. In these configurations, the positive input channels have the range of GND to $V_{REF}$. The negative input channels are a sense referred to $V_{REF}/2$ for bipolar pairs, or GND for unipolar pairs. The positive channel is configured with CFG[9:7]. If CFG[9:7] is even, then IN0, IN2, IN4, and IN6 are used. If CFG[9:7] is odd, then IN1, IN3, IN5, and IN7 are used, as indicated by the channels with parentheses in Figure 32 (C). For example, for IN0/IN1 pairs with the positive channel on IN0, CFG[9:7] = $000_2$. For IN4/IN5 pairs with the positive channel on IN5, CFG[9:7] = $101_2$. Note that for the sequencer, detailed in the Channel Sequencer section, the positive channels are always IN0, IN2, IN4, and IN6.
- Figure 32 (D), inputs configured in any of the preceding combinations (showing that the AD7682/AD7689 can be configured dynamically).

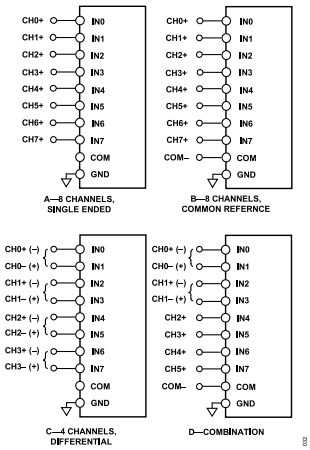



*Figure 32. Multiplexed Analog Input Configurations*

### Sequencer

The AD7682/AD7689 include a channel sequencer useful for scanning channels in a repeated fashion. Refer to the Channel Sequencer section for further details on the sequencer operation.

### Source Resistance

When the source impedance of the driving circuit is low, the AD7682/AD7689 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

## THEORY OF OPERATION

### DRIVER AMPLIFIER CHOICE

Although the AD7682/AD7689 are easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7682/AD7689. Note that the AD7682/AD7689 have a noise much lower than most other 16-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise from the amplifier is filtered by the AD7682/AD7689 analog input circuit low-pass filter made by $R_{IN}$ and $C_{IN}$, or by an external filter, if one is used. Because the typical noise of the AD7682/AD7689 is 35 µV rms (with $V_{REF}$ = 5 V), the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{35}{\sqrt{35^2 + \frac{\pi}{2}f_{-3db}(Ne_N)^2}}\right) \quad (4)$$

  where:
  $f_{-3dB}$ is the input bandwidth in megahertz of the AD7682/AD7689 (1.7 MHz in full BW or 425 kHz in ¼ BW), or the cutoff frequency of an input filter, if one is used.
  $N$ is the noise gain of the amplifier (for example, 1 in buffer configuration).
  $e_N$ is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver must have a THD performance commensurate with the AD7682/AD7689. Figure 20 shows THD vs. frequency for the AD7682/AD7689.
- For multichannel, multiplexed applications on each input or input pair, the driver amplifier and the AD7682/AD7689 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

*Table 11. Recommended Driver Amplifiers*

| Amplifier | Typical Application |
|---|---|
| ADA4805-1 | Low noise, small size, and low power |
| ADA4807-1 | Very low noise and high frequency |
| ADA4627-1 | Precision, low noise, and low input bias |
| ADA4522-1 | Precision, zero drift, and electromagnetic interference (EMI) enhanced |
| ADA4500-2 | Precision, rail-to-rail input/output, and zero input crossover distortion |

### VOLTAGE REFERENCE OUTPUT/INPUT

The AD7682/AD7689 allow the choice of a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7682/AD7689 provide excellent performance and can be used in almost all applications. There are six possible choices of voltage reference schemes, briefly described in Table 13, with more details in each of the following sections.

#### Internal Reference/Temperature Sensor

The precision internal reference, suitable for most applications, can be set for either a 2.5 V or a 4.096 V output, as detailed in Table 13. With the internal reference enabled, the band gap voltage is also present on the REFIN pin, which requires an external 0.1 µF capacitor. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the AD8605. Note that the voltage of REFIN changes depending on the 2.5 V or 4.096 V internal reference.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the AD7682/AD7689, and is therefore useful for performing a system calibration. For applications requiring the use of the temperature sensor, the internal reference must be active (internal buffer can be disabled in this case). Note that, when using the temperature sensor, the output is straight binary referenced from the AD7682/AD7689 GND pin.

The internal reference is temperature compensated to within 10 mV. The reference is trimmed to provide a typical drift of ±10 ppm/°C.

Connect the AD7682/AD7689 as shown in Figure 33 for either a 2.5 V or 4.096 V internal reference.

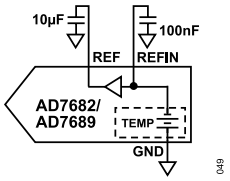



*Figure 33. 2.5 V or 4.096 V Internal Reference Connection*

## THEORY OF OPERATION

### External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer, as shown in Figure 34. The external source is connected to REFIN, the input to the on-chip unity-gain buffer, and the output is produced on the REF pin. An external reference can be used with the internal buffer with or without the temperature sensor enabled. Refer to Table 13 for register details. With the buffer enabled, the gain is unity and is limited to an input/output of VDD = −0.2 V. However, the maximum voltage allowable must be ≤VDD − 0.5 V.

The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications. In addition, a low power reference can be used because the internal buffer provides the necessary performance to drive the SAR architecture of the AD7682/AD7689.

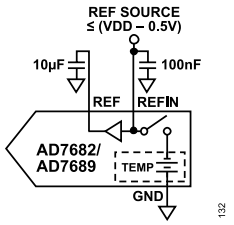



*Figure 34. External Reference Using Internal Buffer*

### External Reference

In any of the six voltage reference schemes, an external reference can be connected directly on the REF pin as shown in Figure 35 because the output impedance of REF is >5 kΩ. To reduce power consumption, power down the reference and buffer. Refer to Table 13 for register details. For improved drift performance, an external reference from the family of devices that includes the ADR430, ADR431, ADR433, ADR434, and ADR435, or the family of devices that includes the ADR440, ADR441, ADR443, ADR444, and ADR445 is recommended.

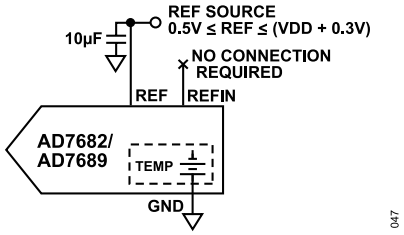



*Figure 35. External Reference*

Note that the best SNR is achieved with a 5 V external reference as the internal reference is limited to 4.096 V. The SNR degradation is as follows:

$$SNR_{LOSS} = 20\log\frac{4.096}{5} \quad (5)$$

### Reference Decoupling

Whether using an internal or external reference, the AD7682/AD7689 voltage reference output/input, REF, has a dynamic input impedance and must be driven by a low impedance source with efficient decoupling between the REF and GND pins. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and GND with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor is appropriate when using the internal reference, a member of the ADR430, ADR431, ADR433, ADR434, and ADR435 family of external references, a member of the ADR440, ADR441, ADR443, ADR444, and ADR445 family of external references, or a low impedance buffer such as the AD8031 or the AD8605.

The placement of the reference decoupling capacitor is also important to the performance of the AD7682/AD7689, as explained in the Layout section. Mount the decoupling capacitor with a thick PCB trace on the same side as the ADC at the REF pin. The GND must also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially on DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

For applications that use multiple AD7682/AD7689 devices or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the temperature coefficient. For instance, a ±10 ppm/°C temperature coefficient of the reference changes full scale by ±1 LSB/°C.

## THEORY OF OPERATION

### POWER SUPPLY

The AD7682/AD7689 use two power supply pins: an analog and digital core supply (VDD), and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD pins can be tied together. The AD7682/AD7689 are independent of power supply sequencing between VIO and VDD. Additionally, they are very insensitive to power supply variations over a wide frequency range, as shown in Figure 36.

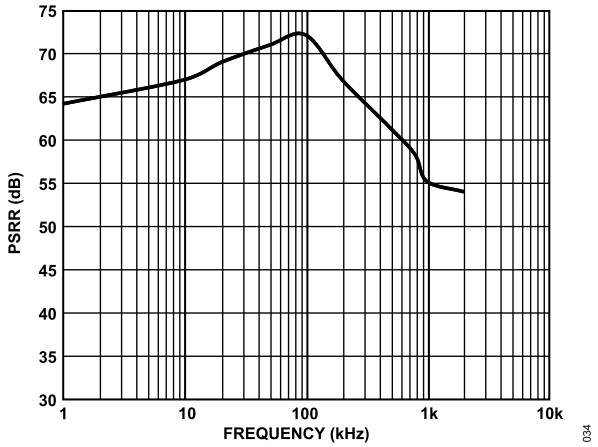



*Figure 36. Power Supply Rejection Ratio (PSRR) vs. Frequency*

The AD7682/AD7689 power down automatically at the end of each conversion phase. Therefore, the operating currents and power scale linearly with the sampling rate. This makes the device ideal for low sampling rates (even of a few hertz), and low battery-powered applications.

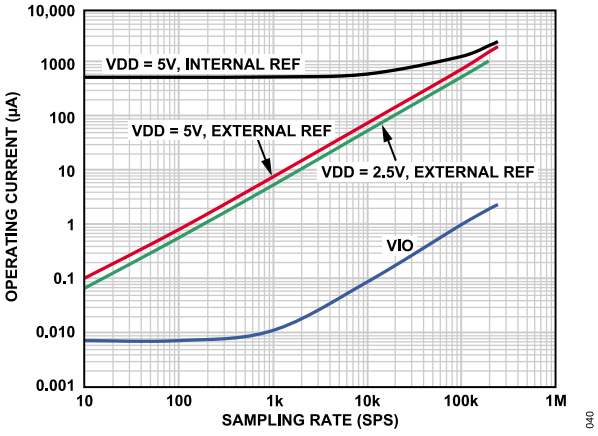



*Figure 37. Operating Currents vs. Sampling Rate*

### SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7682/AD7689, with their low operating current, can be supplied directly using an external reference circuit like the one shown in Figure 38. The reference line can be driven by the following:

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR430, ADR431, ADR433, ADR434, ADR435, ADR440, ADR441, ADR443, ADR444, or ADR445.
- A reference buffer, such as the AD8605, which can also filter the system power supply, as shown in Figure 38.

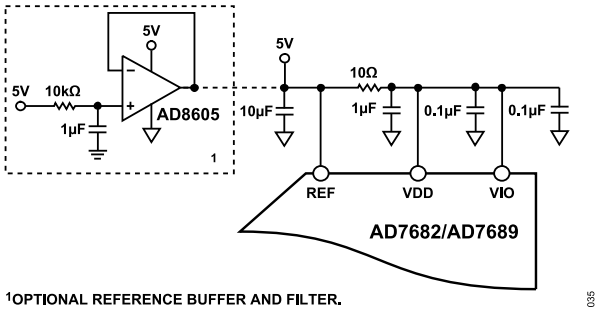



*Figure 38. Example of an Application Circuit*

## DIGITAL INTERFACE

The AD7682/AD7689 use a simple 4-wire interface and are compatible with SPI, MICROWIRE™, QSPI™, digital hosts, and DSPs (for example, Blackfin® ADSP-BF53x, SHARC®, ADSP-219x, and ADSP-218x).

The interface uses the CNV, DIN, SCK, and SDO signals and allows CNV, which initiates the conversion, to be independent of the readback timing. This is useful in low jitter sampling or simultaneous sampling applications.

A 14-bit register, CFG[13:0], is used to configure the ADC for the channel to be converted, the reference selection, and other components, which are detailed in the Configuration Register, CFG section.

When CNV is low, reading/writing can occur during conversion, acquisition, and spanning conversion (acquisition plus conversion). The CFG word is updated on the first 14 SCK rising edges, and conversion results are output on the first 15 (or 16, if busy mode is selected) SCK falling edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word associated with the conversion results with the CFG MSB following the LSB of the conversion result.

A discontinuous SCK is recommended because the device is selected with CNV low, and SCK activity begins to write a new configuration word and clock out data.

The timing diagrams indicate digital activity (SCK, CNV, DIN, and SDO) during the conversion. However, due to the possibility of performance degradation, digital activity occurs only prior to the safe data reading/writing time, $t_{DATA}$, because the AD7682/AD7689 provide error correction circuitry that can correct for an incorrect bit during this time. From $t_{DATA}$ to $t_{CONV}$, there is no error correction, and conversion results may be corrupted. Configure the AD7682/AD7689 and initiate the busy indicator (if desired) prior to $t_{DATA}$. It is also possible to corrupt the sample by having SCK or DIN transitions near the sampling instant. Therefore, it is recommended to keep the digital pins quiet for approximately 20 ns before and 10 ns after the rising edge of CNV, using a discontinuous SCK whenever possible to avoid any potential performance degradation.

### READING/WRITING DURING CONVERSION, FAST HOSTS

When reading/writing during conversion (n), conversion results are for the previous (n − 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

After the CNV is brought high to initiate conversion, it must be brought low again to allow reading/writing during conversion. Reading/writing must only occur up to $t_{DATA}$ and, because this time is limited, the host must use a fast SCK.

The SCK frequency required is calculated by

$$f_{SCK} \geq \frac{Number_SCK_Edges}{t_{DATA}} \quad (6)$$

The time between $t_{DATA}$ and $t_{CONV}$ is a safe time when digital activity must not occur, or sensitive bit decisions may be corrupt.

### READING/WRITING AFTER CONVERSION, ANY SPEED HOSTS

When reading/writing after conversion, or during acquisition (n), conversion results are for the previous (n − 1) conversion, and writing is for the (n + 1) acquisition.

For the maximum throughput, the only time restriction is that the reading/writing take place during the $t_{ACQ}$ (minimum) time. For slow throughputs, the time restriction is dictated by the throughput required by the user, and the host is free to run at any speed. Thus for slow hosts, data access must take place during the acquisition phase.

### READING/WRITING SPANNING CONVERSION, ANY SPEED HOST

When reading/writing spanning conversion, the data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n − 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

Similar to reading/writing during conversion, reading/writing must only occur up to $t_{DATA}$. For the maximum throughput, the only time restriction is that reading/writing take place during the $t_{ACQ}$ + $t_{DATA}$ time.

For slow throughputs, the time restriction is dictated by the required throughput, and the host is free to run at any speed. Similar to reading/writing during acquisition, for slow hosts, the data access must take place during the acquisition phase with additional time into the conversion.

Data access spanning conversion requires the CNV to be driven high to initiate a new conversion, and data access is not allowed when CNV is high. Therefore, the host must perform two bursts of data access when using this method.

### CONFIGURATION REGISTER, CFG

The AD7682/AD7689 use a 14-bit configuration register (CFG[13:0]), as detailed in Table 13, to configure the inputs, the channel to be converted, the one-pole filter bandwidth, the reference, and the channel sequencer. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges. The CFG update is edge dependent, allowing for asynchronous or synchronous hosts.

The register can be written to during conversion, during acquisition, or spanning acquisition/conversion, and is updated at the end of conversion, $t_{CONV}$ (maximum). There is always a one deep delay when writing the CFG register. At power-up, the CFG register is undefined and two dummy conversions are required to update the register. To preload the CFG register with a factory setting, hold DIN high for two conversions (CFG[13:0] = 0x3FFF).

## DIGITAL INTERFACE

This sets the AD7682/AD7689 for the following:

- IN[7:0] unipolar referenced to GND, sequenced in order.
- Full bandwidth for a one-pole filter.
- Internal reference/temperature sensor disabled, buffer enabled.
- Enables the internal sequencer.
- No readback of the CFG register.

Table 13 summarizes the configuration register bit details. See the Theory of Operation section for more details.

*Table 12. Configuration Register Bit Names*

| 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CFG | INCC | INCC | INCC | INx | INx | INx | BW | REF | REF | REF | SEQ | SEQ | RB |

*Table 13. Configuration Register Description*

| Bit(s) | Name | Description |
|---|---|---|
| [13] | CFG | Configuration update.<br>0 = keep current configuration settings.<br>1 = overwrite contents of register. |
| [12:10] | INCC | Input channel configuration. Selection of pseudo bipolar, pseudo differential, pairs, single-ended, or temperature sensor. Refer to the Input Configurations section. |

| Bit 12 | Bit 11 | Bit 10 | Function |
|---|---|---|---|
| 0 | 0 | X[1] | Bipolar differential pairs; INx− referenced to $V_{REF}/2 \pm 0.1$ V. |
| 0 | 1 | 0 | Bipolar; INx referenced to COM = $V_{REF}/2 \pm 0.1$ V. |
| 0 | 1 | 1 | Temperature sensor. |
| 1 | 0 | X[1] | Unipolar differential pairs; INx− referenced to GND ± 0.1 V. |
| 1 | 1 | 0 | Unipolar, INx referenced to COM = GND ± 0.1 V. |
| 1 | 1 | 1 | Unipolar, INx referenced to GND. |

| [9:7] | INx | Input channel selection in binary fashion. |
|---|---|---|

| AD7682 | | | | AD7689 | | | |
|---|---|---|---|---|---|---|---|
| Bit 9 | Bit 8 | Bit 7 | Channel | Bit 9 | Bit 8 | Bit 7 | Channel |
| X[1] | 0 | 0 | IN0 | 0 | 0 | 0 | IN0 |
| X[1] | 0 | 1 | IN1 | 0 | 0 | 1 | IN1 |
| X[1] | 1 | 0 | IN2 | … | … | … | … |
| X[1] | 1 | 1 | IN3 | 1 | 1 | 1 | IN7 |

| [6] | BW | Select bandwidth for low-pass filter. Refer to the Selectable Low-Pass Filter section.<br>0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. Maximum throughput must be reduced to ¼.<br>1 = full BW. |
|---|---|---|
| [5:3] | REF | Reference/buffer selection. Selection of internal, external, external buffered, and enabling of the on-chip temperature sensor. Refer to the Voltage Reference Output/Input section. |

| Bit 5 | Bit 4 | Bit 3 | Function |
|---|---|---|---|
| 0 | 0 | 0 | Internal reference and temperature sensor enabled. REF = 2.5 V buffered output. |
| 0 | 0 | 1 | Internal reference and temperature sensor enabled. REF = 4.096 V buffered output. |
| 0 | 1 | 0 | Use external reference. Temperature sensor enabled. Internal buffer disabled. |
| 0 | 1 | 1 | Use external reference. Internal buffer and temperature sensor enabled. |
| 1 | 0 | 0 | Do not use. |
| 1 | 0 | 1 | Do not use. |
| 1 | 1 | 0 | Use external reference. Internal reference, internal buffer, and temperature sensor disabled. |
| 1 | 1 | 1 | Use external reference. Internal buffer enabled. Internal reference and temperature sensor disabled. |

| [2:1] | SEQ | Channel sequencer. Allows for scanning channels in an IN0 to IN[7:0] fashion. Refer to the Channel Sequencer section. |
|---|---|---|

| Bit 2 | Bit 1 | Function |
|---|---|---|
| 0 | 0 | Disable sequencer. |
| 0 | 1 | Update configuration during sequence. |
| 1 | 0 | Scan IN0 to IN[7:0] (set in CFG[9:7]), then temperature. |

## DIGITAL INTERFACE

*Table 13. Configuration Register Description (Continued)*

| Bit(s) | Name | Description | | |
|---|---|---|---|---|
| | | 1 | 1 | Scan IN0 to IN[7:0] (set in CFG[9:7]). |
| [0] | RB | Read back the CFG register.<br>0 = read back current configuration at end of data.<br>1 = do not read back contents of configuration. | | |

[1] X means don't care.

## DIGITAL INTERFACE

### GENERAL TIMING WITHOUT A BUSY INDICATOR

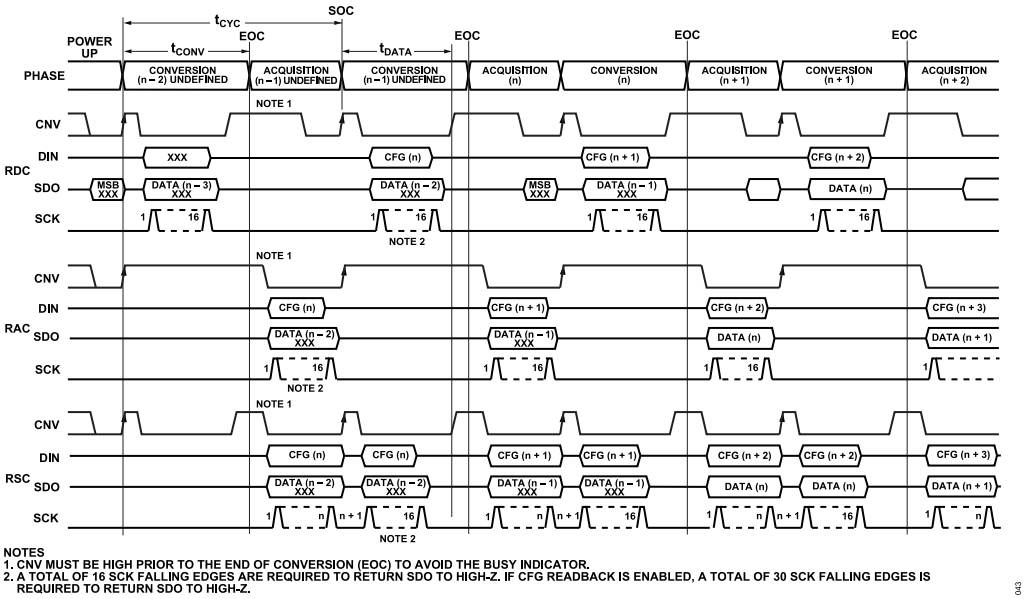
Figure 39 details the timing for all three modes: read/write during conversion (RDC), read/write after conversion (RAC), and read/write spanning conversion (RSC). Note that the gating item for both CFG and data readback is at the end of conversion (EOC). At EOC, if CNV is high, the busy indicator is disabled.

As detailed in the Digital Interface section, the data access must occur up to safe data reading/writing time, $t_{DATA}$. If the full CFG word is not written to prior to EOC, it is discarded and the current configuration remains. If the conversion result is not read out fully prior to EOC, it is lost as the ADC updates SDO with the MSB of the current conversion. For detailed timing, refer to Figure 42 and Figure 43, which depict reading/writing spanning conversion with all timing details, including setup, hold, and SCK.

When CNV is brought low after EOC, SDO is driven from high impedance to the MSB. Falling SCK edges clock out bits starting with MSB − 1.

The SCK can idle high or low depending on the clock polarity (CPOL) and clock phase (CPHA) settings if SPI is used. A simple solution is to use CPOL = CPHA = 0 as shown in Figure 39 with SCK idling low.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the second EOC; therefore, two dummy conversions are required. If the state machine writes the CFG during the power-up state (RDC shown), the CFG register must be rewritten at the next phase. The first valid data occurs in phase (n + 1) when the CFG register is written during phase (n − 1).




NOTES
1. CNV MUST BE HIGH PRIOR TO THE END OF CONVERSION (EOC) TO AVOID THE BUSY INDICATOR.
2. A TOTAL OF 16 SCK FALLING EDGES ARE REQUIRED TO RETURN SDO TO HIGH-Z. IF CFG READBACK IS ENABLED, A TOTAL OF 30 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z.

*Figure 39. General Interface Timing for the AD7682/AD7689 Without a Busy Indicator*

## DIGITAL INTERFACE

### GENERAL TIMING WITH A BUSY INDICATOR

Figure 40 details the timing for all three modes: RDC, RAC, and RSC. Note that the gating item for both CFG and data readback is at EOC. The data access must occur up to safe data reading/writing time, $t_{DATA}$. If the full CFG word is not written to prior to EOC, it is discarded and the current configuration remains.

At the EOC, if CNV is low, the busy indicator enables. In addition, to generate the busy indicator properly, the host must assert a minimum of 17 SCK falling edges to return SDO to high impedance because the last bit on SDO remains active. Unlike the case detailed in the Read/Write Spanning Conversion Without a Busy Indicator section, if the conversion result is not read out fully prior to EOC, the last bit clocked out remains. If this bit is low, the busy signal indicator cannot be generated because the busy generation requires either a high impedance or a remaining bit high-to-low transition. A good example of this occurs when an SPI host sends 16 SCKs because these are usually limited to 8-bit or 16-bit bursts. Therefore, the LSB remains. Because the transition noise of the AD7682/AD7689 is 4 LSBs peak-to-peak (or greater), the LSB is low 50% of the time. For this interface, the SPI host needs to burst 24 SCKs, or a QSPI interface can be used and programmed for 17 SCKs.

The SCK can idle high or low depending on the CPOL and CPHA settings if SPI is used. A simple solution is to use CPOL = CPHA = 1 (not shown) with SCK idling high.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the second EOC. Thus, two dummy conversions are required. Also, if the state machine writes the CFG during the power-up state (RDC shown), the CFG register needs to be rewritten again at the next phase. The first valid data occurs in phase (n + 1) when the CFG register is written during phase (n − 1).

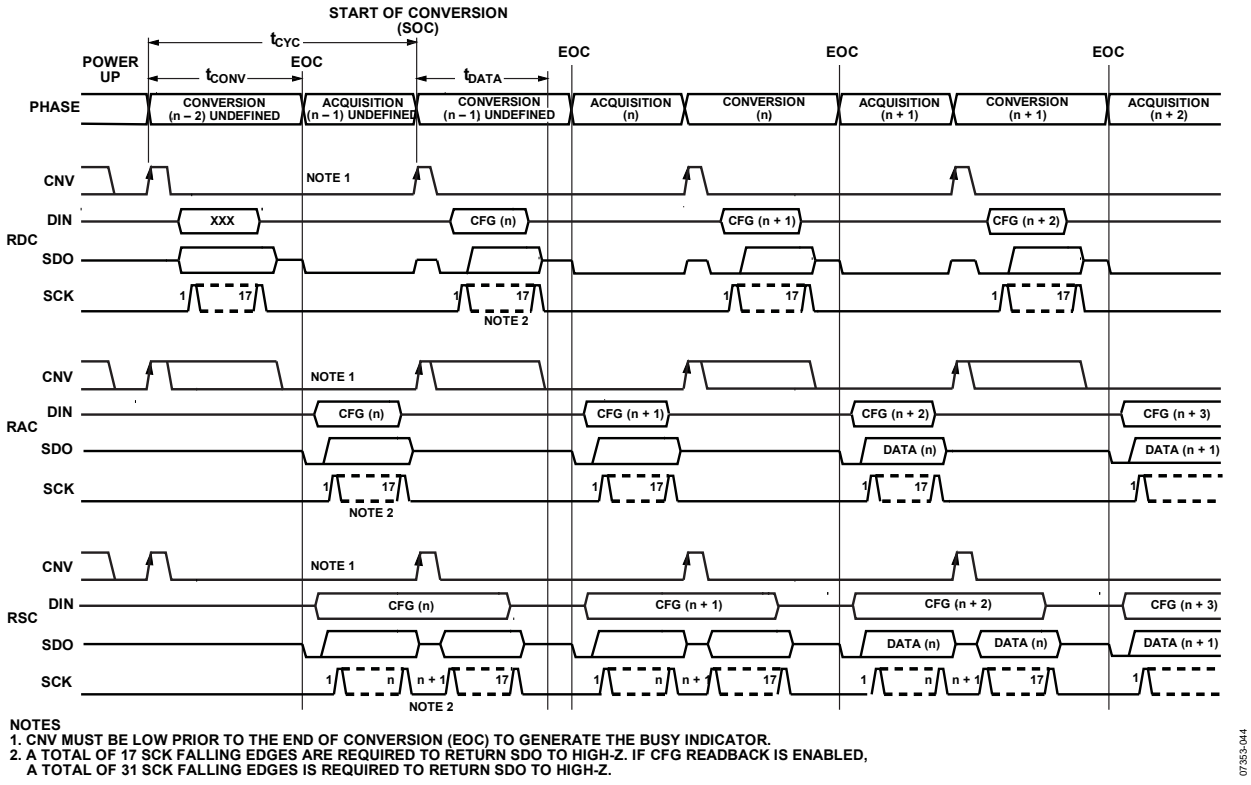



*Figure 40. General Interface Timing for the AD7682/AD7689 With a Busy Indicator*

## DIGITAL INTERFACE

### CHANNEL SEQUENCER

The AD7682/AD7689 include a channel sequencer useful for scanning channels in a repeated fashion. Channels are scanned as singles or pairs, with or without the temperature sensor, after the last channel is sequenced.

The sequencer starts with IN0 and finishes with IN[7:0] set in CFG[9:7]. For paired channels, the channels are paired depending on the last channel set in CFG[9:7]. Note that in sequencer mode, the channels are always paired with the positive input on the even channels (IN0, IN2, IN4, and IN6), and with the negative input on the odd channels (IN1, IN3, IN5, and IN7). For example, setting CFG[9:7] = 110 or 111 scans all pairs with the positive inputs dedicated to IN0, IN2, IN4, and IN6.

CFG[2:1] are used to enable the sequencer. After the CFG register is updated, DIN must be held low while reading data out for Bit 13, or the CFG register begins updating again.

Note that while operating in a sequence, some bits of the CFG register can be changed. However, if changing CFG[11] (paired or single channel) or CFG[9:7] (last channel in sequence), the sequence reinitializes and converts IN0 (or IN0/IN1 pairs) after the CFG register is updated.

Figure 41 details the timing for all three modes without a busy indicator. Refer to the General Timing Without a Busy Indicator section and the Read/Write Spanning Conversion Without a Busy Indicator section for more details. The sequencer can also be used with the busy indicator and details for these timings can be found in the General Timing With a Busy Indicator section and the Read/Write Spanning Conversion With a Busy Indicator section.

For sequencer operation, the CFG register must be set during the (n − 1) phase after power-up. On phase (n), the sequencer setting takes place and acquires IN0. The first valid conversion result is available at phase (n + 1). After the last channel set in CFG[9:7] is converted, the internal temperature sensor data is output (if enabled), followed by acquisition of IN0.

#### Examples

With all channels configured for unipolar mode to GND, including the internal temperature sensor, the sequence scans in the following order:

IN0, IN1, IN2, IN3, IN4, IN5, IN6, IN7, TEMP, IN0, IN1, IN2…

For paired channels with the internal temperature sensor enabled, the sequencer scans in the following order:

IN0, IN2, IN4, IN6, TEMP, IN0…

Note that IN1, IN3, IN5, and IN7 are referenced to a GND sense or $V_{REF}/2$, as detailed in the Input Configurations section.

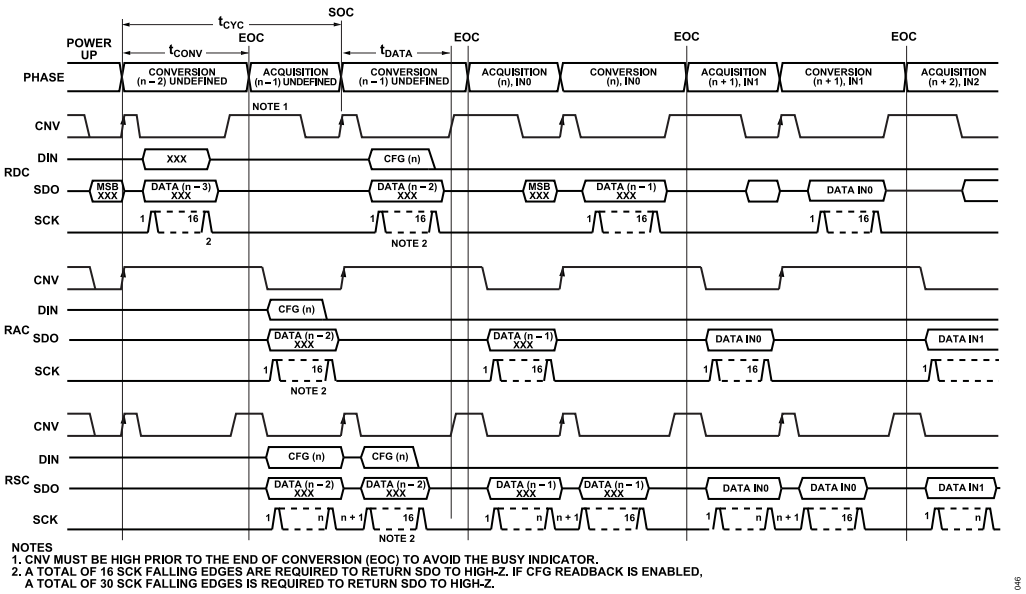



*Figure 41. General Channel Sequencer Timing Without a Busy Indicator*

## DIGITAL INTERFACE

### READ/WRITE SPANNING CONVERSION WITHOUT A BUSY INDICATOR

This mode is used when the AD7682/AD7689 are connected to any host using an SPI, serial port, or FPGA. The connection diagram is shown in Figure 42, and the corresponding timing is given in Figure 43. For the SPI, the host must use CPHA = CPOL = 0. Reading/writing spanning conversion is shown, which covers all three modes detailed in the Digital Interface section. For this mode, the host must generate the data transfer based on the conversion time. For an interrupt driven transfer that uses a busy indicator, refer to the Read/Write Spanning Conversion With a Busy Indicator section.

A rising edge on CNV initiates a conversion, forces SDO to high impedance, and ignores data present on DIN. After a conversion initiates, it continues until completion, irrespective of the state of CNV. CNV must be returned high before the safe data transfer time ($t_{DATA}$), and held high beyond the conversion time ($t_{CONV}$) to avoid generation of the busy signal indicator.

After the conversion is complete, the AD7682/AD7689 enter the acquisition phase and power-down. When the host brings CNV low after $t_{CONV}$ (maximum), the MSB enables on SDO. The host also must enable the MSB of the CFG register at this time (if necessary) to begin the CFG update. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG, and the first 15 SCK falling edges clock out the conversion results starting with MSB − 1. The restriction for both configuring and reading is that they both must occur before the $t_{DATA}$ time of the next conversion elapses. All 14 bits of CFG[13:0] must be written or they are ignored. In addition, if the 16-bit conversion result is not read back before $t_{DATA}$ elapses, it is lost.

The SDO data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th (or 30th) SCK falling edge, or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If CFG readback is enabled, the CFG register associated with the conversion result is read back MSB first following the LSB of the conversion result. A total of 30 SCK falling edges is required to return SDO to high impedance if this is enabled.

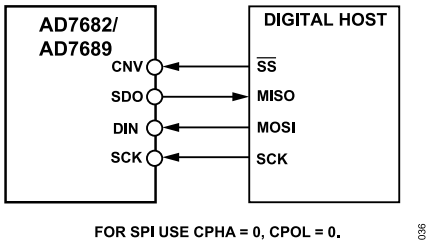



*Figure 42. Connection Diagram for the AD7682/AD7689 Without a Busy Indicator*

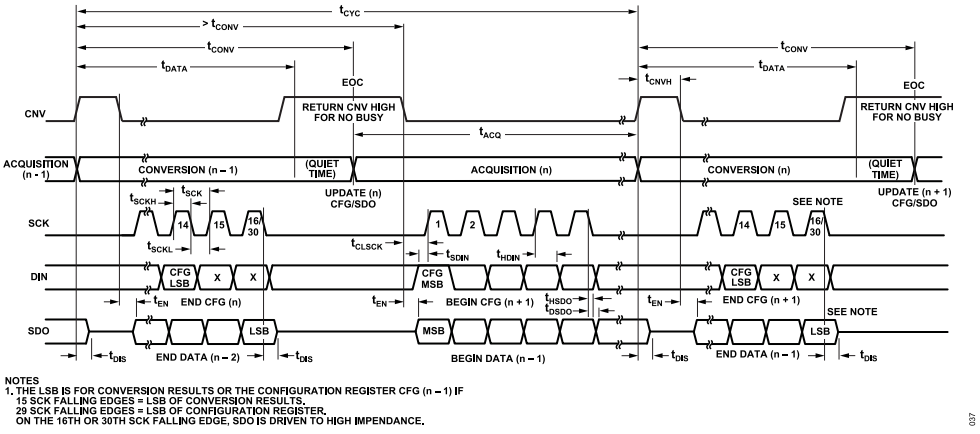



*Figure 43. Serial Interface Timing for the AD7682/AD7689 Without a Busy Indicator*

## DIGITAL INTERFACE

### READ/WRITE SPANNING CONVERSION WITH A BUSY INDICATOR

This mode is used when the AD7682/AD7689 are connected to any host using an SPI, serial port, or FPGA with an interrupt input. The connection diagram is shown in Figure 44, and the corresponding timing is given in Figure 45. For the SPI, the host must use CPHA = CPOL = 1. Reading/writing spanning conversion is shown, which covers all three modes detailed in the Digital Interface section.

A rising edge on CNV initiates a conversion, ignores data present on DIN, and forces SDO to high impedance. After the conversion initiates, it continues until completion, irrespective of the state of CNV. CNV must be returned low before the safe data transfer time ($t_{DATA}$), and then held low beyond the conversion time ($t_{CONV}$) to generate the busy signal indicator. When the conversion is complete, SDO transitions from high impedance to low (data ready), and with a pull-up to VIO, SDO can be used to interrupt the host to begin data transfer.

After the conversion is complete, the AD7682/AD7689 enter the acquisition phase and power-down. The host must enable the MSB of the CFG register at this time (if necessary) to begin the CFG update. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG register, and the first 16 SCK falling edges clock out the conversion results starting with the MSB. The restriction for both configuring and reading is that they both occur before the $t_{DATA}$ time elapses for the next conversion. All 14 bits of CFG[13:0] must be written or they are ignored. If the 16-bit conversion result is not read back before $t_{DATA}$ elapses, it is lost.

The SDO data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th (or 31st) SCK falling edge, SDO returns to high impedance. If the optional SCK falling edge is not used, the busy feature cannot be detected, as described in the General Timing With a Busy Indicator section.

If CFG readback is enabled, the CFG register associated with the conversion result is read back MSB first following the LSB of the conversion result. A total of 31 SCK falling edges is required to return SDO to high impedance if this is enabled.

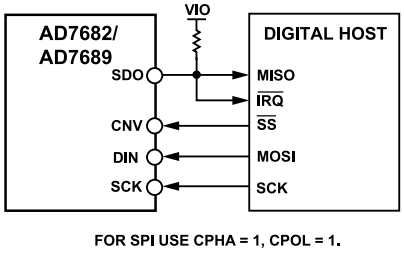



*Figure 44. Connection Diagram for the AD7682/AD7689 with a Busy Indicator*

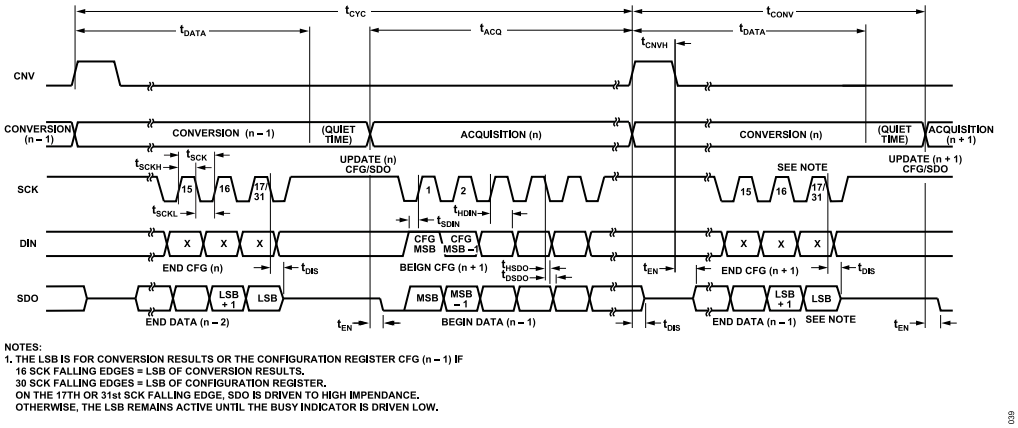



*Figure 45. Serial Interface Timing for the AD7682/AD7689 with a Busy Indicator*

## APPLICATIONS INFORMATION

### LAYOUT

The printed circuit board (PCB) that houses the AD7682/AD7689 must be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pin configuration of the AD7682/AD7689, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die unless a ground plane under the AD7682/AD7689 is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Avoid crossover of digital and analog signals.

Use at least one ground plane. It can be common or split between the digital and analog sections. In the latter case, join the planes underneath the AD7682/AD7689.

The AD7682/AD7689 voltage reference input, REF, has a dynamic input impedance and must be decoupled with minimal parasitic inductances. This is achieved by placing the reference decoupling ceramic capacitor close to (ideally, right up against) the REF and GND pins and connecting them with wide, low impedance traces.

Finally, the power supplies of the AD7682/AD7689 (VDD and VIO) must be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7682/AD7689, and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

The AN-617 Application Note has information on PCB layout and assembly. This information is particularly important for guiding customers who do not have experience with WLCSP.

### EVALUATING THE AD7682/AD7689 PERFORMANCE

Other recommended layouts for the AD7682/AD7689 are outlined in the documentation of the evaluation board for the AD7682/AD7689 (EVAL-AD7682EDZ/EVAL-AD7689EDZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the converter and evaluation development data capture board, EVAL-CED1Z.

## OUTLINE DIMENSIONS

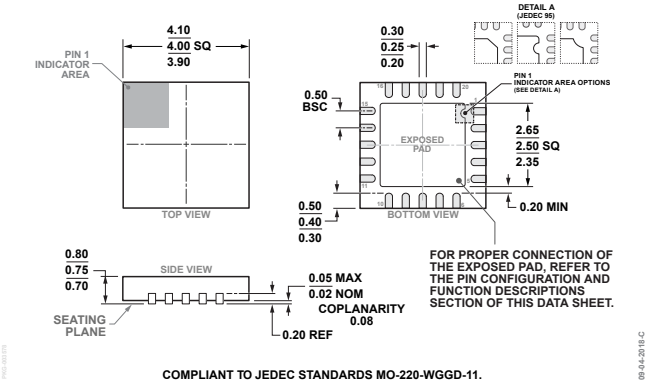



*Figure 46. 20-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-20-10)*
*Dimensions shown in millimeters*

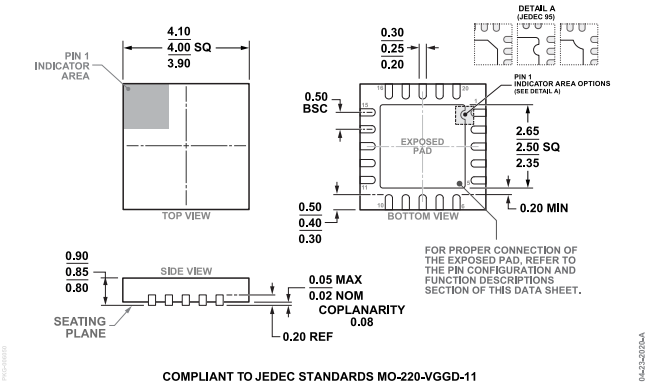



*Figure 47. 20-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.85 mm Package Height*
*(CP-20-22)*
*Dimensions shown in millimeters*

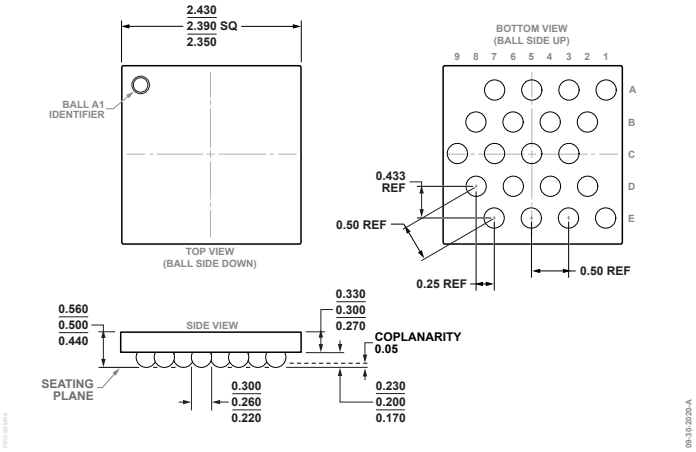



*Figure 48. 20-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-20-12)*
*Dimensions shown in millimeters*

## OUTLINE DIMENSIONS

Updated: September 25, 2023

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| AD7682BCBZ-RL7 | -40°C to +85°C | 20-Ball WLCSP (2.39mm x 2.39mm) | Reel, 1500 | CB-20-12 |
| AD7682BCPZ | -40°C to +85°C | 20-Lead LFCSP (4mm x 4mm w/ EP) | | CP-20-10 |
| AD7682BCPZRL7 | -40°C to +85°C | 20-Lead LFCSP (4mm x 4mm w/ EP) | Reel, 1500 | CP-20-10 |
| AD7689ACPZ | -40°C to +85°C | 20-lead LFCSP (4mm x 4mm x 0.85mm w/EP) | | CP-20-22 |
| AD7689ACPZRL7 | -40°C to +85°C | 20-lead LFCSP (4mm x 4mm x 0.85mm w/EP) | Reel, 1500 | CP-20-22 |
| AD7689BCBZ-RL7 | -40°C to +85°C | 20-Ball WLCSP (2.39mm x 2.39mm) | Reel, 1500 | CB-20-12 |
| AD7689BCPZ | -40°C to +85°C | 20-lead LFCSP (4mm x 4mm x 0.85mm w/EP) | | CP-20-22 |
| AD7689BCPZRL7 | -40°C to +85°C | 20-lead LFCSP (4mm x 4mm x 0.85mm w/EP) | Reel, 1500 | CP-20-22 |
| AD7689CCPZ | -40°C to +125°C | 20-lead LFCSP (4mm x 4mm x 0.85mm w/EP) | | CP-20-22 |
| AD7689CCPZRL7 | -40°C to +125°C | 20-lead LFCSP (4mm x 4mm x 0.85mm w/EP) | Reel, 1500 | CP-20-22 |

[1] Z = RoHS Compliant Part.

### Integral Nonlinearity and No Missing Code

| Model[1] | Integral Nonlinearity | No Missing Code |
|---|---|---|
| AD7682BCBZ-RL7 | ±1.5 LSB maximum | 16 bits |
| AD7682BCPZ | ±1.5 LSB maximum | 16 bits |
| AD7682BCPZRL7 | ±1.5 LSB maximum | 16 bits |
| AD7689ACPZ | ±4 LSB maximum | 15 bits |
| AD7689ACPZRL7 | ±4 LSB maximum | 15 bits |
| AD7689BCBZ-RL7 | ±1.5 LSB maximum | 16 bits |
| AD7689BCPZ | ±1.5 LSB maximum | 16 bits |
| AD7689BCPZRL7 | ±1.5 LSB maximum | 16 bits |
| AD7689CCPZ | ±2 LSB maximum | 16 bits |
| AD7689CCPZRL7 | ±2 LSB maximum | 16 bits |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model[1, 2] | Description |
|---|---|
| EVAL-AD7682EDZ | Evaluation Board |
| EVAL-AD7689EDZ | Evaluation Board |
| EVAL-CED1Z | Converter Evaluation and Development Board |

[1] Z = RoHS Compliant Part.

[2] The EVAL-CED1Z controller board allows a PC to control and communicate with all Analog Devices evaluation boards whose model numbers end in EDZ.

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- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management