THE DATASHEET OF

TSM150P03PQ33 RGG

P-Channel Power MOSFET

-30V, -36A, 15mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive Loss
- Low gate charge for fast power switching
- 100% UIS tested
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

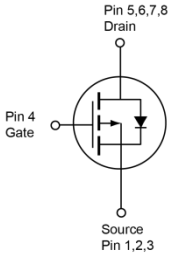
PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-30	V
$R_{DS(on)}$ (max)	V_{GS} = -10V	15	mΩ
	V_{GS} = -4.5V	30	
Q_g		14.3	nC

APPLICATIONS

- DC-DC Converters
- Battery Power Management
- Oring FET/Load Switch

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN33



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	-36	A
	T_A = 25°C		-10	
Pulsed Drain Current (Note 1)		I_{DM}	-144	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	-31	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	48	mJ
Total Power Dissipation	T_C = 25°C	P_D	27.8	W
	T_C = 125°C		5.5	
Total Power Dissipation	T_A = 25°C	P_D	2.3	W
	T_A = 125°C		0.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	4.5	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	53	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static (Note 3)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	$V_{GS(TH)}$	-1.2	-1.6	-2.5	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = -30V	I_{DSS}	--	--	-1	μA
Drain-Source On-State Resistance	V_{GS} = -10V, I_D = -10A	$R_{DS(on)}$	--	13	15	mΩ
	V_{GS} = -4.5V, I_D = -10A		--	22	30	
Forward Transconductance	V_{DS} = -5V, I_D = -10A	g_{fs}	--	19	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{GS} = -10V, V_{DS} = -15V, I_D = -10A	Q_g	--	29.3	--	nC
Total Gate Charge	V_{GS} = -4.5V, V_{DS} = -15V, I_D = -10A	Q_g		14.3		
Gate-Source Charge		Q_{gs}	--	5.9	--	
Gate-Drain Charge		Q_{gd}	--	5.2	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	C_{iss}	--	1829	--	pF
Output Capacitance		C_{oss}	--	227	--	
Reverse Transfer Capacitance		C_{rss}	--	160	--	
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = -10V, V_{DS} = -15V, I_D = -1A, R_G = 6Ω,	$t_{d(on)}$	--	9	--	ns
Rise Time		t_r	--	21.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	59.8	--	
Fall Time		t_f	--	14.4	--	
Source-Drain Diode (Note 3)						
Diode Forward Voltage	V_{GS} = 0V, I_S = -10A	V_{SD}	--	--	-1	V
Reverse Recovery Time	I_S = -10A, di/dt = 100A/μs	t_{rr}	--	34	--	ns
Reverse Recovery Charge		Q_{rr}	--	23	--	nC

Notes:

1. Current limited by package.
2. L = 0.1mH, V_{GS} = -10V, V_{DS} = -25V, R_G = 25Ω, I_{AS} = -31A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

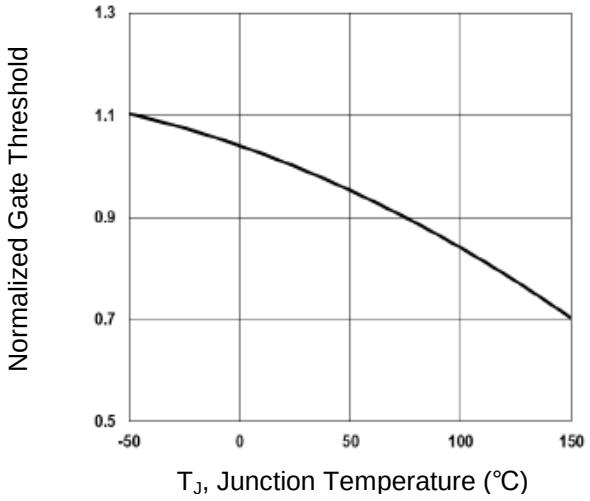
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM150P03PQ33 RGG	PDFN33	5,000pcs / 13” Reel

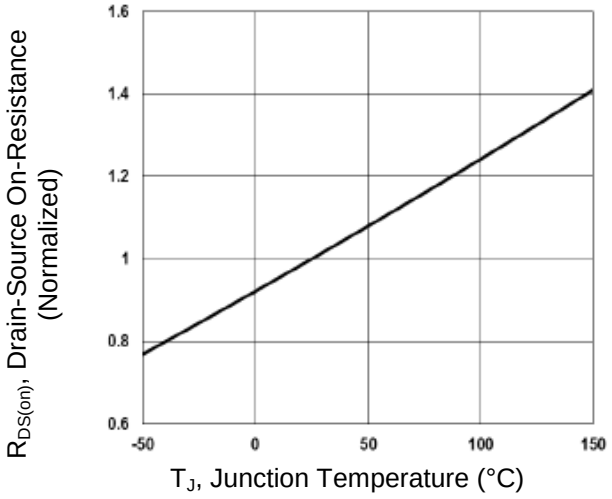
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

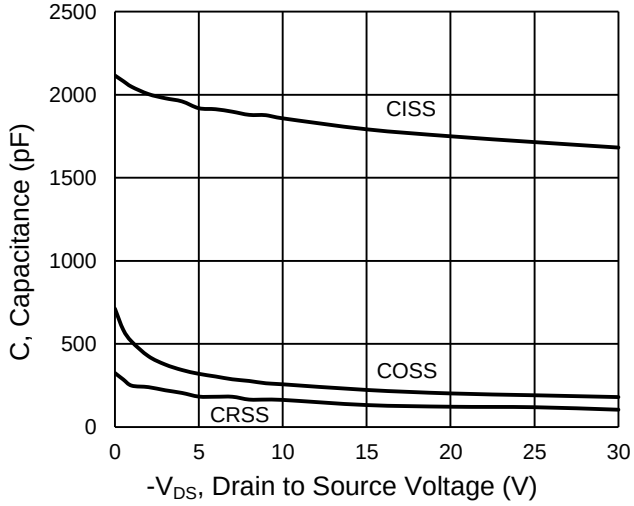
Normalized V_{th} vs. T_J



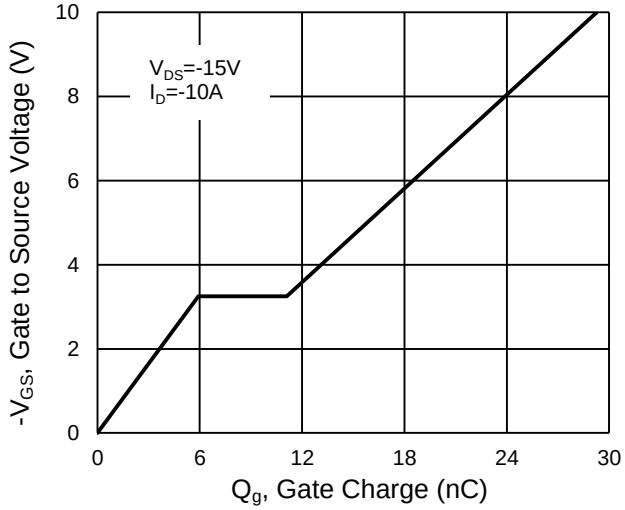
On-Resistance vs. Junction Temperature



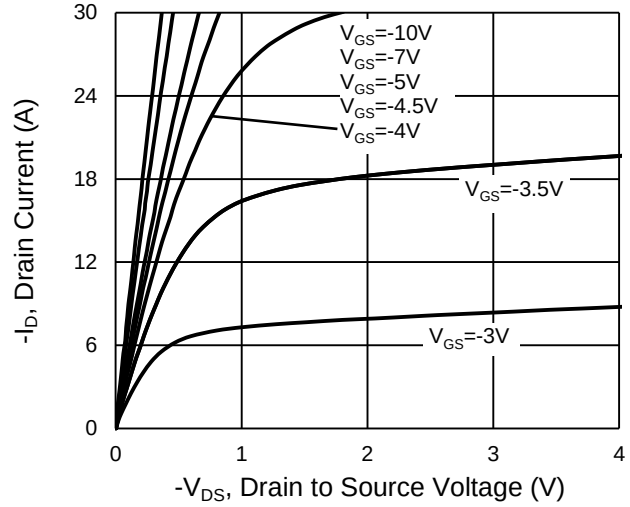
Capacitance vs. Drain-Source Voltage



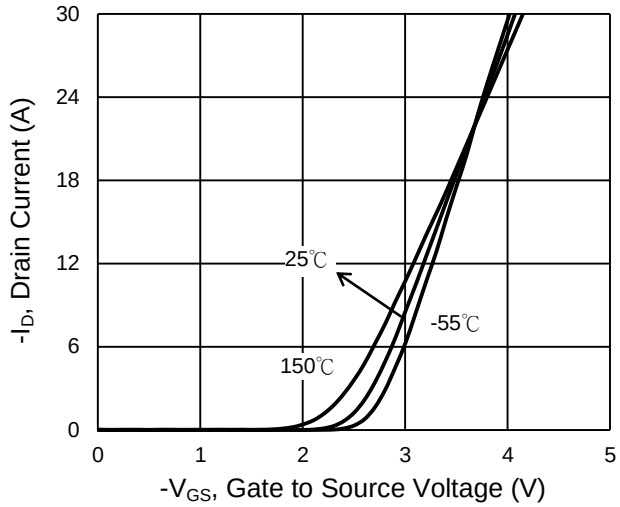
Gate-Source Voltage vs. Gate Charge



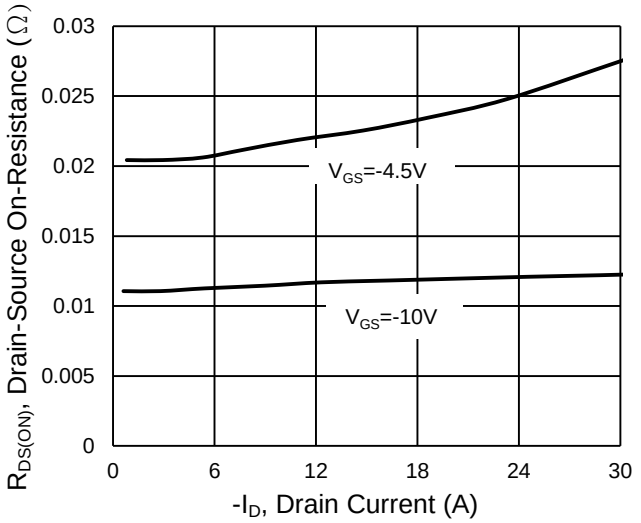
Output Characteristics



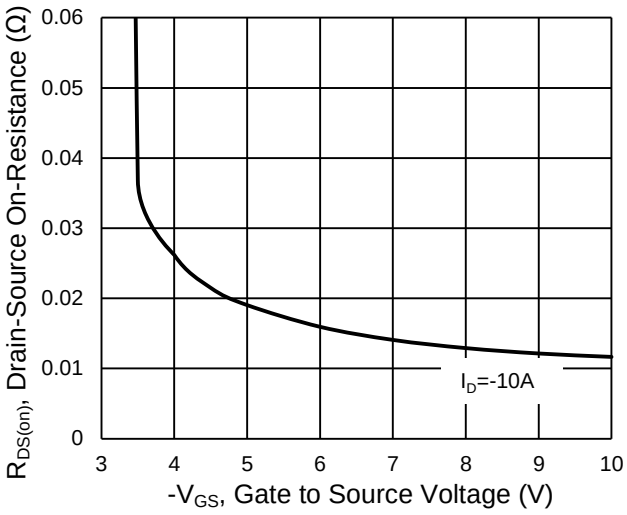
Transfer Characteristics



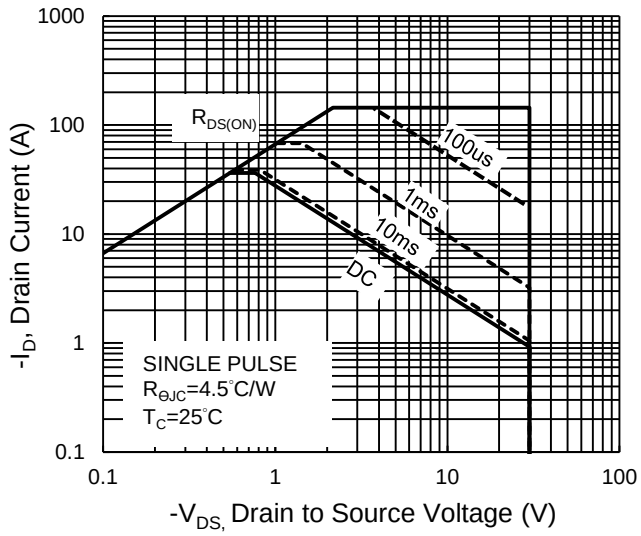
On-Resistance vs. Drain Current



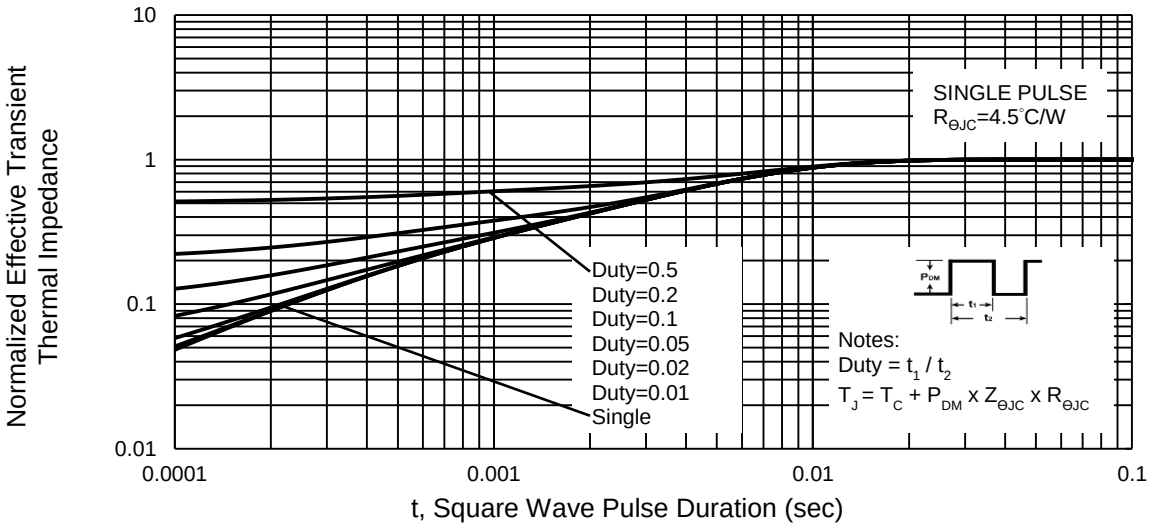
On-Resistance vs. Gate-Source Voltage



Maximum Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

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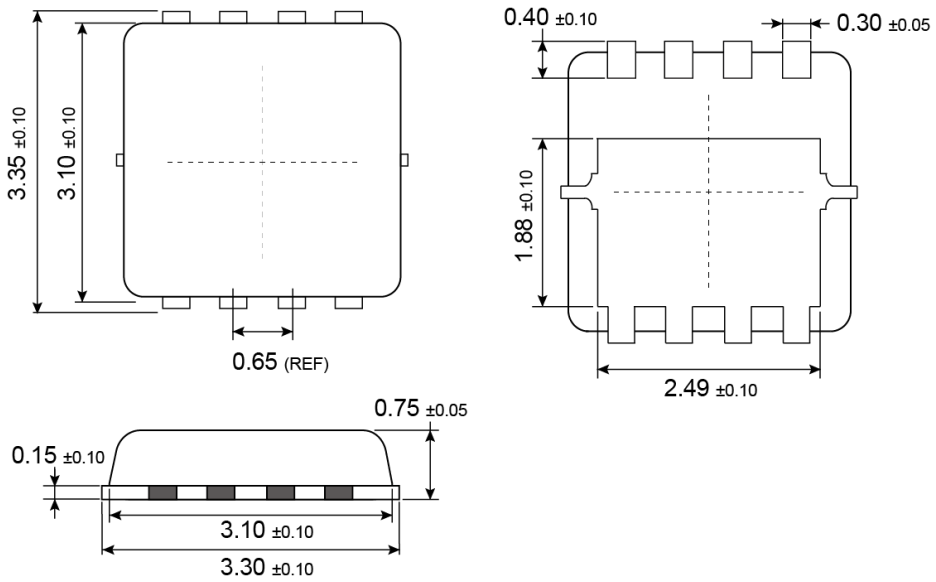
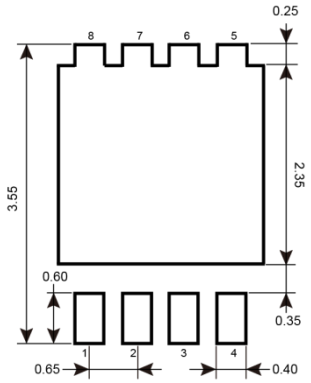
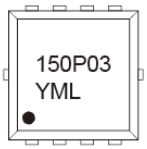


SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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