THE DATASHEET OF

ADS1191IRSMT

Low-Power, 2-Channel, 16-Bit Analog Front-End for Biopotential Measurements

Check for Samples: ADS1191, ADS1192

FEATURES

- **Two Low-Noise PGAs and Two High-Resolution ADCs (ADS1192)**
- **Low Power: 335 µW/channel**
- **Input-Referred Noise: 24 μV_{PP} (150-Hz BW, G = 6)**
- **Input Bias Current: 1 nA**
- **Data Rate: 125 SPS to 8 kSPS**
- **CMRR: –95 dB**
- **Programmable Gain: 1, 2, 3, 4, 6, 8, or 12**
- **Supplies: Unipolar or Bipolar**
  - **Analog: 2.7 V to 5.25 V**
  - **Digital: 1.7 V to 3.6 V**
- **Built-In Right Leg Drive Amplifier, Lead-Off Detection, Test Signals**
- **Built-In Oscillator and Reference**
- **Flexible Power-Down, Standby Mode**
- **SPI™-Compatible Serial Interface**
- **Operating Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Medical Instrumentation (ECG) including:**
  - **Patient monitoring; Holter, event, stress, and vital signs including ECG, AED, telemedicine**
  - **Sports and fitness (heart rate, respiration, and ECG)**

DESCRIPTION

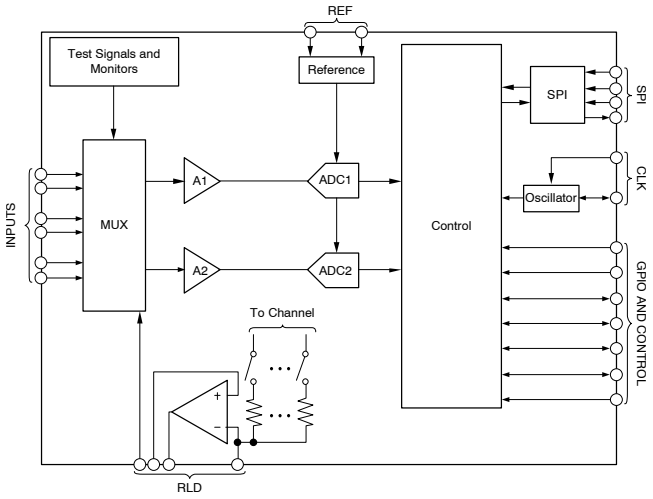
The ADS1191/2 are a family of multichannel, simultaneous sampling, 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator.

The ADS1191/2 incorporate all of the features that are commonly required in portable, low-power medical electrocardiogram (ECG), sports, and fitness applications.

With its high levels of integration and exceptional performance, the ADS1191/2 family enables the creation of scalable medical instrumentation systems at significantly reduced size, power, and overall cost.

The ADS1191/2 have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and lead-off detection. Additionally, any configuration of input channels can be selected for derivation of the right leg drive (RLD) output signal. The ADS1191/2 operate at data rates up to 8 kSPS. Lead-off detection can be implemented internal to the device, using the device internal excitation current sink/source.

The devices are packaged in a 5-mm × 5-mm, 32-pin thin quad flat pack (TQFP). Operating temperature is specified from –40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE OPTION	PACKAGE DESIGNATOR	NUMBER OF CHANNELS	ADC RESOLUTION	MAXIMUM SAMPLE RATE (kSPS)	OPERATING TEMPERATURE RANGE	RESPIRATION CIRCUITRY
ADS1191IPBS	TQFP	PBS	1	16	8	–40°C to +85°C	No
	QFN	RSM	1	24	8	–40°C to +85°C	No
ADS1192IPBS	TQFP	PBS	2	16	8	–40°C to +85°C	No
	QFN	RSM	2	24	8	–40°C to +85°C	No
ADS1291IPBS	TQFP	PBS	1	24	8	–40°C to +85°C	No
	QFN	RSM	1	24	8	–40°C to +85°C	No
ADS1292IPBS	TQFP	PBS	2	24	8	–40°C to +85°C	No
	QFN	RSM	2	24	8	–40°C to +85°C	No
ADS1292RIPBS	TQFP	PBS	2	24	8	–40°C to +85°C	Yes
	QFN	RSM	2	24	8	–40°C to +85°C	Yes

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to AVSS		–0.3 to +7	V
DVDD to DGND		–0.3 to +7	V
AVSS to DGND		–3 to +0.2	V
Analog input to AVSS		AVSS – 0.3 to AVDD + 0.3	V
Digital input to DVDD		DVSS – 0.3 to DVDD + 0.3	V
Input current to any pin except supply pins(2)		±10	mA
Input current	Momentary	±100	mA
	Continuous	±10	mA
Operating temperature range	Industrial-grade devices only	–40 to +85	°C
Storage temperature range		–60 to +150	°C
Maximum junction temperature (T_J)		+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±1000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current limited to 10 mA or less.

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ELECTRICAL CHARACTERISTICS

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8 V, AVDD – AVSS = 3 V(1), V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF(2), and gain = 6, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1191, ADS1192 MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Full-scale differential input voltage (AINP – AINN)			$\pm V_{REF}$/GAIN		V
	Input common-mode range			See the *Input Common-Mode Range* subsection of the *PGA Settings and Input Range* section		
	Input capacitance			20		pF
	Input bias current	Input = 1.5 V			±1	nA
		Input = 1.5 V, T_A = –40°C to +85°C		±2		nA
	DC input impedance	No lead-off	1000			MΩ
		Current source lead-off detection (nA range), AVSS + 0.3 V < AIN < AVDD – 0.3 V		500		MΩ
		Current source lead-off detection (µA range), AVSS + 0.6 V < AIN < AVDD – 0.6 V		100		MΩ
PGA PERFORMANCE						
	Gain settings			1, 2, 3, 4, 6, 8, 12		
BW	Bandwidth	With a 4.7-nF capacitor on PGA output (see *PGA Settings and Input Range* section for details)		8.5		kHz
ADC PERFORMANCE						
	Resolution		16			Bits
DR	Data rate		125		8000	SPS
CHANNEL PERFORMANCE (DC Performance)						
	Input-referred noise	Gain = 6(3), 10 seconds of data		24.6		μV_{PP}
		Gain = 6, 256 points, 0.5 seconds of data		24.6	25	μV_{PP}
		Gain settings other than 6, data rate other than 500 SPS		See *Noise Measurements* section		
INL	Integral nonlinearity	Full-scale with gain = 6, best fit		±1		LSB
	Input-referred offset error			±100		µV
	Input-referred offset error drift			2		µV/°C
	Offset error with calibration			15		µV
	Gain error	Excluding voltage reference error		±0.5		% of FS
	Gain drift	Excluding voltage reference drift		5		ppm/°C
	Gain match between channels			1		% of FS
CHANNEL PERFORMANCE (AC performance)						
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz, 60 Hz(4)	–95			dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz, 60 Hz		90		dB
	Crosstalk	f_{IN} = 50 Hz, 60 Hz		–120		dB
SNR	Signal-to-noise ratio	f_{IN} = 10 Hz input, gain = 6		92		dB
THD	Total harmonic distortion	10 Hz, –0.5 dBFs		–100		dB

(1) Performance is applicable for 5-V operation as well. Production testing for limits is performed at 3 V.
(2) C_{FILTER} is the capacitor accross the PGA outputs; see the *PGA Settings and Input Range* section for details.
(3) Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted (without electrode resistance) over a 10-second interval.
(4) CMRR is measured with a common-mode signal of AVSS + 0.3 V to AVDD – 0.3 V. The values indicated are the minimum of the eight channels.

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ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8 V, AVDD – AVSS = 3 V[1], V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF[2], and gain = 6, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1191, ADS1192			UNIT
			MIN	TYP	MAX	
RIGHT LEG DRIVE (RLD) AMPLIFIER						
	Integrated noise	BW = 150 Hz		1.4		μV_{RMS}
GBP	Gain bandwidth product	50 kΩ || 10 pF load, gain = 1		100		kHz
SR	Slew rate	50 kΩ || 10 pF load, gain = 1		0.07		V/µs
THD	Total harmonic distortion	f_{IN} = 100 Hz, gain = 1		–85		dB
CMIR	Common-mode input range		AVSS + 0.3		AVDD – 0.3	V
	Common-mode resistor matching	Internal 200-kΩ resistor matching		0.1		%
I_{SC}	Short-circuit current			1.1		mA
	Quiescent power consumption	RLD amplifier		5		µA
LEAD-OFF DETECT						
	Frequency	See *Register Map* section for settings		0, f_{DR}/4		kHz
	Current	ILEAD_OFF [1:0] = 00		6		nA
		ILEAD_OFF [1:0] = 01		22		nA
		ILEAD_OFF [1:0] = 10		6		µA
		ILEAD_OFF [1:0] = 11		22		µA
	Current accuracy			±20		%
	Comparator threshold accuracy			±30		mV
EXTERNAL REFERENCE						
	Reference input voltage	AVDD = 3 V, V_{REF} = (VREFP – VREFN)	2	2.5	VDD – 0.3	V
		AVDD = 5 V, V_{REF} = (VREFP – VREFN)	2	4	VDD – 0.3	V
VREFN	Negative input			AVSS		V
VREFP	Positive input			AVSS + 2.5		V
	Input impedance			120		kΩ
INTERNAL REFERENCE						
	Output voltage	CONFIG2.VREF_4V = 0		2.42		V
		CONFIG2.VREF_4V = 1		4.033		V
	Output current drive	Available for external use		100		µA
	V_{REF} accuracy			±0.5		%
	Internal reference drift			45		ppm/°C
	Start-up time	Settled to 0.2% with 10-µF capacitor on VREFP pin		100		ms
	Quiescent current consumption			20		µA

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ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8 V, AVDD – AVSS = 3 V(1), V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF(2), and gain = 6, unless otherwise noted.

PARAMETER			TEST CONDITIONS	ADS1191, ADS1192 MIN	TYP	MAX	UNIT
SYSTEM MONITORS							
	Analog supply reading error				2		%
	Digital supply reading error				2		%
	Device wake up		From power supply ramp after power-on-reset to $\overline{DRDY}$ low		32		ms
			From power-down mode to $\overline{DRDY}$ low		10		ms
			From STANDBY mode to $\overline{DRDY}$ low		10		ms
	VCAP1 settling time		1% accuracy with 1-µF capacitor		0.5		s
	Temperature sensor reading	Voltage	T_A = +25°C		145		mV
		Coefficient			490		µV/°C
TEST SIGNAL							
	Signal frequency		See *Register Map* section for settings		At dc and 1 Hz		Hz
	Signal voltage		See *Register Map* section for settings		±1		mV
	Accuracy				±2		%
CLOCK							
	Internal oscillator clock frequency		Nominal frequency		512		kHz
			T_A = +25°C			±0.5	%
			–40°C ≤ T_A ≤ +85°C			±1.5	%
	Internal oscillator start-up time				32		µs
	Internal oscillator power consumption				30		µW
	External clock input frequency		CLKSEL pin = 0, CLK_DIV = 0	485	512	562.5	kHz
			CLKSEL pin = 0, CLK_DIV = 1	1.94	2.048	2.25	MHz
DIGITAL INPUT/OUTPUT (DVDD = 1.8 V to 3.6 V)							
	Logic level	V_{IH} (DVDD = 1.8 V to 3.6 V)		0.8 DVDD		DVDD + 0.1	V
		V_{IL}(DVDD = 1.8 V to 3.6 V)		–0.1		0.2 DVDD	V
		V_{IH} (DVDD = 1.7 V to 1.8 V)		DVDD – 0.2			V
		V_{IL} (DVDD = 1.7 V to 1.8 V)				0.2	V
		Input current (I_{IN})	0 V < $V_{DigitalInput}$ < DVDD	–10		+10	µA
POWER-SUPPLY REQUIREMENTS (RLD Amplifiers Turned Off)							
AVDD	Analog supply	AVDD – AVSS		2.7	3	5.25	V
DVDD	Digital supply			1.7	1.8	3.6	V
	AVDD – DVDD			–2.1		3.6	V
SUPPLY CURRENT							
	I_{AVDD}	ADS1192	AVDD – AVSS = 3 V		205		µA
			AVDD – AVSS = 5 V		250		µA
	I_{DVDD}	ADS1192	DVDD = 3.3 V		75		µA
			DVDD = 1.8 V		32		µA

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ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8 V, AVDD – AVSS = 3 V[1], V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF[2], and gain = 6, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1191, ADS1192 MIN	TYP	MAX	UNIT
POWER DISSIPATION (Analog Supply = 3 V, RLD Turned Off)						
Quiescent power dissipation	ADS1192	Normal mode		670	740	µW
		Standby mode		160		µW
	ADS1191	Normal mode		450	495	µW
		Standby mode		160		µW
Quiescent power dissipation, per channel	ADS1192	Normal mode		350		µW
	ADS1191	Normal mode		400		µW
POWER DISSIPATION (Analog Supply = 5 V, RLD Turned Off)						
Quiescent power dissipation	ADS1192	Normal mode		1300		µW
		Standby mode		340		µW
	ADS1191	Normal mode		950		µW
		Standby mode		340		µW
Quiescent power dissipation, per channel	ADS1192	Normal mode		670		µW
	ADS1191	Normal mode		860		µW
POWER DISSIPATION IN POWER-DOWN MODE						
Analog supply = 3 V	DVDD = 1.8 V			1		µW
	DVDD = 3.3 V			4		µW
Analog supply = 5 V	DVDD = 1.8 V			5		µW
	DVDD = 3.3 V			10		µW
TEMPERATURE						
Specified temperature range			–40		+85	°C
Operating temperature range			–40		+85	°C
Storage temperature range			–60		+150	°C

THERMAL INFORMATION

THERMAL METRIC[1]		ADS1191, ADS1192 PBS (TQFP) 32 PINS	RSM (QFN) 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	68.4	33.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	25.9	36.4	
θ_{JB}	Junction-to-board thermal resistance	30.5	25.2	
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	
ψ_{JB}	Junction-to-board characterization parameter	24.3	7.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PARAMETER MEASUREMENT INFORMATION

NOISE MEASUREMENTS

The ADS1191/2 noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the PGA value reduces the input-referred noise, which is particularly useful when measuring low-level biopotential signals. Table 1 and Table 2 summarize the noise performance of the ADS1191/2. The data are representative of typical noise performance at T_A = +25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together.

Table 1 and Table 2 show measurements taken with an internal reference. The data are also representative of the ADS1191/2 noise performance when using a low-noise external reference such as the REF5025.

Table 1. Input-Referred Noise (μV_{PP}) 3-V Analog Supply and 2.42-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN						
			x1	x2	x3	x4	x6	x8	x12
			μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}
000	125	32.75	147.1	73.9	49.2	36.9	24.6	18.5	12.3
001	250	65.5	147.7	73.9	49.2	36.9	24.6	18.5	12.3
010	500	131	147.7	73.9	49.2	36.9	24.6	18.5	12.3
011	1000	262	147.7	73.9	49.2	36.9	24.6	18.5	12.3
100	2000	524	221.5	110.8	73.8	55.4	36.9	27.7	18.5
101	4000	1048	810.0	405.0	270.0	202.5	135.0	101.3	67.5
110	8000	2096	3900.0	1950.0	1300.0	975.0	650.0	487.5	325.0

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 2. Input-Referred Noise (μV_{PP}) 5-V Analog Supply and 4.033-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN						
			x1	x2	x3	x4	x6	x8	x12
			μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}	μV_{PP}
000	125	32.75	246.1	123.1	82.0	61.5	41.0	30.8	20.5
001	250	65.5	246.1	123.1	82.0	61.5	41.0	30.8	20.5
010	500	131	246.1	123.1	82.0	61.5	41.0	30.8	20.5
011	1000	262	246.1	123.1	82.0	61.5	41.0	30.8	20.5
100	2000	524	369.2	184.6	123.1	92.3	61.5	46.2	30.8
101	4000	1048	1230.0	615.0	410.0	307.5	205.0	153.8	102.5
110	8000	2096	6800.0	3400.0	2266.7	1700.0	1133.3	850.0	566.7

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

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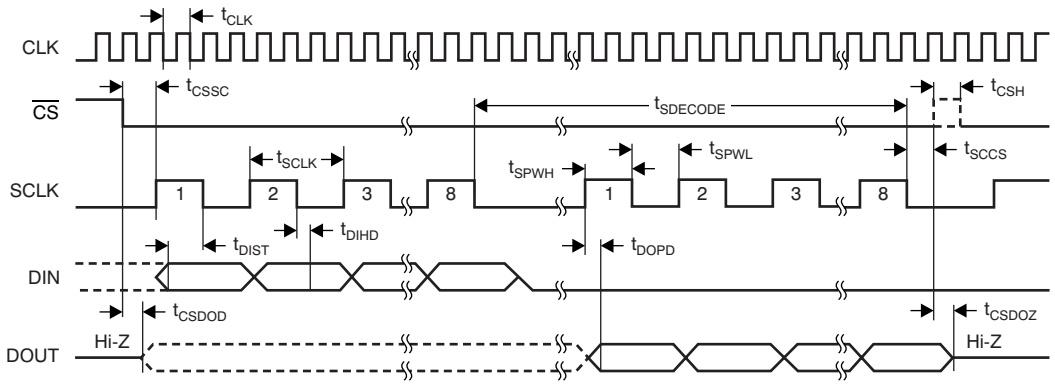
TIMING CHARACTERISTICS



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing

Timing Requirements For Figure 1(1)

PARAMETER	DESCRIPTION	2.7 V ≤ DVDD ≤ 3.6 V			1.6 V ≤ DVDD ≤ 2.7 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{CLK}	Master clock period (CLK_DIV bit of LOFF_STAT register = 0)	TBD		TBD	TBD		TBD	ns
	Master clock period (CLK_DIV bit of LOFF_STAT register = 1)	414		514	514		465	ns
t_{CSSC}	$\overline{CS}$ low to first SCLK, setup time	6			17			ns
t_{SCLK}	SCLK period	50			66.6			ns
$t_{SPWH, L}$	SCLK pulse width, high and low	15			25			ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10			10			ns
t_{DIHD}	Valid DIN after SCLK falling edge: hold time	10			11			ns
t_{DOPD}	SCLK rising edge to DOUT valid: setup time			12			22	ns
t_{CSH}	$\overline{CS}$ high pulse	2			2			t_{CLKs}
t_{CSDOD}	$\overline{CS}$ low to DOUT driven	10			20			ns
t_{SCCS}	Eighth SCLK falling edge to $\overline{CS}$ high	4			4			t_{CLKs}
$t_{SDECODE}$	Command decode time	4			4			t_{CLKs}
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z			10			20	ns

(1) Specified at T_A = –40°C to +85°C, unless otherwise noted. Load on D_{OUT} = 20 pF || 100 kΩ.

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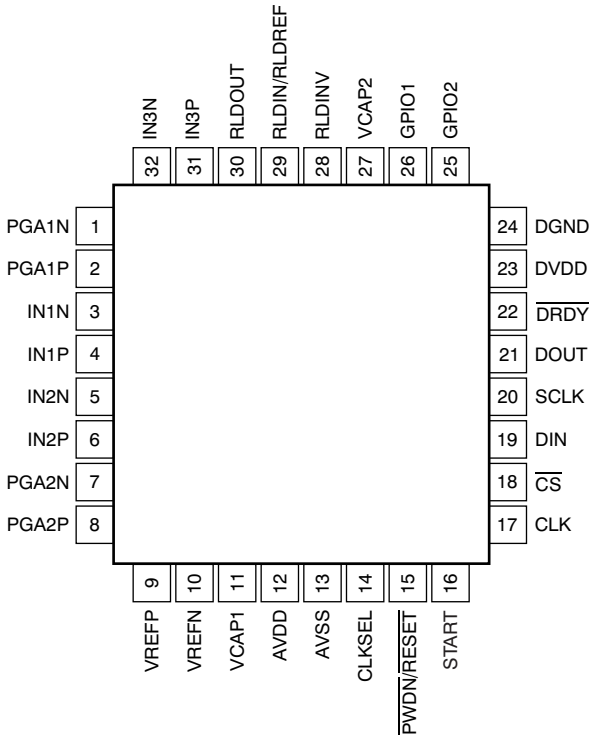
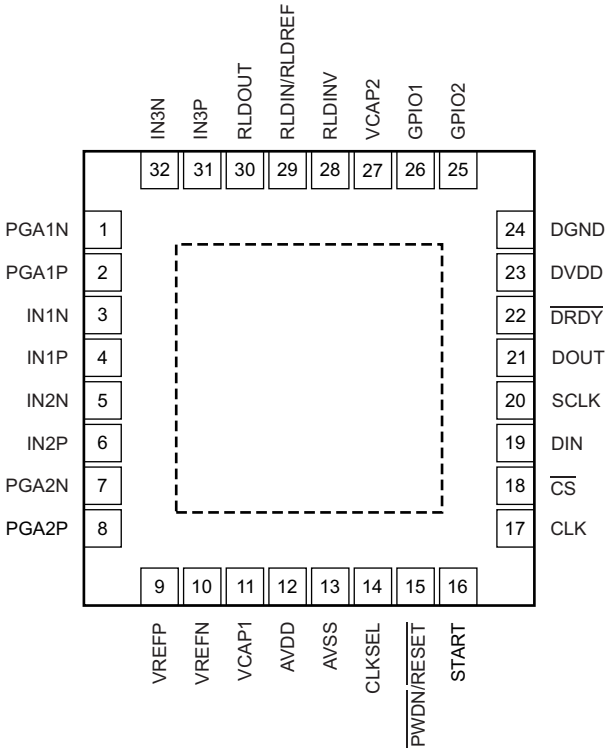
PIN CONFIGURATIONS

PBS PACKAGE
TQFP-32
(TOP VIEW)



RSM PACKAGE
QFN-32
(TOP VIEW)



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PIN ASSIGNMENTS

NAME	TERMINAL	FUNCTION	DESCRIPTION
AVDD	12	Supply	Analog supply
AVSS	13	Supply	Analog ground
$\overline{CS}$	18	Digital input	Chip select
CLK	17	Digital input	Master clock input
CLKSEL	14	Digital input	Master clock select
DGND	24	Supply	Digital ground
DIN	19	Digital input	SPI data in
DOUT	21	Digital output	SPI data out
$\overline{DRDY}$	22	Digital output	Data ready; active low
DVDD	23	Supply	Digital power supply
GPIO1/RCLK1	26	Digital input/output	GPIO1
GPIO2/RCLK2	25	Digital input/output	GPIO2
IN1N(1)	3	Analog input	Differential analog negative input 1
IN1P(1)	4	Analog input	Differential analog positive input 1
IN2N(1)	5	Analog input	Differential analog negative input 2
IN2P(1)	6	Analog input	Differential analog positive input 2
PGA1N	1	Analog output	Differential analog negative output 1
PGA1P	2	Analog output	Differential analog positive output 1
PGA2N	7	Analog output	Differential analog negative output 2
PGA2P	8	Analog output	Differential analog positive output 2
$\overline{PWDN}/\overline{RESET}$	15	Digital input	Power-down/System reset; active low
RLDIN/RLDREF	29	Analog input	Right leg drive input to MUX/RLD reference
RLDINV	28	Analog input	Right leg drive inverting input
RLDOUT	30	Analog input	Right leg drive output
IN3N(1)	32	Analog input/output	Differential analog negative input 3
IN3P(1)	31	Analog input/output	Differential analog positive input 3
SCLK	20	Digital input	SPI clock
START	16	Digital input	Start conversion
VCAP1	11	—	Analog bypass capacitor
VCAP2	27	—	Analog bypass capacitor
VREFN	10	Analog input	Negative reference voltage
VREFP	9	Analog input/output	Positive reference voltage

(1) Excludes effects of noise, linearity, offset, and gain error.

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TYPICAL CHARACTERISTICS

All plots at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.42 V, VREFN = AVSS, external clock = 512 kHz, data rate = 500 SPS, and gain = 6, unless otherwise noted.

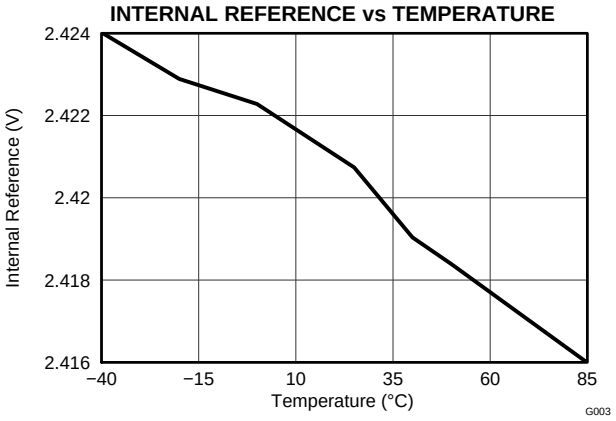

Figure 2.

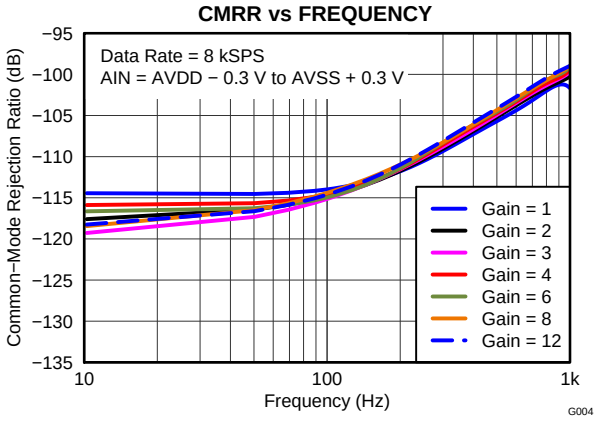

Figure 3.

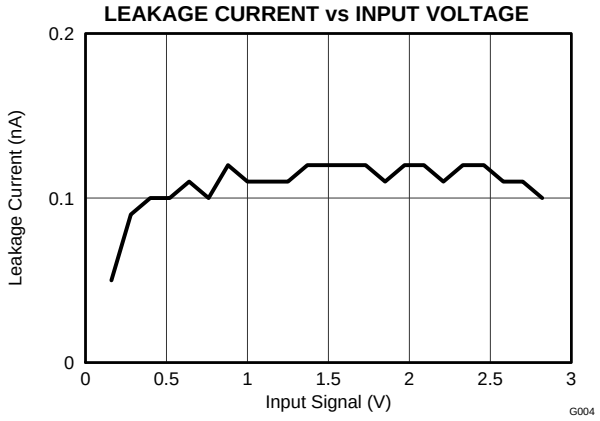

Figure 4.

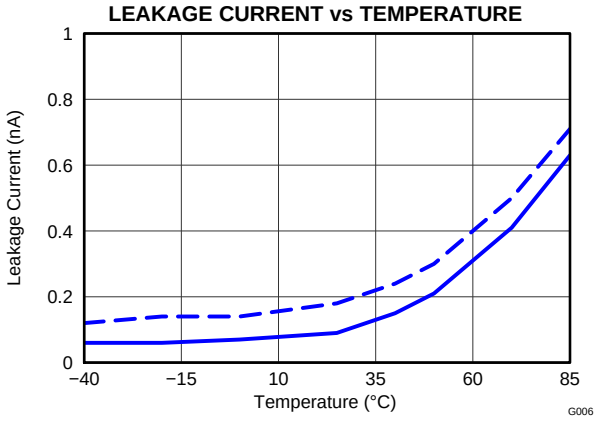

Figure 5.

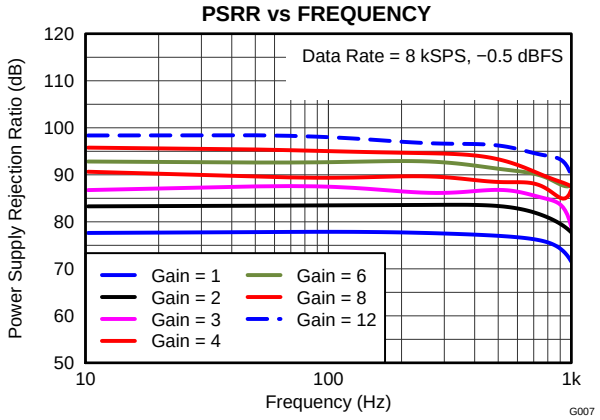

Figure 6.

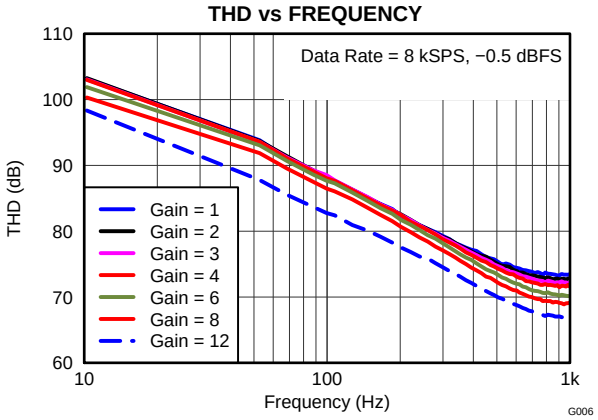

Figure 7.

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TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.42 V, VREFN = AVSS, external clock = 512 kHz, data rate = 500 SPS, and gain = 6, unless otherwise noted.

THD FFT PLOT
(60-Hz Signal)

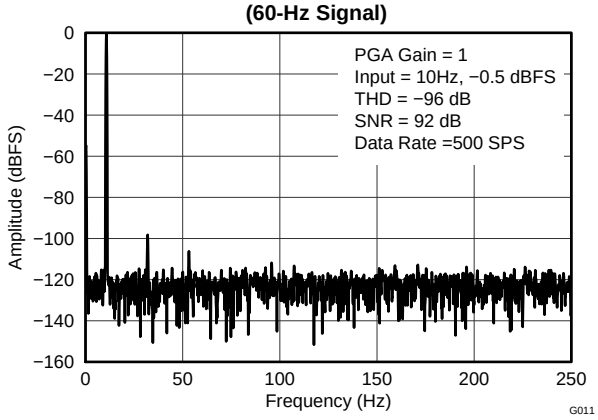

Figure 8.

FFT PLOT
(60-Hz Signal)

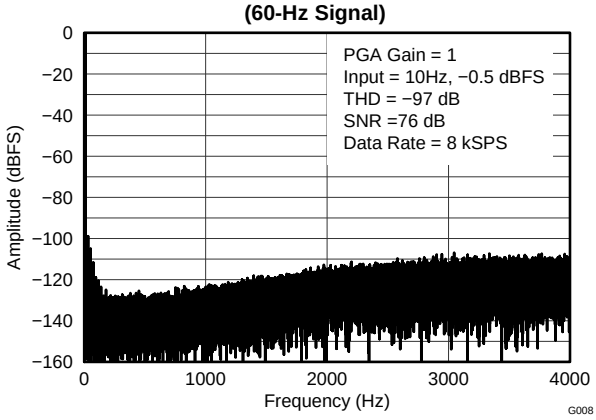

Figure 9.

TEST SIGNAL AMPLITUDE ACCURACY

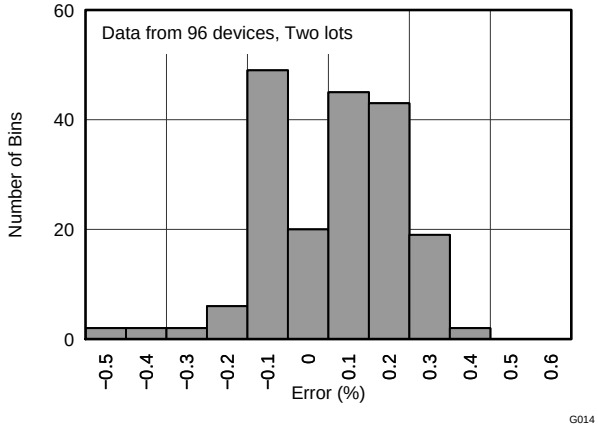

Figure 10.

LEAD-OFF COMPARATOR THRESHOLD ACCURACY

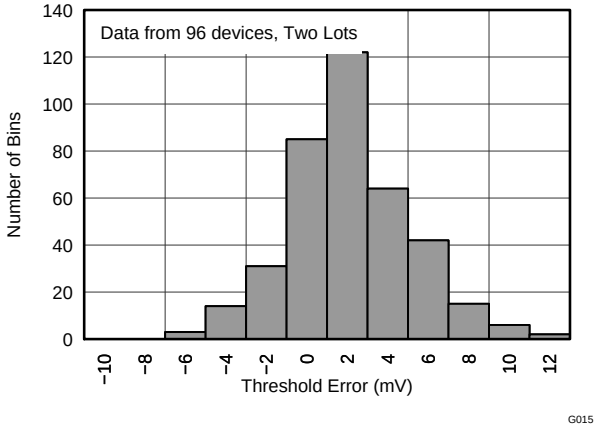

Figure 11.

LEAD-OFF CURRENT SOURCE ACCURACY DISTRIBUTION

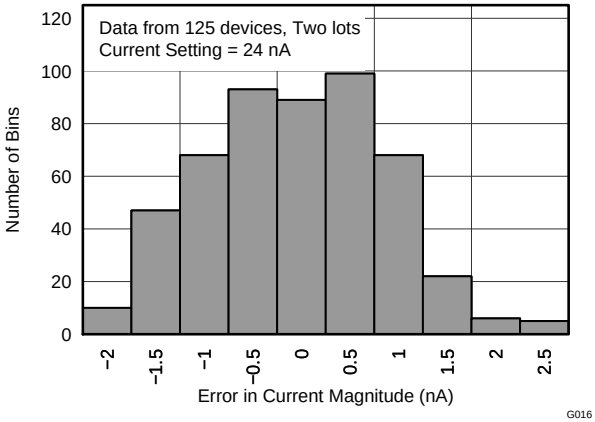

Figure 12.

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OVERVIEW

The ADS1191/2 are low-power, multichannel, simultaneously-sampling, 16-bit delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with integrated programmable gain amplifiers (PGAs). These devices integrate various ECG-specific functions that make them well-suited for scalable electrocardiogram (ECG), sports, and fitness applications. The devices can also be used in high-performance, multichannel data acquisition systems by powering down the ECG-specific circuitry.

The ADS1191/2 have a highly programmable multiplexer that allows for temperature, supply, input short, and RLD measurements. Additionally, the multiplexer allows any of the input electrodes to be programmed as the patient reference drive. The PGA gain can be chosen from one of seven settings (1, 2, 3, 4, 6, 8, and 12). The ADCs in the device offer data rates from 125 SPS to 8 kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides two general-purpose I/O (GPIO) pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to either 2.42 V or 4.033 V. The internal oscillator generates a 512-kHz clock. The versatile right leg drive (RLD) block allows the user to choose the average of any combination of electrodes to generate the patient drive signal. Lead-off detection can be accomplished either by using an external pull-up/pull-down resistor or the device internal current source/sink. An internal ac lead-off detection feature is also available. A detailed diagram of the ADS1191/2 is shown in Figure 13.

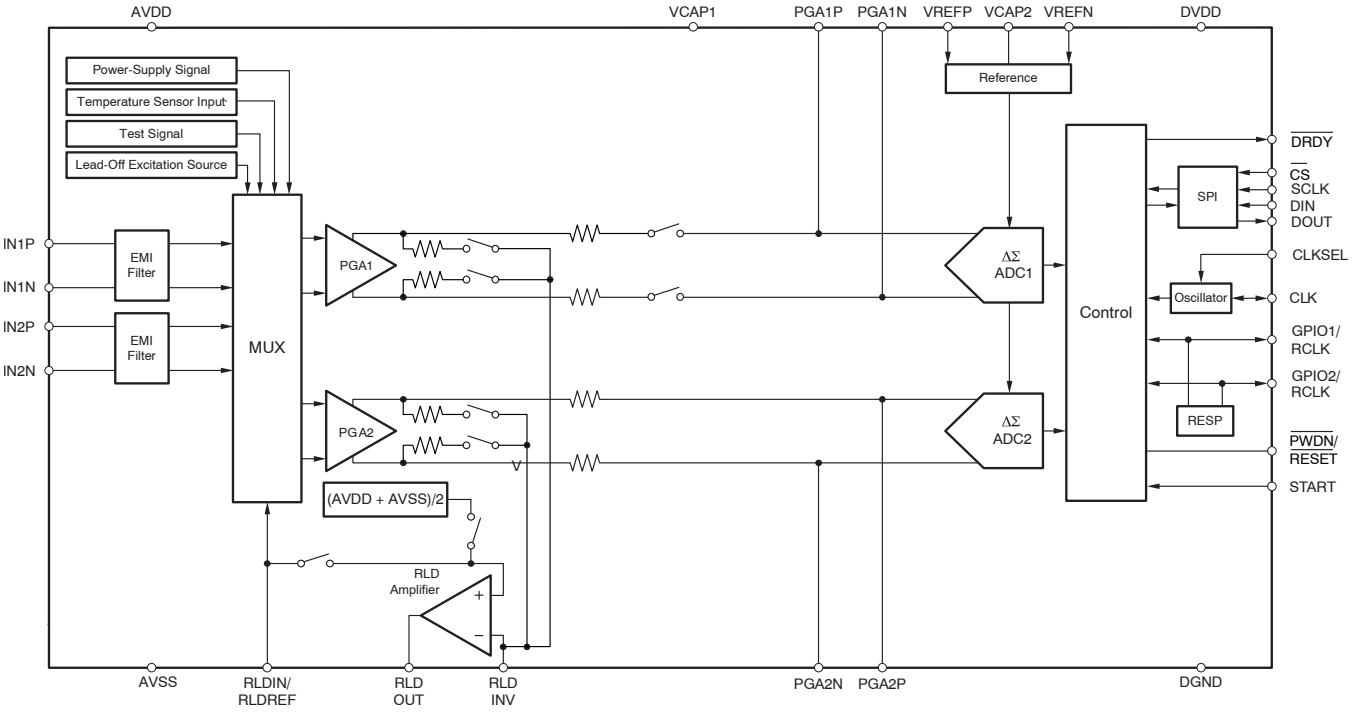

Figure 13. Functional Block Diagram

THEORY OF OPERATION

This section contains details of the ADS1191/2 internal functional elements. The analog blocks are discussed first followed by the digital interface. Blocks implementing ECG-specific functions are covered in the end.

Throughout this document, f_{CLK} denotes the frequency of the signal at the CLK pin, t_{CLK} denotes the period of the signal at the CLK pin, f_{DR} denotes the output data rate, t_{DR} denotes the time period of the output data, and f_{MOD} denotes the frequency at which the modulator samples the input.

EMI FILTER

An RC filter at the input acts as an EMI filter on channels 1 and 2. The –3-dB filter bandwidth is approximately 3 MHz.

INPUT MULTIPLEXER

The ADS1191/2 input multiplexers are very flexible and provide many configurable signal switching options. Refer to Figure 14 for a diagram of the ADS1191/2 multiplexer. Note that IN3P, IN3N, and RLDIN are common to both channels. VINP and VINN are separate for each of the three pins. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Selection of switch settings for each channel is made by writing the appropriate values to the CH1SET or CH2SET register (see the *CH1SET* and *CH2SET* Registers in the *Register Map* section for details.) More details of the ECG-specific features of the multiplexer are discussed in the *Input Multiplexer* subsection of the *ECG-Specifc Functions*.

Device Noise Measurements

Setting CHnSET[3:0] = 0001 sets the common-mode voltage of (VREFP + VREFN)/2 to both inputs of the channel. This setting can be used to test the inherent noise of the device in the user system.

Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. This functionality allows the entire signal chain to be tested out. Although the test signals are similar to the CAL signals described in the IEC60601-2-51 specification, this feature is not intended for use in compliance testing.

Control of the test signals is accomplished through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls switching at the required frequency.

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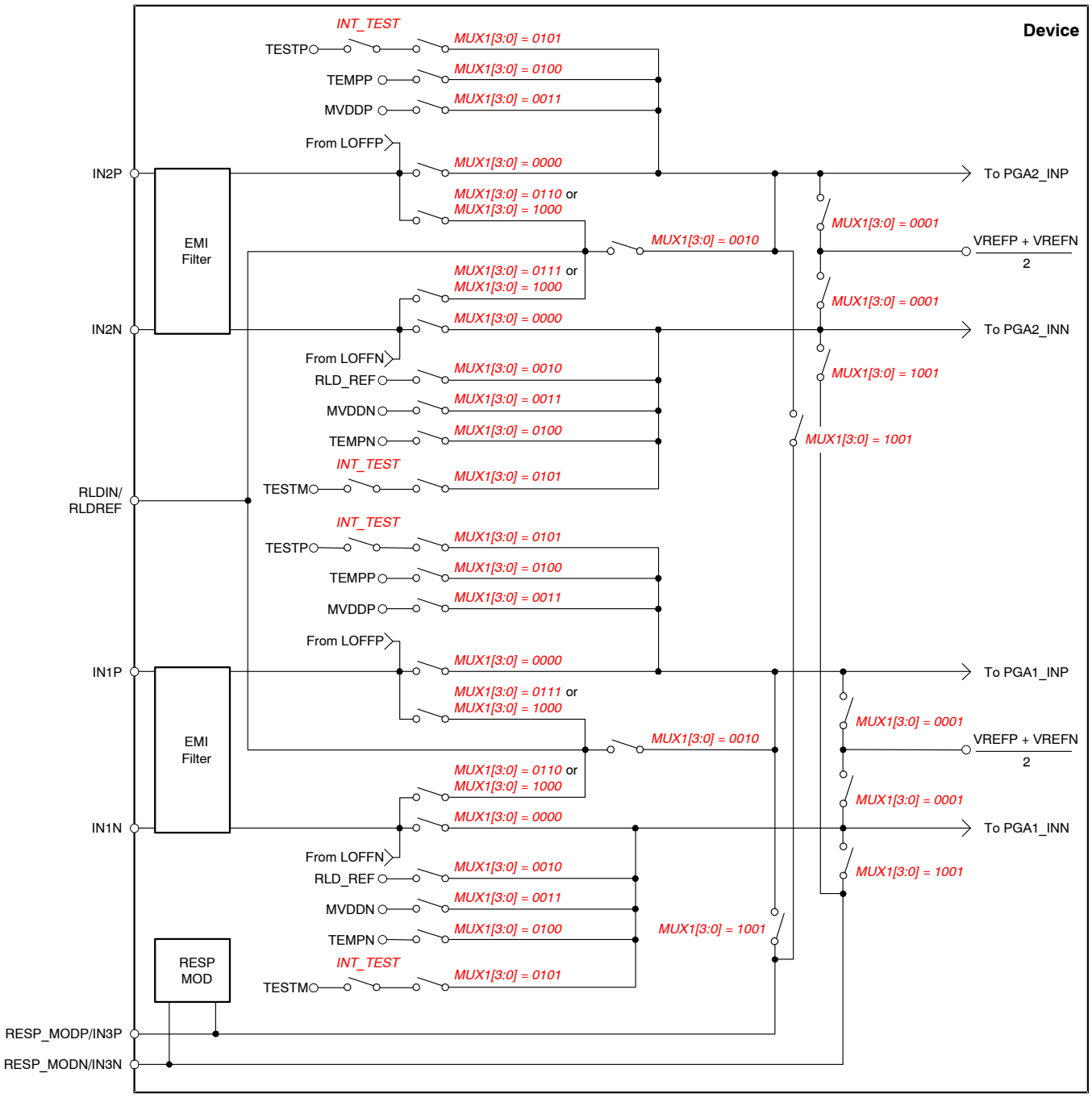

NOTE: MVDD monitor voltage supply depends on channel number; see the *Supply Measurements (MVDDP, MVDDN)* section.

Figure 14. Input Multiplexer Block for Both Channels

Auxiliary Differential Input (IN3N, IN3P)

The IN3N and IN3P signals can be used as a third multiplexed differential input channel. These inputs can be multiplexed to either of the ADC channels.

Temperature Sensor (TempP, TempN)

The ADS1191/2 contain an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 15. The difference in current densities of the diodes yields a difference in voltage that is proportional to absolute temperature.

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADS1191/2 causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 1 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to μV.

$$\text{Temperature (°C)} = \left(\frac{\text{Temperature Reading (}\mu\text{V)} - 168{,}000\ \mu\text{V}}{394\ \mu\text{V/°C}} \right) + 25°\text{C} \quad (1)$$

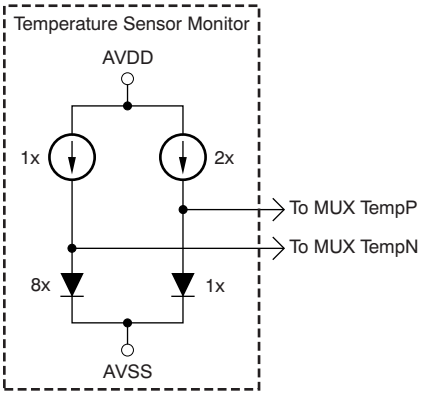

Figure 15. Measurement of the Temperature Sensor in the Input

Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 sets the channel inputs to different supply voltages of the device. For channel 1 (MVDDP – MVDDN) is [0.5(AVDD + AVSS)]; for channel 2 (MVDDP – MVDDN) is DVDD/4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

Lead-Off Excitation Signals (LoffP, LoffN)

The lead-off excitation signals are fed into the multiplexer before the switches. The comparators that detect the lead-off condition are also connected to the multiplexer block before the switches. For a detailed description of the lead-off block, refer to the *Lead-Off Detection* subsection in the *ECG-Specific Functions* section.

Auxiliary Single-Ended Input

The RLDIN pin is primarily used for routing the right leg drive signal to any of the electrodes in case the right leg drive electrode falls off. However, the RLDIN pin can be used as a multiple single-ended input channel. The signal at the RLDIN pin can be measured with respect to the voltage at the RLD_REF pin using either channel. This measurement is done by setting the channel multiplexer setting MUXn[3:0] to '0010' in the CH1SET and CH2SET registers.

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ANALOG INPUT

The analog input to the ADS1191/2 is fully differential. Assuming PGA = 1, the differential input (INP – INN) can span between $-V_{REF}$ to $+V_{REF}$. Refer to Table 4 for an explanation of the correlation between the analog input and the digital codes. There are two general methods of driving the analog input of the ADS1191/2: single-ended or differential, as shown in Figure 16 and Figure 17. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode + 1/2 V_{REF}) and the (common-mode – 1/2 V_{REF}). When the input is differential, the common-mode is given by (INP + INN)/2. Both the INP and INN inputs swing from (common-mode + 1/2 V_{REF} to common-mode – 1/2 V_{REF}). For optimal performance, it is recommended that the ADS1191/2 be used in a differential configuration.

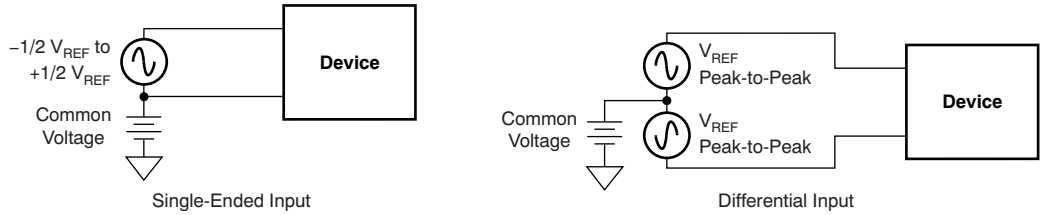
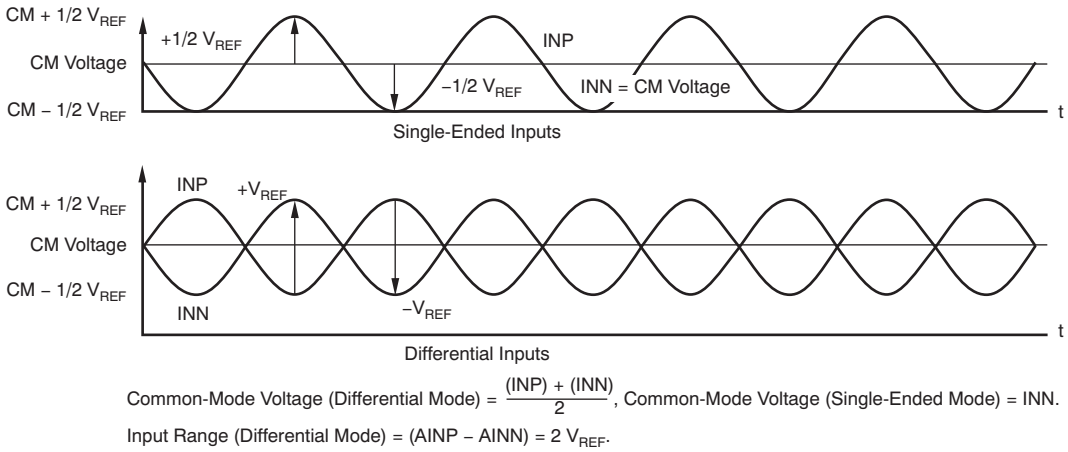


Figure 16. Methods of Driving the ADS1191/2: Single-Ended or Differential



Common-Mode Voltage (Differential Mode) = $\frac{(INP) + (INN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = INN.

Input Range (Differential Mode) = (AINP – AINN) = 2 V_{REF}.

Figure 17. Using the ADS1191/2 in the Single-Ended and Differential Input Modes

PGA SETTINGS AND INPUT RANGE

The PGA is a differential input/differential output amplifier, as shown in Figure 18. It has seven gain settings (1, 2, 3, 4, 6, 8, and 12) that can be set by writing to the CHnSET register (see the *CH1SET* and *CH2SET* Registers in the *Register Map* section for details). The ADS1191/2 have CMOS inputs and hence have negligible current noise.

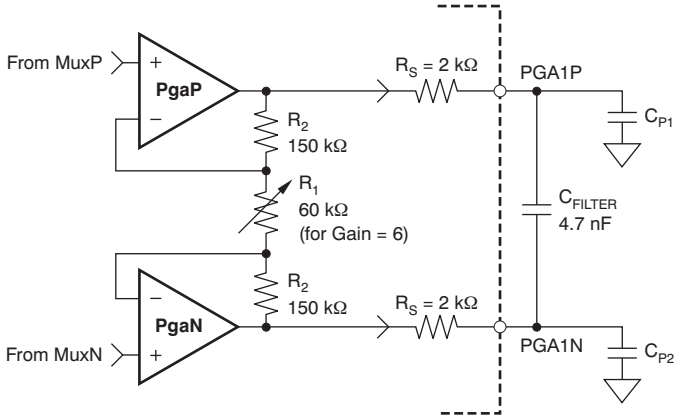


Figure 18. PGA Implementation

The resistor string of the PGA that implements the gain has 360 kΩ of resistance for a gain of 6. This resistance provides a current path across the outputs of the PGA in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input. The output of PGA is filtered by an RC filter before it goes to the ADC. The filter is formed by an internal resistor R_S = 2 kΩ and an external capacitor C_{FILTER} (4.7 nF, typical). This filter acts as an anti-aliasing filter with the –3-dB bandwidth of 8.4 kHz. The internal R_S resistor is accurate to 15% so actual bandwidth will vary. This RC filter also suppresses the glitch at the output of PGA caused by ADC sampling. The minimum value of C_{EXT} that can be used is 4 nF. A larger value C_{FILTER} capacitor can be used for increased attenuation at higher frequencies for anti-aliasing purposes. The tradeoff is that a larger capacitor value gives degraded THD performance. See Figure 19 for a plot showing the THD versus C_{FILTER} value.

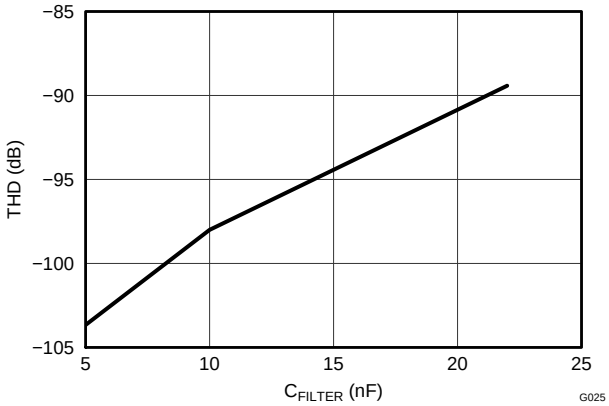


Figure 19. THD versus C_{FILTER} Value

Special care must be taken in PCB layout to minimize the parasitic capacitance C_{P1}/C_{P2}. The absolute value of these capacitances must be less than 20 pF. Ideally, C_{FILTER} should be placed right at the pins to minimize these capacitors. Mismatch between these capacitors will lead to CMRR degradation. Assuming everything else is perfectly matched, the 60 Hz CMRR as a function of this mismatch is given by Equation 2.

$$CMRR = 20\log \frac{Gain}{2\pi \times 2e3 \times \Delta C_P \times 60} \quad (2)$$

where $\Delta C_P = C_{P1} - C_{P2}$

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For example, a mismatch of 20 pF with a gain of 6 limits the CMRR to 112 dB. If ΔC_P is small, then the CMRR is limited by the PGA itself and is as specified in the Electrical Characteristics table. The PGA are chopped internally at either 8, 32, or 64 kSPS. The digital decimation filter filters out the chopping ripple in the normal path so the chopping ripple is not a concern. First-order filtering is provided by the RC filter at the PGA output. Additional filtering may be needed to suppress the chopping ripple. If the PGA output is routed to other circuitry, a 20-kΩ series resistance must be added in the path near the C_{FILTER} capacitor. The routing should be matched to maintain the CMRR performance.

Input Common-Mode Range

The usable input common-mode range of the front end depends on various parameters, including the maximum differential input signal, supply voltage, PGA gain, etc. This range is described in Equation 3:

$$AVDD - 0.4 - \left(\frac{\text{Gain } V_{MAX_DIFF}}{2}\right) > CM > AVSS + 0.4 + \left(\frac{\text{Gain } V_{MAX_DIFF}}{2}\right) \quad (3)$$

where:

V_{MAX_DIFF} = maximum differential signal at the input of the PGA

CM = common-mode range

For example:

If V_{DD} = 3 V, gain = 6, and V_{MAX_DIFF} = 350 mV
Then 1.25 V < CM < 1.75 V

Input Differential Dynamic Range

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. This range is shown in Equation 4.

$$\text{Max (INP – INN)} < \frac{V_{REF}}{\text{Gain}} \quad ; \quad \text{Full-Scale Range} = \frac{\pm V_{REF}}{\text{Gain}} = \frac{2\ V_{REF}}{\text{Gain}} \quad (4)$$

The 3-V supply, with a reference of 2.42 V and a gain of 6 for ECGs, is optimized for power with a differential input signal of approximately 300 mV. For higher dynamic range, a 5-V supply with a reference of 4 V (set by the VREF_4V bit of the CONFIG3 register) can be used to increase the differential dynamic range.

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ADC ΔΣ Modulator

Each channel of the ADS1191/2 has a 16-bit ΔΣ ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of $f_{MOD} = f_{CLK}/4$ or $f_{CLK}/16$, as determined by the CLK_DIV bit. In both cases, the sampling clock has a typical value of 128 kHz. As in the case of any ΔΣ modulator, the noise of the ADS1191/2 is shaped until $f_{MOD}/2$, as shown in Figure 20. The on-chip digital decimation filters explained in the next section can be used to filter out the noise at higher frequencies. These on-chip decimation filters also provide antialias filtering. This feature of the ΔΣ converters drastically reduces the complexity of the analog antialiasing filters that are typically needed with nyquist ADCs.

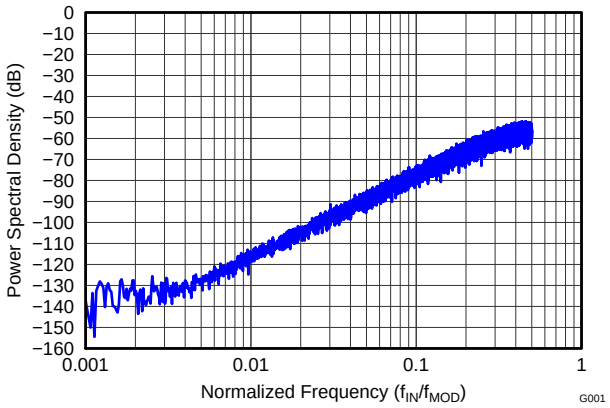

Figure 20. Power Spectral Density (PSD) of a ΔΣ Modulator (4-Bit Quantizer)

DIGITAL DECIMATION FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in ECG applications for implement software pace detection and ac lead-off detection.

The digital filter on each channel consists of a third-order sinc filter. The decimation ratio on the sinc filters can be adjusted by the DR bits in the CONFIG1 register (see the *Register Map* section for details). This setting is a global setting that affects all channels and, therefore, in a device all channels operate at the same data rate.

Sinc Filter Stage (sinx/x)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter.

Equation 5 shows the scaled Z-domain transfer function of the sinc filter.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{1 - Z^{-1}}\right|^{3} \tag{5}$$

The frequency domain transfer function of the sinc filter is shown in Equation 6.

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^{3} \tag{6}$$

where:

N = decimation ratio

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The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 21 shows the frequency response of the sinc filter and Figure 22 shows the roll-off of the sinc filter. With a step change at input, the filter takes 3 t_{DR} to settle. After a rising edge of the START signal, the filter takes t_{SETTLE} time to give the first data output. The settling time of the filters at various data rates are discussed in the *START* subsection of the *SPI Interface* section. Figure 23 and Figure 24 show the filter transfer function until $f_{MOD}/2$ and $f_{MOD}/16$, respectively, at different data rates. Figure 25 shows the transfer function extended until 4 f_{MOD}. It can be seen that the passband of the ADS1191/2 repeats itself at every f_{MOD}. The input R-C anti-aliasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

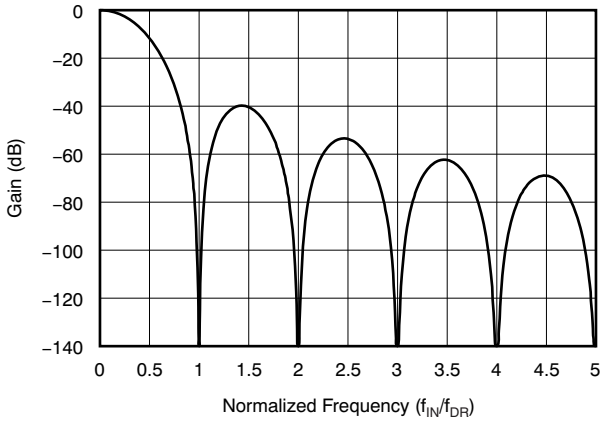

Figure 21. THD vs Frequency

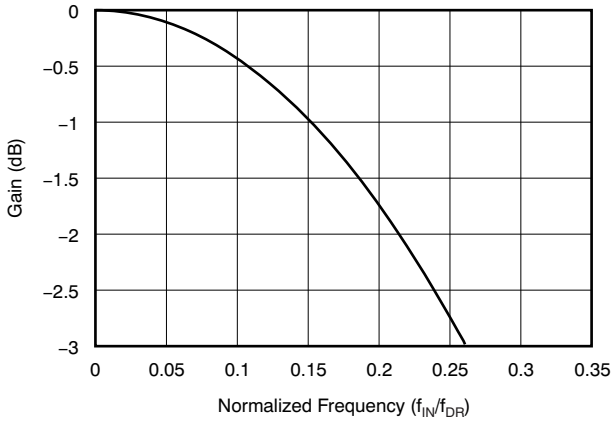

Figure 22. INL vs PGA Gain

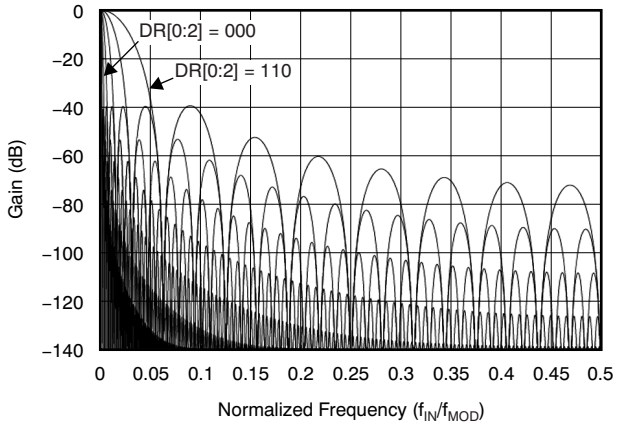

Figure 23. Transfer Function of On-Chip Decimation Filters Until $f_{MOD}/2$

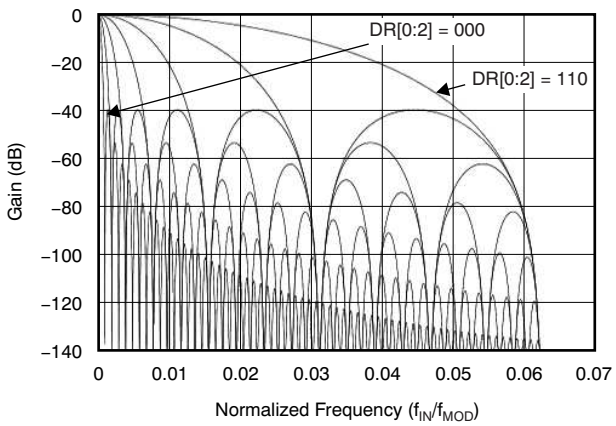

Figure 24. Transfer Function of On-Chip Decimation Filters Until $f_{MOD}/16$

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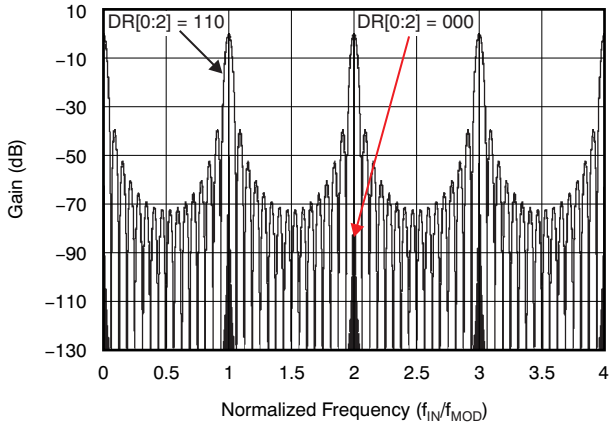
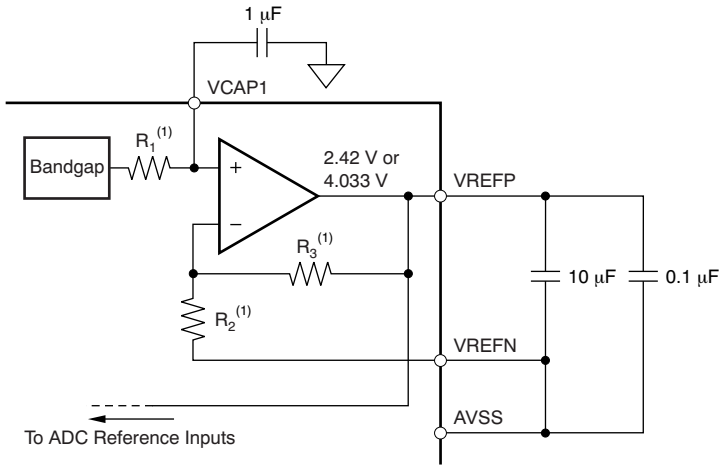


Figure 25. Transfer Function of On-Chip Decimation Filters Until $4f_{MOD}$ for DR[0:2] = 000 and DR[0:2] = 110

REFERENCE

Figure 26 shows a simplified block diagram of the internal reference of the ADS1191/2. The reference voltage is generated with respect to AVSS. The VREFN pin must always be connected to AVSS.



(1) For V_{REF} = 2.42 V: R_1 = 100 kΩ, R_2 = 200 kΩ, and R_3 = 200 kΩ. For V_{REF} = 4.033 V: R_1 = 84 kΩ, R_2 = 120 kΩ, and R_3 = 280 kΩ.

Figure 26. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end ECG systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10 Hz, so that the reference noise does not dominate the system noise. When using a 3-V analog supply, the internal reference must be set to 2.42 V. In case of a 5-V analog supply, the internal reference can be set to 4.033 V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be applied externally. Figure 27 shows a typical external reference drive circuitry. Power-down is controlled by the $\overline{\text{PD_REFBUF}}$ bit in the CONFIG3 register. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

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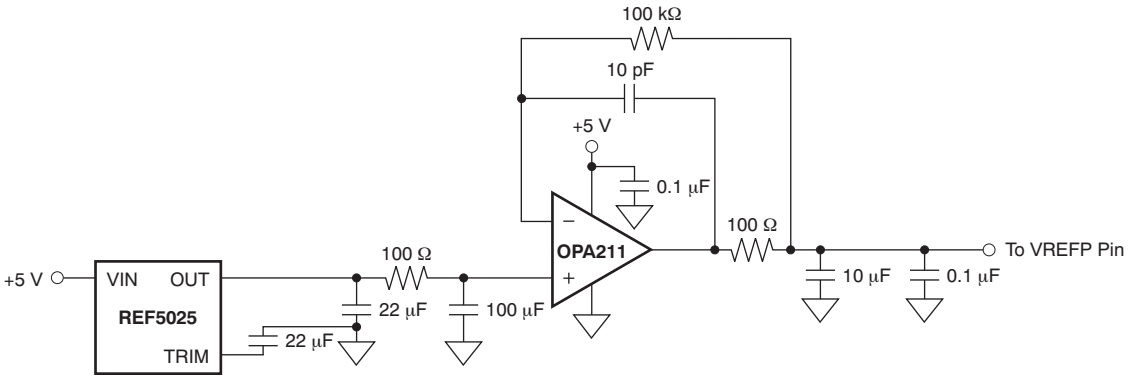

Figure 27. External Reference Driver

CLOCK

The ADS1191/2 provide two different methods for device clocking: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Over the specified temperature range the accuracy varies; see the Electrical Characteristics. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 3. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. It is recommended that during power-down the external clock be shut down to save power.

Table 3. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

The ADS1191/2 have the option to choose between two different external clock frequencies (512 kHz or 2.048 MHz). This frequency is selected by setting the CLK_DIV bit (bit 6) in the LOFF_STAT register. The modulator must be clocked at 128 kHz, regardless of the external clock frequency. Figure 28 shows the relationship between the external clock (f_{CLK}) and the modulator clock (f_{MOD}). The default mode of operation is f_{CLK} = 512 kHz. The higher frequency option has only been provided to allow the SPI to run at a higher speed. SCLK can be only twice the speed of f_{CLK} during a register read and/or write.

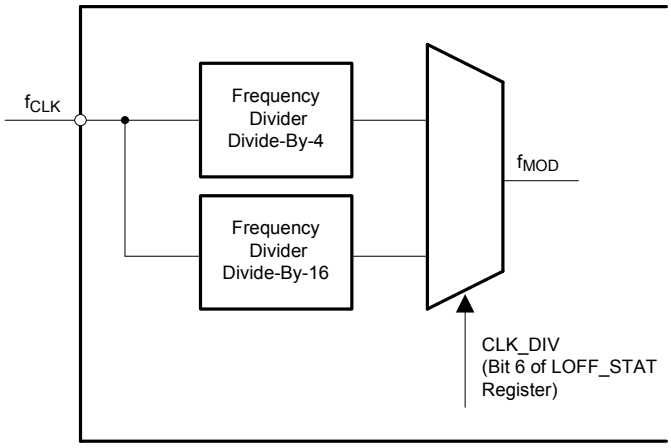

Figure 28. Relationship Between External Clock (f_{CLK}) and Modulator Clock (f_{MOD})

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DATA FORMAT

The ADS1191/2 outputs 16 bits of data per channel in binary twos complement format, MSB first. The LSB has a weight of $V_{REF}/(2^{15} - 1)$. A positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals exceeding full-scale. Table 4 summarizes the ideal output codes for different input signals. All 16 bits toggle when the analog input is at positive or negative full-scale.

Table 4. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ V_{REF}	7FFFh
$+V_{REF}/(2^{15} - 1)$	0001h
0	0000h
$-V_{REF}/(2^{15} - 1)$	FFFFh
≤ $-V_{REF}$ $(2^{15}/2^{15} - 1)$	8000h

(1) Excludes effects of noise, linearity, offset, and gain error.

SPI INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls the ADS1191/2 operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) selects the ADS1191/2 for SPI communication. $\overline{CS}$ must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. It is used to shift in commands and shift out data from the device. The serial clock (SCLK) features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS1191/2. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum limit for SCLK is specified in the *Serial Interface Timing* table. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed needed for the SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Cascade Mode* subsection of the *Multiple Device Configuration* section.)

$$t_{SCLK} < (t_{DR} - 4\ t_{CLK})/(N_{BITS}N_{CHANNELS} + 24) \quad (7)$$

For example, if the ADS1191/2 is used in a 500-SPS mode (two channels, 16-bit resolution), the minimum SCLK speed is approximately 36 kHz.

Data retrieval can be done either by putting the device in RDATAC mode or by issuing a RDATA command for data on demand. The above SCLK rate limitation applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. The above calculation assumes that there are no other commands issued in between data captures. SCLK can only be twice the speed of f_{CLK} during register reads and writes. For faster SPI interface, use f_{CLK} = 2.048 MHz and set the CLK_DIV register bit (in the LOFF_STAT register) to '1'.

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Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADS1191/2 (opcode commands and register data). The device latches data on DIN on the falling edge of SCLK.

Data Output (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADS1191/2. Data on DOUT are shifted out on the rising edge of SCLK. DOUT goes to a high-impedance state when $\overline{CS}$ is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and the system controller.

Figure 29 shows the data output protocol for ADS1192.

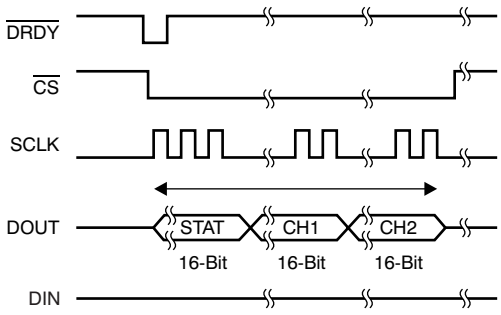

Figure 29. SPI Bus Data Output for the ADS1192 (Two Channels)

Data Retrieval

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the *RDATAC: Read Data Continuous* section) can be used to set the device in a mode to read the data continuously without sending opcodes. The read data command (see the *RDATA: Read Data* section) can be used to read just one data output from the device (see the *SPI Command Definitions* section for more details). The conversion data are read by shifting the data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{DRDY}$ returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADS1191/2, the number of data outputs is (16 status bits + 16 bits × 2 channels) = 48 bits. The format of the 16 status bits is (1100 + LOFF_STAT[4:0] + GPIO[1:0] + 5 zeros). The data format for each channel data are twos complement and MSB first. When channels are powered down using the user register setting, the corresponding channel output is set to '0'. However, the sequence of channel outputs remains the same.

The ADS1191/2 also provide a multiple readback feature. The data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte.

Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an output. When it transitions low, new conversion data are ready. The $\overline{CS}$ signal has no effect on the data ready signal. The behavior of $\overline{DRDY}$ is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the *RDATAC: Read Data Continuous* and *RDATA: Read Data* subsections of the *SPI Command Definitions* section for further details).

When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode.

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Figure 30 shows the relationship between $\overline{\text{DRDY}}$, DOUT, and SCLK during data retrieval (in case of an ADS1191/2 with a selected data rate that gives 16-bit resolution). DOUT is latched out at the rising edge of SCLK. $\overline{\text{DRDY}}$ is pulled high at the falling edge of SCLK. Note that $\overline{\text{DRDY}}$ goes high on the first falling edge SCLK regardless of the status of the $\overline{\text{CS}}$ signal and regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin.

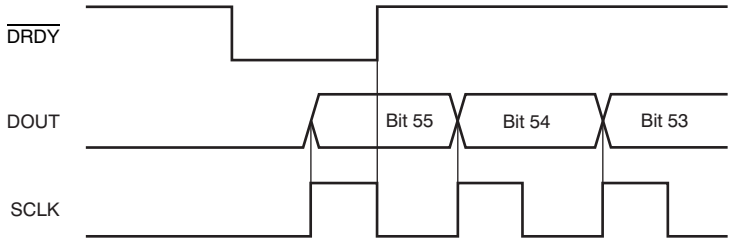

Figure 30. $\overline{\text{DRDY}}$ with Data Retrieval ($\overline{\text{CS}}$ = 0)

GPIO

The ADS1191/2 have a total of two general-purpose digital I/O (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or as outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float). The GPIO pins are set as inputs after power-on or after a reset. Figure 31 shows the GPIO port structure. The pins should be shorted to DGND with a series resistor if not used.

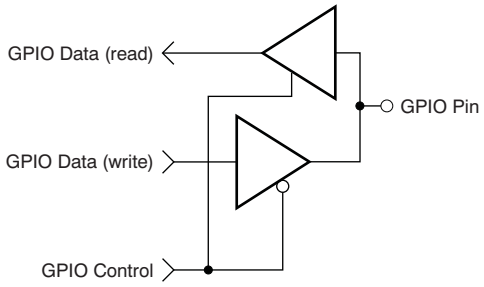

Figure 31. GPIO Port Pin

Power-Down/Reset ($\overline{\text{PWDN}}$/$\overline{\text{RESET}}$)

The $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pins are shared. If $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ is held low for longer than 2^9 t_{MOD}s, the device is powered down. The implementation is such that the device is always reset when $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ makes a transition from high to low. If the device is powered down it is reset first and then if 2^{10} clock elapses it is powered down. Hence, when powering up the device from a power-down state, all registers must be rewritten.

There are two methods to reset the ADS1191/2: pull the $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pin low, or send the RESET opcode command. When using the $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset it takes 18 t_{CLK} cycles to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever the CONFIG1 register is set to a new value with a WREG command.

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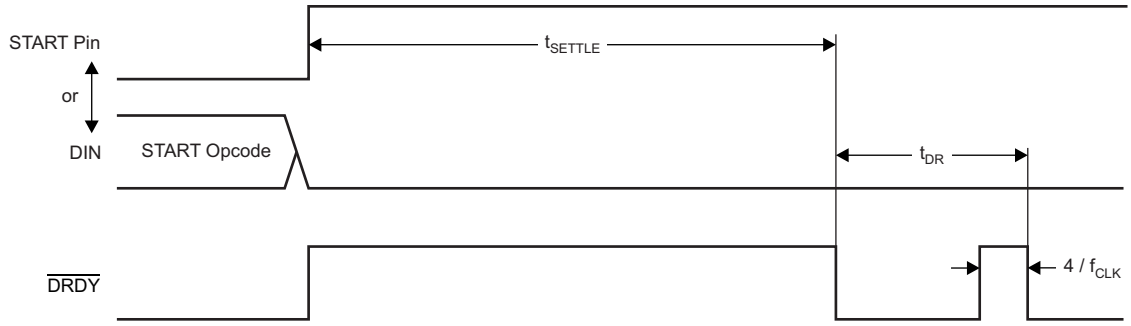
START

The START pin must be set high or the START command sent to begin conversions. When START is low or if the START command has not been sent, the device does not issue a $\overline{\text{DRDY}}$ signal (conversions are halted).

When using the START opcode to control conversion, hold the START pin low. The ADS1191/2 feature two modes to control conversion: continuous mode and single-shot mode. The mode is selected by SINGLE_SHOT (bit 7 of the CONFIG1 register). In multiple device configurations the START pin is used to synchronize devices (see the *Multiple Device Configuration* subsection of the *SPI Interface* section for more details).

Settling Time

The settling time (t_{SETTLE}) is the time it takes for the converter to output fully settled data when the START signal is pulled high. Once START is pulled high, $\overline{\text{DRDY}}$ is also pulled high. The next falling edge of $\overline{\text{DRDY}}$ indicates that data are ready. Figure 32 shows the timing diagram and Table 5 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). Table 4 shows the settling time as a function of t_{CLK}. Note that when START is held high and there is a step change in the input signal, it takes 3 t_{DR} for the filter to settle to the new value. Settled data are available on the fourth $\overline{\text{DRDY}}$ pulse. Settling time number uncertainty is one t_{MOD} cycle. Therefore, it is recommended to add one t_{MOD} cycle delay before issuing SCLK to retrieve data.



(1) Settling time uncertainty is one t_{MOD} cycle.

Figure 32. Settling Time

Table 5. Settling Time for Different Data Rates

DR[2:0]	SETTLING TIME(1)	UNIT(2)
000	4100	t_{MOD}
001	2052	t_{MOD}
010	1028	t_{MOD}
011	516	t_{MOD}
100	260	t_{MOD}
101	132	t_{MOD}
110	68	t_{MOD}
111	—	—

(1) Settling time uncertainty is one t_{MOD} cycle.
(2) t_{MOD} = 4 t_{CLK} for CLK_DIV = 0 and t_{MOD} = 16 t_{CLK} for CLK_DIV = 1.

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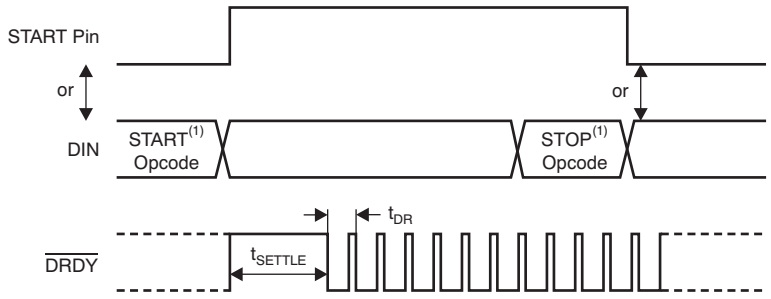
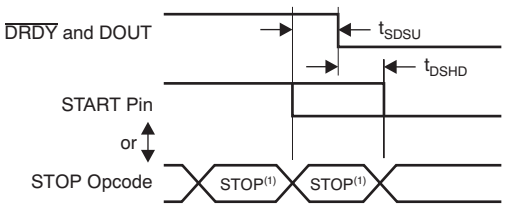
Continuous Mode

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 33, the $\overline{\text{DRDY}}$ output goes high when conversions are started and goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 34 and Table 6 show the required timing of $\overline{\text{DRDY}}$ to the START pin and the START/STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high. Note that when switching from pulse mode to continuous mode, the START signal is pulsed or a STOP command must be issued followed by a START command. This conversion mode is ideal for applications that require a fixed continuous stream of conversions results.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 33. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 34. START to $\overline{\text{DRDY}}$ Timing

Table 6. Timing Characteristics for Figure 34(1)

SYMBOL	DESCRIPTION	MIN	UNIT
t_{SDSU}	START pin low or STOP opcode to $\overline{\text{DRDY}}$ setup time to halt further conversions	8	t_{MOD}
t_{DSHD}	START pin low or STOP opcode to complete current conversion	8	t_{MOD}

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

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Single-Shot Mode

The single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG1 register to '1'. In single-shot mode, the ADS1191/2 perform a single conversion when the START pin is taken high or when the START opcode command is sent. As seen in Figure 34, when a conversion is complete, $\overline{\text{DRDY}}$ goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, $\overline{\text{DRDY}}$ remains low. To begin a new conversion, take the START pin low and then back high, or transmit the START opcode again. When switching from continuous mode to pulse mode, make sure the START signal is pulsed or issue a STOP command followed by a START command.

This conversion mode is provided for applications that require non-standard or non-continuous data rates. Issuing a START command or toggling the START pin high resets the digital filter, effectively dropping the data rate by a factor of four. Note that this mode leaves the system more susceptible to aliasing effects, requiring more complex analog anti-aliasing filters at the inputs. Loading on the host processor increases because it must toggle the START pin or send a START command to initiate a new conversion cycle.

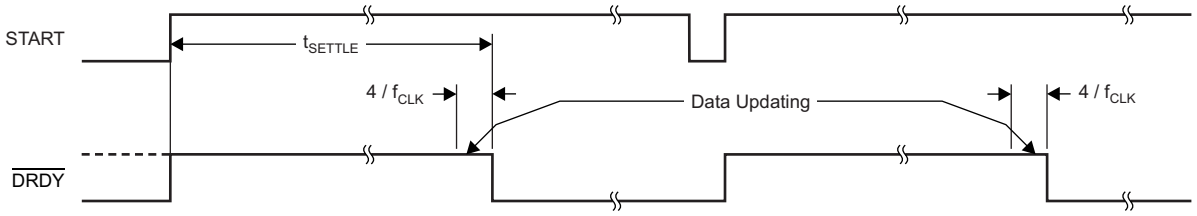

Figure 35. $\overline{\text{DRDY}}$ with No Data Retrieval in Single-Shot Mode

MULTIPLE DEVICE CONFIGURATION

The ADS1191/2 are designed to provide configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{\text{CS}}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface *n* devices is 3 + *n*.

The right leg drive amplifiers can be daisy-chained as explained in the *RLD Configuration with Multiple Devices* subsection of the *ECG-Specific Functions* section. To use the internal oscillator in a daisy-chain configuration, one of the devices must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to '1'. This master device clock is used as the external clock source for the other devices.

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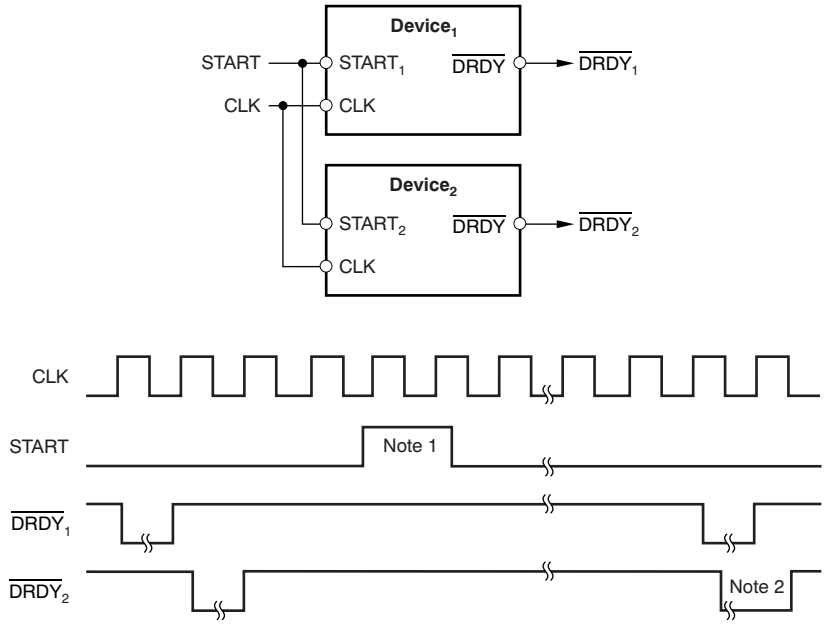
When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{\text{DRDY}}$ signal is fixed for a fixed data rate (see the *START* subsection of the *SPI Interface* section for more details on the settling times). Figure 36 shows the behavior of two devices when synchronized with the START signal.



(1) Start pulse must be at least one t_{MOD} cycle wide.

(2) Settling time number uncertainty is one t_{MOD} cycle.

Figure 36. Synchronizing Multiple Converters

Standard Mode

Figure 37 shows a configuration with two devices cascaded together. One of the devices is an ADS1192 (two-channel) and the other is an ADS1192 (two-channel). Together, they create a system with four channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{\text{CS}}$ being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus.

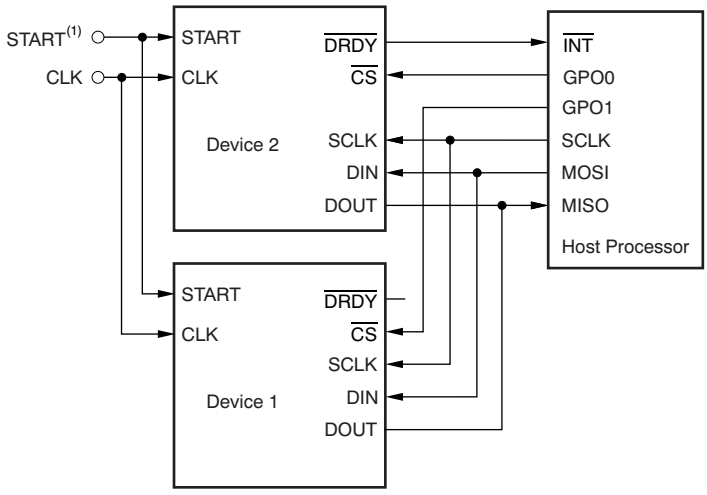


Figure 37. Multiple Device Configurations

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SPI COMMAND DEFINITIONS

The ADS1191/2 provide flexible configuration control. The opcode commands, summarized in Table 7, control and configure the operation of the ADS1191/2. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the ADS1191/2 on the seventh falling edge of SCLK. The register read/write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 7. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start/restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversion	0000 1010 (0Ah)	
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	
Data Read Commands			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	
Register Read Commands			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read/written – 1. For example, to read/write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read/write opcodes.

WAKEUP: Exit STANDBY Mode

This opcode exits the low-power standby mode; see the *STANDBY: Enter STANDBY Mode* subsection of the *SPI Command Definitions* section. Time is required when exiting standby mode (see the Electrical Characteristics for details). **There are no restrictions on the SCLK rate for this command and it can be issued any time.** Any following command must be sent after 4 t_{CLK} cycles.

STANDBY: Enter STANDBY Mode

This opcode command enters the low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the Electrical Characteristics. **There are no restrictions on the SCLK rate for this command and it can be issued any time.** Do not send any other command other than the wakeup command after the device enters the standby mode.

RESET: Reset Registers to Default Values

This command resets the digital filter cycle and returns all register settings to the default values. See the *Reset (RESET)* subsection of the *SPI Interface* section for more details. **There are no restrictions on the SCLK rate for this command and it can be issued any time.** It takes 9 f_{MOD} cycles to execute the RESET command. Avoid sending any commands during this time.

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START: Start Conversions

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command then have a gap of 4 t_{CLK} cycles between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the *START* subsection of the *SPI Interface* section for more details.) **There are no restrictions on the SCLK rate for this command and it can be issued any time.**

STOP: Stop Conversions

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no restrictions on the SCLK rate for this command and it can be issued any time.

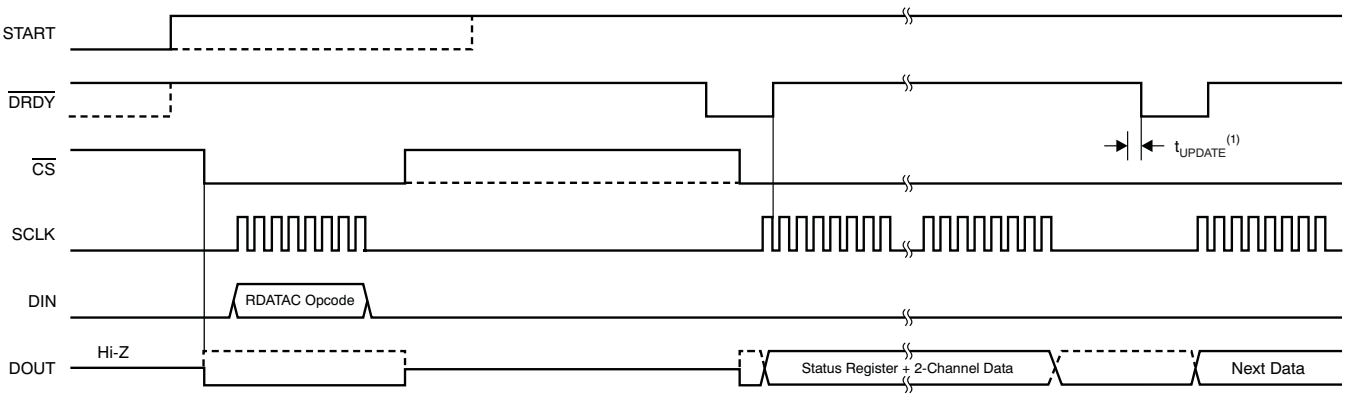
OFFSETCAL: Channel Offset Calibration

This command is used to cancel the channel offset. The CALIB_ON bit in the MISC2 register must be set to '1' before issuing this command. OFFSETCAL must be executed every time there is a change in the PGA gain settings.

RDATAC: Read Data Continuous

This opcode enables the output of conversion data on each $\overline{DRDY}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the default mode of the device and the device defaults in this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, an SDATAC command must be issued before any other commands can be sent to the device. There is no restriction on the SCLK rate for this command. However, the subsequent data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles. The timing for RDATAC is shown in Figure 38. As Figure 38 shows, there is a *keep out* zone of 4 t_{CLK} cycles around the $\overline{DRDY}$ pulse where this command cannot be issued in. If no data are retrieved from the device, DOUT and $\overline{DRDY}$ behave similarly in this mode. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 38 shows the recommended way to use the RDATAC command. RDATAC is ideally suited for applications such as data loggers or recorders where registers are set once and do not need to be re-configured.



(1) $t_{UPDATE} = 4 * t_{CLK}$. Do not read data during this time.

Figure 38. RDATAC Usage

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SDATAC: Stop Read Data Continuous

This opcode cancels the Read Data Continuous mode. There is no restriction on the SCLK rate for this command, but the following command must wait for 4 t_{CLK} cycles.

RDATA: Read Data

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There is no restriction on the SCLK rate for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after the RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption. Figure 39 shows the recommended way to use the RDATA command. RDATA is best suited for ECG- and EEG-type systems where register setting must be read or changed often between conversion cycles.

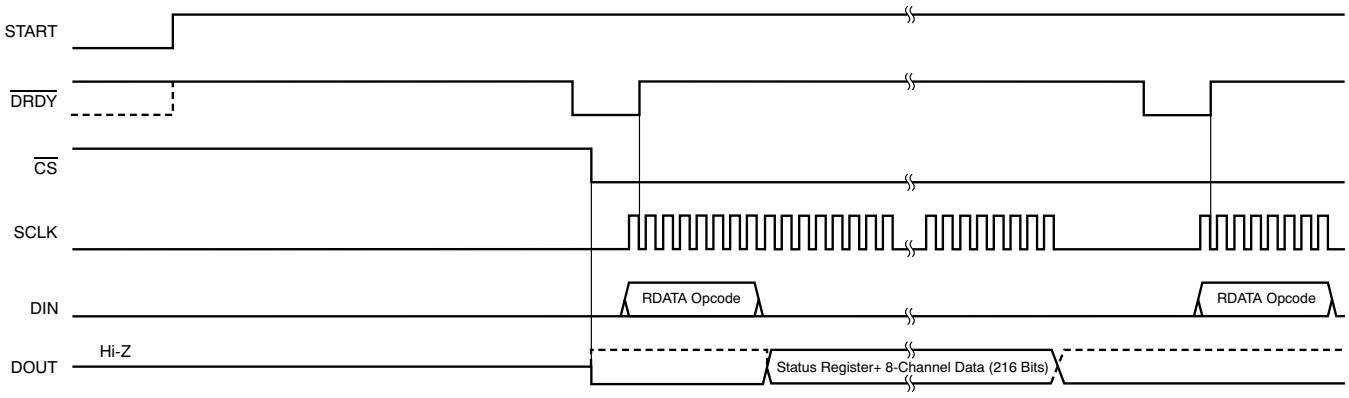

Figure 39. RDATA Usage

Sending Multi-Byte Commands

The ADS1191/2 serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assume CLK is 512 kHz, then $t_{SDECODE}$ (4 t_{CLK}) is 7.8125 µs. When SCLK is 16 MHz, one byte can be transferred in 500 ns. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay must be inserted so the end of the second byte arrives 7.3125 µs later. If SCLK is 1 MHz, one byte is transferred in 8 µs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to cease single-byte transfer per cycle to multiple bytes.

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RREG: Read From Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.

First opcode byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 40. When the device is in read data continuous mode it is necessary to issue a SDATAC command before the RREG command can be issued. The RREG command can be issued any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

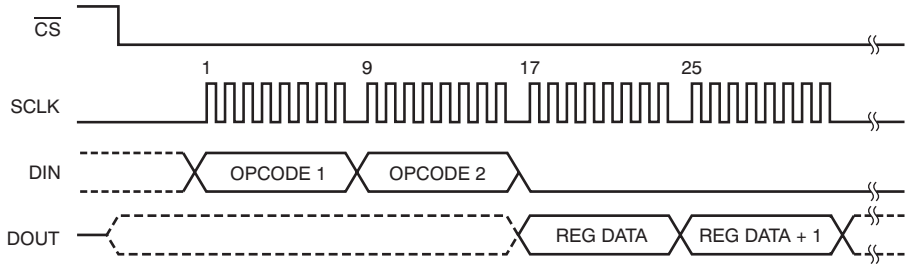

Figure 40. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address.

The second byte of the opcode specifies the number of registers to write – 1.

First opcode byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 41. The WREG command can be issued any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

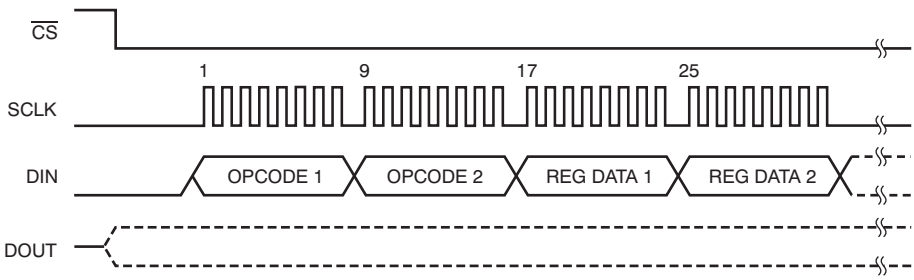

Figure 41. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

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REGISTER MAP

Table 8 describes the various ADS1191/2 registers.

Table 8. Register Assignments

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Settings (Read-Only Registers)										
00h	ID	XX	REV_ID7	REV_ID6	REV_ID5	1	0	0	REV_ID1	REV_ID0
Global Settings Across Channels										
01h	CONFIG1	02	SINGLE_SHOT	0	0	0	0	DR2	DR1	DR0
02h	CONFIG2	80	1	PDB_LOFF_COMP	PDB_REFBUF	VREF_4V	CLK_EN	0	INT_TEST	TEST_FREQ
03h	LOFF	10	COMP_TH2	COMP_TH1	COMP_TH0	1	ILEAD_OFF1	ILEAD_OFF0	0	FLEAD_OFF
Channel-Specific Settings										
04h	CH1SET	00	PD1	GAIN1_2	GAIN1_1	GAIN1_0	MUX1_3	MUX1_2	MUX1_1	MUX1_0
05h	CH2SET	00	PD2	GAIN2_2	GAIN2_1	GAIN2_0	MUX2_3	MUX2_2	MUX2_1	MUX2_0
06h	RLD_SENS	00	0	0	PDB_RLD	RLD_LOFF_SENS	RLD2N	RLD2P	RLD1N	RLD1P
07h	LOFF_SENS	00	0	0	FLIP2	FLIP1	LOFF2N	LOFF2P	LOFF1N	LOFF1P
08h	LOFF_STAT	00	0	CLK_DIV	0	RLD_STAT (read only)	IN2N_OFF	IN2P_OFF	IN1N_OFF	IN1P_OFF
GPIO and Other Registers										
09h	MISC1	00	0	0	0	0	0	0	1	0
0Ah	MISC2	02	CALIB_ON	0	0	0	0	0	RLDREF_INT	0
0Bh	GPIO	0C	0	0	0	0	GPIOC2	GPIOC1	GPIOD2	GPIOD1

User Register Description

ID: ID Control Register (Factory-Programmed, Read-Only)

Address = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REV_ID7	REV_ID6	REV_ID5	1	0	0	REV_ID1	REV_ID0

The ID Control Register is programmed during device manufacture to indicate device characteristics.

Bits[7:5] **REV_ID[7:5]: Revision identification**

000 = Reserved
001 = Reserved
010 = ADS1x9x device
011 = ADS1292R device
100 = Reserved
101 = Reserved
110 = Reserved
111 = Reserved

Bit 4 **Reads high**

Bits[3:2] **Reads low**

Bits[1:0] **REV_ID[1:0]: Revision identification**

00 = ADS1191
01 = ADS1192
10 = ADS1291
11 = ADS1292/2R

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CONFIG1: Configuration Register 1

Address = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SINGLE_SHOT	0	0	0	0	DR2	DR1	DR0

Configuration Register 1 configures each ADC channel sample rate.

Bit 7 **SINGLE_SHOT: Single-shot conversion**

This bit sets the conversion mode
0 = Continuous conversion mode (default)
1 = Single-shot mode

Bits[6:3] **Must be set to '0'**

Bits[2:0] **DR[2:0]: Channel oversampling ratio**

These bits determine the oversampling ratio of both channel 1 and channel 2.

BIT	OVERSAMPLING RATIO	DATA RATE(1)
000	f_{MOD}/1024	125 SPS
001	f_{MOD}/512	250 SPS
010	f_{MOD}/256	500 SPS (default)
011	f_{MOD}/128	1 kSPS
100	f_{MOD}/64	2 kSPS
101	f_{MOD}/32	4 kSPS
110	f_{MOD}/16	8 kSPS
111	Do not use	Do not use

(1) f_{CLK} = 512 kHz and CLK_DIV = 0 or f_{CLK} = 2.048 MHz and CLK_DIV = 1.

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CONFIG2: Configuration Register 2

Address = 02h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	PDB_LOFF_COMP	PDB_REFBUF	VREF_4V	CLK_EN	0	INT_TEST	TEST_FREQ

Configuration Register 2 configures the test signal, clock, reference, and LOFF buffer.

Bit 7 **Must be set to '1'**

Bit 6 **PDB_LOFF_COMP: Lead-off comparator power-down**

This bit powers down the lead-off comparators.
0 = Lead-off comparators disabled (default)
1 = Lead-off comparators enabled

Bit 5 **PDB_REFBUF: Reference buffer power-down**

This bit powers down the internal reference buffer so that the external reference can be used.
0 = Reference buffer is powered down (default)
1 = Reference buffer is enabled

Bit 4 **VREF_4V: Enables 4-V reference**

This bit chooses between 2.42-V and 4.033-V reference.
0 = 2.42-V reference (default)
1 = 4.033-V reference

Bit 3 **CLK_EN: CLK connection**

This bit determines if the internal oscillator signal is connected to the CLK pin when an internal oscillator is used.
0 = Oscillator clock output disabled (default)
1 = Oscillator clock output enabled

Bit 2 **Must be set to '0'**

Bit 1 **INT_TEST: Test signal selection**

This bit determines whether the test signal is turned on or off.
0 = Off (default)
1 = On; amplitude = ±(VREFP – VREFN)/2420

Bit 0 **TEST_FREQ: Test signal frequency.**

This bit determines the test signal frequency.
0 = At dc (default)
1 = Square wave at 1 Hz

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LOFF: Lead-Off Control Register

Address = 03h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	1	ILEAD_OFF1	ILEAD_OFF0	0	FLEAD_OFF

The Lead-Off Control Register configures the Lead-Off detection operation.

Bits[7:5] **COMP_TH[2:0]: Lead-off comparator threshold**

These bits determine the lead-off comparator threshold. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for a detailed description.

Comparator positive side

000 = 95% (default)
001 = 92.5%
010 = 90%
011 = 87.5%
100 = 85%
101 = 80%
110 = 75%
111 = 70%

Comparator negative side

000 = 5% (default)
001 = 7.5%
010 = 10%
011 = 12.5%
100 = 15%
101 = 20%
110 = 25%
111 = 30%

Bit 4 **Must be set to '1'**

Bits[3:2] **ILEAD_OFF[1:0]: Lead-off current magnitude**

These bits determine the magnitude of current for the current lead-off mode.
00 = 6 nA (default)
01 = 22 nA
10 = 6 µA
11 = 22 µA

Bit 1 **Must be set to '0'**

Bit 0 **FLEAD_OFF: Lead-off frequency**

This bit selects ac or dc lead-off.
0 = At dc lead-off detect (default)
1 = At ac lead-off detect at $f_{DR}/4$ (500 Hz for an 2-kHz output rate)

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CH1SET: Channel 1 Settings

Address = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD1	GAIN1_2	GAIN1_1	GAIN1_0	MUX1_3	MUX1_2	MUX1_1	MUX1_0

The CH1SET Control Register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details.

Bit 7 **PD1: Channel 1 power-down**

0 = Normal operation (default)
1 = Channel 1 power-down

Bits[6:4] **GAIN1[2:0]: Channel 1 PGA gain setting**

These bits determine the PGA gain setting for channel 1.

000 = 6 (default)
001 = 1
010 = 2
011 = 3
100 = 4
101 = 8
110 = 12
111 = Not available

Bits[3:0] **MUX1[3:0]: Channel 1 input selection**

These bits determine the channel 1 input selection.

0000 = Normal electrode input (default)
0001 = Input shorted (for offset measurements)
0010 = RLD_MEASURE
0011 = MVDD for supply measurement
0100 = Temperature sensor
0101 = Test signal
0110 = RLD_DRP (positive input is connected to RLDIN)
0111 = RLD_DRM (negative input is connected to RLDIN)
1000 = RLD_DRPM (both positive and negative inputs are connected to RLDIN)
1001 = Route IN3P and IN3N to channel 1 inputs
1010 = Reserved
1011 = Reserved
1100 = Reserved
1101 = Reserved
1110 = Reserved
1111 = Reserved

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CH2SET: Channel 2 Settings

Address = 05h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD2	GAIN2_2	GAIN2_1	GAIN2_0	MUX2_3	MUX2_2	MUX2_1	MUX2_0

The CH2SET Control Register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details.

Bit 7 **PD2: Channel 2 power-down**

0 = Normal operation (default)
1 = Channel 2 power-down

Bits[6:4] **GAIN2[2:0]: Channel 2 PGA gain setting**

These bits determine the PGA gain setting for channel 2.

000 = 6 (default)
001 = 1
010 = 2
011 = 3
100 = 4
101 = 8
110 = 12

Bits[3:0] **MUX2[3:0]: Channel 2 input selection**

These bits determine the channel 2 input selection.

0000 = Normal electrode input (default)
0001 = Input shorted (for offset measurements)
0010 = RLD_MEASURE
0011 = VDD/2 for supply measurement
0100 = Temperature sensor
0101 = Test signal
0110 = RLD_DRP (positive electrode is the driver)
0111 = RLD_DRM (negative electrode is the driver)
1000 = Reserved
1001 = Route IN3P and IN3N to channel 2 inputs
1010 = Reserved
1011 = Reserved
1100 = Reserved
1101 = Reserved
1110 = Reserved
1111 = Reserved

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RLD_SENS: Right Leg Drive Sense Selection

Address = 06h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	PDB_RLD	RLD_LOFF_SENS	RLD2N	RLD2P	RLD1N	RLD1P

This register controls the selection of the positive and negative signals from each channel for right leg drive derivation. See the *Right Leg Drive (RLD DC Bias Circuit)* subsection of the *ECG-Specific Functions* section for details.

Bits[7:6] **Must be set to '0'**

Bit 5 **PDB_RLD: RLD buffer power**

This bit determines the RLD buffer power state.
0 = RLD buffer is powered down (default)
1 = RLD buffer is enabled

Bit 4 **RLD_LOFF_SENSE: RLD lead-off sense function**

This bit enables the RLD lead-off sense function.
0 = RLD lead-off sense is disabled (default)
1 = RLD lead-off sense is enabled

Bit 3 **RLD2N: Channel 2 RLD negative inputs**

This bit controls the selection of negative inputs from channel 2 for right leg drive derivation.
0 = Not connected (default)
1 = RLD connected to IN2N

Bit 2 **RLD2P: Channel 2 RLD positive inputs**

This bit controls the selection of positive inputs from channel 2 for right leg drive derivation.
0 = Not connected (default)
1 = RLD connected to IN2P

Bit 1 **RLD1N: Channel 1 RLD negative inputs**

This bit controls the selection of negative inputs from channel 1 for right leg drive derivation.
0 = Not connected (default)
1 = RLD connected to IN1N

Bit 0 **RLD1P: Channel 1 RLD positive inputs**

This bit controls the selection of positive inputs from channel 1 for right leg drive derivation.
0 = Not connected (default)
1 = RLD connected to IN1P

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LOFF_SENS: Lead-Off Sense Selection

Address = 07h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	FLIP2	FLIP1	LOFF2N	LOFF2P	LOFF1N	LOFF1P

This register selects the positive and negative side from each channel for lead-off detection. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Note that the LOFF_STAT register bits should be ignored if the corresponding LOFF_SENS bits are set to '1'.

Bits[7:6] **Must be set to '0'**

Bit 5 **FLIP2: Current direction selection**

This bit controls the direction of the current used for lead-off derivation for channel 2.
0 = Disabled (default)
1 = Enabled

Bit 4 **FLIP1: Current direction selection**

This bit controls the direction of the current used for lead-off derivation for channel 1.
0 = Disabled (default)
1 = Enabled

Bit 3 **LOFF2N: Channel 2 lead-off detection negative inputs**

This bit controls the selection of negative input from channel 2 for lead-off detection.
0 = Disabled (default)
1 = Enabled

Bit 2 **LOFF2P: Channel 2 lead-off detection positive inputs**

This bit controls the selection of positive input from channel 2 for lead-off detection.
0 = Disabled (default)
1 = Enabled

Bit 1 **LOFF1N: Channel 1 lead-off detection negative inputs**

This bit controls the selection of negative input from channel 1 for lead-off detection.
0 = Disabled (default)
1 = Enabled

Bit 0 **LOFF1P: Channel 1 lead-off detection positive inputs**

This bit controls the selection of positive input from channel 1 for lead-off detection.
0 = Disabled (default)
1 = Enabled

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LOFF_STAT: Lead-Off Status

Address = 08h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	CLK_DIV	0	RLD_STAT (read only)	IN2N_OFF (read only)	IN2P_OFF (read only)	IN1N_OFF (read only)	IN1P_OFF (read only)

This register stores the status of whether the positive or negative electrode on each channel is on or off. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Ignore the LOFF_STAT values if the corresponding LOFF_SENS bits are not set to '1'.

'0' is lead-on (default) and '1' is lead-off. When the LOFF_SENS bits[3:0] are '0', the LOFF_STAT bits should be ignored.

Bit 7 **Must be set to '0'**

Bit 6 **CLK_DIV: Clock divider selection**

This bit sets the divider ratio between f_{CLK} and f_{MOD}. Two external clock values are supported: 512 kHz and 2.048 MHz. This bit must be set so that f_{MOD} = 128 kHz.
0 = f_{MOD}/4 (default, when f_{CLK} = 512 kHz)
1 = f_{MOD}/16 (when f_{CLK} = 2.048 MHz)

Bit 5 **Must be set to '0'**

Bit 4 **RLD_STAT: RLD lead-off status**

This bit determines the status of RLD.
0 = RLD is connected (default)
1 = RLD is not connected

Bit 3 **IN2N_OFF: Channel 2 negative electrode status**

This bit determines if the channel 2 negative electrode is connected or not.
0 = Connected (default)
1 = Not connected

Bit 2 **IN2P_OFF: Channel 2 positive electrode status**

This bit determines if the channel 2 positive electrode is connected or not.
0 = Connected (default)
1 = Not connected

Bit 1 **IN1N_OFF: Channel 1 negative electrode status**

This bit determines if the channel 1 negative electrode is connected or not.
0 = Connected (default)
1 = Not connected

Bit 0 **IN1P_OFF: Channel 1 positive electrode status**

This bit determines if the channel 1 positive electrode is connected or not.
0 = Connected (default)
1 = Not connected

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MISC1: Miscellaneous Control Register 1

Address = 09h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	1	0

This register controls the miscellaneous functionality. For the ADS1191 and ADS1192 devices, 02h must be written to the MISC1 register.

Bits[7:2] **Must be set to '0'**

Bit 6 **Must be set to '1'**

Bit 0 **Must be set to '0'**

MISC2: Miscellaneous Control Register 2

Address = 0Ah

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CALIB_ON	0	0	0	0	0	RLDREF_INT	0

This register controls the calibration functionality.

Bit 7 **CALIB_ON: Calibration on**

This bit is used to enable offset calibration.
0 = Off (default)
1 = On

Bits[6:2] **Must be '0'**

Bit 1 **RLDREF_INT: RLDREF signal**

This bit determines the RLDREF signal source.
0 = RLDREF is external (default)
1 = RLDREF is fed internally

Bit 0 **Must be set to '0'**

GPIO: General-Purpose I/O Register

Address = 0Bh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	GPIOC2	GPIOC1	GPIOD2	GPIOD1

This register controls the GPIO pins.

Bits[7:4] **Must be '0'**

Bits[3:2] **GPIOC[2:1]: GPIO 1 and 2 control**

These bits determine if the corresponding GPIOD pin is an input or output.
0 = Output
1 = Input (default)

Bits[1:0] **GPIOD[2:1]: GPIO 1 and 2 data**

These bits are used to read and write data to the GPIO ports.
When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.

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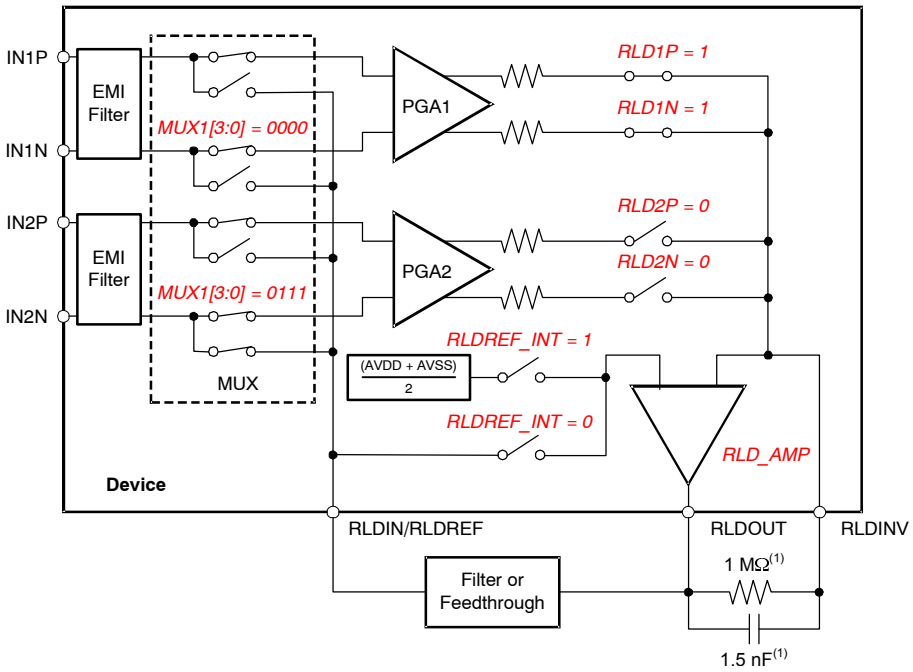
ECG-SPECIFIC FUNCTIONS

INPUT MULTIPLEXER (REROUTING THE RIGHT LEG DRIVE SIGNAL)

The input multiplexer has ECG-specific functions for the right leg drive signal. The RLD signal is available at the RLDOUT pin once the appropriate channels are selected for the RLD derivation, feedback elements are installed external to the chip, and the loop is closed. This signal can be fed after filtering or fed directly into the RLDIN pin as shown in Figure 42. This RLDIN signal can be multiplexed into any one of the input electrodes by setting the MUX bits of the appropriate channel set registers to '0110' for P-side or '0111' for N-side. Figure 42 shows the RLD signal generated from channel 1 and routed to the N-side of channel 2. This feature can be used to dynamically change the electrode that is used as the reference signal to drive the patient body. Note that the corresponding channel cannot be used and can be powered down.



(1) Typical values for example only.

Figure 42. Example of RLDOUT Signal Configured to be Routed to IN2N

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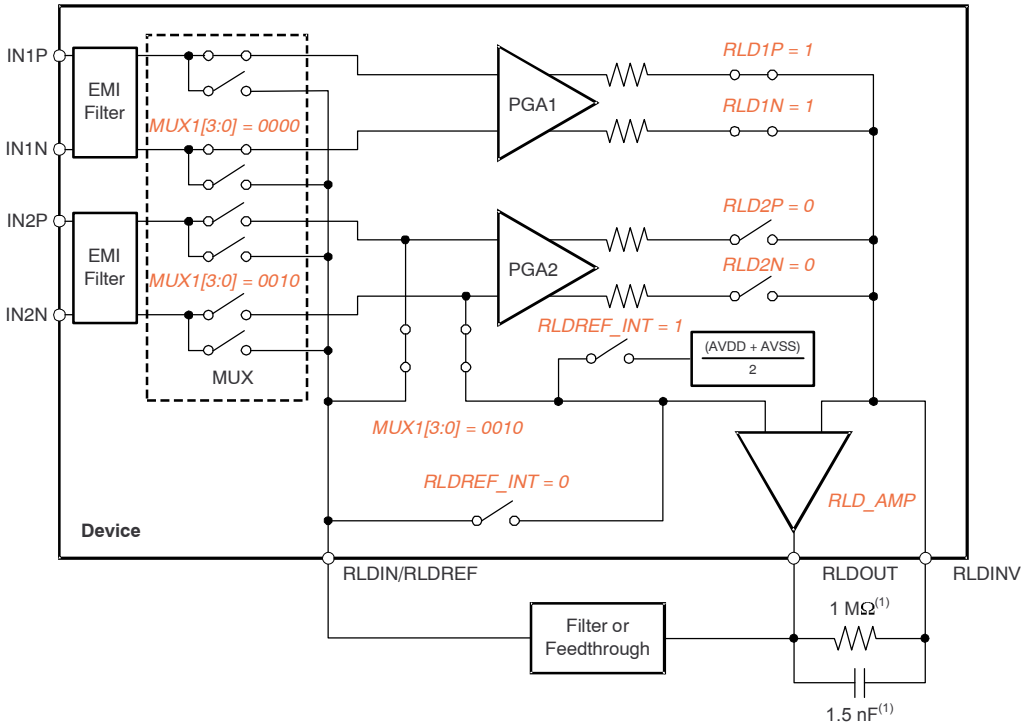
Input Multiplexer (Measuring the Right Leg Drive Signal)

Also, the RLDOUT signal can be routed to a channel (that is not used for the calculation of RLD) for measurement. Figure 43 shows the register settings to route the RLDIN signal to channel 2. The measurement is done with respect to the voltage on the RLDREF pin. If RLDREF is chosen to be internal, it would be at (AVDD + AVSS)/2. This feature is useful for debugging purposes during product development.



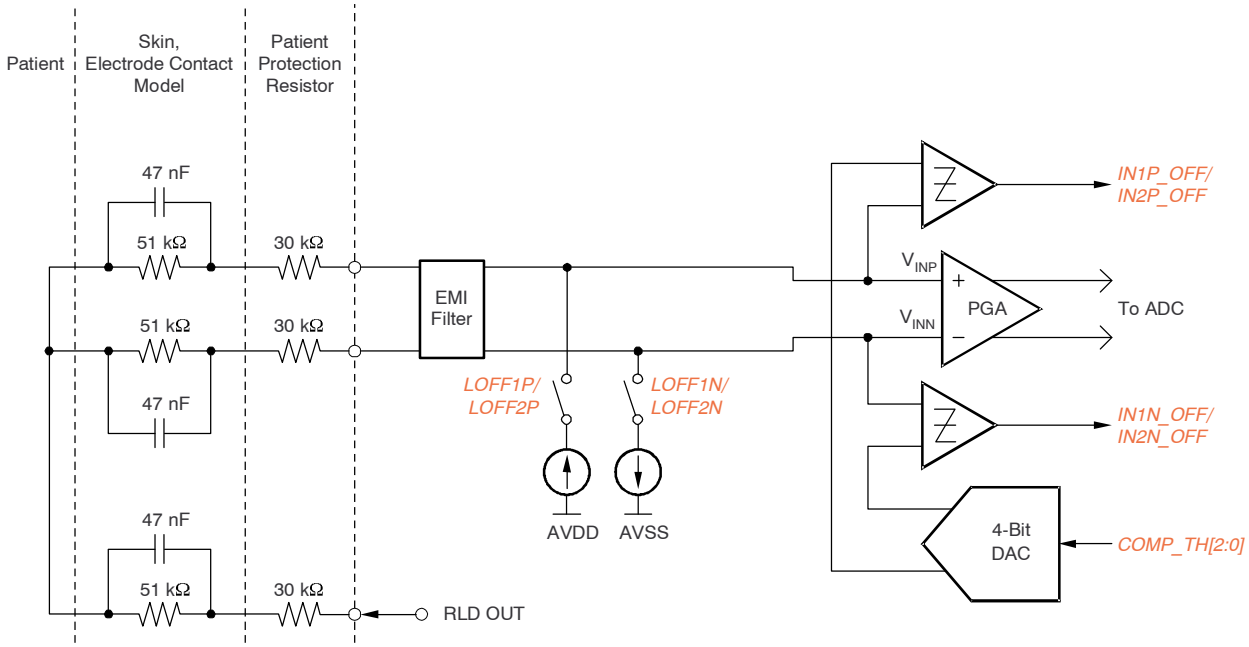
(1) Typical values for example only.

Figure 43. RLDOUT Signal Configured to be Read Back by Channel 2

LEAD-OFF DETECTION

Patient electrode impedances are known to decay over time. It is necessary to continuously monitor these electrode connections to verify a suitable connection is present. The ADS1191/2 lead-off detection functional block provides significant flexibility to the user to choose from various lead-off detection strategies. Though called lead-off detection, this is in fact an *electrode-off* detection.

The basic principle is to inject an excitation signal and measure the response to find out if the electrode is off. As shown in the lead-off detection functional block diagram in Figure 44, this circuit provides two different methods of determining the state of the patient electrode. The methods differ in the frequency content of the excitation signal. Lead-off can be selectively done on a per channel basis using the LOFF_SENS register. Also, the internal excitation circuitry can be disabled and just the sensing circuitry can be enabled.



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification the latest revision of IEC 60601).

Figure 44. Lead-Off Detection

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DC Lead-Off

In this method, the lead-off excitation is with a dc signal. The dc excitation signal can be chosen from either an external pull-up/pull-down resistor or a current source/sink, as shown in Figure 45. One side of the channel is pulled to supply and the other side is pulled to ground. The internal current source and current sink can be swapped by setting thebits in the LOFF_FLIP register. In case of current source/sink, the magnitude of the current can be set by using the ILEAD_OFF[1:0] bits in the LOFF register. The current source/sink gives larger input impedance compared to the 10-MΩ pull-up/pull-down resistor.

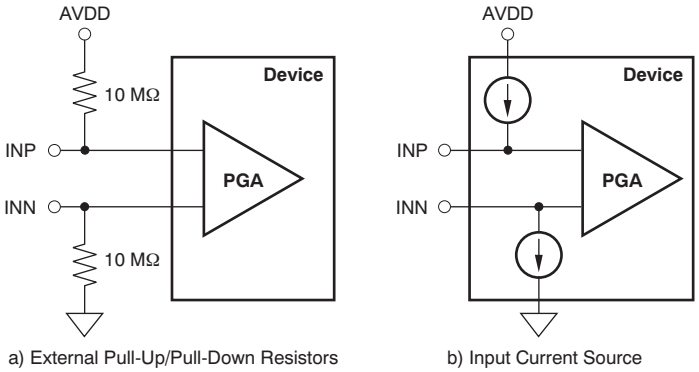

Figure 45. DC Lead-Off Excitation Options

Sensing of the response can be done either by looking at the digital output code from the device or by monitoring the input voltages with an on-chip comparator. If either of the electrodes is off, the pull-up resistors and/or the pull-down resistors saturate the channel. By looking at the output code it can be determined that either the P-side or the N-side is off. To pinpoint which one is off, the comparators must be used. The input voltage is also monitored using a comparator and a 4-bit digital-to-analog converter (DAC) whose levels are set by the COMP_TH[2:0] bits in the LOFF register. The output of the comparators are stored in the LOFF_STAT register. These two registers are available as a part of the output data stream. (See the *Data Output Protocol (DOUT)* subsection of the *SPI Interface* section.) If dc lead-off is not used, the lead-off comparators can be powered down by setting the PD_LOFF_COMP bit in the CONFIG2 register.

An example procedure to turn on dc lead-off is given in the *Lead-Off* subsection of the *Quick-Start Guide* section.

AC Lead-Off

In this method, an out-of-band ac signal is used for excitation. The ac signal is generated by alternatively providing an internal current source and current sink at the input with a fixed frequency. The excitation frequency is a function of the output data rate and is $f_{DR}/4$. This out-of-band excitation signal is passed through the channel and measured at the output.

Sensing of the ac signal is done by passing the signal through the channel to digitize it and measure at the output. The ac excitation signals are introduced at a frequency that is above the band of interest, generating an out-of-band differential signal that can be filtered out separately and processed. By measuring the magnitude of the excitation signal at the output spectrum, the lead-off status can be calculated. Therefore, the ac lead-off detection can be accomplished simultaneously with the ECG signal acquisition.

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RLD Lead-Off

The ADS1191/2 provide two modes for determining whether the RLD is correctly connected:

- RLD lead-off detection during normal operation
- RLD lead-off detection during power-up

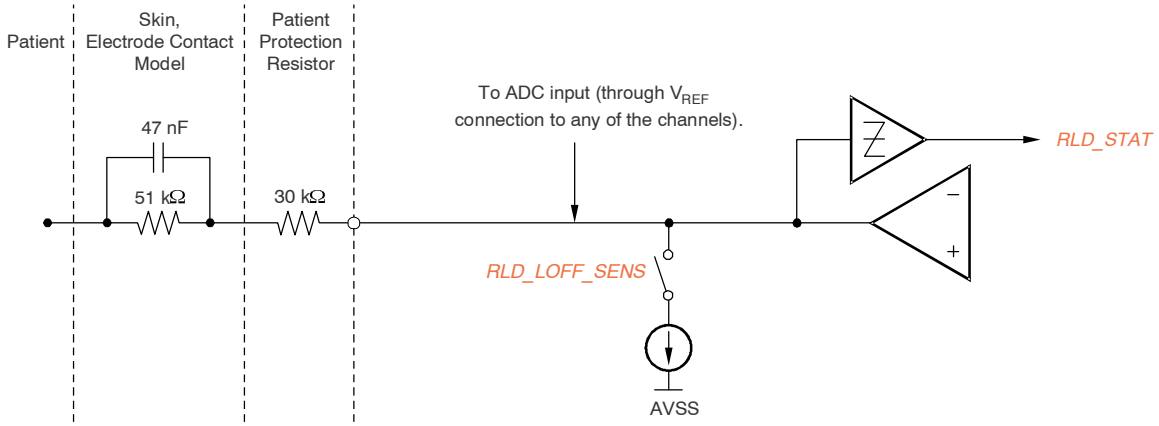
The following sections provide details of the two modes of operation.

RLD Lead-Off Detection During Normal Operation

During normal operation, the ADS1191/2 RLD lead-off at power-up function cannot be used because it is necessary to power off the RLD amplifier.

RLD Lead-Off Detection At Power-Up

This feature is included in the ADS1191/2 for use in determining whether the right leg electrode is suitably connected. At power-up, the ADS1191/2 provides a procedure to determine the RLD electrode connection status using a current sink, as shown in Figure 46. The reference level of the comparator is set to determine the acceptable RLD impedance threshold.



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification the latest revision of IEC 60601).

Figure 46. RLD Lead-Off Detection at Power-Up

When the RLD amplifier is powered on, the current source has no function. Only the comparator can be used to sense the voltage at the output of the RLD amplifier. The comparator thresholds are set by the same LOFF[7:5] bits used to set the thresholds for other negative inputs.

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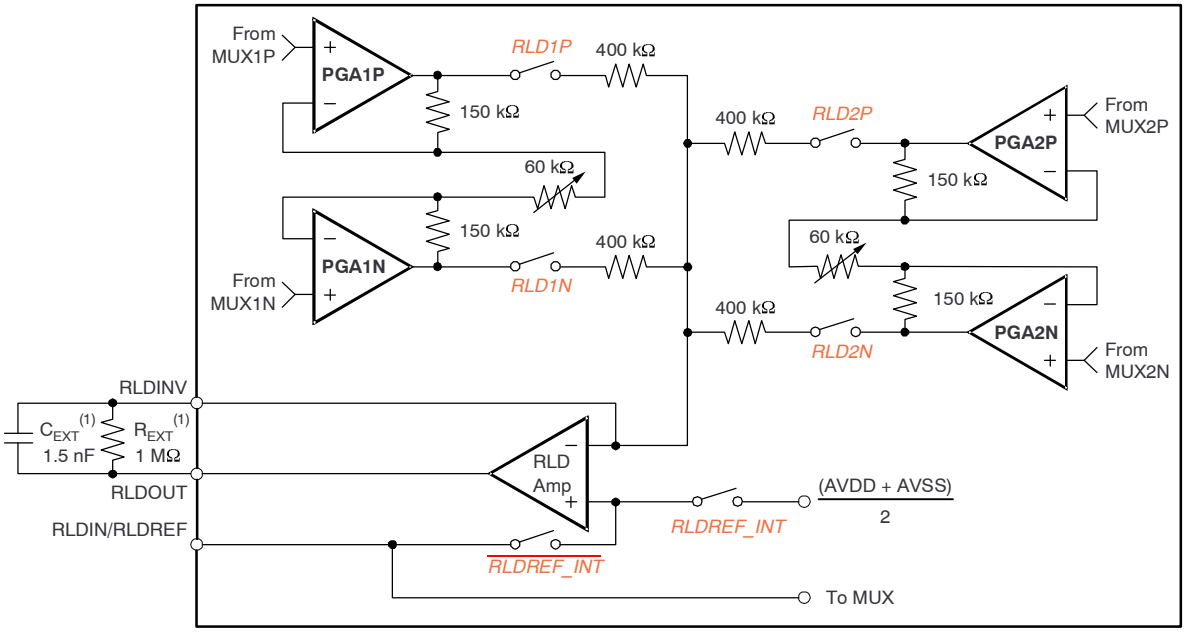
Right Leg Drive (RLD DC Bias Circuit)

The right leg drive (RLD) circuitry is used as a means to counter the common-mode interference in an ECG system as a result of power lines and other sources, including fluorescent lights. The RLD circuit senses the common-mode of a selected set of electrodes and creates a negative feedback loop by driving the body with an inverted common-mode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual user system based on the various poles in the loop. The ADS1191/2 integrates the muxes to select the channel and an operational amplifier. All the amplifier terminals are available at the pins, allowing the user to choose the components for the feedback loop. The circuit shown in Figure 47 shows the overall functional connectivity for the RLD bias circuit.



(1) Typical values.

Figure 47. RLD Channel Selection

The reference voltage for the right leg drive can be chosen to be internally generated (AVDD + AVSS)/2 or it can be provided externally with a resistive divider. The selection of an internal versus external reference voltage for the RLD loop is defined by writing the appropriate value to the RLDREF_INT bit in the MISC2 register.

If the RLD function is not used, the amplifier can be powered down using the PDB_RLD bit. This bit is also used in daisy-chain mode to power-down all but one of the RLD amplifiers.

The functionality of the RLDIN pin is explained in the *Input Multiplexer* section. An example procedure to use the RLD amplifier is shown in the *Right Leg Drive* subsection of the *Quick-Start Guide* section.

RLD Configuration with Multiple Devices

Figure 48 shows multiple devices connected to an RLD.

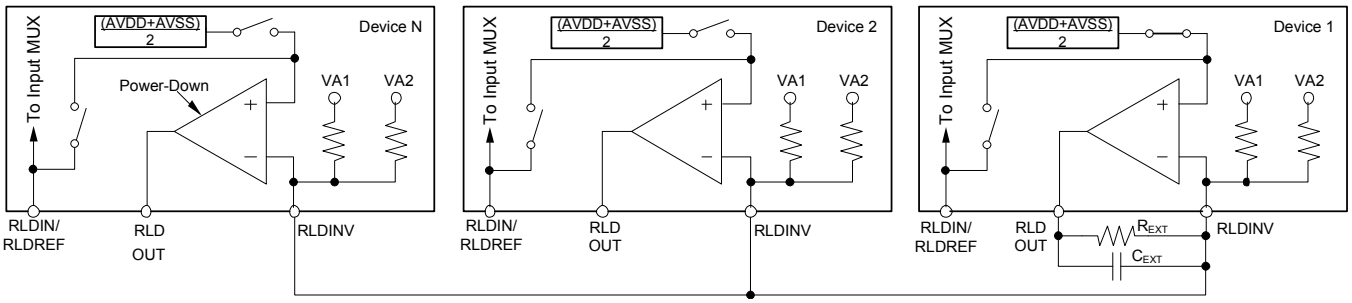


Figure 48. RLD Connection for Multiple Devices

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QUICK-START GUIDE

PCB LAYOUT

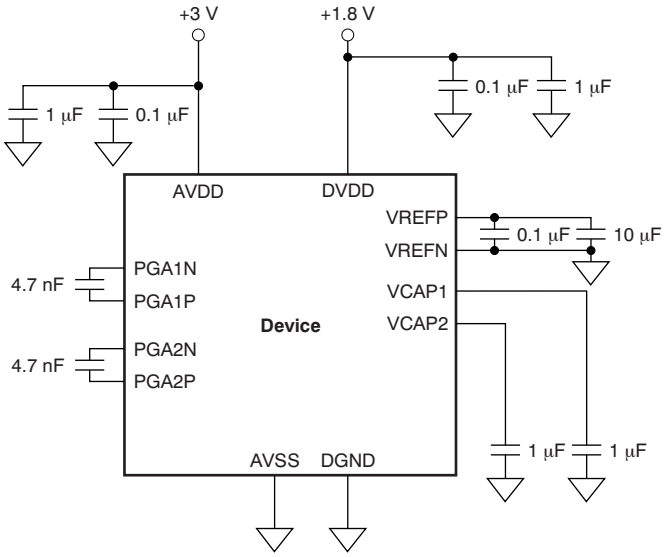
Power Supplies and Grounding

The ADS1191/2 have two supplies: AVDD and DVDD. AVDD should be as quiet as possible. AVDD provides the supply to the charge pump block and has transients at f_{CLK}. It is important to eliminate noise from AVDD that is non-synchronous with the ADS1191/2 operation. Each supply of the ADS1191/2 should be bypassed with 10-µF and a 0.1-µF solid ceramic capacitors. It is recommended that placement of the digital circuits (DSP, microcontrollers, FPGAs, etc.) in the system is done such that the return currents on those devices do not cross the analog return path of the ADS1191/2. The ADS1191/2 can be powered from unipolar or bipolar supplies.

The capacitors used for decoupling can be of the surface-mount, low-cost, low-profile multi-layer ceramic type. In most cases the VCAP1 capacitor can also be a multi-layer ceramic, but in systems where the board is subjected to high or low frequency vibration, it is recommend that a non-ferroelectric capacitor such as a tantalum or class 1 capacitor (for example, C0G or NPO) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, X8R, etc.) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using internal reference, noise on the VCAP1 node results in performance degradation.

Connecting the Device to Unipolar (+3 V/+1.8 V) Supplies

Figure 49 illustrates the ADS1191/2 connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to analog ground (AVSS) and the digital supply (DVDD) is referenced to digital ground (DGND).

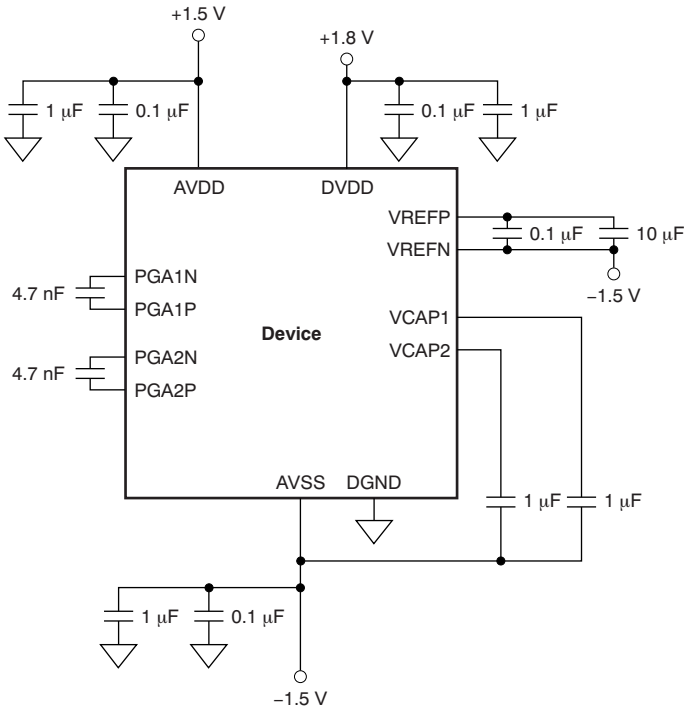


NOTE: Place the capacitors for supply, reference, VCAP1, and VCAP2 as close to the package as possible.

Figure 49. Single-Supply Operation

Connecting the Device to Bipolar (±1.5 V/1.8 V) Supplies

Figure 50 illustrates the ADS1191/2 connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



NOTE: Place the capacitors for supply, reference, VCAP1, and VCAP2 as close to the package as possible.

Figure 50. Bipolar Supply Operation

Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the ADS1191/2 if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

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POWER-UP SEQUENCING

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 51. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed, see the *CONFIG1: Configuration Register 1* subsection of the *Register Map* section for details. The power-up sequence timing is shown in Table 9.

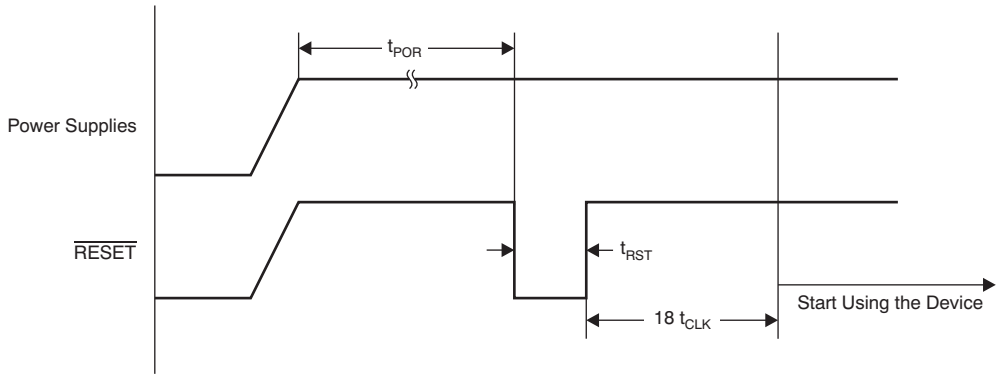

Figure 51. Power-Up Timing Diagram

Table 9. Power-Up Sequence Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{POR}	Wait after power-up until reset	2^{11}			t_{MOD}
t_{RST}	Reset low width	1			t_{MOD}

SETTING THE DEVICE FOR BASIC DATA CAPTURE

The following section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user's system. It is recommended that this procedure be followed initially to get familiar with the device settings. Once this procedure has been verified, the device can be configured as needed. For details on the timings for commands refer to the appropriate sections in the data sheet. Also, some sample programming codes are added for the ECG-specific functions.

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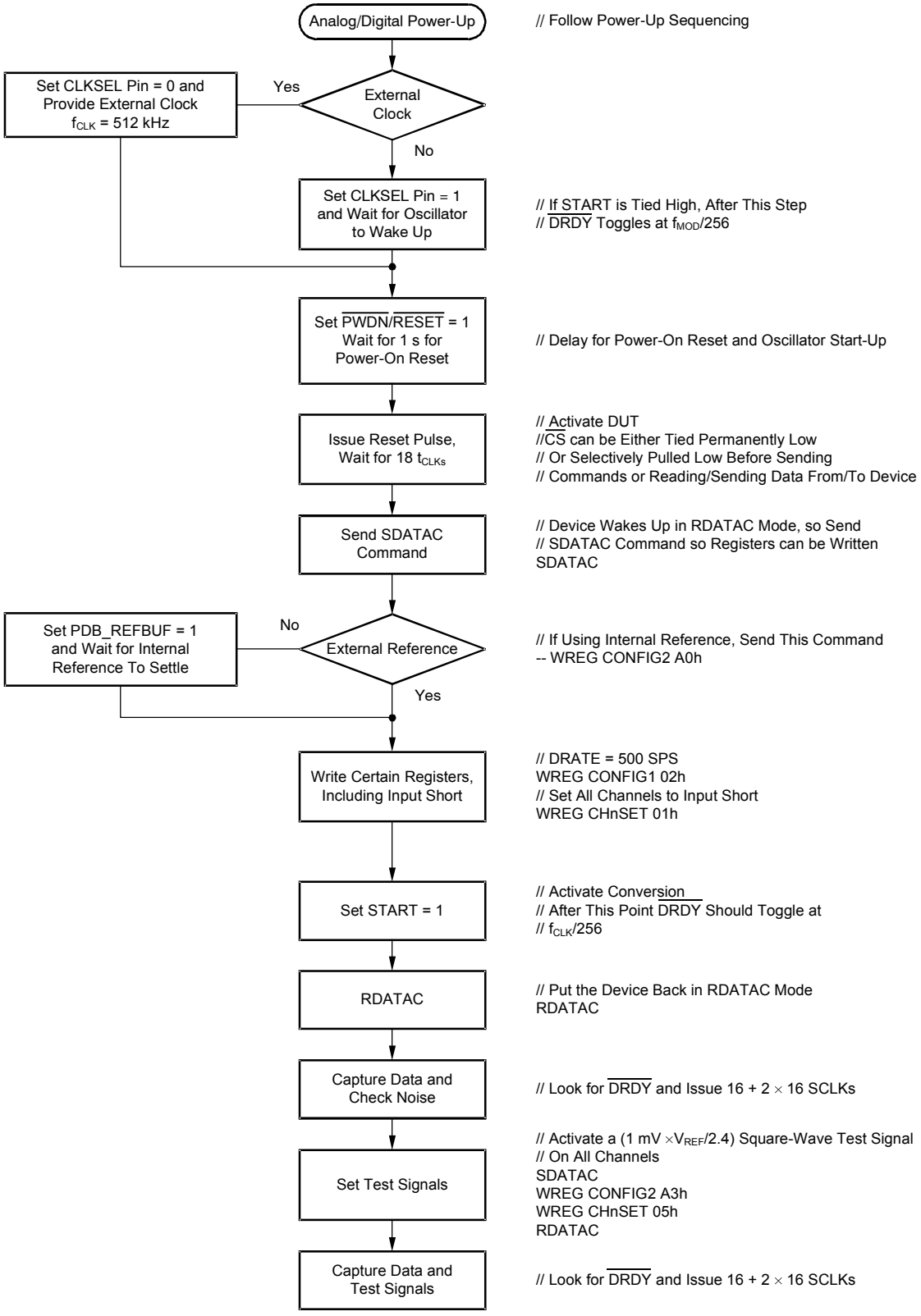

Figure 52. Initial Flow at Power-Up

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Lead-Off

Sample code to set dc lead-off with current source/sink resistors on all channels

WREG LOFF 10h // Comparator threshold at 95% and 5%, current source/sink resistor // DC lead-off

WREG CONFIG2 E0h // Turn-on dc lead-off comparators

WREG LOFF_SENS 0Fh // Turn on both P- and Nside of all channels for lead-off sensing

Observe the status bits of the output data stream to monitor lead-off status.

Right Leg Drive

Sample code to choose RLD as an average of the first three channels.

WREG RLD_SENSP 07h // Select channel 1—3 P-side for RLD sensing

WREG RLD_SENSN 07h // Select channel 1—3 N-side for RLD sensing

WREG CONFIG3 b'x1xx 1100 // Turn on RLD amplifier, set internal RLDREF voltage

Sample code to route the RLD_OUT signal through channel 4 N-side and measure RLD with channel 5. Make sure the external side to the chip RLDOUT is connected to RLDIN.

WREG CONFIG3 b'xxx1 1100 // Turn on RLD amplifier, set internal RLDREF voltage, set RLD measurement bit

WREG CH4SET b'1xxx 0111 // Route RLDIN to channel 4 N-side

WREG CH5SET b'1xxx 0010 // Route RLDIN to be measured at channel 5 w.r.t RLDREF

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2011) to Revision A	Page
• Added RSM data to Family and Ordering Information table	2
• Changed AVSS to DGND row in Absolute Maximum Ratings table	2
• Changed Channel Performance (AC performance), *SNR* typical specification in Electrical Characteristics table	3
• Changed Supply Current parameters in Electrical Characteristics table	5
• Changed *ADS1192/2R* to *ADS1192* in 3 V Power Dissipation, *Quiescent power dissipation* parameter of Electrical Characteristics table	6
• Added RSM pinout package	9
• Changed f_{CLK} to f_{MOD} in bit 6 description of LOFF_STAT: Lead-Off Status register	44

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS1191IPBS	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1191	Samples
ADS1191IPBSR	ACTIVE	TQFP	PBS	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1191	Samples
ADS1191IRSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1191	Samples
ADS1191IRSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1191	Samples
ADS1192IPBS	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1192	Samples
ADS1192IPBSR	ACTIVE	TQFP	PBS	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1192	Samples
ADS1192IRSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1192	Samples
ADS1192IRSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1192	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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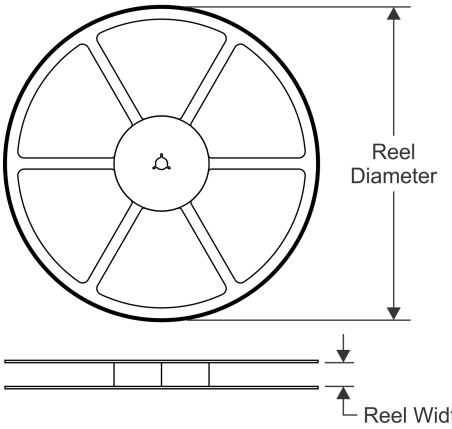
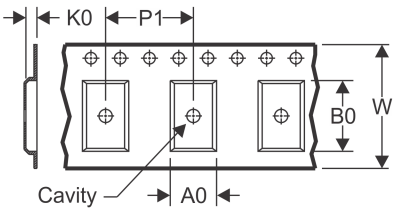
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

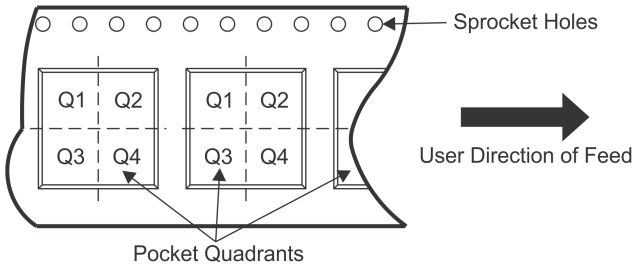


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

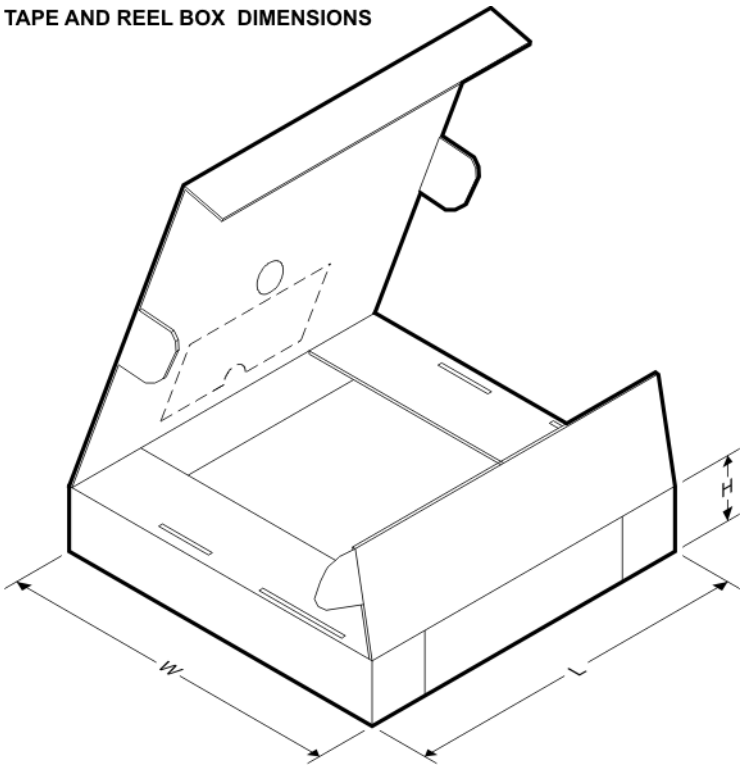
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1191IPBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS1191IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1191IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1192IPBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS1192IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1192IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1191IPBSR	TQFP	PBS	32	1000	350.0	350.0	43.0
ADS1191IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADS1191IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADS1192IPBSR	TQFP	PBS	32	1000	350.0	350.0	43.0
ADS1192IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADS1192IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

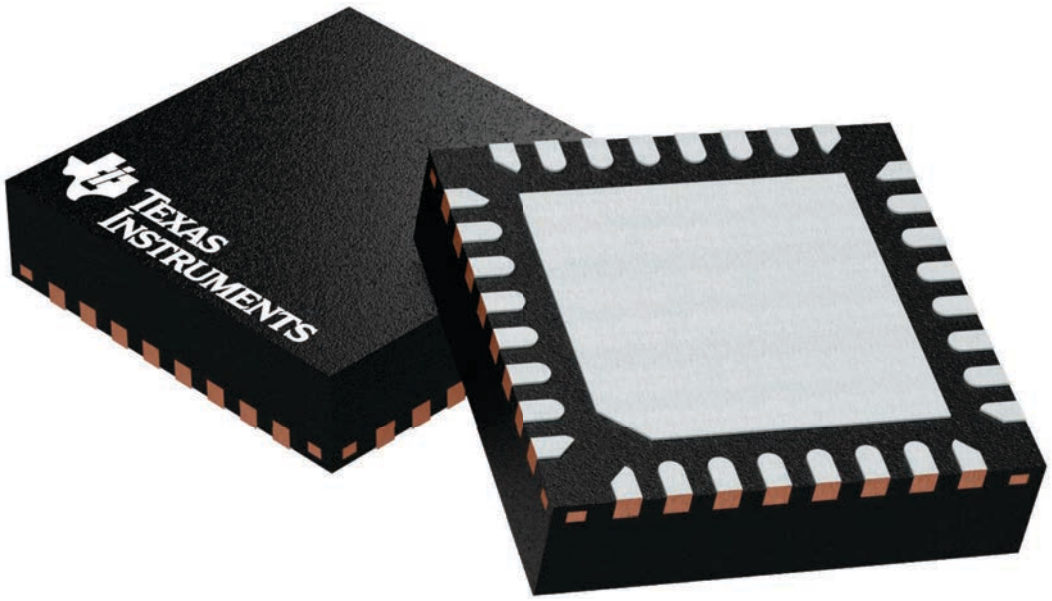
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



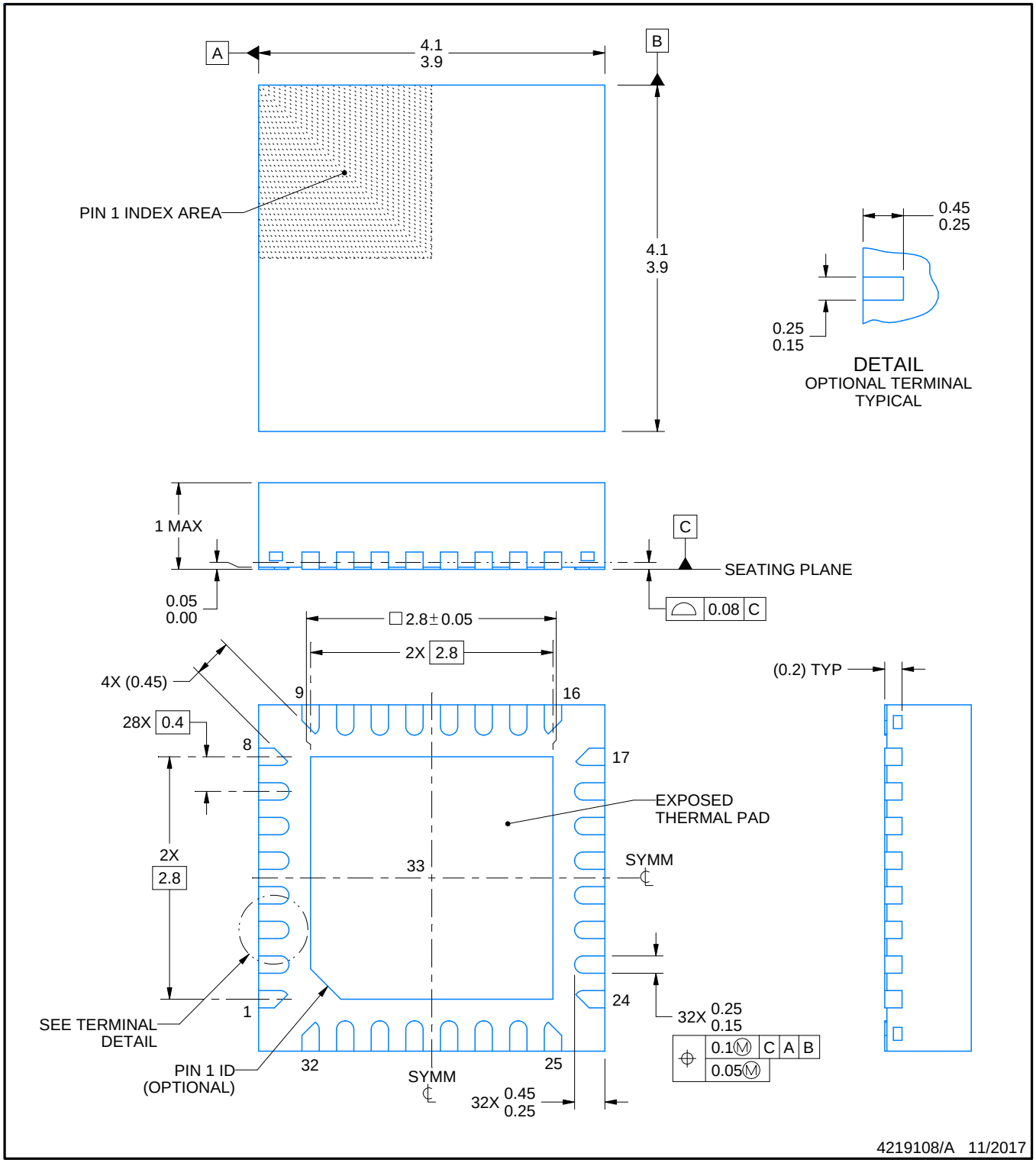
4224982/A

PACKAGE OUTLINE

RSM0032B

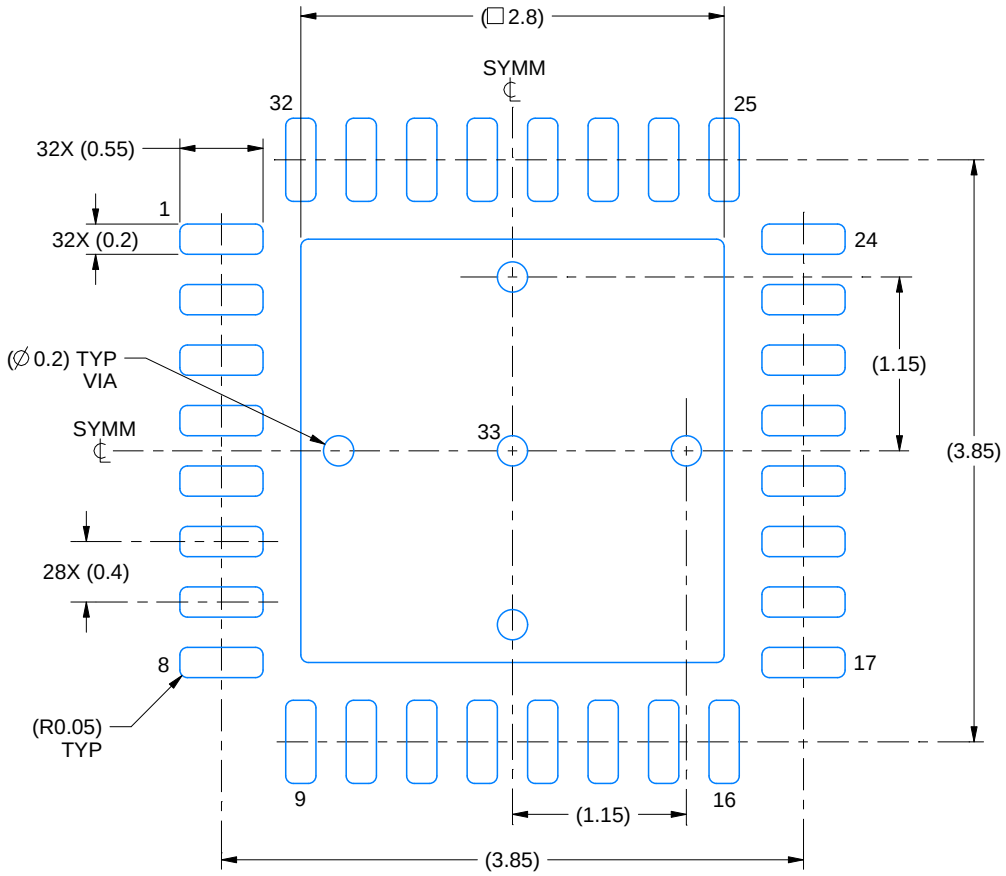
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

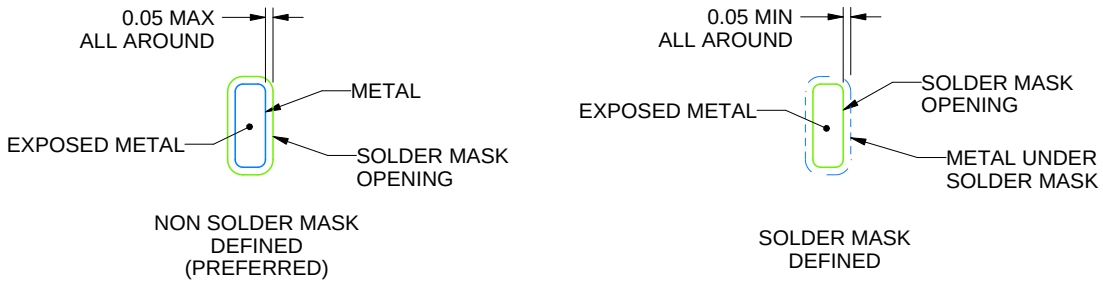


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

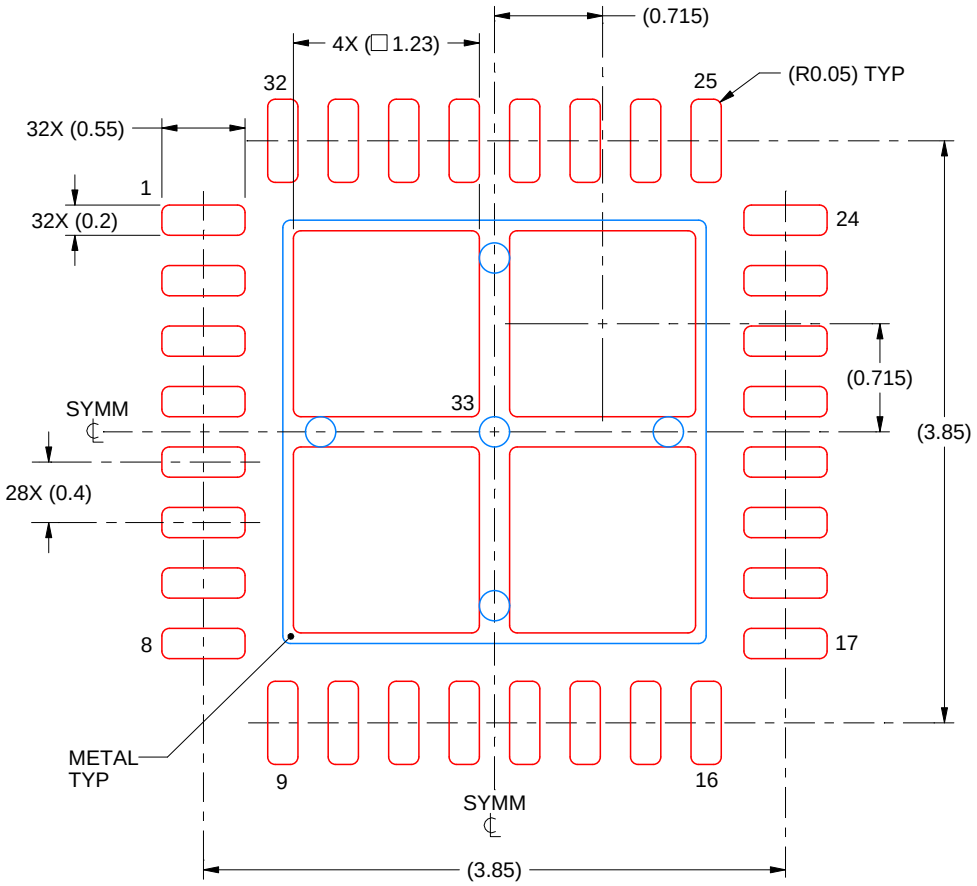


SOLDER MASK DETAILS

4219108/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

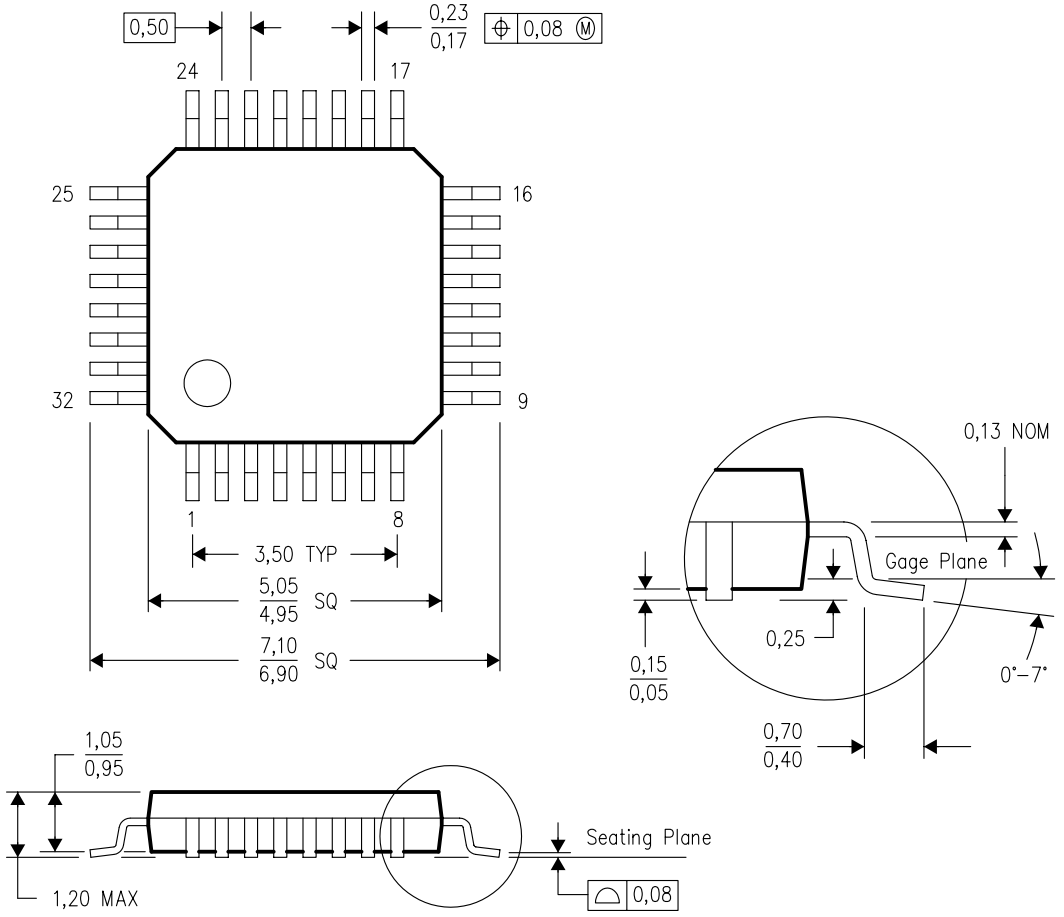
EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

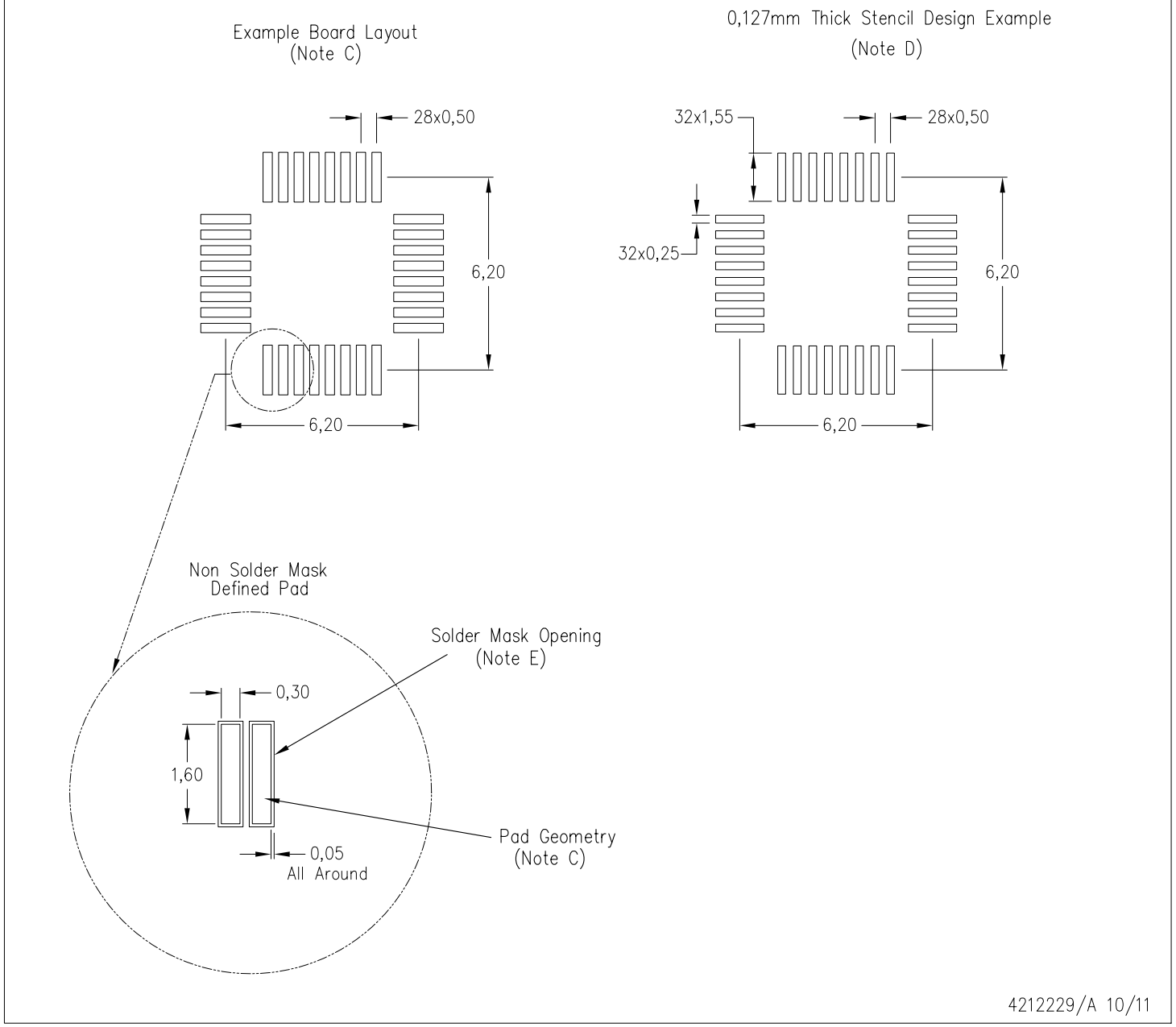
PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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