

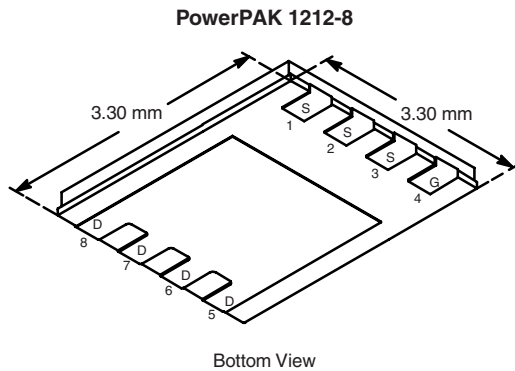


**THE DATASHEET OF
SI7402DN-T1-E3**



N-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
12	0.0057 at V _{GS} = 4.5 V	20
	0.0067 at V _{GS} = 2.5 V	18.8
	0.0085 at V _{GS} = 1.8 V	16.5



Ordering Information: Si7402DN-T1-E3 (Lead (Pb)-free)
Si7402DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

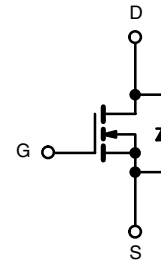
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- PA Switch, Load Switch and Battery Switch for Portable Devices
- Point-of-Load for 5 V or 3.3 V BUS Stepdown



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	12		V	
Gate-Source Voltage	V _{GS}	± 8			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	20	13	A
		T _A = 70 °C	16	10	
Pulsed Drain Current	I _{DM}	50			
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3	W	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8		1.5
		T _A = 70 °C	2.4		1.0
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	24	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.4	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

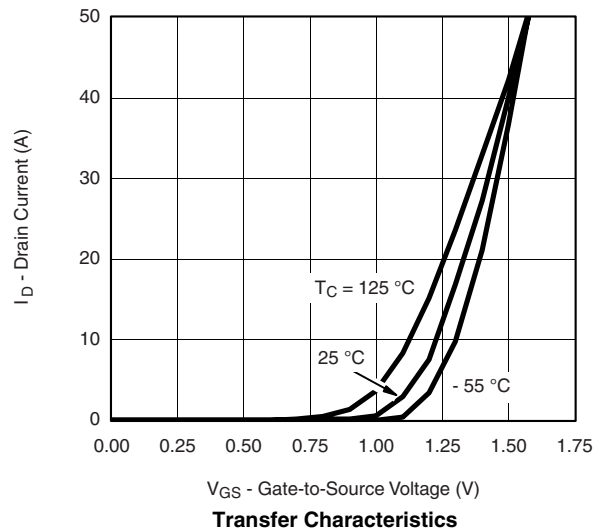
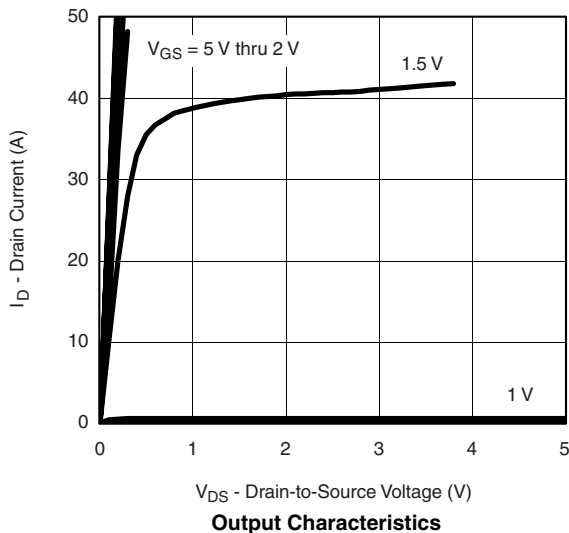
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.45		0.85	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0045	0.0057	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 18\text{ A}$		0.0053	0.0067	
		$V_{GS} = 1.8\text{ V}, I_D = 10\text{ A}$		0.0065	0.0085	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		100		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2\text{ A}, V_{GS} = 0\text{ V}$		0.70	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		36	55	nC
Gate-Source Charge	Q_{gs}		4			
Gate-Drain Charge	Q_{gd}		9.5			
Gate Resistance	R_g			1.8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 6\text{ }\Omega$		35	55	ns
Rise Time	t_r			65	100	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			60	90	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		40	80	

Notes:

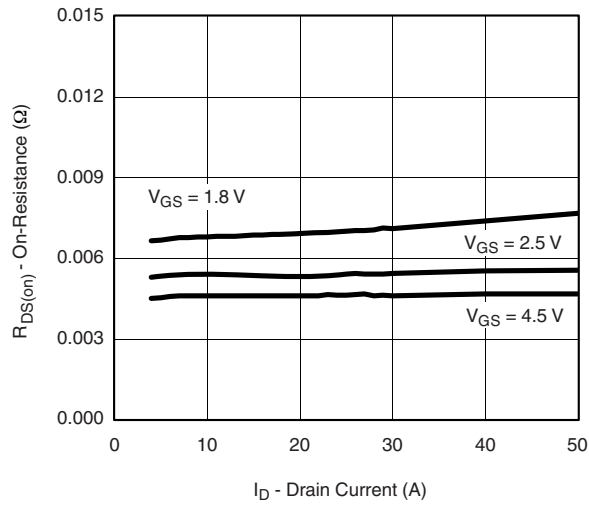
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

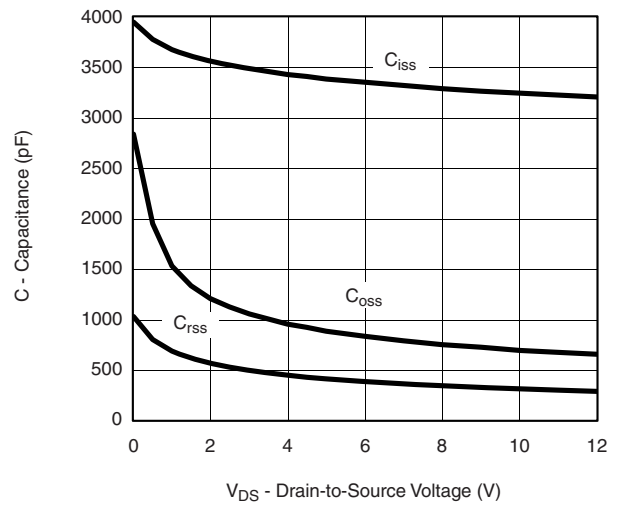
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



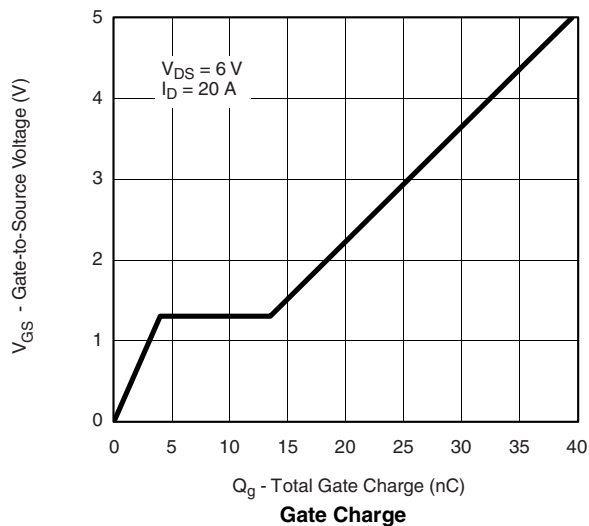
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



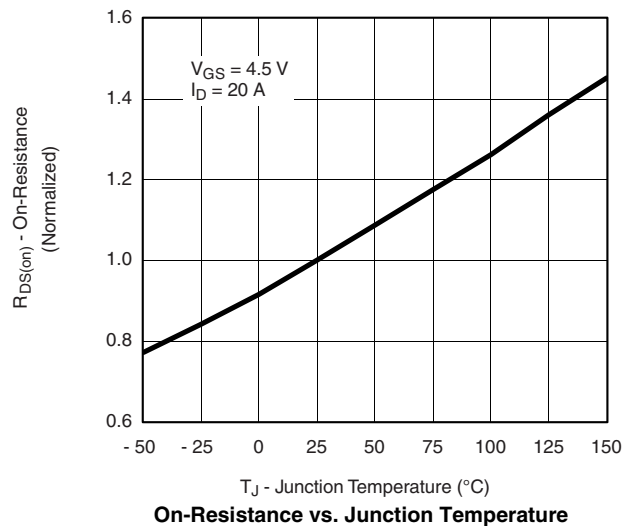
On-Resistance vs. Drain Current



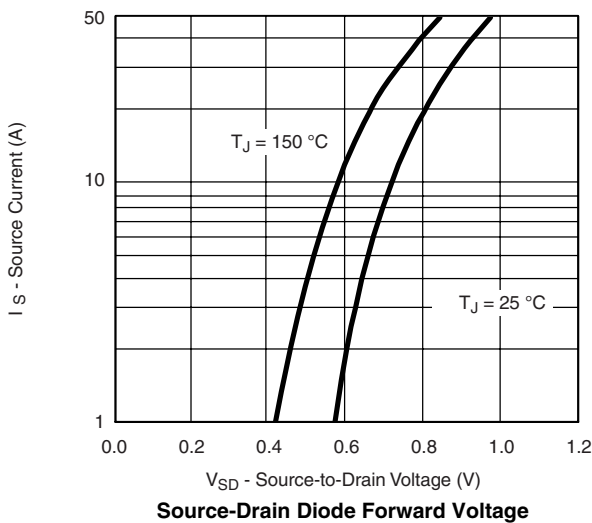
Capacitance



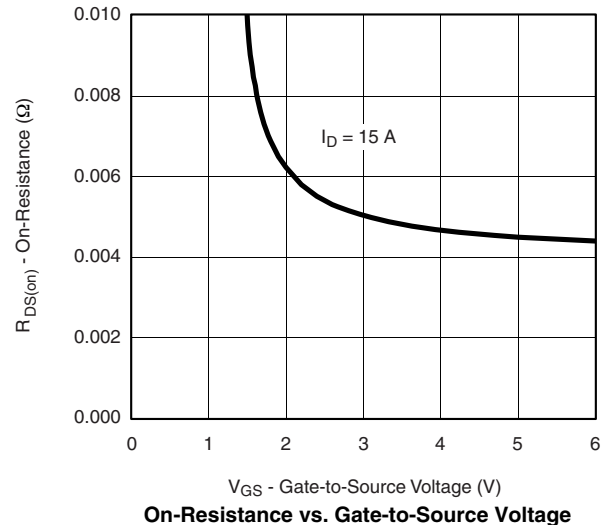
Gate Charge



On-Resistance vs. Junction Temperature

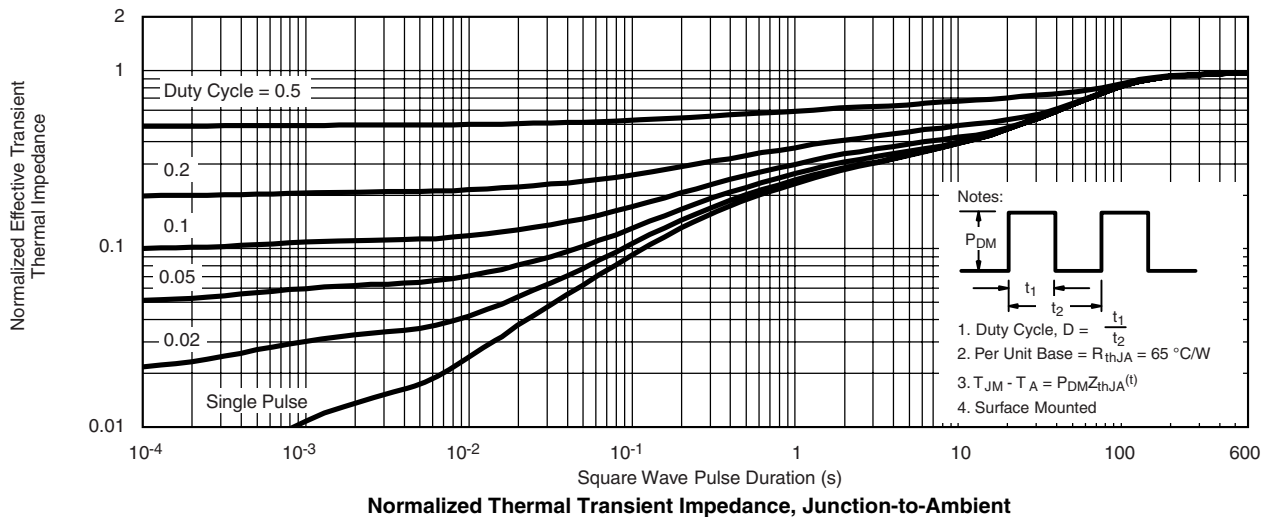
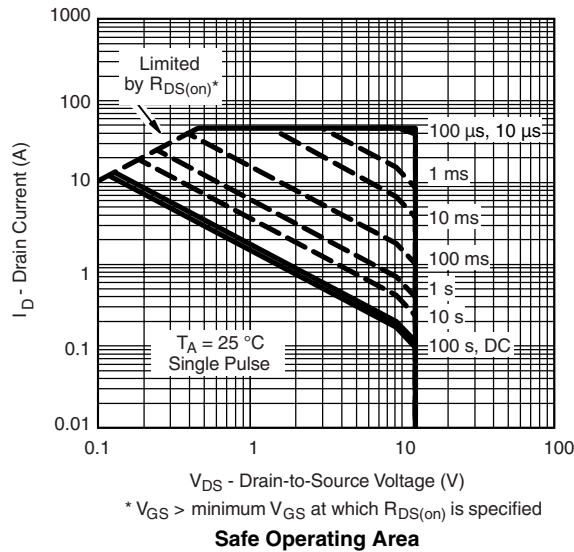
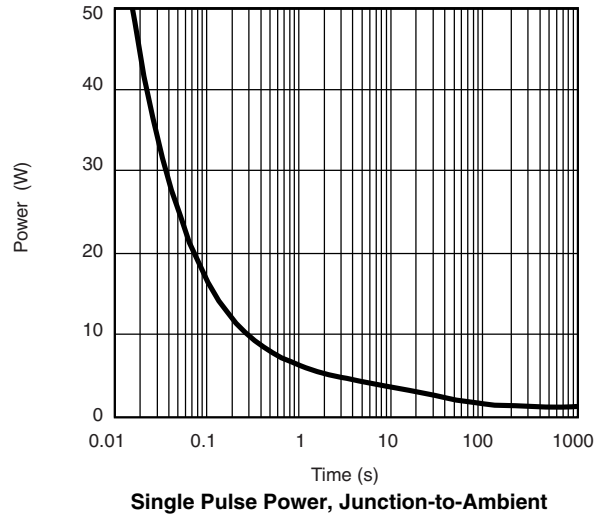
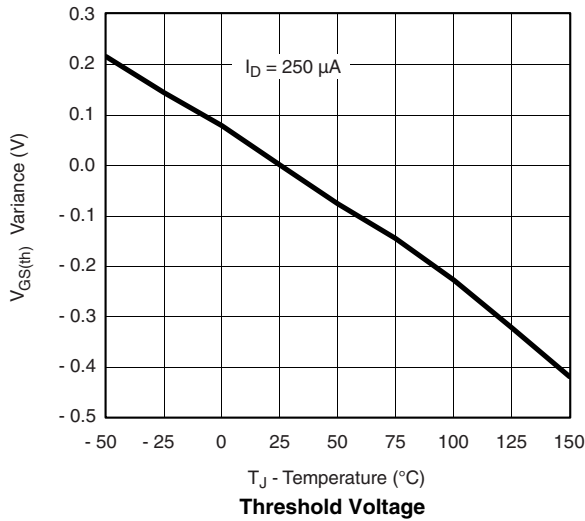


Source-Drain Diode Forward Voltage

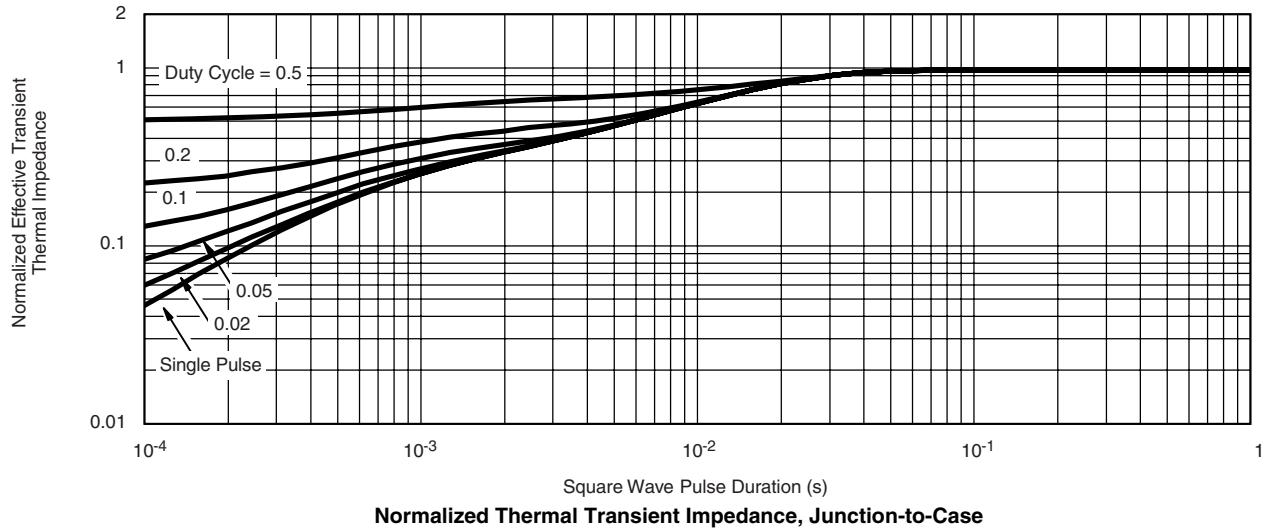


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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