



**THE DATASHEET OF  
IRF8721GTRPBF**



# IRF8721GPbF

HEXFET® Power MOSFET

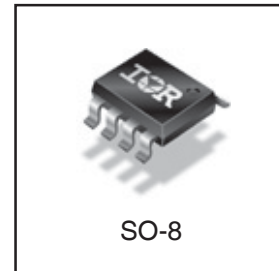
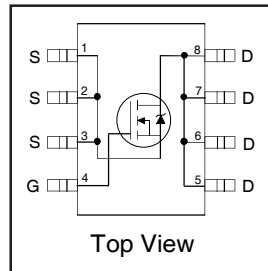
## Applications

- Control MOSFET of Sync-Buck Converters used for Notebook Processor Power
- Control MOSFET for Isolated DC-DC Converters in Networking Systems

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>Qg</b>
<b>30V</b>	<b>8.5mΩ @ V<sub>GS</sub> = 10V</b>	<b>8.3nC</b>

## Benefits

- Very Low Gate Charge
- Low R<sub>DS(on)</sub> at 4.5V V<sub>GS</sub>
- Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- 20V V<sub>GS</sub> Max. Gate Rating
- Lead-Free
- Halogen-Free



## Description

The IRF8721GPbF incorporates the latest HEXFET Power MOSFET Silicon Technology into the industry standard SO-8 package. The IRF8721GPbF has been optimized for parameters that are critical in synchronous buck operation including R<sub>ds(on)</sub> and gate charge to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors for Notebook and Netcom applications.

## Absolute Maximum Ratings

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	14	A
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	11	
I <sub>DM</sub>	Pulsed Drain Current ①	110	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Power Dissipation	2.5	W
P <sub>D</sub> @ T <sub>A</sub> = 70°C	Power Dissipation	1.6	
	Linear Derating Factor	0.02	W/°C
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJL</sub>	Junction-to-Drain Lead ⑤	—	20	°C/W
R <sub>θJA</sub>	Junction-to-Ambient ⑥	—	50	

Notes ① through ⑥ are on page 9

# IRF8721GPbF

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IR Rectifier

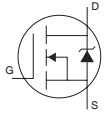
## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

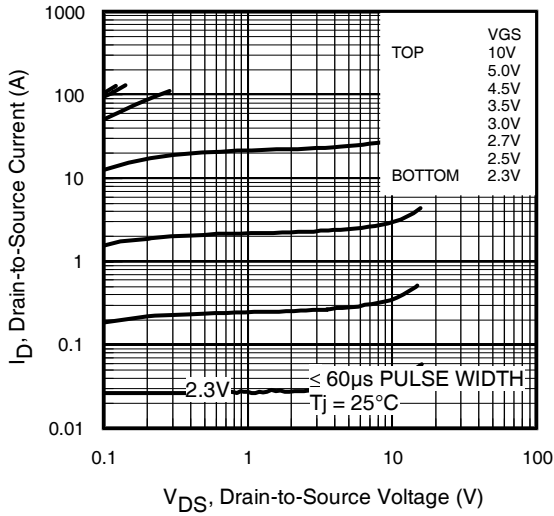
	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.021	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.9	8.5	$\text{m}\Omega$	$V_{GS} = 10V, I_D = 14A$ ③
		—	10.6	12.5		$V_{GS} = 4.5V, I_D = 11A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	—	2.35	V	$V_{DS} = V_{GS}, I_D = 25\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-6.2	—	$\text{mV}/^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu A$	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	27	—	—	S	$V_{DS} = 15V, I_D = 11A$
$Q_g$	Total Gate Charge	—	8.3	12	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 11A$ See Fig. 16a and 16b
$Q_{gs1}$	Pre-V <sub>th</sub> Gate-to-Source Charge	—	2.0	—		
$Q_{gs2}$	Post-V <sub>th</sub> Gate-to-Source Charge	—	1.0	—		
$Q_{gd}$	Gate-to-Drain Charge	—	3.2	—		
$Q_{godr}$	Gate Charge Overdrive	—	2.0	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	4.2	—		
$Q_{oss}$	Output Charge	—	5.0	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
$R_G$	Gate Resistance	—	1.8	3.0	$\Omega$	
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ $I_D = 11A$ $R_G = 1.8\Omega$ See Fig. 15a
$t_r$	Rise Time	—	11	—		
$t_{d(off)}$	Turn-Off Delay Time	—	8.1	—		
$t_f$	Fall Time	—	7.0	—		
$C_{iss}$	Input Capacitance	—	1040	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	229	—		
$C_{riss}$	Reverse Transfer Capacitance	—	114	—		

## Avalanche Characteristics

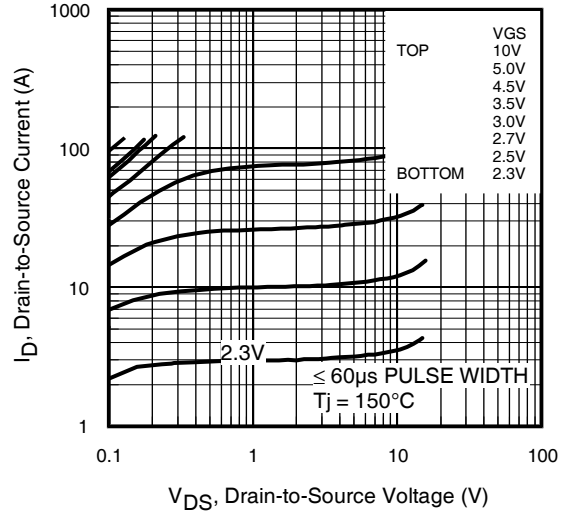
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	68	mJ
$I_{AR}$	Avalanche Current ①	—	11	A

## Diode Characteristics

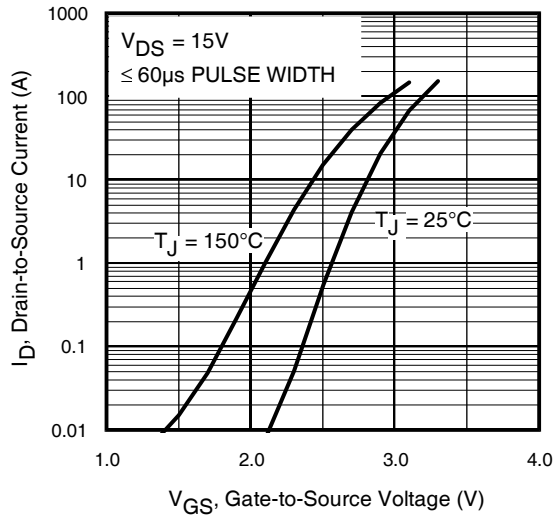
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	112		
$V_{SD}$	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 11A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	14	21	ns	$T_J = 25^\circ\text{C}, I_F = 11A, V_{DD} = 15V$
$Q_{rr}$	Reverse Recovery Charge	—	15	23	nC	$di/dt = 300A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



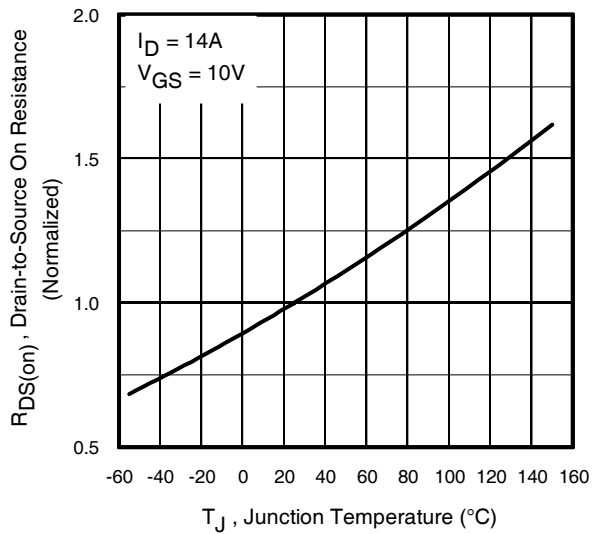
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

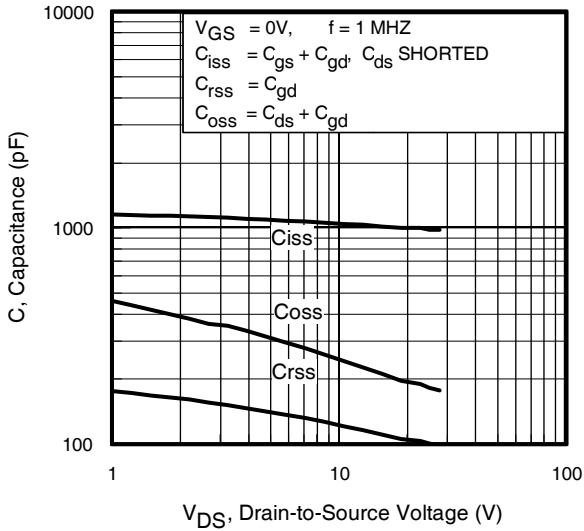


**Fig 3.** Typical Transfer Characteristics

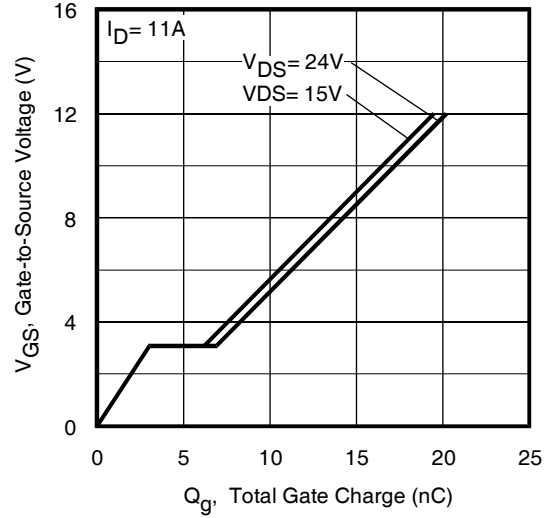


**Fig 4.** Normalized On-Resistance Vs. Temperature

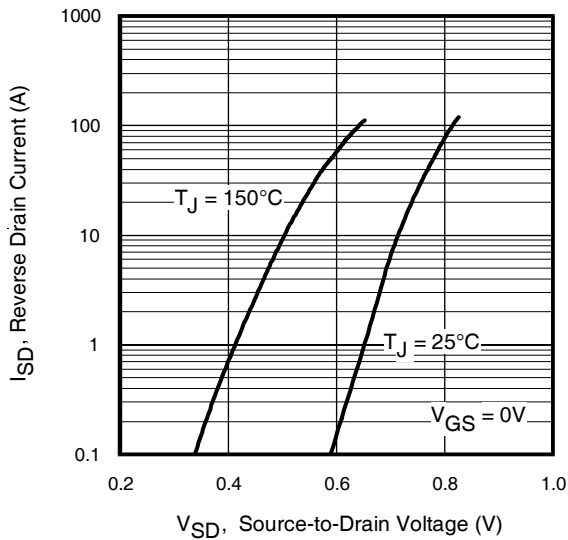
# IRF8721GPbF



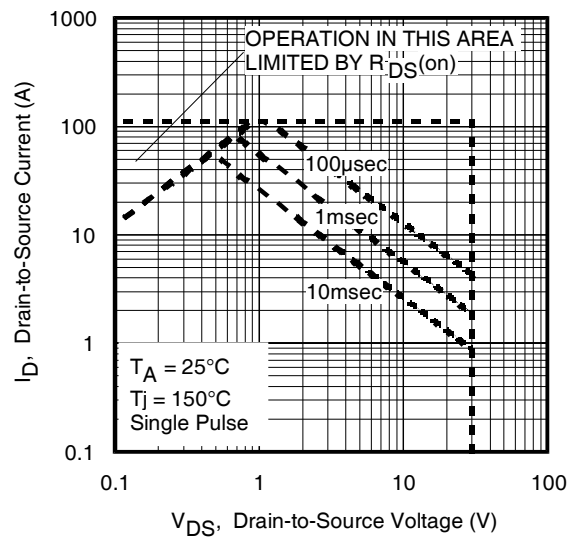
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



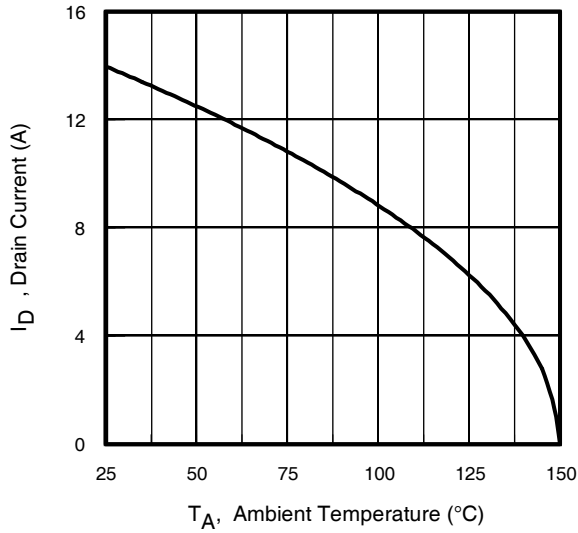
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



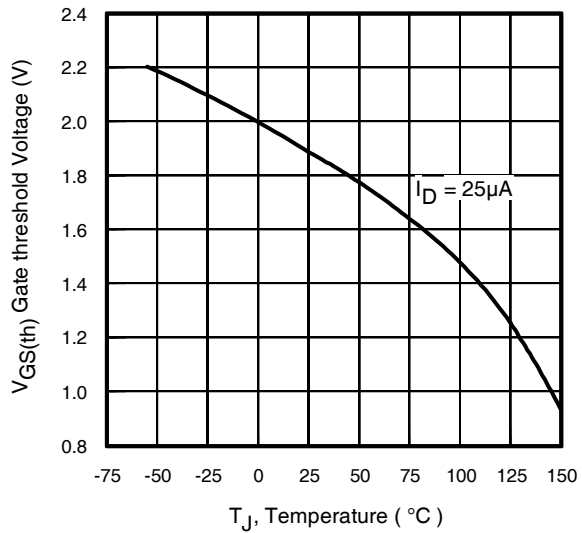
**Fig 7.** Typical Source-Drain Diode Forward Voltage



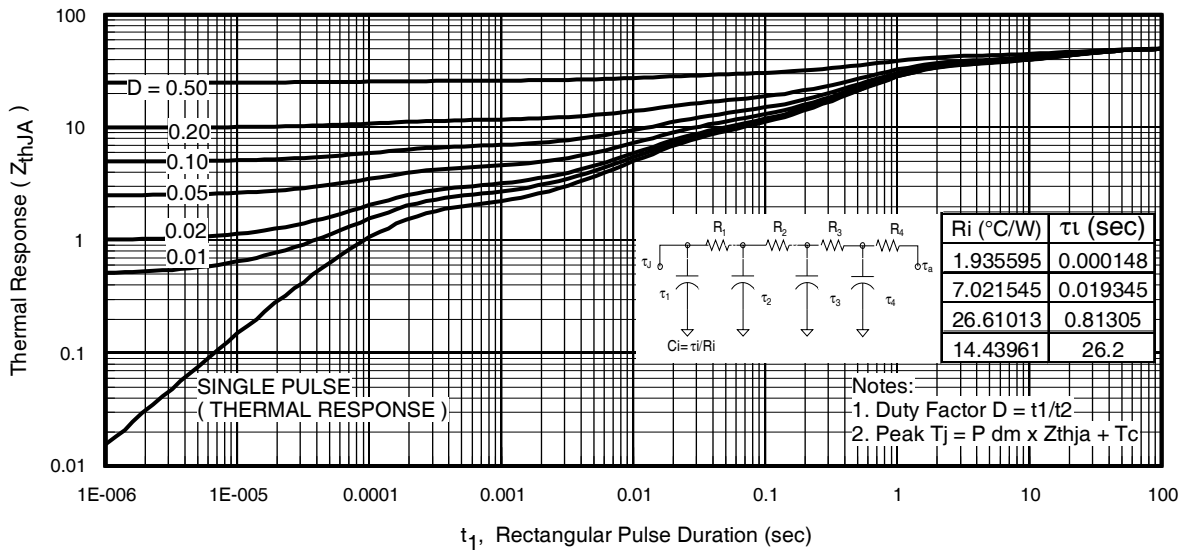
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature



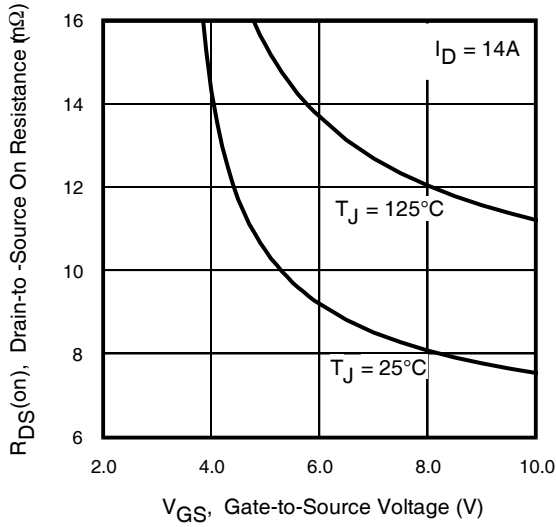
**Fig 10.** Threshold Voltage Vs. Temperature



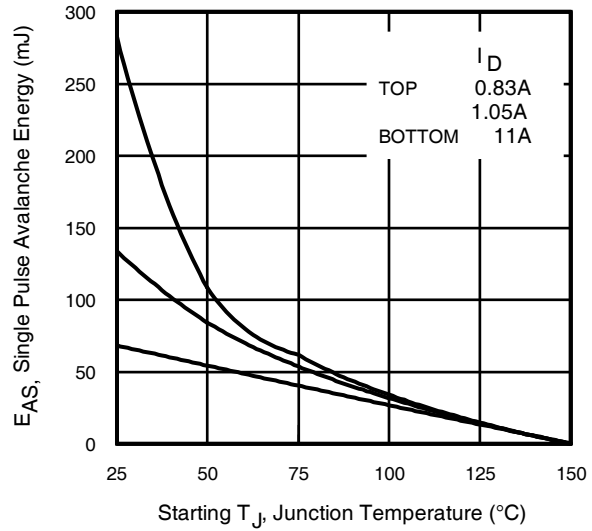
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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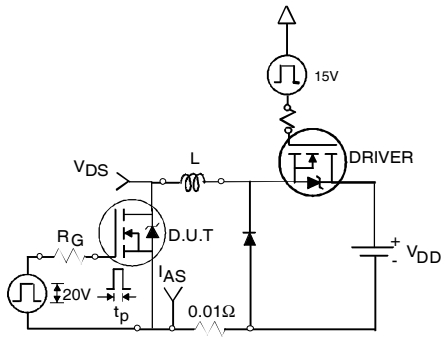
International  
**IR** Rectifier



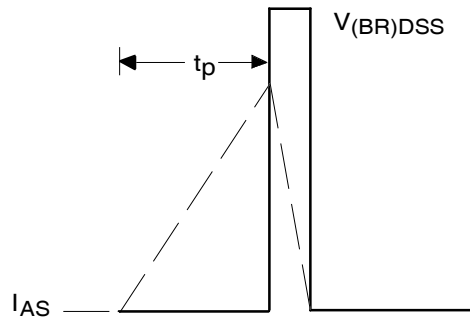
**Fig 12.** On-Resistance vs. Gate Voltage



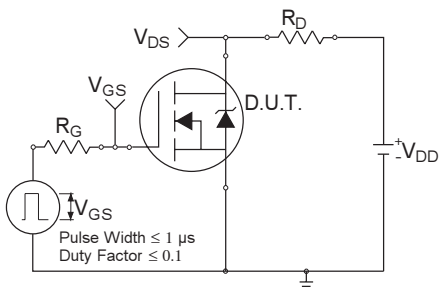
**Fig 13.** Maximum Avalanche Energy vs. Drain Current



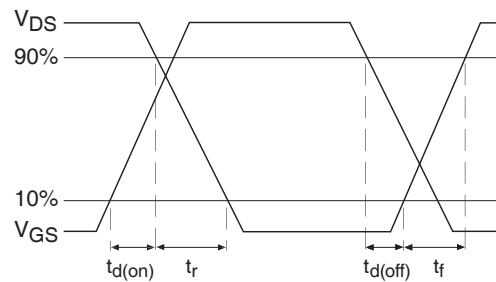
**Fig 14a.** Unclamped Inductive Test Circuit



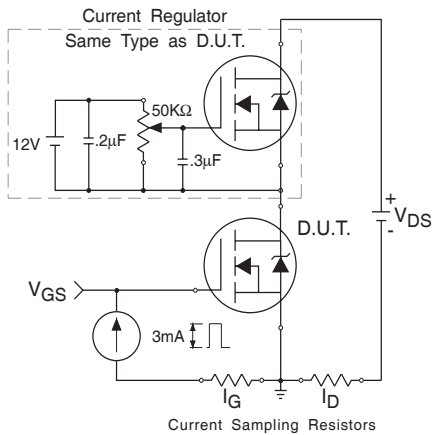
**Fig 14b.** Unclamped Inductive Waveforms



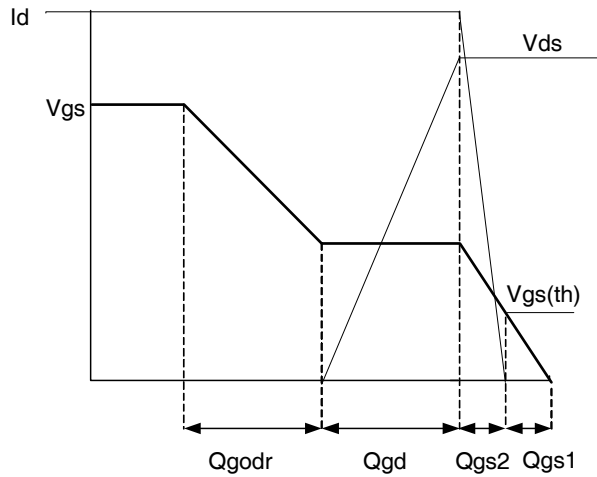
**Fig 15a.** Switching Time Test Circuit



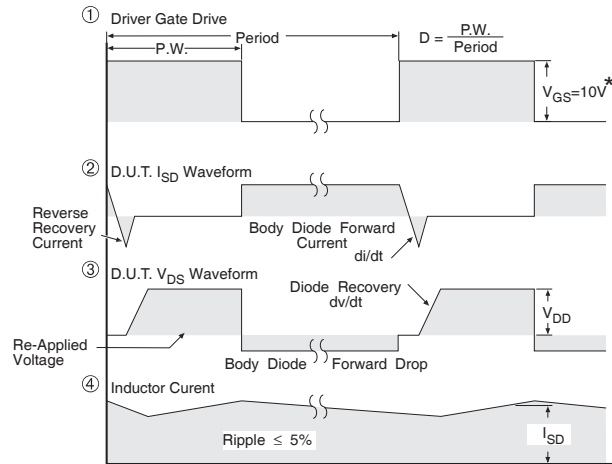
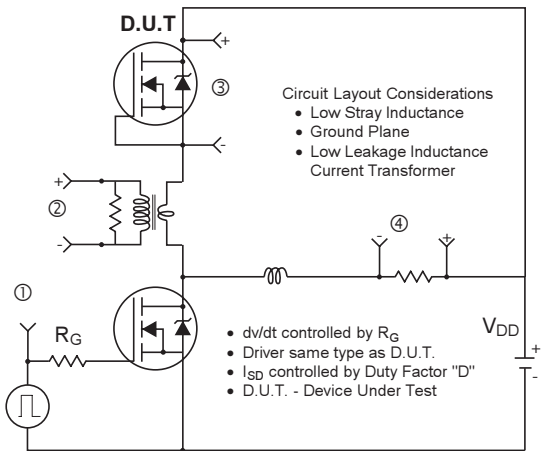
**Fig 15b.** Switching Time Waveforms



**Fig 16a.** Gate Charge Test Circuit



**Fig 16b.** Gate Charge Waveform



\*  $V_{GS} = 5V$  for Logic Level Devices

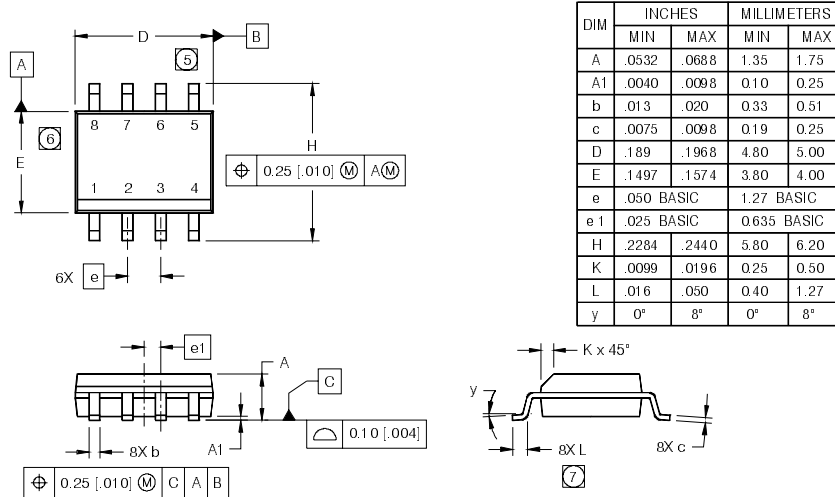
**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

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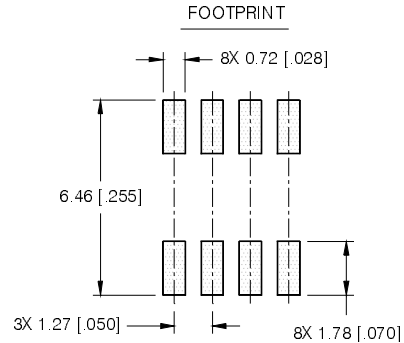
## SO-8 Package Outline (MOSFET & Fetky)

Dimensions are shown in millimeters (inches)



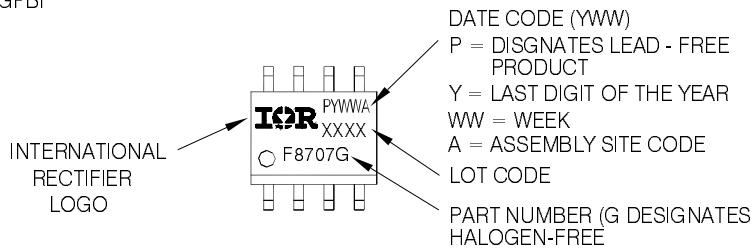
**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



## SO-8 Part Marking Information

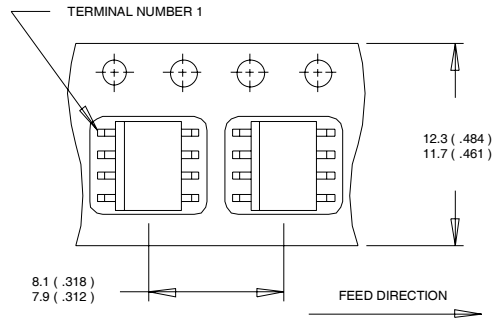
EXAMPLE: THIS IS AN IRF8707GPBF



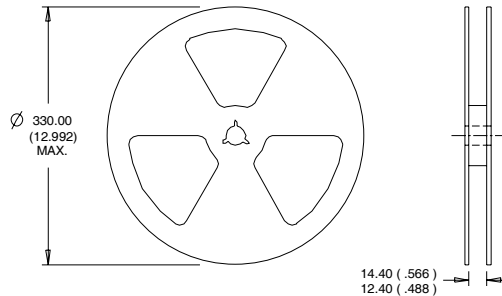
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
  2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.09\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 11\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ When mounted on 1 inch square copper board.
- ⑤  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice.

This product has been designed and qualified for the Consumer market.

Qualification Standards can be found on IR's Web site.

## Looking for pricing, stock, or lifecycle information?

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 [Infineon Technologies](#) Information

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