



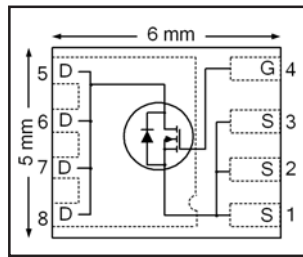
**THE DATASHEET OF  
IRFH7446TRPBF**



HEXFET® Power MOSFET

**Applications**

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters



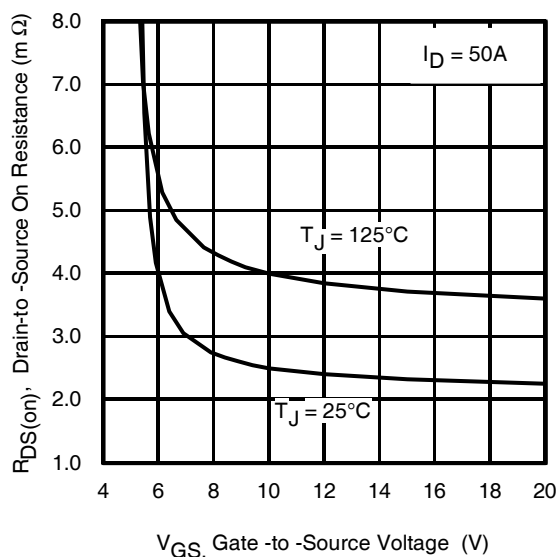
<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ. max.</b>	<b>2.5mΩ</b>
	<b>3.3mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>117A</b> Ⓢ
<b>I<sub>D</sub> (Package Limited)</b>	<b>85A</b>

**Benefits**

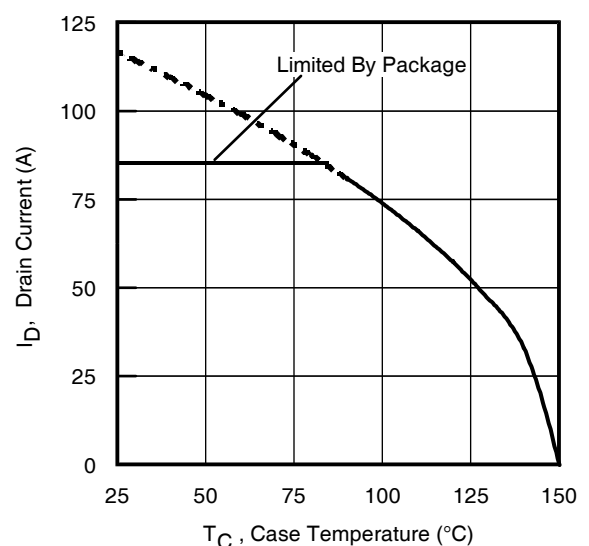
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- RoHS Compliant containing no Lead, no Bromide, and no Halogen



Base Part Number	Package Type	Standard Pack		Orderable part number	Note
		Form	Quantity		
IRFH7446PBF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7446TRPBF	
	PQFN 5mm x 6mm	Tape and Reel	400	IRFH7446TR2PBF	EOL notice #259



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	117 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	74 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	85	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	468	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	78	W
	Linear Derating Factor	0.63	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	78	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>④</sup>	152	
$I_{AR}$	Avalanche Current <sup>⑤</sup>	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>⑥</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case <sup>⑦</sup>	—	1.6	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case <sup>⑦</sup>	—	31	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑧</sup>	—	35	
$R_{\theta JA} (<10\text{s})$	Junction-to-Ambient <sup>⑧</sup>	—	23	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1.0\text{mA}$ <sup>⑨</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.5	3.3	m $\Omega$	$V_{GS} = 10\text{V}, I_D = 50\text{A}$ <sup>⑩</sup>
		—	3.8	—	m $\Omega$	$V_{GS} = 6.0\text{V}, I_D = 50\text{A}$ <sup>⑩</sup>
$V_{GS(th)}$	Gate Threshold Voltage	2.2	—	3.9	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Internal Gate Resistance	—	1.5	—	$\Omega$	

**Notes:**

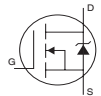
- ① Calculated continuous current based on maximum allowable junction temperature. Current is limited to 85A by source bond technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.062\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 50\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 50\text{A}$ ,  $di/dt \leq 1123\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1 inch square 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.
- ⑨  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑩ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 18\text{A}$ ,  $V_{GS} = 10\text{V}$

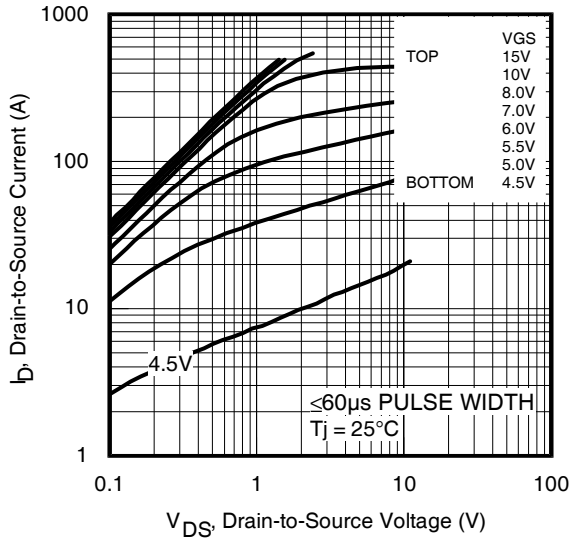
**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	159	—	—	S	$V_{DS} = 10\text{V}, I_D = 50\text{A}$
$Q_g$	Total Gate Charge	—	65	98	nC	$I_D = 50\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 10\text{V}$ ⑤
$Q_{gs}$	Gate-to-Source Charge	—	16	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	23	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	42	—		
$t_{d(on)}$	Turn-On Delay Time	—	11	—		
$t_r$	Rise Time	—	37	—		
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		
$t_f$	Fall Time	—	26	—		
$C_{iss}$	Input Capacitance	—	3174	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	479	—		
$C_{rss}$	Reverse Transfer Capacitance	—	332	—		
$C_{oss}$ eff. (ER)	Effective Output Capacitance (Energy Related)	—	637	—		
$C_{oss}$ eff. (TR)	Effective Output Capacitance (Time Related)	—	656	—		

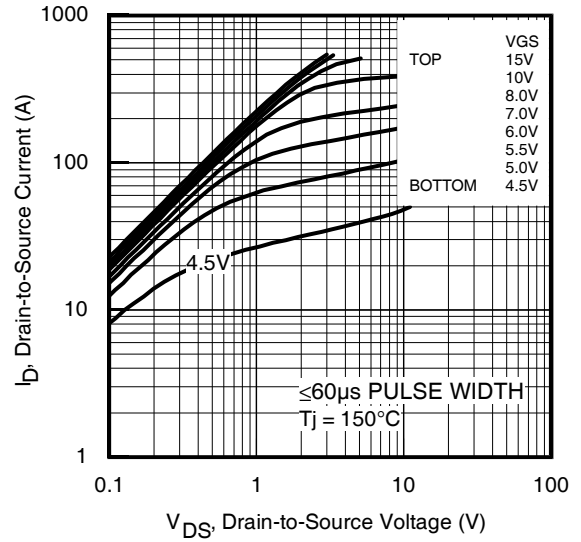
**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	85 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	468	A	
$V_{SD}$	Diode Forward Voltage	—	0.9	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50\text{A}, V_{GS} = 0\text{V}$ ③
dv/dt	Peak Diode Recovery ④	—	2.6	—	V/ns	$T_J = 150^\circ\text{C}, I_S = 50\text{A}, V_{DS} = 40\text{V}$
$t_{rr}$	Reverse Recovery Time	—	16	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 34\text{V},$ $T_J = 125^\circ\text{C}$ $I_F = 50\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	18	—		
$Q_{rr}$	Reverse Recovery Charge	—	5.0	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤ $T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	6.9	—		
$I_{RRM}$	Reverse Recovery Current	—	0.50	—	A	$T_J = 25^\circ\text{C}$

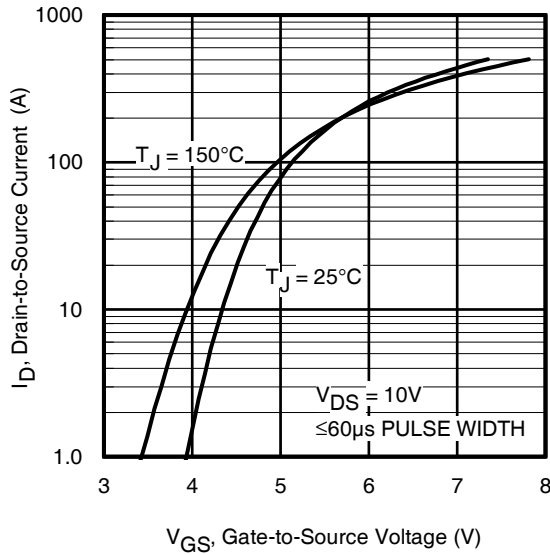




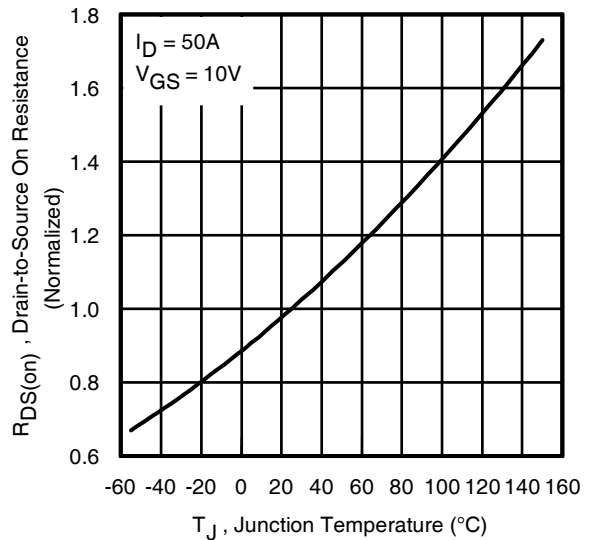
**Fig 3.** Typical Output Characteristics



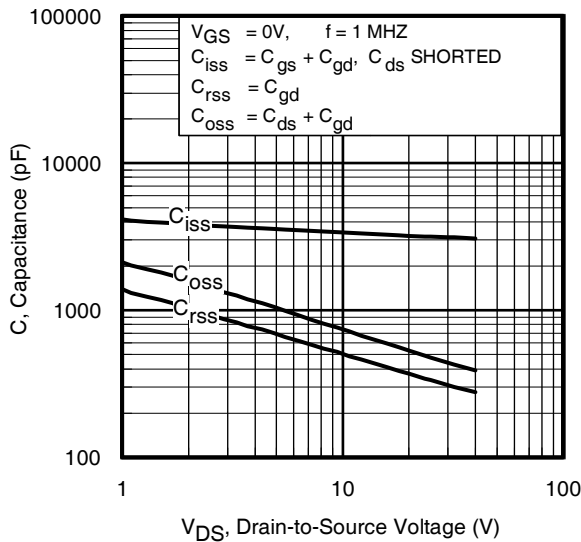
**Fig 4.** Typical Output Characteristics



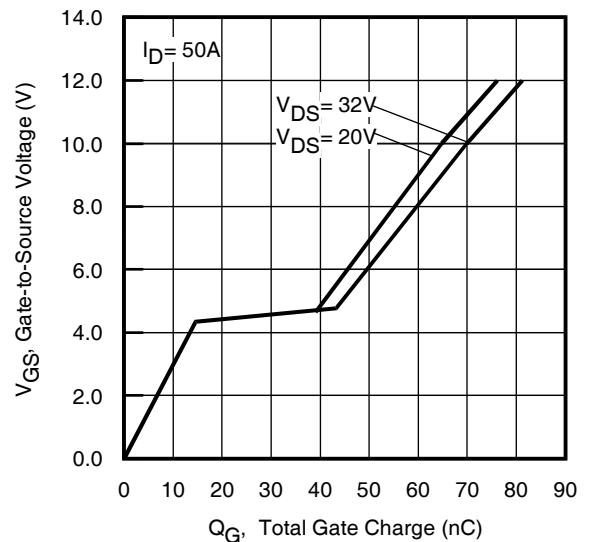
**Fig 5.** Typical Transfer Characteristics



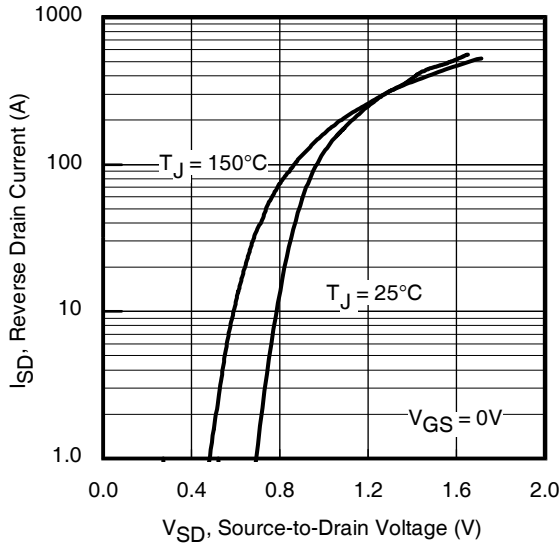
**Fig 6.** Normalized On-Resistance vs. Temperature



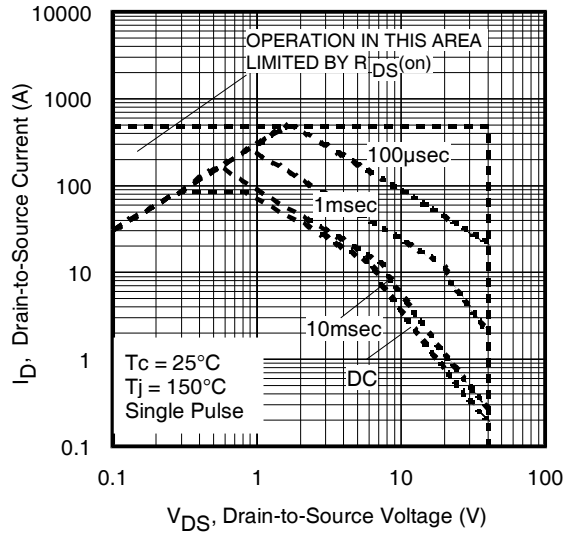
**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage



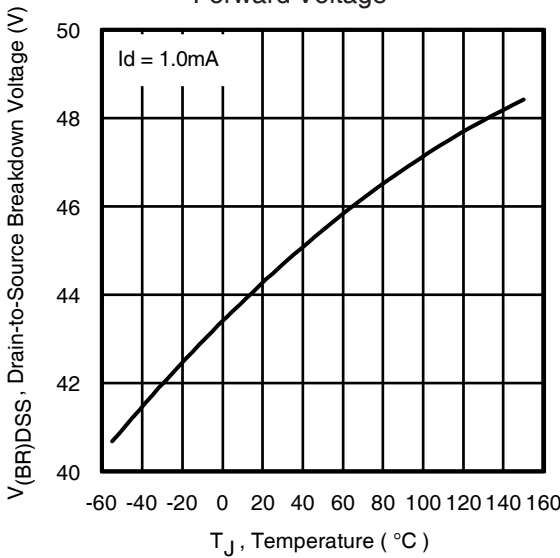
**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage



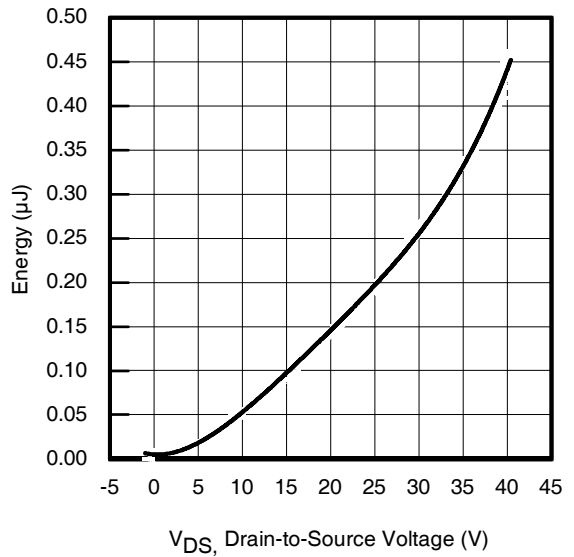
**Fig 9.** Typical Source-Drain Diode Forward Voltage



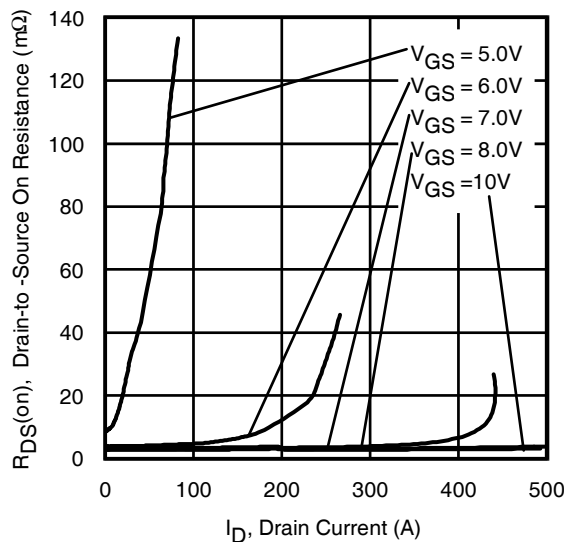
**Fig 10.** Maximum Safe Operating Area



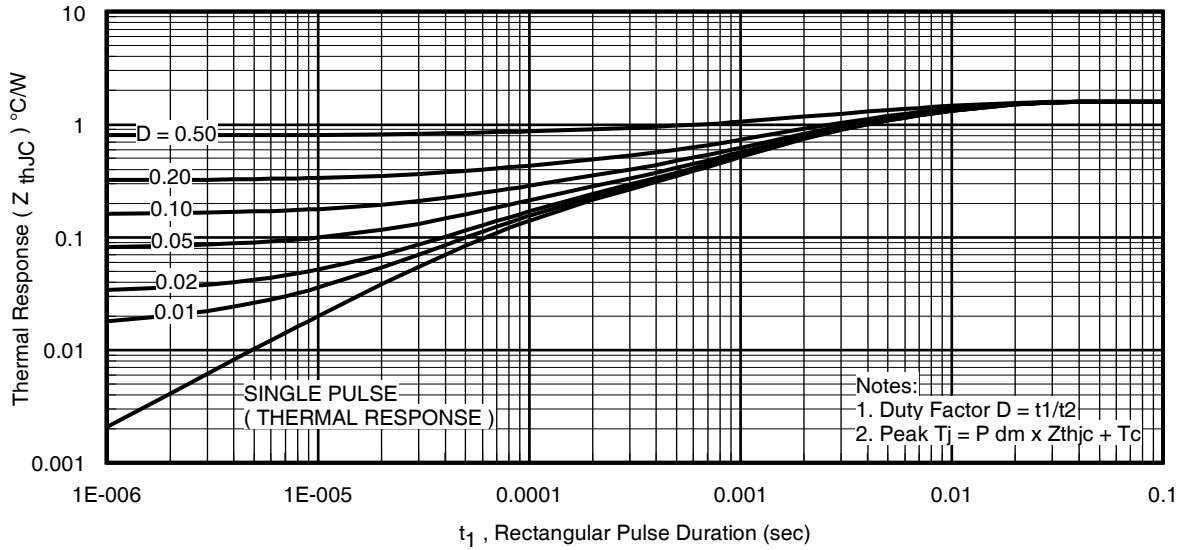
**Fig 11.** Drain-to-Source Breakdown Voltage



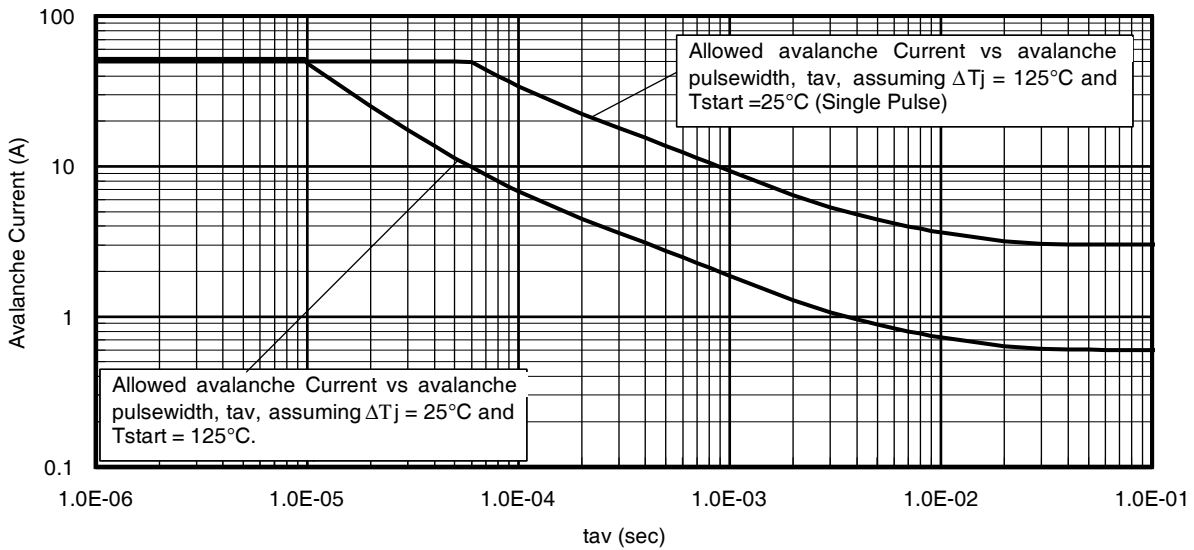
**Fig 12.** Typical  $C_{OSS}$  Stored Energy



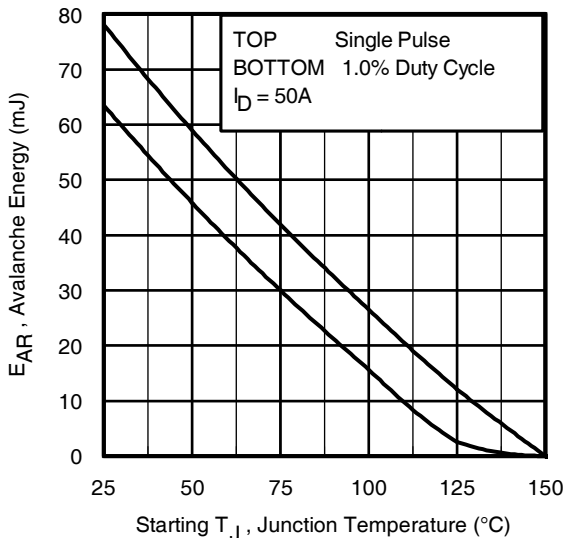
**Fig 13.** Typical On-Resistance vs. Drain Current



**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 15.** Typical Avalanche Current vs. Pulsewidth



**Fig 16.** Maximum Avalanche Energy vs. Temperature

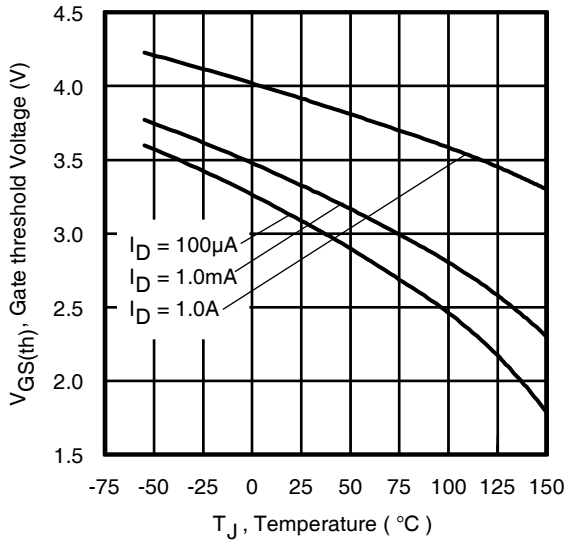
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
 (For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thjC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

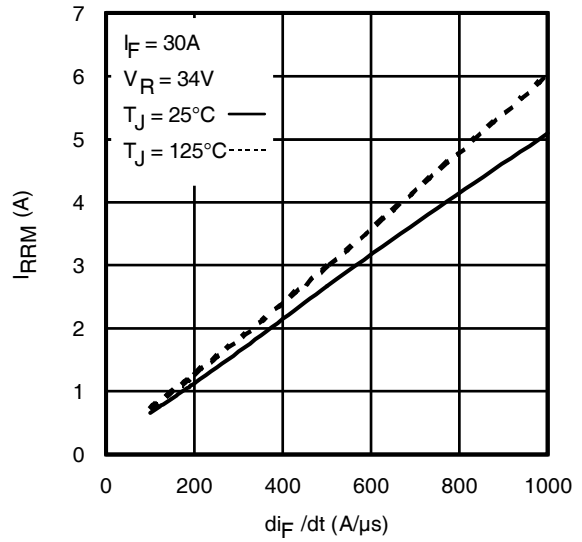
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thjC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thjC}]$$

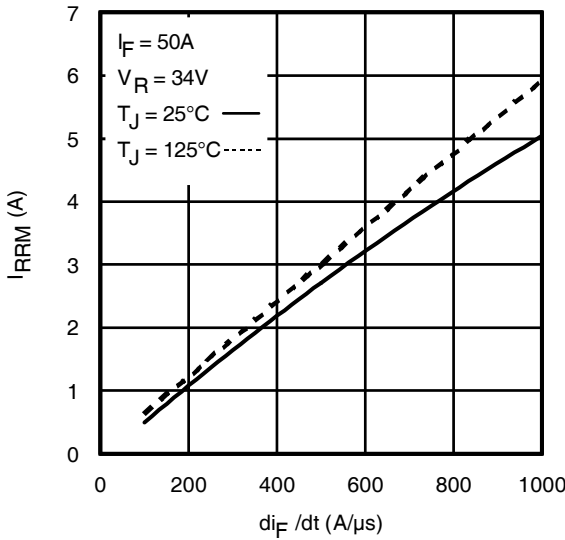
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



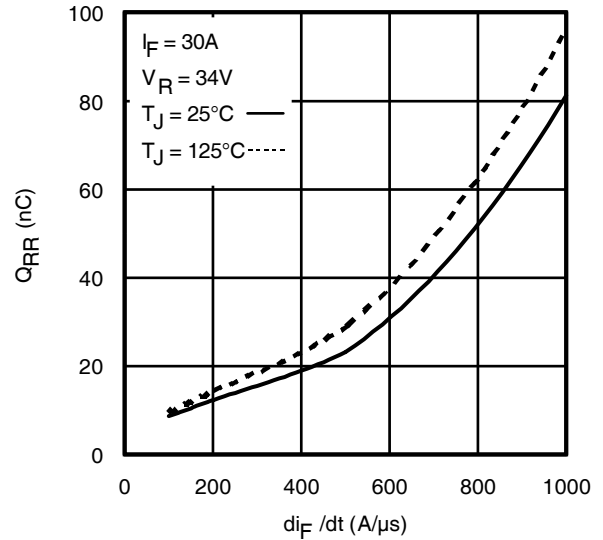
**Fig 17.** Threshold Voltage vs. Temperature



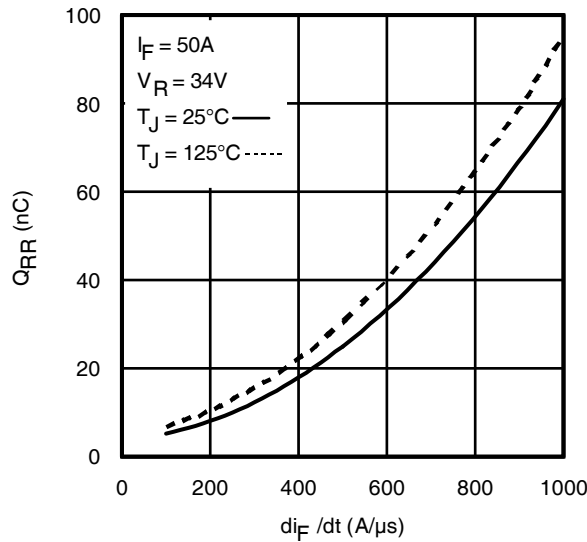
**Fig. 18 -** Typical Recovery Current vs.  $di_f/dt$



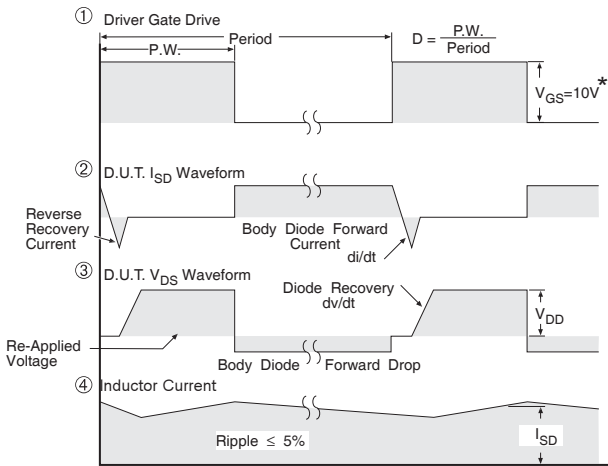
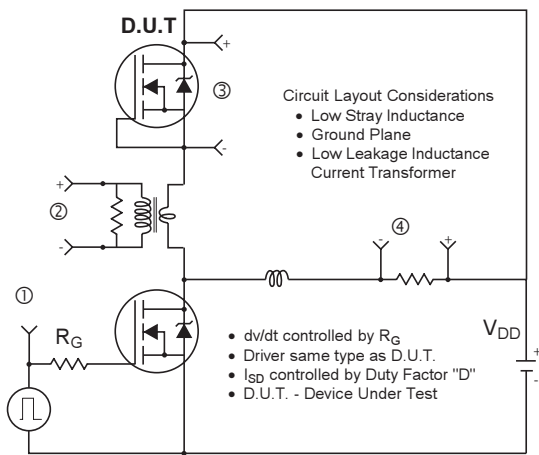
**Fig. 19 -** Typical Recovery Current vs.  $di_f/dt$



**Fig. 20 -** Typical Stored Charge vs.  $di_f/dt$

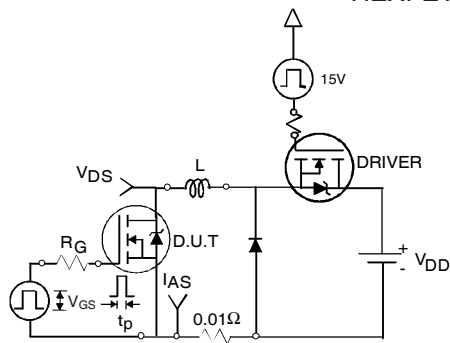


**Fig. 21 -** Typical Stored Charge vs.  $di_f/dt$

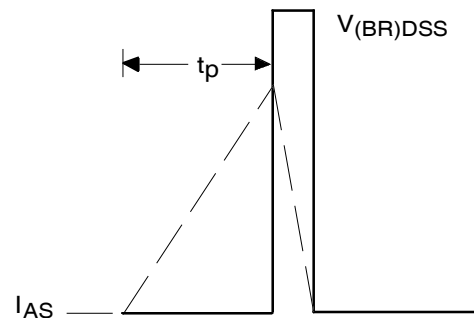


\*  $V_{GS} = 5V$  for Logic Level Devices

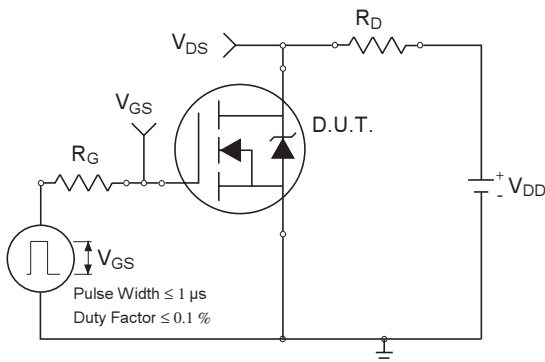
**Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



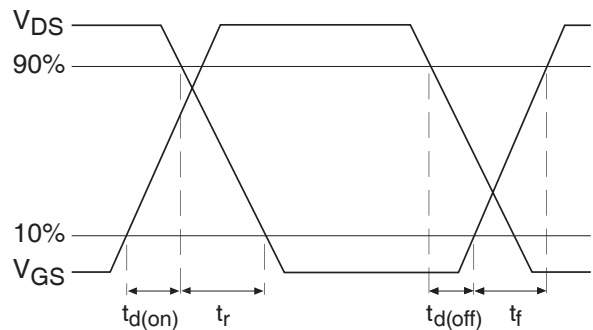
**Fig 22a. Unclamped Inductive Test Circuit**



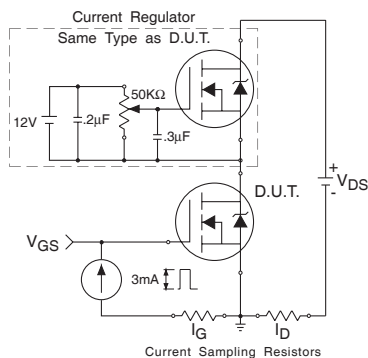
**Fig 22b. Unclamped Inductive Waveforms**



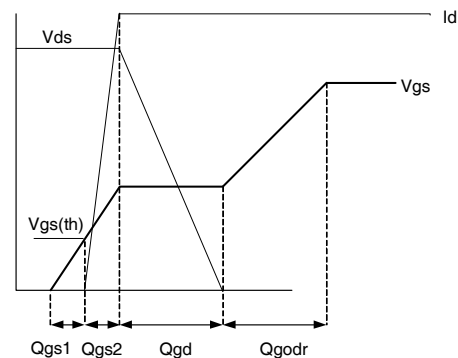
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**

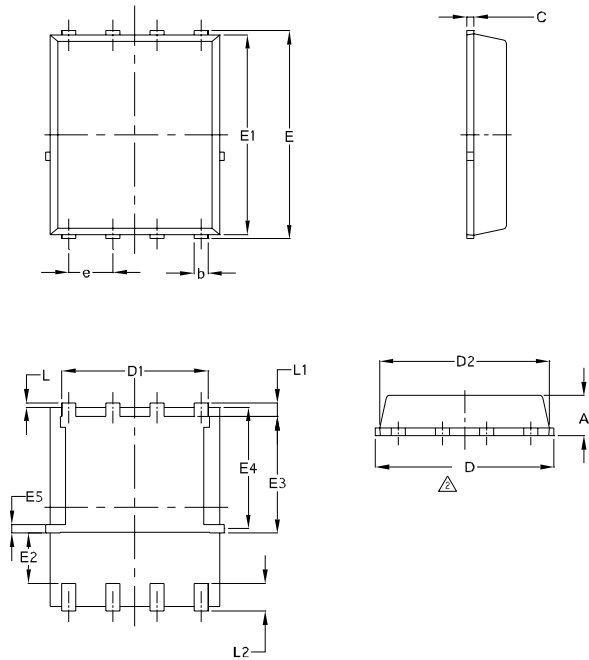


**Fig 24a. Gate Charge Test Circuit**



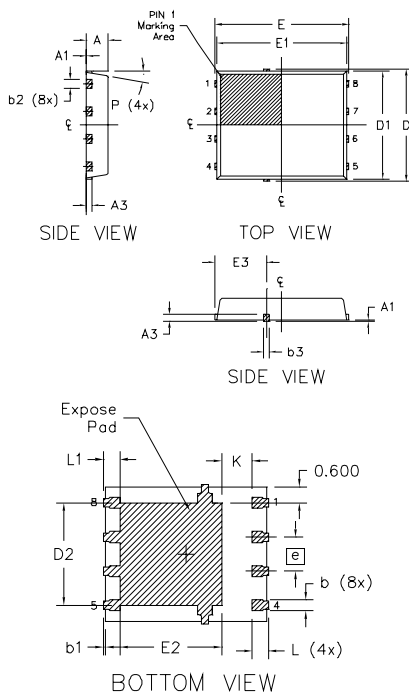
**Fig 24b. Gate Charge Waveform**

## PQFN 5x6 Outline "E" Package Details



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.17	0.0354	0.0461
b	0.33	0.48	0.0130	0.0189
C	0.195	0.300	0.0077	0.0118
D	4.80	5.15	0.1890	0.2028
D1	3.91	4.31	0.1539	0.1697
D2	4.80	5.00	0.1890	0.1968
E	5.90	6.15	0.2323	0.2421
E1	5.65	6.00	0.2224	0.2362
E2	1.51	—	0.0594	—
E3	3.32	3.78	0.1307	0.1480
E4	3.42	3.58	0.1346	0.1409
E5	0.18	0.32	0.0071	0.0126
e	1.27	BSC	0.050	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.66	0.0150	0.0260
L2	0.51	0.86	0.0201	0.0339
I	0	0.18	0	0.0071

## PQFN 5x6 Outline "G" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254	REF	0.0100	REF
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150	BSC	0.2028	BSC
D1	5.000	BSC	0.1969	BSC
D2	3.700	3.900	0.1457	0.1535
E	6.150	BSC	0.2421	BSC
E1	6.000	BSC	0.2362	BSC
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27	REF	0.050	REF
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

**Note:**

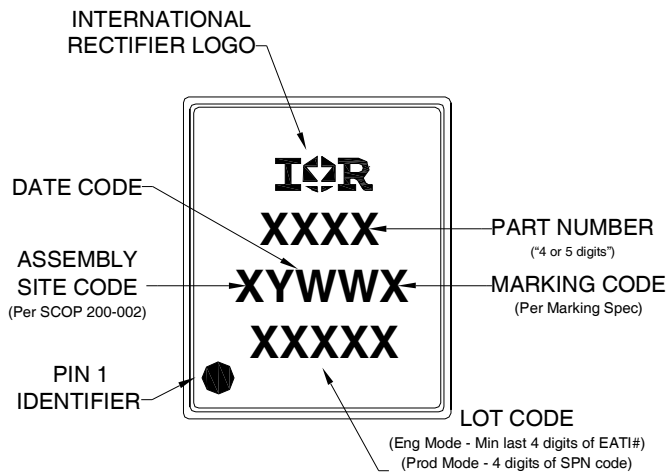
- Dimensions and tolerancing conform to ASME Y14.5M-1994
- Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
- Coplanarity applies to the expose Heat Slug as well as the terminal
- Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

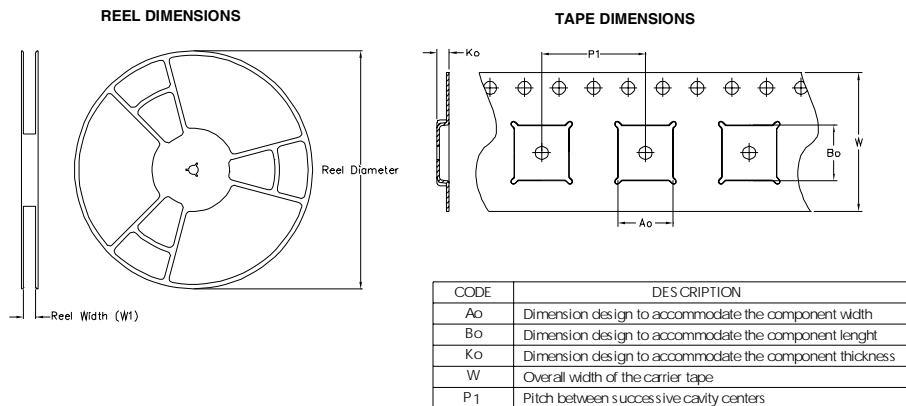
For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

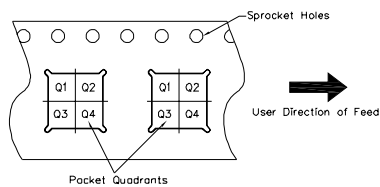
# PQFN 5x6 Part Marking



# PQFN 5x6 Tape and Reel



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial (per JEDEC JES D47F guidelines) <sup>††</sup>	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
1/17/2014	• Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259).
2/19/2015	• Updated $E_{AS(L=1mH)} = 152mJ$ on page 2 • Updated note 10 "Limited by $T_{Jmax}$ , starting $T_J = 25^{\circ}C$ , $L = 1mH$ , $R_G = 50\Omega$ , $I_{AS} = 18A$ , $V_{GS} = 10V$ ". on page 2
6/2/2015	• Updated package outline for "option E" and added package outline for "option G" on page 9. • Updated "IFX" logo on page 1 & 11. • Updated tape and reel on page 10.
7/7/2015	• Corrected package outline for "option E" on page 9.
8/19/2015	• Corrected Fig 10 - SOA Curve with Package Limitation = 85A instead of 50A on PW = DC Curve - page 5.
8/28/2015	• Notes: Number 1 - Corrected from "Current is limited to 71A ---" to "Current is limited to 85A -----" - page 2

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View IRFH7446TRPBF on WIN SOURCE](#)

 [Infineon Technologies](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management