THE DATASHEET OF

AD7715ARUZ-5

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3 V/5 V, 450 µA 16-Bit, Sigma-Delta ADC

Data Sheet **AD7715**

FEATURES

- **Charge-balancing ADC**
  - **16-bits no missing codes**
  - **0.0015% nonlinearity**
- **Programmable gain front end**
  - **Gains of 1, 2, 32 and 128**
  - **Differential input capability**
- **Three-wire serial interface**
- **SPI-, QSPI™-, MICROWIRE™-, and DSP-compatible**
- **Ability to buffer the analog input**
- **3 V (AD7715-3) or 5 V (AD7715-5) operation**
- **Low supply current: 450 µA maximum @ 3 V supplies**
- **Low-pass filter with programmable output update**
- **16-lead SOIC/PDIP/TSSOP**

FUNCTIONAL BLOCK DIAGRAM

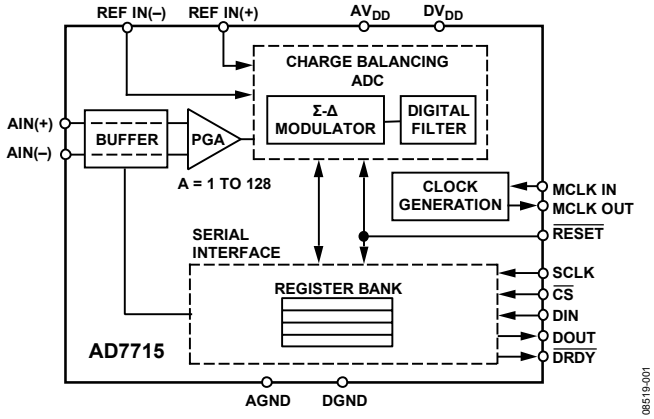

Figure 1.

GENERAL DESCRIPTION

The AD7715 is a complete analog front end for low frequency measurement applications. The part can accept low level input signals directly from a transducer and outputs a serial digital word. It employs a Σ-Δ conversion technique to realize up to 16 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and output update rate.

The AD7715 features a differential analog input as well as a differential reference input. It operates from a single supply (3 V or 5 V). It can handle unipolar input signal ranges of 0 mV to 20 mV, 0 mV to 80 mV, 0 V to 1.25 V and 0 V to 2.5 V. It can also handle bipolar input signal ranges of ±20 mV, ±80 mV, ±1.25 V and ±2.5 V. These bipolar ranges are referenced to the negative input of the differential analog input. The AD7715 thus performs all signal conditioning and conversion for a single channel system.

The AD7715 is ideal for use in smart, microcontroller, or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity, and update rate selection can be configured in software using the input serial port. The part contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system.

CMOS construction ensures very low power dissipation, and power-down mode reduces the standby power consumption to 50 µW typical. The part is available in a 16-lead, 0.3 inch-wide, plastic dual-in-line package (PDIP) as well as a 16-lead 0.3 inch wide small outline (SOIC_W) package and a 16-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. The AD7715 consumes less than 450 µA in total supply current at 3 V supplies and 1 MHz master clock, making it ideal for use in low-power systems. Standby current is less than 10 µA.
2. The programmable gain input allows the AD7715 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
3. The AD7715 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of optocouplers required in isolated systems. The part contains on-chip registers which allow software control over output update rate, input gain, signal polarity, and calibration modes.
4. The part features excellent static performance specifications with 16-bits no missing codes, ±0.0015% accuracy, and low rms noise (<550 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.

Rev. E Document Feedback
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REVISION HISTORY

6/15—Rev. D to Rev. E

Changes to Table 10 ... 13
Changed ADSP-2103/ADSP-2105 to ADSP-2184N/ADSP-2185N/ADSP-2186N/ADSP-2187N/ADSP-2188N/ADSP-2189N ... 33
Updated Outline Dimensions ... 39
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12/09—Rev. C to Rev. D

Updated Format ... Universal
Changes to Table 5 ... 9
Updated Outline Dimensions ... 39

2/00—Rev. B to Rev. C

SPECIFICATIONS

AD7715-5

AV_{DD} = 5 V, DV_{DD} = 3 V or 5 V, REF IN(+) = 2.5 V; REF IN(−) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
STATIC PERFORMANCE					
No Missing Codes	16			Bits	Guaranteed by design; filter notch ≤ 60 Hz
Output Noise		See Table 15 to Table 18			Depends on filter cutoffs and selected gain
Integral Nonlinearity			±0.0015	% of FSR	Filter notch ≤ 60 Hz
Unipolar Offset Error[2]		See Table 15 to Table 22			
Unipolar Offset Drift[3]		0.5		μV/°C	
Bipolar Zero Error[2]		See Table 15 to Table 22			
Bipolar Zero Drift[3]		0.5		μV/°C	
Positive Full-Scale Error[2, 4]		See Table 15 to Table 22			
Full-Scale Drift[3, 5]		0.5		μV/°C	
Gain Error[2, 6]		See Table 15 to Table 22			
Gain Drift[3, 7]		0.5		ppm of FSR/°C	
Bipolar Negative Full-Scale Error[2]			±0.0015	% of FSR	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[3]		1		μV/°C	For gains of 1 and 2
		0.6		μV/°C	For gains of 32 and 128
ANALOG INPUTS/REFERENCE INPUTS					Specifications for AIN and REF IN unless noted
Input Common-Mode Rejection (CMR)	90			dB	At dc; typically 102 dB
Normal-Mode 50 Hz Rejection[8]	98			dB	For filter notches of 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[8]	98			dB	For filter notches of 20 Hz, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[8]	150			dB	For filter notches of 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[8]	150			dB	For filter notches of 20 Hz, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode Voltage Range[9]	AGND		AV_{DD}	V	AIN for the BUF bit of setup register = 0 and REF IN
Absolute AIN/REF IN Voltage[8]	AGND − 0.03		AV_{DD} + 0.03	V	AIN for the BUF bit of setup register = 0 and REF IN
Absolute/Common-Mode AIN Voltage[9]	AGND + 0.05		AV_{DD} − 1.5	V	BUF bit of setup register = 1
AIN DC Input Current[8]			1	nA	
AIN Sampling Capacitance[8]			10	pF	
AIN Differential Voltage Range[10]		0 to +V_{REF}/GAIN[11]		nom	Unipolar input range ($\overline{B}$/U bit of setup register = 1)
		±V_{REF}/GAIN		nom	Bipolar input range ($\overline{B}$/U bit of setup register = 0)
AIN Input Sampling Rate, f_S		GAIN × $f_{CLK\ IN}$/64			For gains of 1 and 2
		$f_{CLK\ IN}$/8			For gains of 32 and 128
REF IN(+) − REF IN(−) Voltage		2.5		V nom	±1% for specified performance; functional with lower V_{REF}
REF IN Input Sampling Rate, f_S		$f_{CLK\ IN}$/64			
LOGIC INPUTS					
Input Current			±10	μA	
All Inputs Except MCLK IN					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
V_{INL}, Input Low Voltage			0.4	V	DV_{DD} = 3.3 V
V_{INH}, Input High Voltage	2.4			V	DV_{DD} = 5 V
V_{INH}, Input High Voltage	2.0			V	
MCLK IN Only					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
V_{INL}, Input Low Voltage			0.4	V	DV_{DD} = 3.3 V
V_{INH}, Input High Voltage	3.5			V	DV_{DD} = 5 V
V_{INH}, Input High Voltage	2.5			V	DV_{DD} = 3.3 V

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
LOGIC OUTPUTS (Including MCLK OUT)					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 800 μA except for MCLK OUT[12]; DV_{DD} = 5 V
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 100 μA except for MCLK OUT[12]; DV_{DD} = 3.3 V
V_{OH}, Output High Voltage	4.0			V	I_{SOURCE} = 200 μA except for MCLK OUT[12]; DV_{DD} = 5 V
V_{OH}, Output High Voltage	DV_{DD} − 0.6			V	I_{SOURCE} = 100 μA except for MCLK OUT[12]; DV_{DD} = 3.3 V
Floating State Leakage Current			±10	μA	
Floating State Output Capacitance[13]		9		pF	
Data Output Coding		Binary			Unipolar mode
		Offset binary			Bipolar mode

[1] Temperature range as follows: A version, −40°C to +85°C.
[2] A calibration is effectively a conversion, so these errors are of the order of the conversion noise shown in Table 15 to Table 22. This applies after calibration at the temperature of interest.
[3] Recalibration at any temperature removes these drift errors.
[4] Positive full-scale error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges.
[5] Full-scale drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and applies to both unipolar and bipolar input ranges.
[6] Gain error does not include zero-scale errors. It is calculated as full-scale error–unipolar offset error for unipolar ranges and full-scale error–bipolar zero error for bipolar ranges.
[7] Gain error drift does not include unipolar offset drift/bipolar zero drift. It is effectively the drift of the part if zero scale calibrations only were performed.
[8] These numbers are guaranteed by design and/or characterization.
[9] This common-mode voltage range is allowed provided that the input voltage on AIN(+) or AIN(–) does not go more positive than AV_{DD} + 30 mV or go more negative than AGND − 30 mV.
[10] The analog input voltage range on AIN(+) is given here with respect to the voltage on AIN(–). The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than AGND − 30 mV.
[11] V_{REF} = REF IN(+) − REF IN(–).
[12] These logic output levels apply to the MCLK OUT only when it is loaded with one CMOS load.
[13] Sample tested at 25°C to ensure compliance.

AD7715-3

AV_{DD} = 3 V, DV_{DD} = 3 V, REF IN (+) = 1.25 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
STATIC PERFORMANCE					
No Missing Codes	16			Bits	Guaranteed by design; filter notch ≤ 60 Hz
Output Noise		See Table 18 to Table 22			Depends on filter cutoffs and selected gain
Integral Nonlinearity			±0.0015	% of FSR	Filter notch ≤ 60 Hz
Unipolar Offset Error[2]		See Table 15 to Table 22			
Unipolar Offset Drift[3]		0.2		µV/°C	
Bipolar Zero Error[2]		See Table 15 to Table 22			
Bipolar Zero Drift[3]		0.2		µV/°C	
Positive Full-Scale Error[2, 4]		See Table 15 to Table 22			
Full-Scale Drift[3, 5]		0.2		µV/°C	
Gain Error[2, 6]		See Table 15 to Table 22			
Gain Drift[3, 7]		0.2		ppm of FSR/°C	
Bipolar Negative Full-Scale Error[2]			±0.003	% of FSR	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[3]		1		µV/°C	For gains of 1 and 2
		0.6		µV/°C	For gains of 32 and 128
ANALOG INPUTS/REFERENCE INPUTS					Specifications for AIN and REF IN unless noted
Input Common-Mode Rejection (CMR)	90			dB	At dc; tpically 102 dB
Normal-Mode 50 Hz Rejection[8]	98			dB	For filter notches of 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal-Mode 60 Hz Rejection[8]	98			dB	For filter notches of 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 50 Hz Rejection[8]	150			dB	For filter notches of 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[8]	150			dB	For filter notches of 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode Voltage Range[9]	AGND		AV_{DD}	V	AIN for BUF bit of setup register = 0 and REF IN
Absolute AIN/REF IN Voltage[8]	AGND – 0.03		AV_{DD} + 0.03	V	AIN for BUF bit of setup register = 0 and REF IN
Absolute/Common-Mode AIN Voltage[9]	AGND + 0.05		AV_{DD} – 1.5	V	BUF bit of setup register = 1
AIN DC Input Current[8]			1	nA	
AIN Sampling Capacitance[8]			10	pF	
AIN Differential Voltage Range[10]		0 to $+V_{REF}/GAIN$[11]		nom	Unipolar input range ($\overline{B}$/U bit of setup register = 1)
		$\pm V_{REF}/GAIN$		nom	Bipolar input range ($\overline{B}$/U bit of setup register = 0)
AIN Input Sampling Rate, f_S		$GAIN \times f_{CLK\ IN}/64$			For gains of 1 and 2
		$f_{CLK\ IN}/8$			For gains of 32 and 128
REF IN(+) – REF IN(–) Voltage		1.25		V nom	±1% for specified performance; functional with lower V_{REF}
REF IN Input Sampling Rate, f_S		$f_{CLK\ IN}/64$			
LOGIC INPUTS					
Input Current			±10	µA	
All Inputs Except MCLK IN					
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.0			V	
MCLK IN Only					
V_{INL}, Input Low Voltage			0.4	V	
V_{INH}, Input High Voltage	2.5			V	

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
LOGIC OUTPUTS (Including MCLK OUT)					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 100 μA except for MCLK OUT[12]
V_{OH}, Output High Voltage	DV_{DD} − 0.6			V	I_{SOURCE} = 100 μA except for MCLK OUT[12]
Floating State Leakage Current			±10	μA	
Floating State Output Capacitance[13]		9		pF	
Data Output Coding		Binary			Unipolar mode
		Offset binary			Bipolar mode

[1] Temperature range as follows: A version, −40°C to +85°C.
[2] A calibration is effectively a conversion, so these errors are of the order of the conversion noise shown in Table 15 to Table 22. This applies after calibration at the temperature of interest.
[3] Recalibration at any temperature removes these drift errors.
[4] Positive full-scale error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges.
[5] Full-scale drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and applies to both unipolar and bipolar input ranges.
[6] Gain error does not include zero-scale errors. It is calculated as full-scale error−unipolar offset error for unipolar ranges and Full-Scale Error−Bipolar Zero Error for bipolar ranges.
[7] Gain error drift does not include unipolar offset drift/bipolar zero drift. It is effectively the drift of the part if zero scale calibrations only were performed.
[8] These numbers are guaranteed by design and/or characterization.
[9] This common-mode voltage range is allowed provided that the input voltage on AIN(+) or AIN(−) does not go more positive than AV_{DD} + 30 mV or go more negative than AGND − 30 mV.
[10] The analog input voltage range on AIN(+) is given here with respect to the voltage on AIN(−). The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than AGND − 30 mV.
[11] V_{REF} = REF IN(+) − REF IN(−).
[12] These logic output levels apply to the MCLK OUT only when it is loaded with one CMOS load.
[13] Sample tested at 25°C to ensure compliance.

AV_{DD} = 3 V to 5 V, DV_{DD} = 3 V to 5 V, REF IN(+) = 1.25 V (AD7715-3) or 2.5 V (AD7715-5); REF IN(−) = AGND; MCLK IN = 1 MHz to 2.4576 MHz, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
SYSTEM CALIBRATION					
Positive Full-Scale Calibration Limit[1]			(1.05 × V_{REF})/GAIN	V	GAIN Is the selected PGA gain (1, 2, 32, or 128)
Negative Full-Scale Calibration Limit[1]			−(1.05 × V_{REF})/GAIN	V	GAIN Is the selected PGA gain (1, 2, 32, or 128)
Offset Calibration Limit[2]			−(1.05 × V_{REF})/GAIN	V	GAIN Is the selected PGA gain (1, 2, 32, or 128)
Input Span[2]	0.8 × V_{REF}/GAIN			V	GAIN Is the selected PGA gain (1, 2, 32, or 128)
			(2.1 × V_{REF})/GAIN	V	GAIN Is the selected PGA gain (1, 2, 32, or 128)
POWER REQUIREMENTS					
Power Supply Voltages					
AV_{DD} Voltage (AD7715-3)	3		3.6	V	For specified performance
AV_{DD} Voltage (AD7715-5)	4.75		5.25	V	For specified performance
DV_{DD} Voltage	3		5.25	V	For specified performance
Power Supply Currents					
AV_{DD} Current					AV_{DD} = 3.3 V or 5 V. gain = 1 to 128 ($f_{CLK\ IN}$ = 1 MHz) or gain = 1 or 2 ($f_{CLK\ IN}$ = 2.4576 MHz)
			0.27	mA	Typically 0.2 mA; BUF bit of the setup register = 0
			0.6	mA	Typically 0.4 mA; BUF bit of the setup register = 1, AV_{DD} = 3.3 V or 5 V; gain = 32 or 128 ($f_{CLK\ IN}$ = 2.4576 MHz)[3]
			0.5	mA	Typically 0.3 mA; BUF bit of the setup register = 0
			1.1	mA	Typically 0.8 mA; BUF bit of the setup register = 1
DV_{DD} Current[4]					Digital inputs = 0 V or DV_{DD}; external MCLK IN
			0.18	mA	Typically 0.15 mA. DV_{DD} = 3.3 V. $f_{CLK\ IN}$ = 1 MHz
			0.4	mA	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 1 MHz
			0.5	mA	Typically 0.4 mA. DV_{DD} = 3.3 V. $f_{CLK\ IN}$ = 2.4576 MHz
			0.8	mA	Typically 0.6 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Power Supply Rejection[5]		Depends on gain[6]		dB	
Normal-Mode Power Dissipation[4]					AV_{DD} = DV_{DD} = 3.3 V; digital inputs = 0 V or DV_{DD}; external MCLK IN
			1.5	mW	BUF bit = 0. all gains 1 MHz clock
			2.65	mW	BUF bit = 1. all gains 1 MHz clock
			3.3	mW	BUF bit = 0. Gain = 32 or 128 @ $f_{CLK\ IN}$ = 2.4576 MHz
			5.3	mW	BUF bit = 1. Gain = 32 or 128 @ $f_{CLK\ IN}$ = 2.4576 MHz
Normal-Mode Power Dissipation[4]					AV_{DD} = DV_{DD} = 5 V. digital inputs = 0 V or DV_{DD}; external MCLK IN
			3.25	mW	BUF bit = 0; all gains 1 MHz clock
			5	mW	BUF bit = 1; all gains 1 MHz clock
			6.5	mW	BUF bit = 0; gain = 32 or 128 @ $f_{CLK\ IN}$ = 2.4576 MHz
			9.5	mW	BUF bit = 1; gain = 32 or 128 @ $f_{CLK\ IN}$ = 2.4576 MHz
Standby (Power-Down) Current[7]			20	μA	External MCLK IN = 0 V or DV_{DD}. typically 10 μA; V_{DD} = 5 V
Standby (Power-Down) Current[7]			10	μA	External MCLK IN = 0 V or DV_{DD}. typically 5 μA; V_{DD} = 3.3 V

[1] After calibration, if the analog input exceeds positive full scale, the converter outputs all 1s. If the analog input is less than negative full scale, then the device outputs all 0s.
[2] These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.
[3] Assumes CLK Bit of setup register is set to correct status corresponding to the master clock frequency.
[4] When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the DV_{DD} current and power dissipation will vary depending on the crystal or resonator type (see the Clocking and Oscillator Circuit section).
[5] Measured at dc and applies in the selected pass-band. PSRR at 50 Hz exceeds 120 dB with filter notches of 25 Hz or 50 Hz. PSRR at 60 Hz exceeds 120 dB with filter notches of 20 Hz or 60 Hz.
[6] PSRR depends on gain. Gain of 1:85 dB typical; gain of 2:90 dB typical; gains of 32 and 128:95 dB typical.
[7] If the external master clock continues to run in standby mode, the standby current increases to 50 μA typical. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode and the power dissipation depends on the crystal or resonator type (see the Standby Mode section).

TIMING CHARACTERISTICS

DV_{DD} = 3 V to 5.25 V; AV_{DD} = 3 V to 5.25 V; AGND = DGND = 0 V; f_{CLKIN} = 2.4576 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise noted.

Table 4.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (A Version)	Unit	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master clock frequency: crystal oscillator or externally supplied for specified performance
	2.5	MHz max	
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master clock input low time; $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master clock input high time
t_1	500 × $t_{CLK\ IN}$	ns nom	$\overline{DRDY}$ high time
t_2	100	ns min	$\overline{RESET}$ pulsewidth
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ setup time
t_4	120	ns min	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_5[5]	0	ns min	SCLK falling edge to data valid delay
	80	ns max	DV_{DD} = 5 V
	100	ns max	DV_{DD} = 3.3 V
t_6	100	ns min	SCLK high pulsewidth
t_7	100	ns min	SCLK low pulsewidth
t_8	0	ns min	$\overline{CS}$ rising edge to SCLK rising edge hold time
t_9[6]	10	ns min	Bus relinquish time after SCLK rising edge
	60	ns max	DV_{DD} = +5 V
	100	ns max	DV_{DD} = +3.3 V
t_{10}	100	ns max	SCLK falling edge to $\overline{DRDY}$ high[7]
Write Operation			
t_{11}	120	ns min	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_{12}	30	ns min	Data valid to SCLK rising edge setup time
t_{13}	20	ns min	Data valid to SCLK rising edge hold time
t_{14}	100	ns min	SCLK high pulsewidth
t_{15}	100	ns min	SCLK low pulsewidth
t_{16}	0	ns min	$\overline{CS}$ rising edge to SCLK rising edge hold time

[1] Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 8 and Figure 9.
[3] CLKIN Duty Cycle range is 45% to 55%. CLKIN must be supplied whenever the AD7715 is not in standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.
[4] The AD7715 is production tested with f_{CLKIN} at 2.4576 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.
[5] These numbers are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[6] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[7] $\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high although take care that subsequent reads do not occur close to the next output update.

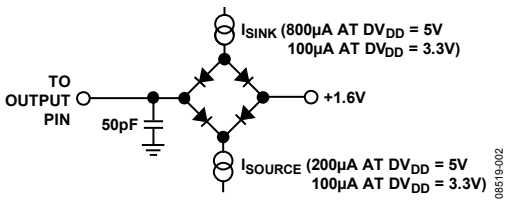


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
AV_{DD} to DGND	−0.3 V to +7 V
AV_{DD} to DV_{DD}	−0.3 V to +7 V
DV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
DGND to AGND	−0.3 V to +7 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Commercial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Plastic DIP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	105°C/W
Lead Temperature, (Soldering, 10 sec)	260°C
SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature, Reflow Soldering	260°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	128°C/W
Lead Temperature, Reflow Soldering	+260°C
Power Dissipation (Any Package) to +75°C	450 mW
ESD Rating	>4000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

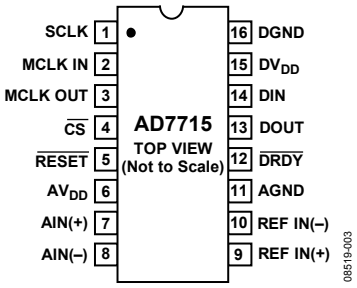


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock. Logic input. An external serial clock is applied to this input to access serial data from the AD7715. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7715 in smaller batches of data.
2	MCLK IN	Master Clock Signal for the Device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The part is specified with clock input frequencies of both 1 MHz and 2.4576 MHz.
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuitry.
4	$\overline{CS}$	Chip Select. Active low logic input used to select the AD7715. With this input hardwired low, the AD7715 can operate in its three-wire interface mode with SCLK, DIN, and DOUT used to interface to the device. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7715.
5	$\overline{RESET}$	Logic Input. Active low input which resets the control logic, interface logic, calibration coefficients, digital filter, and analog modulator of the part to power-on status.
6	AV_{DD}	Analog Positive Supply Voltage, 3.3 V nominal (AD7715-3) or 5 V nominal (AD7715-5).
7	AIN(+)	Analog Input. Positive input of the programmable gain differential analog input to the AD7715.
8	AIN(–)	Analog Input. Negative input of the programmable gain differential analog input to the AD7715.
9	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7715. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.
10	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7715. The REF IN(–) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(–).
11	AGND	Ground Reference Point for Analog Circuitry. For correct operation of the AD7715, no voltage on any of the other pins should go more than 30 mV negative with respect to AGND.
12	$\overline{DRDY}$	Logic Output. A logic low on this output indicates that a new output word is available from the AD7715 data register. The $\overline{DRDY}$ pin returns high upon completion of a read operation of a full output word. If no data read has taken place between output updates, the $\overline{DRDY}$ line returns high for 500 × $t_{CLK\ IN}$ cycles prior to the next output update. While $\overline{DRDY}$ is high, a read operation should not be attempted or in progress to avoid reading from the data register as it is being updated. The $\overline{DRDY}$ line returns low again when the update has taken place. $\overline{DRDY}$ is also used to indicate when the AD7715 has completed its on-chip calibration sequence.
13	DOUT	Serial data output with serial data being read from the output shift register on the part. This output shift register can contain information from the setup register, communications register or data register depending on the register selection bits of the communications register.
14	DIN	Serial data input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the setup register or communications register depending on the register selection bits of the communications register.
15	DV_{DD}	Digital Supply Voltage, 3.3 V or 5 V nominal.
16	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero-scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 … 000 to 000 … 001) and Full-Scale, a point 0.5 LSB above the last code transition (111 … 110 to 111 … 111). The error is expressed as a percentage of full scale.

Positive Full-Scale Error
Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(−) + V_{REF}/GAIN −3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

Unipolar Offset Error
Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(−) + 0.5 LSB) when operating in the unipolar mode.

Bipolar Zero Error
This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(−) − 0.5 LSB) when operating in the bipolar mode.

Gain Error
This is a measure of the span error of the ADC. It includes full-scale errors but not zero-scale errors. For unipolar input ranges it is defined as (full scale error—unipolar offset error) while for bipolar input ranges it is defined as (full-scale error—bipolar zero error).

Bipolar Negative Full-Scale Error
This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(−) − VREF/GAIN + 0.5 LSB), when operating in the bipolar mode.

Positive Full-Scale Overrange
Positive full-scale overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN−) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

Negative Full-Scale Overrange
This is the amount of overhead available to handle voltages on AIN(+) below AIN(−) −V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input accepts negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(−) and greater than AGND − 30 mV.

Offset Calibration Range
In the system calibration modes, the AD7715 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7715 can accept and still calibrate offset accurately.

Full-Scale Calibration Range
This is the range of voltages that the AD7715 can accept in the system calibration mode and still calibrate full scale correctly.

Input Span
In system calibration schemes, two voltages applied in sequence to the AD7715's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7715 can accept and still calibrate gain accurately.

ON-CHIP REGISTERS

The AD7715 contains four on-chip registers, which can be accessed by via the serial port on the part. The first of these is a communications register that decides whether the next operation is a read or write operation and also decides which register the read or write operation accesses. All communications to the part must start with a write operation to the communications register. After power-on or RESET, the device expects a write to its communications register. The data written to this register determines whether the next operation to the part is a write or a read operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the communications register followed by a write to the selected register. A read operation from any register on the part (including the communications register itself and the output data register) starts with a write operation to the communications register followed by a read operation from the selected register. The communication register also controls the standby mode and the operating gain of the part. The $\overline{\text{DRDY}}$ status is also available by reading from the communications register. The second register is a setup register that determines calibration modes, filter selection and bipolar/unipolar operation. The third register is the data register from which the output data from the part is accessed. The final register is a test register that is accessed when testing the device. It is advised that the user does not attempt to access or change the contents of the test register as it may lead to unspecified operation of the device. The registers are discussed in more detail in the following sections.

COMMUNICATIONS REGISTER (RS1, RS0 = 0, 0)

The communications register is an eight-bit register from which data can either be read or to which data can be written. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation and to which register this operation takes place. Once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface, and on power-up or after a reset, the AD7715 is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, if a write operation to the device of sufficient duration (containing at least 32 serial clock cycles) takes place with DIN high, the AD7715 returns to this default state. Table 7 outlines the bit designations for the communications register.

Table 7. Communications Register

0/$\overline{\text{DRDY}}$	ZERO	RS1	RS0	R/$\overline{\text{W}}$	STBY	G1	G0

Table 8.

Bit Name	Description
0/$\overline{\text{DRDY}}$	For a write operation, a 0 must be written to this bit so that the write operation to the communications register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. Instead, it stays at this bit location until a 0 is written to this bit. Once a 0 is written to this bit, the next 7 bits are loaded to the communications register. For a read operation, this bit provides the status of the $\overline{\text{DRDY}}$ flag from the part. The status of this bit is the same as the $\overline{\text{DRDY}}$ output pin.
ZERO	For a write operation, a 0 must be written to this bit for correct operation of the part. Failure to do this results in unspecified operation of the device. For a read operation, a 0 is read back from this bit location.
RS1, RS0	Register Selection Bits. These bits select to which one of four on-chip registers the next read or write operation takes place as shown in Table 9 along with the register size. When the read or write to the selected register is complete, the part returns to where it is waiting for a write operation to the Communications Register. It does not remain in a state where it continues to access the selected register.
R/$\overline{\text{W}}$	Read/Write Select. This bit selects whether the next operation is a read or write operation to the selected register. A 0 indicates a write cycle as the next operation to the appropriate register, while a 1 indicates a read operation from the appropriate register.
STBY	Standby. Writing a 1 to this bit puts the part in its standby or power-down mode. In this mode, the part consumes only 10 µA of power supply current. The part retains its calibration and control word information when in STANDBY. Writing a 0 to this bit places the part in its normal operating mode. The default value for this bit after power-on or RESET is 0.
G1, G0	Gain Select bits. See Table 10.

Table 9. Register Section

RS1	RS0	Register	Register Size
0	0	Communications register	8 bits
0	1	Setup register	8 bits
1	0	Test register	8 bits
1	1	Data register	16 bits

Table 10.

G1	G0	Gain Setting
0	0	1
0	1	2
1	0	32
1	1	128

SETUP REGISTER (RS1, RS0 = 0, 1); POWER ON/RESET STATUS: 28 HEX

The setup register is an eight-bit register from which data can either be read or to which data can be written. This register controls the setup that the device is to operate in such as the calibration mode, and output rate, unipolar/bipolar operation etc. Table 11 outlines the bit designations for the setup register.

Table 11. Setup Register

MD1	MD0	CLK	FS1	FS0	$\overline{B}$/U	BUF	FSYNC

Table 12.

Bit Name	Description
MD1, MD0	Mode select bits. These bits select the operating mode of the AD7715 (see Table 13).
CLK	The clock bit (CLK) should be set in accordance with the operating frequency of the AD7715. If the device has a master clock frequency of 2.4576 MHz, then this bit should be set to a 1. If the device has a master clock frequency of 1 MHz, then this bit should be set to a 0. This bit sets up the correct scaling currents for a given master clock and also chooses (along with FS1 and FS0) the output update rate for the device. If this bit is not set correctly for the master clock frequency of the device, then the device may not operate to specification. The default value for this bit after power-on or reset is 1.
FS1, FS0	Along with the CLK bit, FS1 and FS0 determine the output update rate, filter first notch and −3 dB frequency as outlined in Table 14. The on-chip digital filter provides a $sinc^3$ (or $(Sinx/x)^3$) filter response. In association with the gain selection, it also determines the output noise (and therefore, the resolution) of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Table 15 through Table 22 show the effect of the filter notch frequency and gain on the output noise and effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 500 Hz, a new word is available every 2 ms. The default value for these bits is 1, 0. The settling-time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms maximum. If the first notch is at 500 Hz, the settling time of the filter to a full-scale input step is 8 ms max. This settling-time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the FSYNC bit high, the settling-time time is 3 × 1/(output data rate) from when FSYNC returns low. The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: *filter −3 dB frequency* = 0.262 × *filter first notch frequency*
B/U	A 0 in this bipolar/unipolar operation bit selects bipolar operation. This is the default (power-on or reset) status of this bit. A 1 in this bit selects unipolar operation.
BUF	With this buffer control bit low, the on-chip buffer on the analog input is shorted out. With the buffer shorted out, the current flowing in the AV_{DD} line is reduced to 250 µA (all gains at $f_{CLK\,IN}$ = 1 MHz and gain of 1 or 2 at $f_{CLK\,IN}$ = 2.4576 MHz) or 500 µA (gains of 32 and 128 @ $f_{CLK\,IN}$ = 2.4576 MHz) and the output noise from the part is at its lowest. When this bit is high, the on-chip buffer is in series with the analog input allowing the input to handle higher source impedances.
FSYNC	When this filter synchronization bit is high, the nodes of the digital filter, the filter control logic and the this bit goes low, the modulator and filter start to process data and a valid word is available in 3 × 1/(output update rate), that is, the settling-time of the filter. This FSYNC bit does not affect the digital interface and does not reset the $\overline{DRDY}$ output if it is low.

Table 13.

MD1	MD0	Operating Mode
0	0	Normal mode. This operating mode is the default mode of operation of the device whereby the device is performing normal conversions. The AD7705 is placed in this mode after power-on or reset.
0	1	Self-calibration. This is a one step calibration sequence and when complete the part returns to normal mode with MD1 and MD0 returning to 0, 0. The $\overline{\text{DRDY}}$ output or $\overline{\text{DRDY}}$bit goes high when calibration is initiated and returns low when this self-calibration is complete and a new valid word is available in the data register. The zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs and the full-scale calibration is performed at the selected gain on an internally generated V_{REF}/selected gain.
1	0	Zero-scale system calibration. Zero-scale system calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The $\overline{\text{DRDY}}$ output or $\overline{\text{DRDY}}$ bit goes high when calibration is initiated and returns low when this zero-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to normal mode with MD1 and MD0 returning to 0, 0.
1	1	Full-scale system calibration. Full-scale system calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The $\overline{\text{DRDY}}$ output or $\overline{\text{DRDY}}$ bit goes high when calibration is initiated and returns low when this full-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to normal mode with MD1 and MD0 returning to 0, 0.

Table 14. Output Update Rates

CLK[1]	FS1	FS0	Output Update Rate	−3 dB Filter Cutoff
0	0	0	20 Hz	5.24 Hz
0	0	1	25 Hz	6.55 Hz
0	1	0	100 Hz	26.2 Hz
0	1	1	200 Hz	52.4 Hz
1	0	0	50 Hz	13.1 Hz
1	0	1	60 Hz	15.7 Hz (default status)
1	1	0	250 Hz	65.5 Hz
1	1	1	500 Hz	131 Hz

[1] Assumes correct clock frequency at MCLK IN pin.

TEST REGISTER (RS1, RS0 = 1, 0)

The part contains a test register, which is used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (power-on or reset) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising $\overline{\text{RESET}}$ will exit the part from the mode. An alternative scheme for getting the part out of one of its test modes, is to reset the interface by writing 32 successive 1s to the part and then load all 0s to the test register.

DATA REGISTER (RS1, RS0 = 1, 1)

The data register on the part is a read-only 16-bit register that contains the most up-to-date conversion result from the AD7715. If the communications register data sets up the part for a write operation to this register, a write operation must actually take place to return the part to where it is expecting a write operation to the communications register (the default state of the interface). However, the 16 bits of data written to the part will be ignored by the AD7715.

OUTPUT NOISE

AD7715-5

Table 15 shows the AD7715-5 output rms noise for the selectable notch and −3 dB frequencies for the part, as selected by FS1 and FS0 of the setup register. The numbers given are for the bipolar input ranges with a V_{REF} of 2.5 V. These numbers are typical and are generated at a differential analog input voltage of 0 V with the part used in unbuffered mode (BUF bit of the setup register = 0). Table 16 meanwhile shows the output peak-to-peak noise for the selectable notch and −3 dB frequencies for the part. It is important to note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. The numbers given are for the bipolar input ranges with a V_{REF} of 2.5 V and for the BUF bit of the setup register = 0. These numbers are typical, are generated at an analog input voltage of 0 V and are rounded to the nearest LSB.

Meanwhile, Table 17 and Table 18 show rms noise and peak-to-peak resolution respectively with the AD7715-5 operating under the same conditions as above except that now the part is operating in buffered mode (BUF bit of the setup register = 1).

Table 15. Output RMS Noise vs. Gain and Output Update Rate for AD7715-5 (Unbuffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Output RMS Noise (μV)			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	3.8	1.9	0.6	0.52
60 Hz	25 Hz	15.72 Hz	6.55 Hz	4.8	2.4	0.6	0.62
250 Hz	100 Hz	65.5 Hz	26.2 Hz	103	45	3.0	1.6
500 Hz	200 Hz	131 Hz	52.4 Hz	530	250	18	5.5

Table 16. Peak-to-Peak Resolution vs. Gain and Output Update Rate for AD7715-5 (Unbuffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Peak-to-Peak Resolution in Bits			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	16	16	16	14
60 Hz	25 Hz	15.72 Hz	6.55 Hz	16	16	16	13
250 Hz	100 Hz	65.5 Hz	26.2 Hz	13	13	13	12
500 Hz	200 Hz	131 Hz	52.4 Hz	10	10	10	10

Table 17. Output RMS Noise vs. Gain and Output Update Rate for AD7715-5 (Buffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Output RMS Noise (μV)			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	4.3	2.2	0.9	0.9
60 Hz	25 Hz	15.72 Hz	6.55 Hz	5.1	3.1	1.0	1.0
250 Hz	100 Hz	65.5 Hz	26.2 Hz	103	50	3.9	2.1
500 Hz	200 Hz	131 Hz	52.4 Hz	550	280	18	6

Table 18. Peak-to-Peak Resolution vs. Gain and Output Update Rate for AD7715-5 (Buffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Peak-to-Peak Resolution in Bits			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	16	16	15	13
60 Hz	25 Hz	15.72 Hz	6.55 Hz	16	16	15	13
250 Hz	100 Hz	65.5 Hz	26.2 Hz	13	13	13	12
500 Hz	200 Hz	131 Hz	52.4 Hz	10	10	10	10

AD7715-3

Table 19 shows the AD7715-3 output rms noise for the selectable notch and −3 dB frequencies for the part, as selected by FS1 and FS0 of the setup register. The numbers given are for the bipolar input ranges with a V_{REF} of 1.25 V. These numbers are typical and are generated at an analog input voltage of 0 V with the part used in unbuffered mode (BUF bit of the setup register = 0). Table 20 meanwhile shows the output peak-to-peak noise for the selectable notch and −3 dB frequencies for the part. It is important to note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. The numbers given are for the bipolar input ranges with a V_{REF} of 1.25 V and for the BUF bit of the setup register = 0. These numbers are typical, are generated at an analog input voltage of 0 V and are rounded to the nearest LSB.

Meanwhile, Table 21 and Table 22 show rms noise and peak-to-peak resolution respectively with the AD7715-3 operating under the same conditions as above except that now the part is operating in buffered mode (BUF bit of the setup register = 1).

Table 19. Output RMS Noise vs. Gain and Output Update Rate for AD7715-3 (Unbuffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Output RMS Noise (μV)			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	3.0	1.7	0.7	0.65
60 Hz	25 Hz	15.72 Hz	6.55 Hz	3.4	2.1	0.7	0.7
250 Hz	100 Hz	65.5 Hz	26.2 Hz	45	20	2.2	1.6
500 Hz	200 Hz	131 Hz	52.4 Hz	270	135	9.7	3.3

Table 20. Peak-to-Peak Resolution vs. Gain and Output Update Rate for AD7715-3 (Unbuffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Peak-to-Peak Resolution in Bits			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	16	16	14	12
60 Hz	25 Hz	15.72 Hz	6.55 Hz	16	16	14	12
250 Hz	100 Hz	65.5 Hz	26.2 Hz	13	13	13	11
500 Hz	200 Hz	131 Hz	52.4 Hz	11	11	10	10

Table 21. Output RMS Noise vs. Gain and Output Update Rate for AD7715-3 (Buffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Output RMS Noise (μV)			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	4.5	2.4	0.9	0.9
60 Hz	25 Hz	15.72 Hz	6.55 Hz	5.1	2.9	0.9	1.0
250 Hz	100 Hz	65.5 Hz	26.2 Hz	50	25	2.6	2
500 Hz	200 Hz	131 Hz	52.4 Hz	270	135	9.7	3.3

Table 22. Peak-to-Peak Resolution vs. Gain and Output Update Rate for AD7715-3 (Buffered Mode)

Filter First Notch and Output Data Rate		−3 dB Frequency		Typical Peak-to-Peak Resolution in Bits			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	Gain = 1	Gain = 2	Gain = 32	Gain = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	16	16	14	12
60 Hz	25 Hz	15.72 Hz	6.55 Hz	16	16	14	12
250 Hz	100 Hz	65.5 Hz	26.2 Hz	13	13	12	11
500 Hz	200 Hz	131 Hz	52.4 Hz	10	11	10	10

CALIBRATION SEQUENCES

The AD7715 contains a number of calibration options as outlined in Table 13. Table 23 summarizes the calibration types, the operations involved and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor when $\overline{\text{DRDY}}$ returns low at the end of the sequence. $\overline{\text{DRDY}}$ not only indicates when the sequence is complete but also that the part has a valid new sample in its data register. This valid new sample is the result of a normal conversion which follows the calibration sequence. The second method of determining when calibration is complete is to monitor the MD1 and MD0 bits of the setup register. When these bits return to 0, 0 following a calibration command, it indicates that the calibration sequence is complete. This method does not give any indication of there being a valid new result in the data register. However, it gives an earlier indication than $\overline{\text{DRDY}}$ that calibration is complete. The duration to when the mode bits (MD1 and MD0) return to 0, 0 represents the duration of the calibration carried out. The sequence to when $\overline{\text{DRDY}}$ goes low also includes a normal conversion and a pipeline delay, t_P, to correctly scale the results of this first conversion. t_P will never exceed 2000 × $t_{CLK\,IN}$. The time for both methods is given in Table 23.

Table 23. Calibration Sequences

Calibration Type	MD1, MD0	Calibration Sequence	Duration to Mode Bits	Duration to $\overline{\text{DRDY}}$
Self Calibration	0, 1	Internal ZS Cal @ Selected Gain + Internal FS Cal @ Selected Gain	6 × 1/Output Rate	9 ×1/Output Rate + t_P
ZS System Calibration	1, 0	ZS Cal on AIN @ Selected Gain	3 × 1/Output Rate	4 × 1/Output Rate + t_P
FS System Calibration	1, 1	FS Cal on AIN @ Selected Gain	3 × 1/Output Rate	4 × 1/Output Rate + t_P

CIRCUIT DESCRIPTION

The AD7715 is a Σ-Δ ADC with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a Σ-Δ (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter, and a bidirectional serial communications port. The part consumes only 450 μA of power supply current, making it ideal for battery-powered or loop-powered instruments. The part comes in two versions, the AD7715-5 which is specified for operation from a nominal 5 V analog supply (AV_{DD}) and the AD7715-3 which is specified for operation from a nominal 3.3 V analog supply. Both versions can be operated with a digital supply (DV_{DD}) voltage of 3.3 V or 5 V.

The part contains a programmable-gain fully differential analog input channel. The selectable gains on this input are 1, 2, 32, and 128 allowing the part to accept unipolar signals of between 0 mV to 20 mV and 0 V to 2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals 2.5 V. With a reference voltage of 1.25 V, the input ranges are from 0 mV to 10 mV to 0 V to +1.25 V in unipolar mode and from ±10 mV to ±1.25 V in bipolar mode. Note that the bipolar ranges are with respect to AIN(−) and not with respect to AGND.

The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing ADC (Σ-Δ modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this Σ-Δ modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the Σ-Δ modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and therefore its −3 dB frequency) can be programmed via the setup register bits, FS0 and FS1. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency is from 50 Hz to 500 Hz giving a programmable range for the −3 dB frequency of 13.1 Hz to 131 Hz. With a master clock frequency of 1 MHz, the programmable range for this first notch frequency is from 20 Hz to 200 Hz giving a programmable range for the −3 dB frequency of 5.24 Hz to 52.4 Hz.

The basic connection diagram for the AD7715-5 is shown in Figure 4. This shows both the AV_{DD} and DV_{DD} pins of the AD7715 being driven from the analog 5 V supply. Some applications have AV_{DD} and DV_{DD} driven from separate supplies. An AD780, precision 2.5 V reference, provides the reference source for the part. On the digital side, the part is configured for three-wire operation with $\overline{CS}$ tied to DGND. A quartz crystal or ceramic resonator provides the master clock source for the part. In most cases, it is necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors vary depending on the manufacturer's specifications.

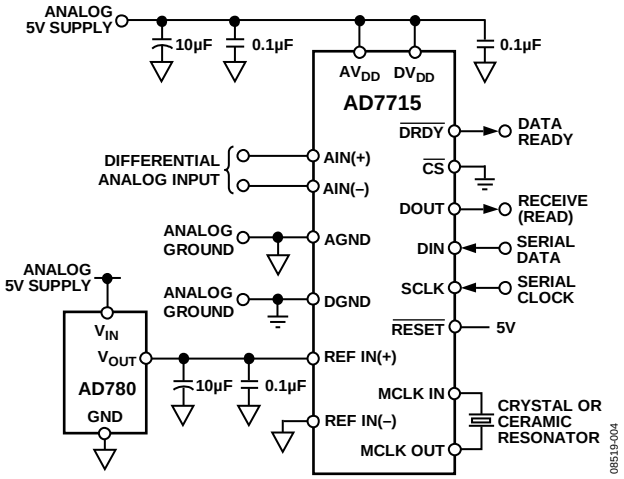


Figure 4. AD7715-5 Basic Connection Diagram

ANALOG INPUT

Analog Input Ranges

The AD7715 contains a differential analog input pair AIN(+) and AIN(−). This input pair provides a programmable-gain, differential input channel which can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN(−) input of the input pair.

In unbuffered mode, the common-mode range of the input is from AGND to AV_{DD} provided that the absolute value of the analog input voltage lies between AGND − 30 mV and AV_{DD} + 30 mV. This means that in unbuffered mode the part can handle both unipolar and bipolar input ranges for all gains. In buffered mode, the analog inputs can handle much larger source impedances but the absolute input voltage range is restricted to between AGND + 50 mV to AV_{DD} − 1.5 V, which also places restrictions on the common-mode range. This means that in buffered mode there are some restrictions on the allowable gains for bipolar input ranges. Care must be taken in setting up the common-mode voltage and input voltage range so that the above limits are not exceeded, otherwise there is a degradation in linearity performance.

In unbuffered mode, the analog inputs look directly into the input sampling capacitor, C_{SAMP}. The dc input leakage current in this unbuffered mode is 1 nA maximum. As a result, the analog inputs see a dynamic load that is switched at the input sample rate (see Figure 5). This sample rate depends on master clock frequency and selected gain. C_{SAMP} is charged to AIN(+) and discharged to AIN(−) every input sample cycle. The effective on-resistance of the switch, R_{SW}, is typically 7 kΩ.

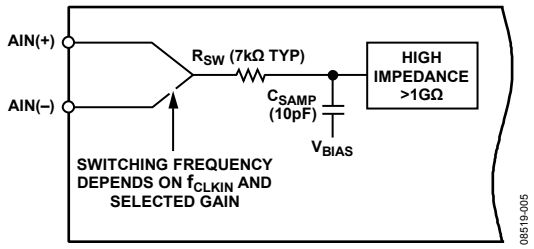


Figure 5. Unbuffered Analog Input Structure

C_{SAMP} must be charged through R_{SW} and through any external source impedances every input sample cycle. Therefore, in unbuffered mode, source impedances mean a longer charge time for C_{SAMP}, and this may result in gain errors on the part. Table 24 shows the allowable external resistance/capacitance values, for unbuffered mode, such that no gain error to the 16-bit level is introduced on the part. Note that these capacitances are total capacitances on the analog input, external capacitance plus 10 pF capacitance from the pins and lead frame of the device.

Table 24. External R, C Combination for No 16-Bit Gain Error (Unbuffered Mode Only)

	External Capacitance (pF)					
Gain	**10**	**50**	**100**	**500**	**1000**	**5000**
1	152 kΩ	53.9 kΩ	31.4 kΩ	8.4 kΩ	4.76 kΩ	1.36 kΩ
2	75.1 kΩ	26.6 kΩ	15.4 kΩ	4.14 kΩ	2.36 kΩ	670 Ω
32	16.7 kΩ	5.95 kΩ	3.46 kΩ	924 Ω	526 Ω	150 Ω
128	16.7 kΩ	5.95 kΩ	3.46 kΩ	924 Ω	526 Ω	150 Ω

In buffered mode, the analog inputs look into the high impedance inputs stage of the on-chip buffer amplifier. C_{SAMP} is charged via this buffer amplifier such that source impedances do not affect the charging of C_{SAMP}. This buffer amplifier has an offset leakage current of 1 nA. In this buffered mode, large source impedances result in a small dc offset voltage developed across the source impedance but not in a gain error.

Input Sample Rate

The modulator sample frequency for the AD7715 remains at $f_{CLK\ IN}/128$ (19.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz) regardless of the selected gain. However, gains greater than 1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table 25). In buffered mode, the input is buffered before the input sampling capacitor. In unbuffered mode, where the analog input looks directly into the sampling capacitor, the effective input impedance is $1/C_{SAMP} \times f_S$ where C_{SAMP} is the input sampling capacitance and f_S is the input sample rate.

Table 25. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/64$ (38.4 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
2	$2 \times f_{CLK\ IN}/64$ (76.8 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
32	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
128	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)

Bipolar/Unipolar Inputs

The analog input on the AD7715 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages on its analog input since the analog input cannot go more negative than −30 mV to ensure correct operation of the part. The input channel is fully differential. As a result, the voltage to which the unipolar and bipolar signals on the AIN(+) input are referenced is the voltage on the respective AIN(−) input. For example, if AIN(−) is 2.5 V and the AD7715 is configured for unipolar operation with a gain of 2 and a V_{REF} of 2.5 V, the input voltage range on the AIN(+) input is 2.5 V to 3.75 V. If AIN(−) is 2.5 V and the AD7715 is configured for bipolar mode with a gain of 2 and a V_{REF} of 2.5 V, the analog input range on the AIN(+) input is 1.25 V to 3.75 V (that is, 2.5 V ± 1.25 V). If AIN(−) is at AGND, the part cannot be configured for bipolar ranges in excess of ±30 mV.

Bipolar or unipolar options are chosen by programming the B/U bit of the setup register. This programs the channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding and the points on the transfer function where calibrations occur.

REFERENCE INPUT

The reference inputs of the AD7715, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The nominal reference voltage, V_{REF} (REF IN(+) − REF IN(−)), for specified operation is 2.5 V for the AD7715-5 and 1.25 V for the AD7715-3. The part is functional with V_{REF} voltages down to 1 V but with degraded performance as the output noise will, in terms of LSB size, be larger. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7715.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs in unbuffered mode. The maximum dc input leakage current is ±1 nA over temperature and source resistance may result in gain errors on the part. In this case, the sampling switch resistance is 5 kΩ typical and the reference capacitor (C_{REF}) varies with gain. The sample rate on the reference inputs is $f_{CLK\ IN}/64$ and does not vary with gain. For gains of 1 and 2, C_{REF} is 8 pF; for a gain of 32, it is 4.25 pF, and for a gain of 128, it is 3.3125 pF.

The output noise performance outlined in Table 15 through Table 22 is for an analog input of 0 V which effectively removes the effect of noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7715. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7715. In applications where the excitation voltage for the bridge transducer on the analog input also derives the reference voltage for the part, the effect of the noise in the excitation voltage will be removed as the application is ratiometric. Recommended reference voltage sources for the AD7715-5 include the AD780, REF43 and REF192, while the recommended reference sources for the AD7715-3 include the AD589 and AD1580. It is generally recommended to decouple the output of these references to further reduce the noise level.

DIGITAL FILTERING

The AD7715 contains an on-chip low-pass digital filter that processes the output of the part's Σ-Δ modulator. Therefore, the part not only provides the analog-to-digital conversion function but it also provides a level of filtering. Users should be aware that there are a number of system differences when the filtering function is provided in the digital domain rather than the analog domain.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Also, the digital filter can be made programmable far more readily than an analog filter. Depending on the digital filter design, this gives the user the capability of programming cutoff frequency and output update rate.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7715 has overrange headroom built into the Σ-Δ modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This provides an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

In addition, the digital filter does not provide any rejection at integer multiples of the digital filter's sample frequency. However, the input sampling on the part provides attenuation at multiples of the digital filter's sampling frequency so that the unattenuated bands actually occur around multiples of the sampling frequency f_S (as defined in Table 25). Thus the unattenuated bands occur at $n \times f_S$ (where n = 1, 2, 3 …). At these frequencies, there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is the cutoff frequency of the digital filter) at either side where noise passes unattenuated to the output.

Filter Characteristics

The AD7715's digital filter is a low-pass filter with a (sinx/x)^3 response (also called sinc^3). The transfer function for this filter is described in the z-domain by

$$H(z) = \left[\frac{1}{N} \times \frac{1 - z^{-N}}{1 - z^{-1}}\right]^3$$

and in the frequency domain by

$$|H(f)| = \left|\frac{1}{N} \times \frac{Sin\left(N \times \pi \times \frac{f}{f_S}\right)}{Sin\left(\pi \times \frac{f}{f_S}\right)}\right|^3$$

where N is the ratio of the modulator rate to the output rate and f_{MOD} is the modulator rate.

Figure 6 shows the filter frequency response for a cutoff frequency of 15.72 Hz which corresponds to a first filter notch frequency of 60 Hz. The plot is shown from dc to 390 Hz. This response is repeated at either side of the digital filter's sample frequency and at either side of multiples of the filter's sample frequency.

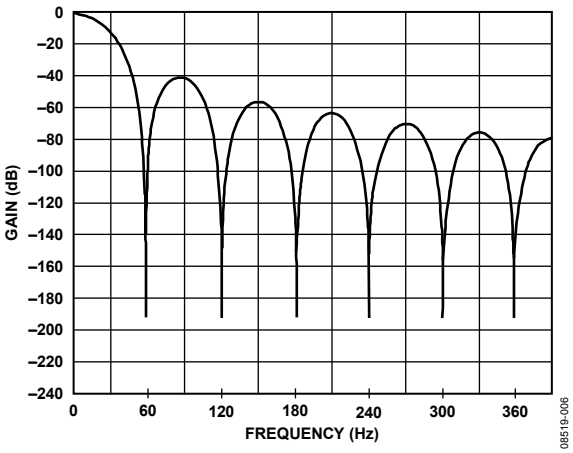


Figure 6. Frequency Response of AD7715 Filter

The response of the filter is similar to that of an averaging filter but with a sharper roll-off. The output rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Thus, for the plot of Figure 6 where the output rate is 60 Hz, the first notch of the filter is at 60 Hz. The notches of this (sinx/x)^3 filter are repeated at multiples of the first notch. The filter provides attenuation of better than 100 dB at these notches.

The cutoff frequency of the digital filter is determined by the value loaded to the FS0 to FS1 bits in the setup register. programming a different cutoff frequency via FS0 and FS1 does not alter the profile of the filter response; it changes the frequency of the notches. The output update of the part and the frequency of the first notch correspond.

Because the AD7715 contains this on-chip, low-pass filtering, there is a settling time associated with step function inputs and data on the output is invalid after a step change until the settling time has elapsed. The settling time depends upon the output rate chosen for the filter. The settling time of the filter to a full-scale step input can be up 4 times the output data period. For a synchronized step input (using the FSYNC function), the settling time is 3 times the output data period.

Post-Filtering

The on-chip modulator provides samples at a 19.2 kHz output rate with $f_{CLK\,IN}$ at 2.4576 MHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Because the output data rate is higher than the Nyquist criterion, the output rate for a given bandwidth satisfys most application requirements. However, there may be some applications that require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate do require some post-filtering following the digital filter of the AD7715.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7715 at the 100 Hz rate giving a –3 dB bandwidth of 26.2 Hz. Post-filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post-filtering can also be used to reduce the output noise from the device for bandwidths below 13.1 Hz. At a gain of 128 and a bandwidth of 13.1 Hz, the output rms noise is 520 nV. This is essentially device noise or white noise and because the input is chopped, the noise has a primarily flat frequency response. By reducing the bandwidth below 13.1 Hz, the noise in the resultant pass-band can be reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately 1.25 in the output rms noise. This additional filtering results in a longer settling time.

ANALOG FILTERING

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency, as outlined earlier. However, due to the high oversampling ratio of AD7715, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. This means that the analog filtering requirements in front of the AD7715 are considerably reduced vs. a conventional converter with no on-chip filtering. In addition, because the part's common-mode rejection performance of 95 dB extends out to several kilohertz, common-mode noise in this frequency range is substantially reduced.

Depending on the application, however, it may be necessary to provide attenuation in front of the AD7715 to eliminate unwanted frequencies from these bands which the digital filter will pass. It may also be necessary in some applications to provide analog filtering in front of the AD7715 to ensure that differential noise signals outside the band of interest do not saturate the analog modulator.

If passive components are placed in front of the AD7715, in unbuffered mode, take care to ensure that the source impedance is low enough so as not to introduce gain errors in the system. This significantly limits the amount of passive antialiasing filtering which can be provided in front of the AD7715 when it is used in unbuffered mode. However, when the part is used in buffered mode, large source impedances simply result in a small dc offset error (a 10 kΩ source resistance causes an offset error of less than 10 μV). Therefore, if the system requires any significant source impedances to provide passive analog filtering in front of the AD7715, it is recommended that the part be operated in buffered mode.

CALIBRATION

The AD7715 provides a number of calibration options that can be programmed via the MD1 and MD0 bits of the setup register. The different calibration options are outlined in the setup register and calibration sequences sections. A calibration cycle may be initiated at any time by writing to the MD1 and MD0 bits of the setup register. Calibration on the AD7715 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch or bipolar/unipolar input range.

The AD7715 offers self-calibration and system-calibration facilities. For full calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are zero-scale and full-scale points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. As a result, the accuracy of the calibration can only be as good as the noise level that it provides in normal mode. The result of the zero-scale calibration conversion is stored in the zero-scale calibration register while the result of the full-scale calibration conversion is stored in the full-scale calibration register. With these readings, the on-chip microcontroller can calculate the offset and the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of 16 bits.

Self-Calibration

A self-calibration is initiated on the AD7715 by writing the appropriate values (0, 1) to the MD1 and MD0 bits of the setup register. In the self-calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is with the inputs of the differential pair internally shorted on the part (that is, AIN(+) = AIN(−) = internal bias voltage). The PGA is set for the selected gain (as per G1 and G0 bits in the communications register) for this zero-scale calibration conversion. The full-scale calibration conversion is performed at the selected gain on an internally generated voltage of V_{REF}/selected gain.

The duration time for the calibration is 6 × 1/output rate. This is made up of 3 × 1/output rate for the zero-scale calibration and 3 × 1/output rate for the full-scale calibration. At this time, the MD1 and MD0 bits in the setup register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 9 × 1/output rate. This is made up of 3 × 1/output rate for the zero-scale calibration, 3 × 1/output rate for the full-scale calibration, 3 × 1/output rate for a conversion on the analog input and some overhead to set up the coefficients correctly. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command write to the setup register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit is written to the setup register in the calibration command.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points are exactly the same as above, but because the part is configured for bipolar operation, the shorted inputs point is actually midscale of the transfer function.

System Calibration

System calibration allows the AD7715 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self calibration but uses voltage values presented by the system to the AIN inputs for the zero- and full-scale points. full system calibration requires a two step process, a zero-scale system calibration followed by a full-scale system calibration.

For a full system calibration, the zero-scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. Once the system zero scale voltage has been set up, a zero-scale system calibration is then initiated by writing the appropriate values (1, 0) to the MD1 and MD0 bits of the setup register. The zero-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/output rate. At this time, the MD1 and MD0 bits in the setup register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 4 × 1/output rate as the part performs a normal conversion on the AIN voltage before $\overline{\text{DRDY}}$ goes low. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command write to the setup register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit is written to the setup register in the calibration command.

After the zero-scale point is calibrated, the full-scale point is applied to AIN and the second step of the calibration process is initiated by again writing the appropriate values (1, 1) to MD1 and MD0. Again, the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. The full-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/output rate. At this time, the MD1 and MD0 bits in the setup register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 4 × 1/output rate as the part performs a normal conversion on the AIN voltage before $\overline{\text{DRDY}}$ goes low. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command, write to the setup register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit is written to the setup register in the calibration command.

In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function. In the bipolar mode, it is performed between midscale (zero differential voltage) and positive full scale.

The fact that the system calibration is a two-step calibration offers another feature. After the sequence of a full system calibration has been completed, additional offset or gain calibrations can be performed by themselves to adjust the system zero reference point or the system gain. Calibrating one of the parameters, either system offset or system gain, does not affect the other parameter.

System calibration can also be used to remove any errors from source impedances on the analog input when the part is used in unbuffered mode. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage but the system calibration can be used to remove this error.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span which can be accommodated. The overriding requirement in determining the amount of offset and gain that can be accommodated by the part is the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}/GAIN$. This allows the input range to go 5% above the nominal range. The in-built headroom in the analog modulator of the AD7715 ensures that the part still operates correctly with a positive full-scale voltage which is 5% beyond the nominal.

The range of input span in both the unipolar and bipolar modes has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$. However, the span (which is the difference between the bottom of the AD7715's input range and the top of its input range) must take into account the limitation on the positive full-scale voltage. The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. Once again, the offset must take into account the limitation on the positive full-scale voltage. In unipolar mode, there is considerable flexibility in handling negative (with respect to AIN(–)) offsets. In both unipolar and bipolar modes, the range of positive offsets which can be handled by the part depends on the selected span. Therefore, in determining the limits for system zero-scale and full-scale calibrations, the user has to ensure that the offset range plus the span range does exceed $1.05 \times V_{REF}/GAIN$. This is best illustrated by looking at the following examples.

If the part is used in unipolar mode with a required span of $0.8 \times V_{REF}/GAIN$, then the offset range which the system calibration can handle is from $-1.05 \times V_{REF}/GAIN$ to $+0.25 \times V_{REF}/GAIN$. If the part is used in unipolar mode with a required span of $V_{REF}/GAIN$, then the offset range which the system calibration can handle is from $-1.05 \times V_{REF}/GAIN$ to $+0.05 \times V_{REF}/GAIN$. Similarly, if the part is used in unipolar mode and required to remove an offset of $0.2 \times V_{REF}/GAIN$, then the span range which the system calibration can handle is $0.85 \times V_{REF}/GAIN$.

If the part is used in bipolar mode with a required span of $\pm 0.4 \times V_{REF}/GAIN$, then the offset range which the system calibration can handle is from $-0.65 \times V_{REF}/GAIN$ to $+0.65 \times V_{REF}/GAIN$. If the part is used in bipolar mode with a required span of $\pm V_{REF}/GAIN$, then the offset range which the system calibration can handle is from $-0.05 \times V_{REF}/GAIN$ to $+0.05 \times V_{REF}/GAIN$. Similarly, if the part is used in bipolar mode and required to remove an offset of $\pm 0.2 \times V_{REF}/GAIN$, then the span range which the system calibration can handle is $\pm 0.85 \times V_{REF}/GAIN$.

Power-Up and Calibration

On power-up, the AD7715 performs an internal reset that sets the contents of the internal registers to a known state. There are default values loaded to all registers after a power-on or reset. The default values contain nominal calibration coefficients for the calibration registers. However, to ensure correct calibration for the device a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7715 are low, and no warm-up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated. Similarly, if the clock source for the part is generated from a crystal or resonator across the MCLK pins, the start-up time for the oscillator circuit should elapse before a calibration is initiated on the part (see the Clocking and Oscillator Circuit section).

USING THE AD7715

CLOCKING AND OSCILLATOR CIRCUIT

The AD7715 requires a master clock input, which may be an external CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal or ceramic resonator of the correct frequency can be connected between MCLK IN and MCLK OUT in which case the clock circuit functions as an oscillator, providing the clock source for the part. The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate, and double the calibration time. The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but does not affect the current drawn from the AV_{DD} power supply.

Using the part with a crystal or ceramic resonator between the MCLK IN and MCLK OUT pins generally causes more current to be drawn from DV_{DD} than when the part is clocked from a driven clock signal at the MCLK IN pin. This is because the on-chip oscillator circuit is active in the case of the crystal or ceramic resonator. Therefore, the lowest possible current on the AD7715 is achieved with an externally applied clock at the MCLK IN pin with MCLK OUT unconnected and unloaded.

The amount of additional current taken by the oscillator depends on a number of factors—first, the larger the value of capacitor placed on the MCLK IN and MCLK OUT pins, then the larger the DV_{DD} current consumption on the AD7715. Take care not to exceed the capacitor values recommended by the crystal and ceramic resonator manufacturers to avoid consuming unnecessary DV_{DD} current. Typical values recommended by crystal or ceramic resonator manufacturers are in the range of 30 pF to 50 pF, and if the capacitor values on MCLK IN and MCLK OUT are kept in this range, they will not result in any excessive DV_{DD} current. Another factor that influences the DV_{DD} current is the effective series resistance (ESR) of the crystal which appears between the MCLK IN and MCLK OUT pins of the AD7715. As a general rule, the lower the ESR value then the lower the current taken by the oscillator circuit.

When operating with a clock frequency of 2.4576 MHz, there is 50 µA difference in the DV_{DD} current between an externally applied clock and a crystal resonator when operating with a DV_{DD} of 3 V. With DV_{DD} = 5 V and $f_{CLK\ IN}$ = 2.4576 MHz, the typical DV_{DD} current increases by 200 µA for a crystal/resonat or supplied clock vs. an externally applied clock. The ESR values for crystals and resonators at this frequency tend to be low and as a result there tends to be little difference between different crystal and resonator types.

When operating with a clock frequency of 1 MHz, the ESR value for different crystal types varies significantly. As a result, the DV_{DD} current drain varies across crystal types. When using a crystal with an ESR of 700 Ω or when using a ceramic resonator, the increase in the typical DV_{DD} current over an externally-applied clock is 50 µA with DV_{DD} = 3 V and 175 µA with DV_{DD} = 5 V. When using a crystal with an ESR of 3 kΩ, the increase in the typical DV_{DD} current over an externally applied clock is 100 µA with DV_{DD} = 3 V and 400 µA with DV_{DD} = 5 V.

The on-chip oscillator circuit also has a start-up time associated with it before it is oscillating at its correct frequency and correct voltage levels. The typical start-up time for the circuit is 10 ms with a DV_{DD} of 5 V and 15 ms with a DV_{DD} of 3 V. At 3 V supplies, depending on the loading capacitances on the MCLK pins, a 1 MΩ feedback resistor may be required across the crystal or resonator to keep the start up times around the 15 ms duration.

The master clock of AD7715 appears on the MCLK OUT pin of the device. The maximum recommended load on this pin is one CMOS load. When using a crystal or ceramic resonator to generate the clock of the AD7715, it may be desirable to then use this clock as the clock source for the system. In this case, it is recommended that the MCLK OUT signal is buffered with a CMOS buffer before being applied to the rest of the circuit.

SYSTEM SYNCHRONIZATION

The FSYNC bit of the setup register allows the user to reset the modulator and digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, that is, when the FSYNC is changed from 1 to 0.

With a 1 in the FSYNC bit of the setup register, the digital filter and analog modulator are held in a known reset state and the part is not processing any input samples. When a 0 is then written to the FSYNC bit, the modulator and filter are taken out of this reset state and on the next master clock edge the part starts to gather samples again.

The FSYNC input can also be used as a software start convert command allowing the AD7715 to be operated in a conventional converter fashion. In this mode, writing to the FSYNC bit starts a conversion and the falling edge of $\overline{DRDY}$ indicates when the conversion is complete. The disadvantage of this scheme is that the settling time of the filter has to be taken into account for every data register update. This means that the rate at which the data register is updated is three times slower in this mode.

Because the FSYNC bit resets the digital filter, the full settling time of 3 × 1/output rate must elapse before there is a new word loaded to the output register on the part. If the DRDY signal is low when FSYNC goes to a 0, the DRDY signal will not be reset high by the FSYNC command. This is because the AD7715 recognizes that there is a word in the data register that has not been read. The DRDY line stays low until an update of the data register takes place at which time it goes high for 500 × $t_{CLK\ IN}$ before returning low again. A read from the data register resets the DRDY signal high, and it does not return low until the settling time of the filter has elapsed (from the FSYNC command) and there is a valid new word in the data register. If the DRDY line is high when the FSYNC command is issued, the DRDY line will not return low until the settling time of the filter has elapsed.

RESET INPUT

The RESET input on the AD7715 resets all the logic, the digital filter, and the analog modulator while all on-chip registers are reset to their default state. DRDY is driven high and the AD7715 ignores all communications to any of its registers while the RESET input is low. When the RESET input returns high, the AD7715 starts to process data, and DRDY returns low in 3 × 1/output rate indicating a valid new word in the data register. However, the AD7715 operates with its default setup conditions after a reset and it is generally necessary to set up all registers and carry out a calibration after a reset command.

The on-chip oscillator circuit of the AD7715 continues to function even when the RESET input is low. The master clock signal continues to be available on the MCLK OUT pin. Therefore, in applications where the system clock is provided by the clock of the AD7715, the AD7715 produces an uninterrupted master clock during RESET commands.

STANDBY MODE

The STBY bit in the communications register of the AD7715 allows the user to place the part in a power-down mode when it is not required to provide conversion results. The AD7715 retains the contents of all its on-chip registers (including the data register) while in standby mode. When released from standby mode, the part starts to process data and a new word is available in the data register in 3 × 1/output rate from when a 0 is written to the STBY bit.

The STBY bit does not affect the digital interface, and it does not affect the status of the DRDY line. If DRDY is high when the STBY bit is brought low, it will remain high until there is a valid new word in the data register. If DRDY is low when the STBY bit is brought low, it will remain low until the data register is updated at which time the DRDY line returns high for 500 × $t_{CLK\ IN}$ before returning low again. If DRDY is low when the part enters its standby mode (indicating a valid unread word in the data register), the data register can be read while the part is in standby. At the end of this read operation, the DRDY line will be reset high as normal.

Placing the part in standby mode reduces the total current to 5 μA typical when the part is operated from an external master clock provided this master clock is stopped. If the external clock continues to run in standby mode, the standby current increases to 150 μA typical with 5 V supplies and 75 μA typical with 3.3 V supplies. If a crystal or ceramic resonator is used as the clock source, then the total current in standby mode is 400 μA typical with 5 V supplies and 90 μA with 3.3 V supplies. This is because the on-chip oscillator circuit continues to run when the part is in its standby mode. This is important in applications where the system clock is provided by the clock of the AD7715, so that the AD7715 produces an uninterrupted master clock even when it is in its standby mode.

ACCURACY

Σ-Δ ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7715 achieves excellent linearity by the use of high quality, on-chip capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7715 uses digital calibration techniques which minimize offset and gain error.

DRIFT CONSIDERATIONS

The AD7715 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES

There is no specific power sequence required for the AD7715; either the AV_{DD} or the DV_{DD} supply can come up first. While the latch-up performance of the AD7715 is good, it is important that power is applied to the AD7715 before signals at REF IN, AIN, or the logic input pins to avoid excessive currents. If this is not possible, then the current that flows in any of these pins should be limited. If separate supplies are used for the AD7715 and the system digital circuitry, then the AD7715 should be powered up first. If it is not possible to guarantee this, then current limiting resistors should be placed in series with the logic inputs to again limit the current.

During normal operation the AD7715 analog supply (AV_{DD}) should always be greater than or equal to its digital supply (DV_{DD}).

Supply Current

The current consumption on the AD7715 is specified for supplies in the range 3 V to 3.6 V and in the range 4.75 V to 5.25 V. The part operates over a 2.85 V to 5.25 V supply range and the I_{DD} for the part varies as the supply voltage varies over this range. Figure 7 shows the variation of the typical I_{DD} with V_{DD} voltage for both a 1 MHz external clock and a 2.4576 MHz external clock at 25°C. The AD7715 is operated in unbuffered mode. The relationship shows that the I_{DD} is minimized by operating the part with lower V_{DD} voltages. I_{DD} on the AD7715 is also minimized by using an external master clock or by optimizing external components when using the on-chip oscillator circuit.

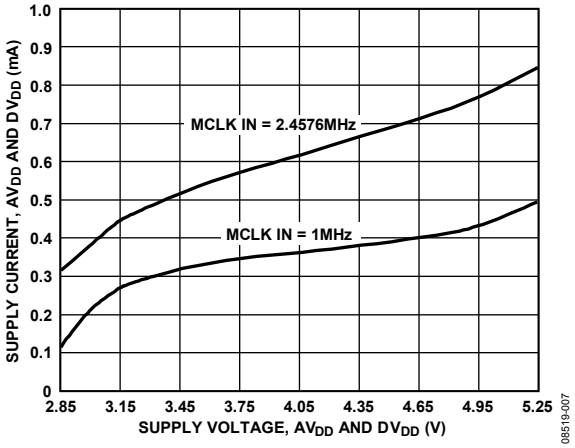


Figure 7. I_{DD} vs. Supply Voltage

Grounding and Layout

Because the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs. The analog and digital supplies to the AD7715 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided those noise sources do not saturate the analog modulator. As a result, the AD7715 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7715 is so high and the noise levels from the AD7715 so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7715 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7715 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7715. If the AD7715 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7715.

Avoid running digital lines under the device as these couples noise onto the die. The analog ground plane should be allowed to run under the AD7715 to avoid noise coupling. The power supply lines to the AD7715 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF disc ceramic capacitors to DGND. In systems where a common supply voltage is used to drive both the AV_{DD} and DV_{DD} of the AD7715, it is recommended that the AV_{DD} supply of the system is used. This supply should have the recommended analog supply decoupling capacitors between the AV_{DD} pin of the AD7715 and AGND and the recommended digital supply decoupling capacitor between the DV_{DD} pin of the AD7715 and DGND.

Evaluating the AD7715 Performance

The recommended layout for the AD7715 is outlined in the evaluation board for the AD7715. The evaluation board package includes a fully assembled and tested evaluation board, documentation, software for controlling the board over the USB port of a PC and software for analyzing the performance of the AD7715 on the PC. The evaluation board model number is EVAL-AD7715-3EBZ .

Noise levels in the signals applied to the AD7715 may also affect performance of the part. The AD7715 software evaluation package allows the user to evaluate the true performance of the part, independent of the analog input signal. The scheme involves using a test mode on the part where the differential inputs to the AD7715 are internally shorted together to provide a zero differential voltage for the analog modulator. External to the device, connect the AIN(−) input to a voltage which is within the allowable common-mode range of the part. This scheme should be used after a calibration has been performed on the part.

DIGITAL INTERFACE

The programmable functions of the AD7715 are controlled using a set of on-chip registers as outlined previously. Data is written to these registers via the serial interface of the part and read access to the on-chip registers is also provided by this interface. All communications to the part must start with a write operation to the communications register. After power-on or RESET, the device expects a write to its communications register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the communications register followed by a write to the selected register. A read operation from any other register on the part (including the output data register) starts with a write operation to the communications register followed by a read operation from the selected register.

The serial interface of the AD7715 consists of five signals, $\overline{CS}$, SCLK, DIN, DOUT, and $\overline{DRDY}$. The DIN line is used for transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the data register of the AD7715. $\overline{DRDY}$ goes low when a new data word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select the device. It can be used to decode the AD7715 in systems where a number of parts are connected to the serial bus.

Figure 8 and Figure 9 show timing diagrams for interfacing to the AD7715 with $\overline{CS}$ used to decode the part. Figure 8 is for a read operation from the AD7715's output shift register, while Figure 9 shows a write operation to the input shift register. It is possible to read the same data twice from the output register even though the $\overline{DRDY}$ line returns high after the first read operation. Take care, however, to ensure that the read operations have been completed before the next output update is about to take place.

The AD7715 serial interface can operate in three-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN and DOUT lines are used to communicate with the AD7715 and the status of $\overline{DRDY}$ can be obtained by interrogating the MSB of the communications register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that the SCLK idles high between data transfers.

The AD7715 can also be operated with $\overline{CS}$ used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$ because $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided the timing numbers are obeyed.

The serial interface can be reset by exercising the $\overline{RESET}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7715 DIN line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in three-wire systems that if the interface gets lost either via a software error or by some glitch in the system, it can be reset back into a known state. This state returns the interface to where the AD7715 is expecting a write operation to its communications register. This operation in itself does not reset the contents of any registers, but because the interface was lost, the information that was written to any of the registers is unknown and it is advisable to set up all registers again.

Some microprocessor or microcontroller serial interfaces have a single serial data line. In this case, it is possible to connect the DOUT and DIN lines of the AD7715 together and connect them to the single data line of the processor. A 10 kΩ pull-up resistor should be used on this single data line. In this case, if the interface gets lost, because the read and write operations share the same line the procedure to reset it back to a known state is somewhat different than described previously. It requires a read operation of 24 serial clocks followed by a write operation where a Logic 1 is written for at least 32 serial clock cycles to ensure that the serial interface is back into a known state.

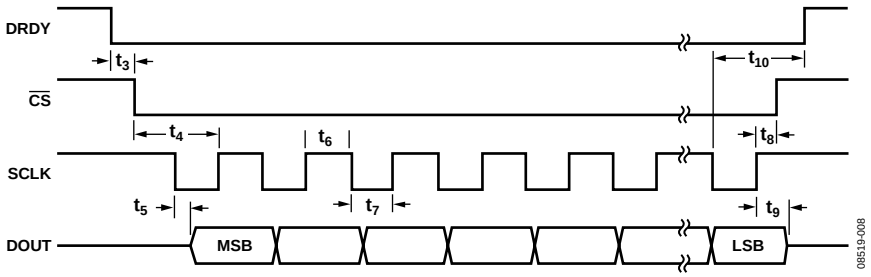


Figure 8. Read Cycle Timing Diagram

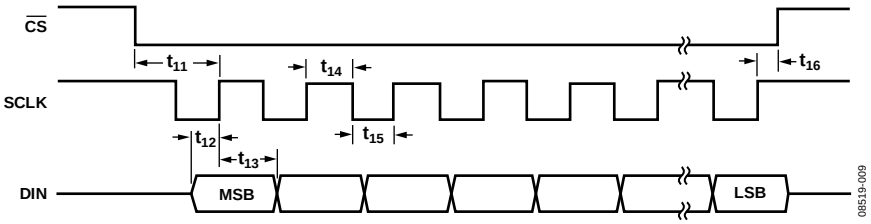


Figure 9. Write Cycle Timing Diagram

CONFIGURING THE AD7715

The AD7715 contains three on-chip registers which the user accesses via the serial interface. Communication with any of these registers is initiated by writing to the communications register first. Figure 10 outlines a flow chart of the sequence which is used to configure all registers after a power-up or reset. The flowchart also shows two different read options—the first where the $\overline{\text{DRDY}}$ pin is polled to determine when an update of the data register has taken place, the second where the $\overline{\text{DRDY}}$ bit of the communications register is interrogated to see if a data register update has taken place. Also included in the flowing diagram is a series of words which should be written to the registers for a particular set of operating conditions. These conditions are gain of 1, no filter sync, bipolar mode, buffer off, clock of 2.4576 MHz, and an output rate of 60 Hz.

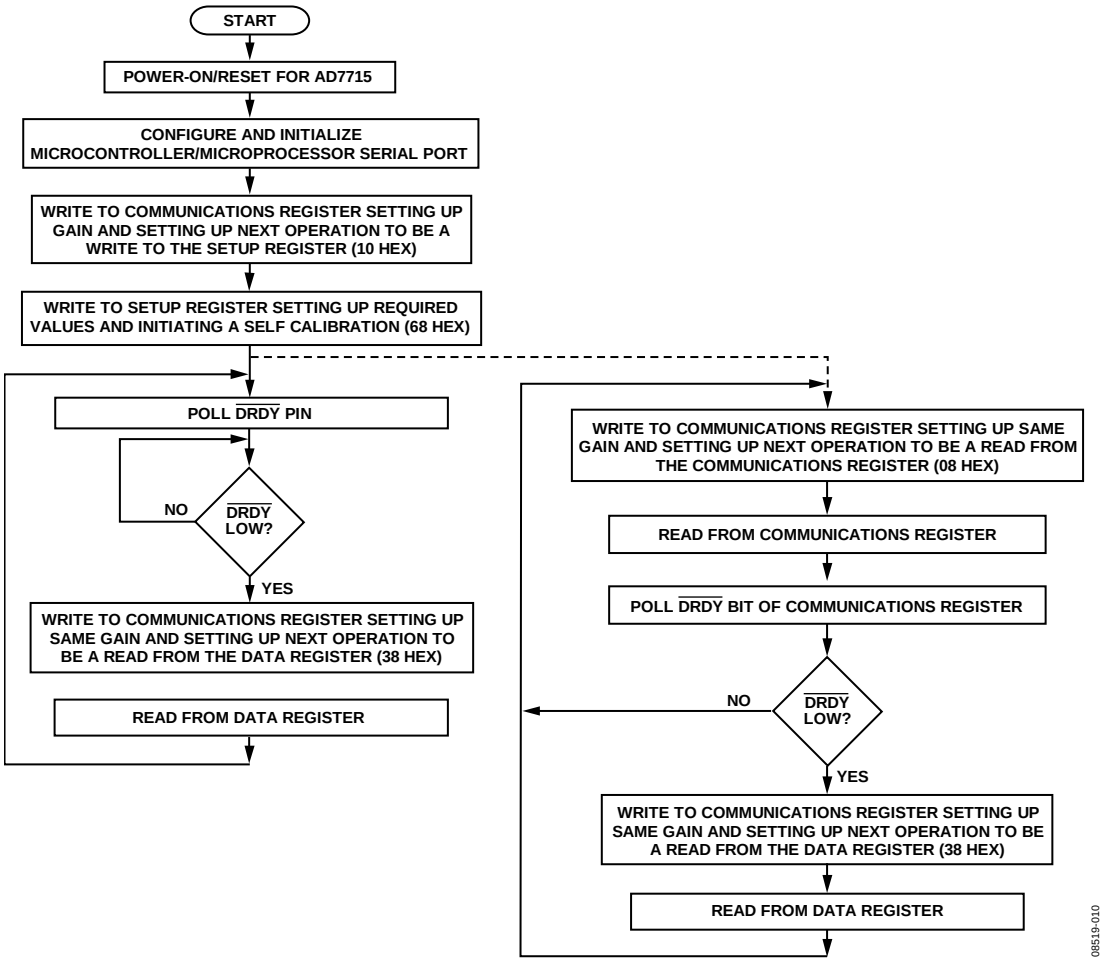


Figure 10. Flow Chart for Setting Up and Reading from the AD7715

MICROCONTROLLER/MICROPROCESSOR INTERFACING

The flexible serial interface of the AD7715 allows for easy interface to most microcontrollers and microprocessors. The flow chart of Figure 10 outlines the sequence which should be followed when interfacing a microcontroller or microprocessor to the AD7715. Figure 11, Figure 12, and Figure 13 show some typical interface circuits.

The serial interface on the AD7715 has the capability of operating from just three wires and is compatible with SPI interface protocols. The three-wire operation makes the part ideal for isolated systems where minimizing the number of interface lines minimizes the number of opto-isolators required in the system. The rise and fall times of the digital inputs to the AD7715 (especially the SCLK input) should be no longer than 1 µs.

Most of the registers on the AD7715 are 8-bit registers. This facilitates easy interfacing to the 8-bit serial ports of microcontrollers. Some of the registers on the part are up to 16 bits, but data transfers to these 16-bit registers can consist of a full 16-bit transfer or two 8-bit transfers to the serial port of the microcontroller. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7715.

Even though some of the registers on the AD7715 are only eight bits in length, communicating with two of these registers in successive write operations can be handled as a single 16-bit data transfer if required. For example, if the setup register is to be updated, the processor must first write to the communications register (saying that the next operation is a write to the setup register) and then write eight bits to the setup register. This can all be done in a single 16-bit transfer if required because once the eight serial clocks of the write operation to the communications register have been completed, the part immediately sets itself up for a write operation to the setup register.

AD7715 TO 68HC11 INTERFACE

Figure 11 shows an interface between the AD7715 and the 68HC11 microcontroller. The diagram shows the minimum (three-wire) interface with $\overline{CS}$ on the AD7715 hardwired low. In this scheme, the $\overline{DRDY}$ bit of the communications register is monitored to determine when the data register is updated. An alternative scheme, which increases the number of interface lines to four, is to monitor the $\overline{DRDY}$ output line from the AD7715. The monitoring of the $\overline{DRDY}$ line can be done in two ways. First, $\overline{DRDY}$ can be connected to one of the 68HC11's port bits (such as PC0) which is configured as an input. This port bit is then polled to determine the status of $\overline{DRDY}$. The second scheme is to use an interrupt driven system, in which case the $\overline{DRDY}$ output is connected to the $\overline{IRQ}$ input of the 68HC11. For interfaces that require control of the $\overline{CS}$ input on the AD7715, one of the port bits of the 68HC11 (such as PC1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

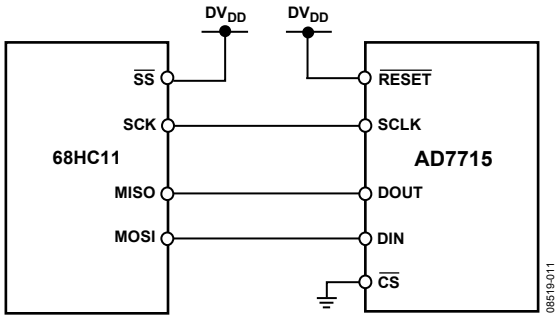


Figure 11. AD7715 to 68HC11 Interface

The 68HC11 is configured in the master mode with its CPOL bit set to a Logic 1 and its CPHA bit set to a Logic 1. When the 68HC11 is configured like this, its SCLK line idles high between data transfers. The AD7715 is not capable of full duplex operation. If the AD7715 is configured for a write operation, no data appears on the DOUT lines even when the SCLK input is active. Similarly, if the AD7715 is configured for a read operation, data presented to the part on the DIN line is ignored even when SCLK is active.

Coding for an interface between the 68HC11 and the AD7715 is given in the C Code for Interfacing AD7715 to 68HC11 section. In this example, the $\overline{DRDY}$ output line of the AD7715 is connected to the PC0 port bit of the 68HC11 and is polled to determine its status.

AD7715 TO 8XC51 INTERFACE

An interface circuit between the AD7715 and the 8XC51 microcontroller is shown in Figure 12. The diagram shows the minimum number of interface connections with $\overline{CS}$ on the AD7715 hardwired low. In the case of the 8XC51 interface, the minimum number of interconnects is just two. In this scheme, the $\overline{DRDY}$ bit of the communications register is monitored to determine when the data register is updated. The alternative scheme, which increases the number of interface lines to three, is to monitor the $\overline{DRDY}$ output line from the AD7715. The monitoring of the $\overline{DRDY}$ line can be done in two ways. First, $\overline{DRDY}$ can be connected to one of the 8XC51's port bits (such as P1.0) which is configured as an input. This port bit is then polled to determine the status of $\overline{DRDY}$. The second scheme is to use an interrupt driven system in which case, the $\overline{DRDY}$ output is connected to the $\overline{INT1}$ input of the 8XC51. For interfaces that require control of the $\overline{CS}$ input on the AD7715, one of the port bits of the 8XC51 (such as P1.1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

The 8XC51 is configured in its Mode 0 serial interface mode. Its serial interface contains a single data line. As a result, the DOUT and DIN pins of the AD7715 should be connected together with a 10 kΩ pull-up resistor. The serial clock on the 8XC51 idles high between data transfers. The 8XC51 outputs the LSB first in a write operation while the AD7715 rearranged before being written to the output serial register. Similarly, the AD7715 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data which is read into the serial buffer needs to be rearranged before the correct data word from the AD7715 is available in the accumulator.

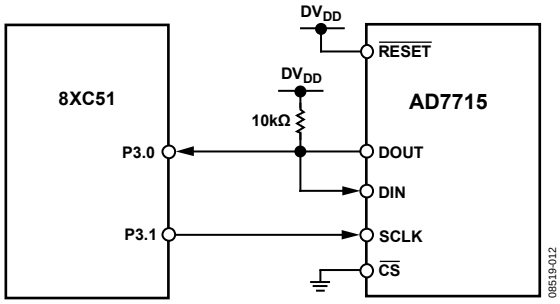


Figure 12. AD7715 to 8XC51 Interface

AD7715 TO ADSP-2184N/ADSP-2185N/ ADSP-2186N/ADSP-2187N/ADSP-2188N/ ADSP-2189N INTERFACE

Figure 13 shows an interface between the AD7715 and the ADSP-2184N/ADSP-2185N/ADSP-2186N/ADSP-2187N/ ADSP-2188N/ADSP-2189N DSP processor. In the interface shown, the $\overline{DRDY}$ bit of the communications register is monitored to determine when the data register is updated. The alternative scheme is to use an interrupt driven system, in which case the $\overline{DRDY}$ output is connected to the $\overline{IRQ2}$ input of the DSP processor The serial interface of the DSP processor is set up for alternate framing mode. The $\overline{RFS}$ and $\overline{TFS}$ pins of the DSP processor are configured as active low outputs, and the DSP processor serial clock line, SCLK, is also configured as an output. The $\overline{CS}$ for the AD7715 is active when either the $\overline{RFS}$ or $\overline{TFS}$ outputs from the DSP processor are active. The serial clock rate on the DSP processor should be limited to 3 MHz to ensure correct operation with the AD7715.

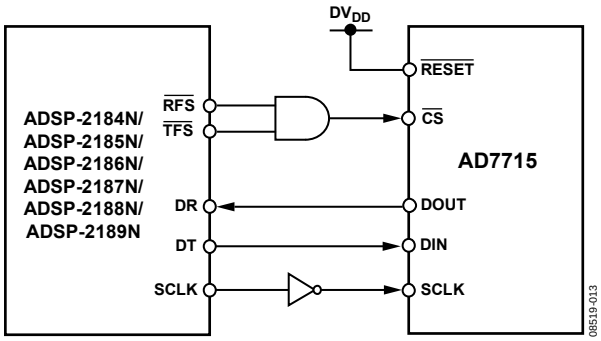


Figure 13. AD7715 to ADSP-2184N/ADSP-2185N/ADSP-2186N/ ADSP-2187N/ADSP-2188N/ADSP-2189N Interface

CODE FOR SETTING UP THE AD7715

The C Code for Interfacing AD7715 to 68HC11 section gives a set of read and write routines in C code for interfacing the 68HC11 microcontroller to the AD7715. The sample program sets up the various registers on the AD7715 and reads 1000 samples from the part into the 68HC11. The setup conditions on the part are exactly the same as those outlined for the flowchart of Figure 10. In the example code given here, the DRDY output is polled to determine if a new valid word is available in the data register.

The sequence of the events in this program are as follows:

1. Write to the communications register, setting the gain to 1 with standby inactive.
2. Write to the setup register, setting bipolar mode, buffer off, no filter synchronization, confirming a clock frequency of 2.4576 MHz, setting the output rate for 60 Hz and initiating a self-calibration.
3. Poll the DRDY output.
4. Read the data from the data register.
5. Loop around doing Step 3 and Step 4 until the specified number of samples have been taken.

C CODE FOR INTERFACING AD7715 TO 68HC11

```
/* This program has read and write routines for the 68HC11 to interface to the AD7715 and the sample
program sets the various registers and then reads 1000 samples from the part. */
#include <math.h>
#include <io6811.h>
#define NUM_SAMPLES 1000 /* change the number of data samples */
#define MAX_REG_LENGTH 2 /* this says that the max length of a register is 2 bytes */
Writetoreg (int);
Read (int,char);
char *datapointer = store;
char store[NUM_SAMPLES*MAX_REG_LENGTH + 30];
void main()
{
        /* the only pin that is programmed here from the 68HC11 is the /CS and this is why the PC2 bit
of PORTC is made as an output */
char a;
DDRC = 0x04; /* PC2 is an output the rest of the port bits are inputs */
PORTC | = 0x04; /* make the /CS line high */
Writetoreg(0x10); /* set the gain to 1, standby off and set the next operation as write to the setup
register */
Writetoreg(0x68); /* set bipolar mode, buffer off, no filter sync, confirm clock as 2.4576MHz, set
output rate to 60Hz and do a self calibration */
while(PORTC & 0x10); /* wait for /DRDY to go low */
for(a=0;a<NUM_SAMPLES;a++);
        {
        Writetoreg(0x38); /*set the next operation for 16 bit read from the data register */
        Read(NUM_SAMPLES,2);
        }
}
Writetoreg(int byteword);
{
int q;
SPCR = 0x3f;
SPCR = 0X7f; /* this sets the WiredOR mode(DWOM=1), Master mode(MSTR=1), SCK idles high(CPOL=1), /SS
can be low always (CPHA=1), lowest clock speed(slowest speed which is master clock /32 */
DDRD = 0x18; /* SCK, MOSI outputs */
q = SPSR;
q = SPDR; /* the read of the staus register and of the data register is needed to clear the interrupt
```

```
which tells the user that the data transfer is complete */
PORTC &= 0xfb; /* /CS is low */
SPDR = byteword; /* put the byte into data register */
while(!(SPSR & 0x80)); /* wait for /DRDY to go low */
PORTC |= 0x4; /* /CS high */
}
Read(int amount, int reglength)
{
int q;
SPCR = 0x3f;
SPCR = 0x7f; /* clear the interrupt */
DDRD = 0x10; /* MOSI output, MISO input, SCK output */
while(PORTC & 0x10); /* wait for /DRDY to go low */
PORTC & 0xfb ; /* /CS is low */
for(b=0;b<reglength;b++)
        {
        SPDR = 0;
        while(!(SPSR & 0x80)); /* wait until port ready before reading */
        *datapointer++=SPDR; /* read SPDR into store array via datapointer */
}
PORTC|=4; /* /CS is high */
}
```

APPLICATIONS INFORMATION

The AD7715 provides a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, it makes the part more immune to noisy environments thus making the part ideal for use in industrial and process control applications. It also provides a programmable gain amplifier, a digital filter and calibration options. Thus, it provides far more system level functionality than off-the-shelf integrating ADCs without the disadvantage of having to supply a high quality integrating capacitor. In addition, using the AD7715 in a system allows the system designer to achieve a much higher level of resolution because noise performance of the AD7715 is significantly better than that of the integrating ADCs.

The on-chip PGA allows the AD7715 to handle an analog input voltage range as low as 10 mV full-scale with V_{REF} = 1.25 V. The differential inputs of the part allow this analog input range to have an absolute value anywhere between AGND and AV_{DD} when the part is operated in unbuffered mode. It allows the user to connect the transducer directly to the input of the AD7715. The programmable gain front end on the AD7715 allows the part to handle unipolar analog input ranges from 0 mV to 20 mV to 0 V to 2.5 V and bipolar inputs of ±20 mV to ±2.5 V. Because the part operates from a single supply, these bipolar ranges are with respect to a biased-up differential input.

PRESSURE MEASUREMENT

One typical application of the AD7715 is pressure measurement. Figure 14 shows the AD7715 used with a pressure transducer, the BP01 from Sensym. The pressure transducer is arranged in a bridge network and gives a differential output voltage between its OUT(+) and OUT(−) terminals. With rated full-scale pressure (in this case 300 mmHg) on the transducer, the differential output voltage is 3 mV/V of the input voltage (that is, the voltage between its IN(+) and IN(−) terminals).

Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 15 mV. The excitation voltage for the bridge is also used to generate the reference voltage for the AD7715. Therefore, variations in the excitation voltage do not introduce errors in the system. Choosing resistor values of 24 kΩ and 15 kΩ as per the diagram give a 1.92 V reference voltage for the AD7715 when the excitation voltage is 5 V.

Using the part with a programmed gain of 128 results in the full-scale input span of the AD7715 being 15 mV which corresponds with the output span from the transducer.

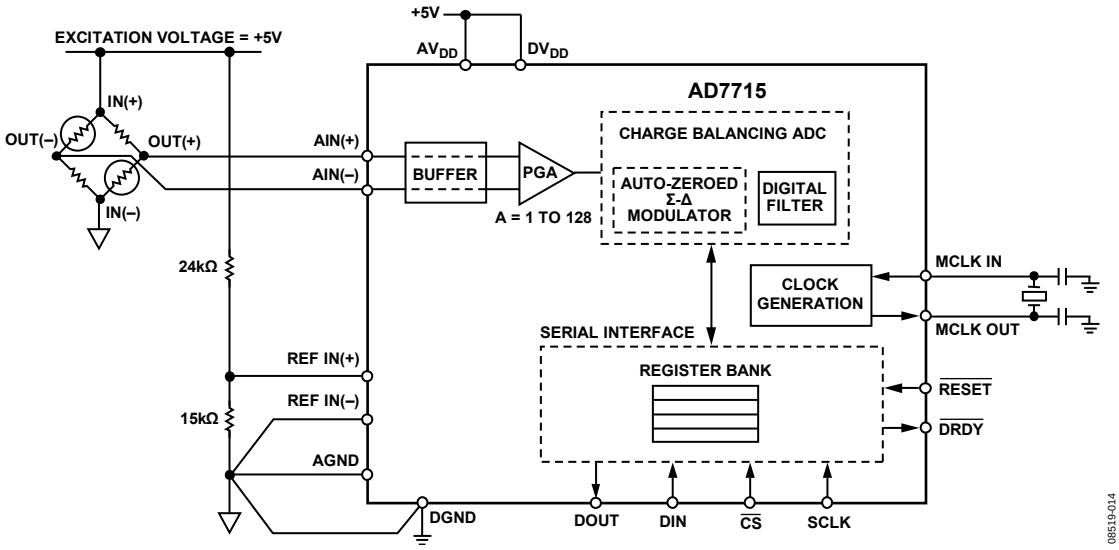


Figure 14. Pressure Measurement Using the AD7715

TEMPERATURE MEASUREMENT

Another application area for the AD7715 is in temperature measurement. Figure 15 outlines a connection from a thermocouple to the AD7715. In this application, the AD7715 is operated in its buffered mode to allow large decoupling capacitors on the front end to eliminate any noise pickup that there may have been in the thermocouple leads. When the AD7715 is operated in buffered mode, it has a reduced common-mode range. To place the differential voltage from the thermocouple on a suitable common-mode voltage, the AIN(−) input of the AD7715 is biased up at the reference voltage, 2.5 V.

Figure 16 shows another temperature measurement application for the AD7715. In this case, the transducer is an resistive temperature device (RTD), a PT100. The arrangement is a 4-lead RTD configuration. There are voltage drops across the lead resistances R_{L1} and R_{L4}, but these simply shift the common-mode voltage. There is no voltage drop across lead resistances R_{L2} and R_{L3} as the input current to the AD7715 is very low. The lead resistances present a small source impedance so it would not generally be necessary to turn on the buffer on the AD7715. If the buffer is required, the common-mode voltage should be set accordingly by inserting a small resistance between the bottom end of the RTD and AGND of the AD7715. In the application shown in Figure 16, an external 400 µA current source provides the excitation current for the PT100 and it also generates the reference voltage for the AD7715 via the 6.25 kΩ resistor. Variations in the excitation current do not affect the circuit as both the input voltage and the reference voltage vary ratiometrically with the excitation current. However, the 6.25 kΩ resistor must have a low temperature coefficient to avoid errors in the reference voltage over temperature.

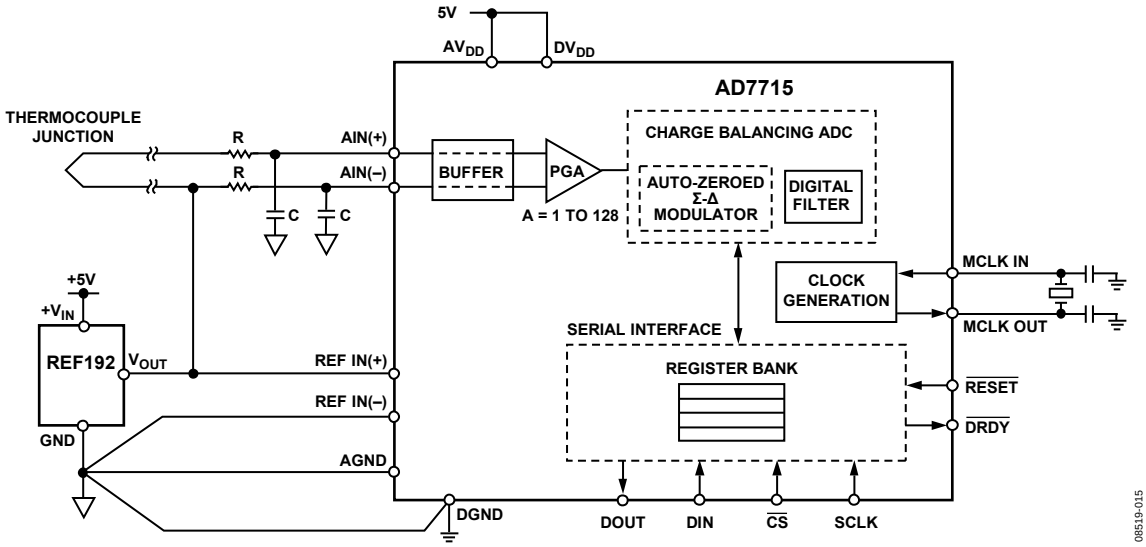


Figure 15. Thermocouple Measurement Using the AD7715

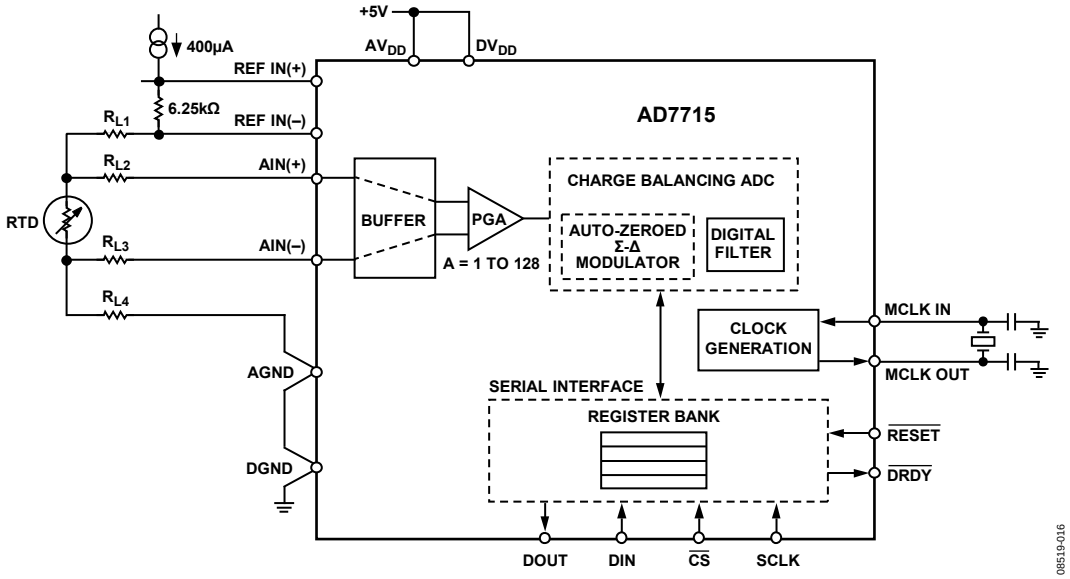


Figure 16. RTD Measurement Using the AD7715

SMART TRANSMITTERS

Another area where the low power, single supply, three-wire interface capabilities is of benefit is in smart transmitters. Here, the entire smart transmitter must operate from the 4 mA to 20 mA loop. Tolerances in the loop mean that the amount of current available to power the transmitter is as low as 3.5 mA.

The AD7715 consumes only 450 µA, leaving 3 mA available for the rest of the transmitter. Figure 17 shows a block diagram of a smart transmitter which includes the AD7715. Not shown in Figure 17 is the isolated power source required to power the front end.

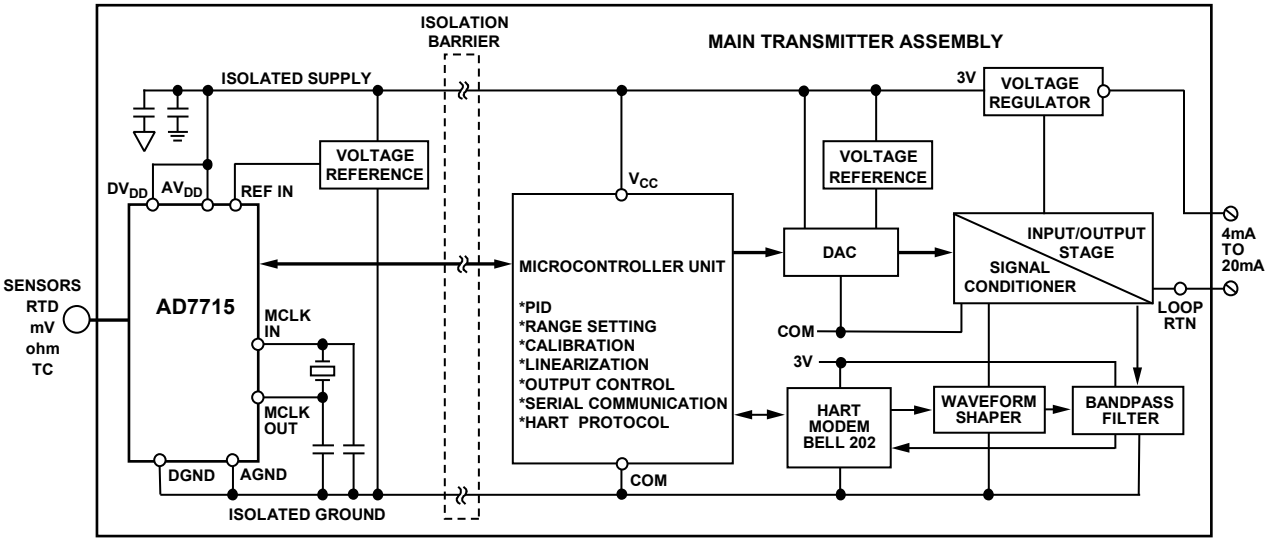
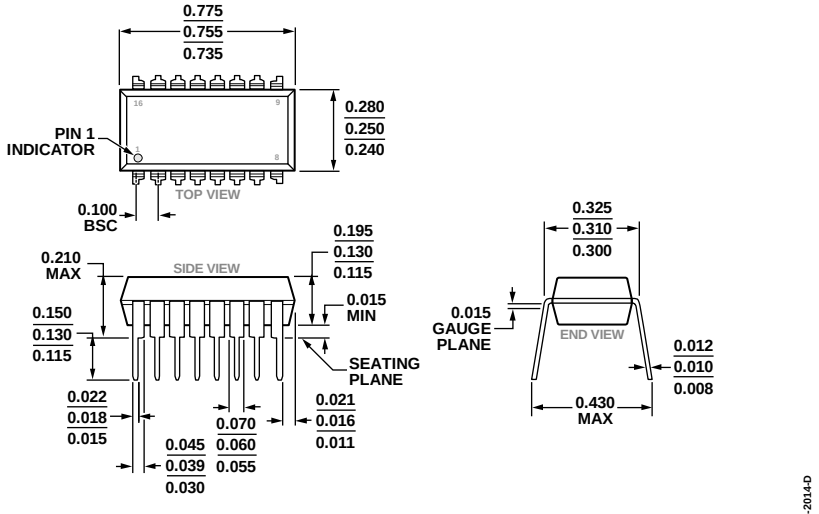


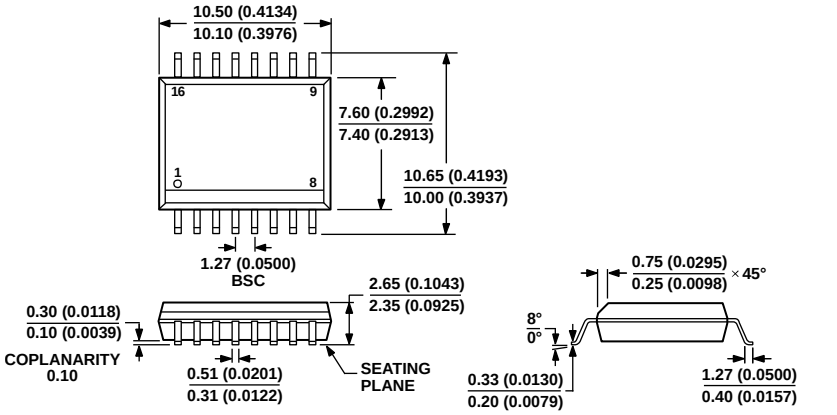
Figure 17. Smart Transmitter Using the AD7715

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 18. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

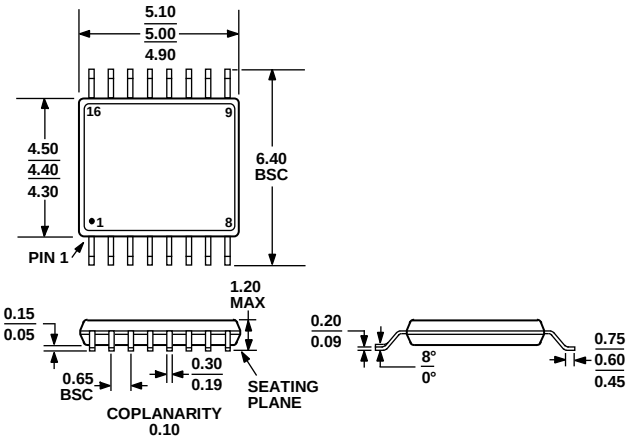


Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	AV_{DD} Supply	Temperature Range	Package Description	Package Option
AD7715AN-5	5 V	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD7715ANZ-5	5 V	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD7715AR-5	5 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715AR-5REEL	5 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715ARZ-5	5 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715ARZ-5REEL	5 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715ARUZ-5	5 V	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7715ARUZ-5REEL7	5 V	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7715ACHIPS-5	5 V	−40°C to +85°C	Chips	
AD7715ANZ-3	3 V	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD7715AR-3	3 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715ARZ-3	3 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715ARZ-3REEL	3 V	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD7715ARUZ-3	3 V	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7715ARUZ-3REEL7	3 V	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7715ACHIPS-3	3 V	−40°C to +85°C	Chips	

[1] Z = RoHS Compliant Part.

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