THE DATASHEET OF

AD7723BSZ-REEL

www.win-source.net 0086-755-83957316

16-Bit, 1.2 MSPS CMOS, Sigma-Delta ADC

AD7723

FEATURES

16-bit Σ-Δ ADC
1.2 MSPS output word rate
32×/16× oversampling ratio
Low-pass and band-pass digital filter
Linear phase
On-chip 2.5 V voltage reference
Standby mode
Flexible parallel or serial interface
Crystal oscillator
Single 5 V supply

GENERAL DESCRIPTION

The AD7723 is a complete 16-bit, sigma-delta ADC. The part operates from a 5 V supply. The analog input is continuously sampled, eliminating the need for an external sample-and-hold. The modulator output is processed by a finite impulse response (FIR) digital filter. The on-chip filtering combined with a high oversampling ratio reduces the external antialias requirements to first order in most cases. The digital filter frequency response can be programmed to be either low-pass or band-pass.

The AD7723 provides 16-bit performance for input bandwidths up to 460 kHz at an output word rate up to 1.2 MHz. The sample rate, filter corner frequencies, and output word rate are set by the crystal oscillator or external clock frequency.

Data can be read from the device in either serial or parallel format. A stereo mode allows data from two devices to share a single serial data line. All interface modes offer easy, high speed connections to modern digital signal processors.

FUNCTIONAL BLOCK DIAGRAM

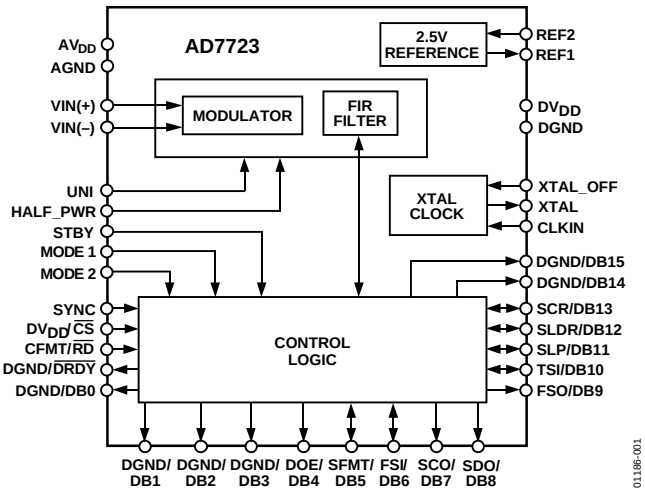

Figure 1.

The part provides an on-chip 2.5 V reference. Alternatively, an external reference can be used.

A power-down mode reduces the idle power consumption to 200 μW.

The AD7723 is available in a 44-lead MQFP package and is specified over the industrial temperature range from –40°C to +85°C.

Two input modes are provided, allowing both unipolar and bipolar input ranges.

Rev. C

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REVISION HISTORY

5/05—Rev. B to Rev. C

Changes to Format ... Universal
Changes to Figure 6 ... 8
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10/03—Rev. A to Rev. B

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9/02—Data Sheet changed from Rev. 0 to Rev. A

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SPECIFICATIONS[1]

AV_{DD} = DV_{DD} = 5 V ± 5%; AGND = AGND1 = AGND2 = DGND = 0 V; f_{CLKIN} = 19.2 MHz; REF2 = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

		B Version			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC SPECIFICATIONS[2, 3]	HALF_PWR = 0 to 1				
	f_{CLKIN} = 10 MHz when HALF_PWR = 1				
Decimate by 32					
Bipolar Mode					
Signal to Noise					
Full Power	2.5 V reference	87	90		dB
	3 V reference	88.5	91		dB
Half Power		86.5	89		dB
Total Harmonic Distortion[4]			−96	−90	dB
Spurious-Free Dynamic Range[4]	2.5 V reference			−92	dB
	3 V reference			−90	dB
Unipolar Mode					
Signal to Noise			87		dB
Total Harmonic Distortion[4]			−89		dB
Spurious-Free Dynamic Range[4]			−90		dB
Band-Pass Filter Mode					
Bipolar Mode					
Signal to Noise		76	79		dB
Decimate by 16					
Bipolar Mode					
Signal to Noise	Measurement bandwidth = 0.383 × F_O				
	2.5 V reference	82	86		dB
	3 V reference	83	87		dB
Signal to Noise	Measurement bandwidth = 0.5 × F_O	78	81.5		dB
Total Harmonic Distortion[4]	2.5 V reference			−88	dB
Spurious-Free Dynamic Range[4]	3 V reference			−86	dB
	2.5 V reference			−90	dB
	3 V reference			−88	dB
Unipolar Mode					
Signal to Noise	Measurement bandwidth = 0.383 × F_O		84		dB
Signal to Noise	Measurement bandwidth = 0.5 × F_O		81		dB
Total Harmonic Distortion[4]			−89		dB
DIGITAL FILTER RESPONSE					
Low-Pass Decimate by 32					
0 kHz to f_{CLKIN}/83.5				±0.001	dB
f_{CLKIN}/66.9		−3			dB
f_{CLKIN}/64		−6			dB
f_{CLKIN}/51.9 to f_{CLKIN}/2				−90	dB
Group Delay			1293/2 f_{CLKIN}		
Settling Time			1293/f_{CLKIN}		

Parameter	Test Conditions/Comments	B Version			Unit
		Min	Typ	Max	
Low-Pass Decimate by 16					
0 kHz to f_{CLKIN}/41.75				±0.001	dB
f_{CLKIN}/33.45		−3			dB
f_{CLKIN}/32		−6			dB
f_{CLKIN}/25.95 to f_{CLKIN}/2				−90	dB
Group Delay			541/2 f_{CLKIN}		
Settling Time			541/f_{CLKIN}		
Band-Pass Decimate by 32					
f_{CLKIN}/51.90 to f_{CLKIN}/41.75				±0.001	dB
f_{CLKIN}/62.95, f_{CLKIN}/33.34		−3			dB
f_{CLKIN}/64, f_{CLKIN}/32		−6			dB
0 kHz to f_{CLKIN}/83.5, f_{CLKIN}/25.95 to f_{CLKIN}/2				−90	dB
Group Delay			1293/2 f_{CLKIN}		
Settling Time			1293/f_{CLKIN}		
Output Data Rate, F_O					
Decimate by 32			f_{CLKIN}/32		
Decimate by 166			f_{CLKIN}/16		
ANALOG INPUTS					
Full-Scale Input Span	VIN(+) − VIN(−)				
Bipolar Mode				±4/5 × V_{REF2}	V
Unipolar Mode		0		8/5 × V_{REF2}	V
Absolute Input Voltage	VIN(+) − VIN(−)	AGND		AV_{DD}	V
Input Sampling Capacitance			2		pF
Input Sampling Rage, f_{CLKIN}				19.2	MHz
CLOCK					
CLKIN Duty Ratio		45		55	%
REFERENCE					
REF1 Output Resistance			3		kΩ
Using Internal Reference					
REF2 Output Voltage		2.39	2.54	2.69	V
REF2 Output Voltage Drift			60		ppm/°C
Using External Reference					
REF2 Input Impedance	REF1 = AGND		4		kΩ
REF2 External Voltage Range		1.2	2.5	3.15	V
STATIC PERFORMANCE					
Resolution		16			Bits
Differential Nonlinearity	Guaranteed monotonic		±0.5	±1	LSB
Integral Nonlinearity			±2		LSB
DC CMRR			80		dB
Offset Error			±20		mV
Gain Error[5]			±0.5		% FSR
LOGIC INPUTS (EXCLUDING CLKIN)					
V_{INH}, Input High Voltage		2.0			V
V_{INL}, Input High Voltage				0.8	V
CLOCK INPUT (CLKIN)					
V_{INH}, Input High Voltage		3.8			V
V_{INL}, Input High Voltage				0.4	V
ALL LOGIC INPUTS					
I_{IN}, Input Current	V_{IN} = 0 V to DV_{DD}			±10	μA
C_{IN}, Input Capacitance				10	pF

Parameter	Test Conditions/Comments	B Version Min	Typ	Max	Unit
LOGIC OUPUTS					
V_{OH}, Output High Voltage	$\|I_{OUT}\|$ = 200 µA	4.0			V
V_{OL}, Output Low Voltage	$\|I_{OUT}\|$ = 1.6 mA			0.4	V
POWER SUPPLIES					
AV_{DD}		4.75		5.25	V
I_{AVDD}	HALF_PWR = Logic Low		50	60	mA
	HALF_PWR = Logic High		25	33	mA
DV_{DD}		4.75		5.25	V
I_{DVDD}	HALF_PWR = Logic Low		25	35	mA
	HALF_PWR = Logic High		15	20	mA
Power Consumption[6]	Standby Mode			200	µW

[1] Operating temperature range is –40°C to +85°C (B: Version).
[2] Typical values for SNR apply for parts soldered directly to the PCB ground plane.
[3] Dynamic specifications apply for input signal frequencies from dc to $0.0240 \times f_{CLKIN}$ in decimate by 16 mode and from dc to $0.0120 \times f_{CLKIN}$ in decimate by 32 mode.
[4] When using the internal reference, THD and SFDR specifications apply only to input signals above 10 kHz with a 10 µF decoupling capacitor between REF2 and AGND2. At frequencies below 10 kHz, THD degrades to 84 dB and SFDR degrades to 86 dB.
[5] Gain error excludes reference error.
[6] CLKIN and digital inputs static and equal to 0 or DV_{DD}.

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 5 V ± 5%; AGND = AGND1 = DGND = 0 V; f_{CLKIN} = 19.2 MHz; C_L = 50 pF; SFMT = logic low or high, CFMT = logic low or high; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
CLKIN Frequency	f_{CLK}	1		19.2	MHz
CLKIN Period (t_{CLK} – $1/f_{CLK}$)	t_1	0.052		1	µs
CLKIN Low Pulse Width	t_2	0.45 × t_1		0.55 × t_1	
CLKIN High Pulse Width	t_3	0.45 × t_1		0.55 × t_1	
CLKIN Rise Time	t_4	5			ns
CLKIN Fall Time	t_5	5			ns
FSI Setup Time	t_6	0		5	ns
FSI Hold Time	t_7	0		5	ns
FSI High Time[1]	t_8			1	t_{CLK}
CLKIN to SCO Delay	t_9		25	40	ns
SCO Period[2], SCR = 1	t_{10}		2		t_{CLK}
SCO Period[2], SCR = 0	t_{10}		1		t_{CLK}
SCO Transition to FSO High Delay	t_{11}		0	5	ns
SCO Transition to FSO Low Delay	t_{12}		0	5	ns
SCO Transition to SDO Valid Delay	t_{13}		5	12	ns
SCO Transition from FSI[3]	t_{14}		60	t_{CLK} + t_2	
SDO Enable Delay Time	t_{15}		5	20	ns
SDO Disable Delay Time	t_{16}		5	20	ns
$\overline{DRDY}$ High Time[2]	t_{17}	2			t_{CLK}
Conversion Time[2] (Refer to Table 3 and Table 4)	t_{18}	16/32			t_{CLK}
CLKIN to $\overline{DRDY}$ Transition	t_{19}		35	50	ns
CLKIN to DATA Valid	t_{20}		20	35	ns
$\overline{CS}$/$\overline{RD}$ Setup Time to CLKIN	t_{21}	0			ns
$\overline{CS}$/$\overline{RD}$ Hold Time to CLKIN	t_{22}	20			ns
Data Access Time	t_{23}		20	35	ns
Bus Relinquish Time	t_{24}		20	35	ns
SYNC Input Pulse Width	t_{25}	1			t_{CLK}
SYNC Low Time before CLKIN Rising	t_{26}	0			ns
$\overline{DRDY}$ High Delay after Rising SYNC	t_{27}		25	35	ns
$\overline{DRDY}$ Low Delay after SYNC Low	t_{28}			2049	t_{CLK}

[1] FSO pulses are gated by the release of FSI (going low).
[2] Guaranteed by design.
[3] Frame sync is initiated on the falling edge of CLKIN.

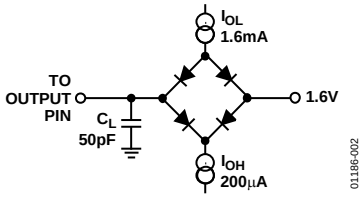


Figure 2. Load Circuit for Timing Specifications

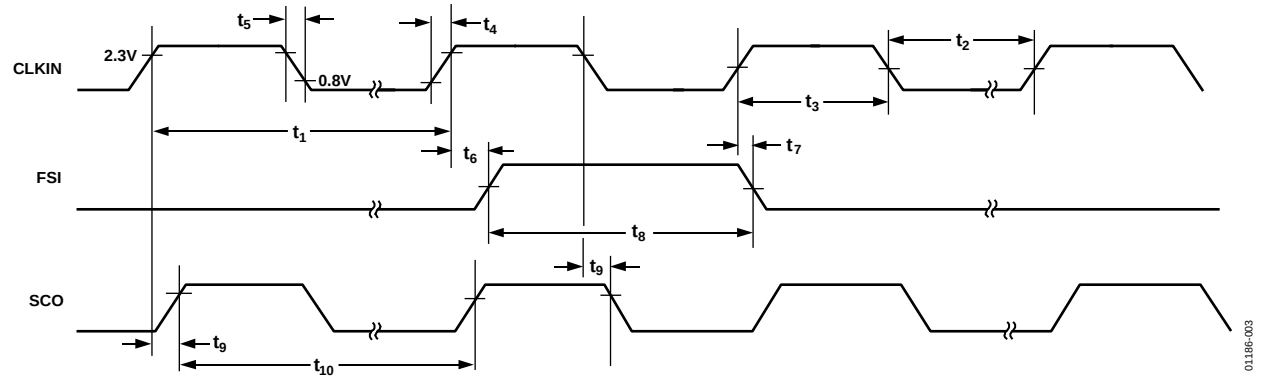


Figure 3. Serial Mode Timing for Clock Input, Frame Sync Input, and Serial Clock Output

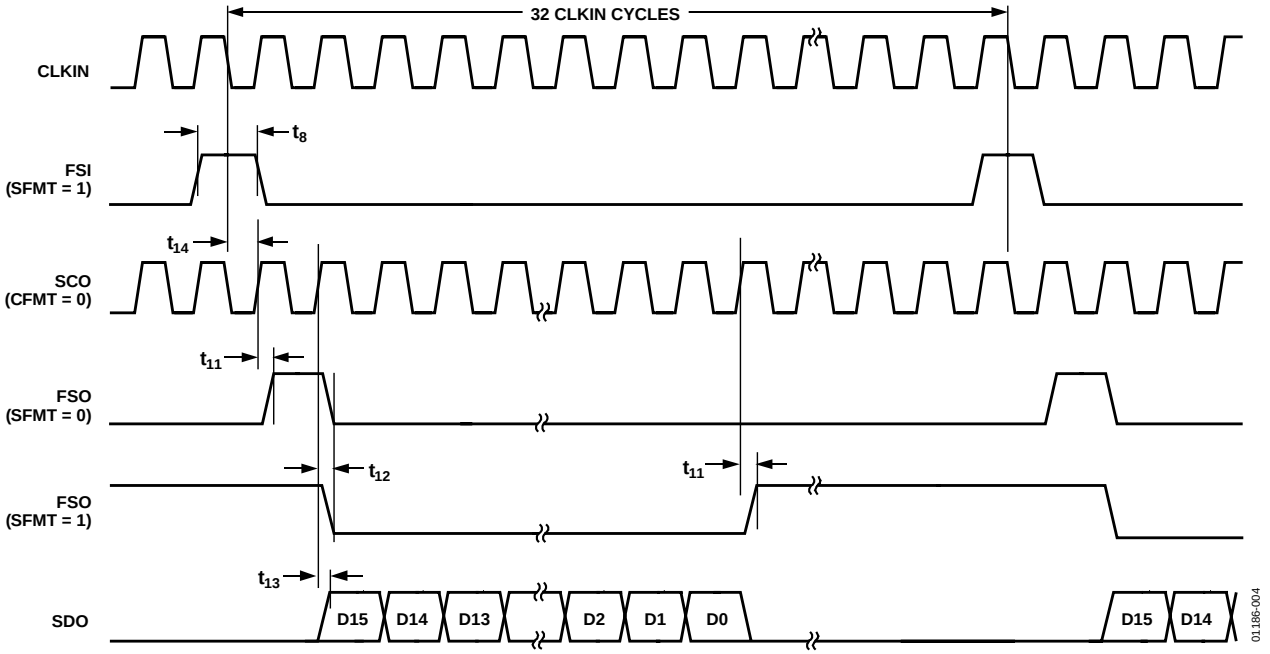


Figure 4. Serial Mode 1: Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output, and Serial Data Output (See Table 3 for Control Inputs, TSI = DOE)

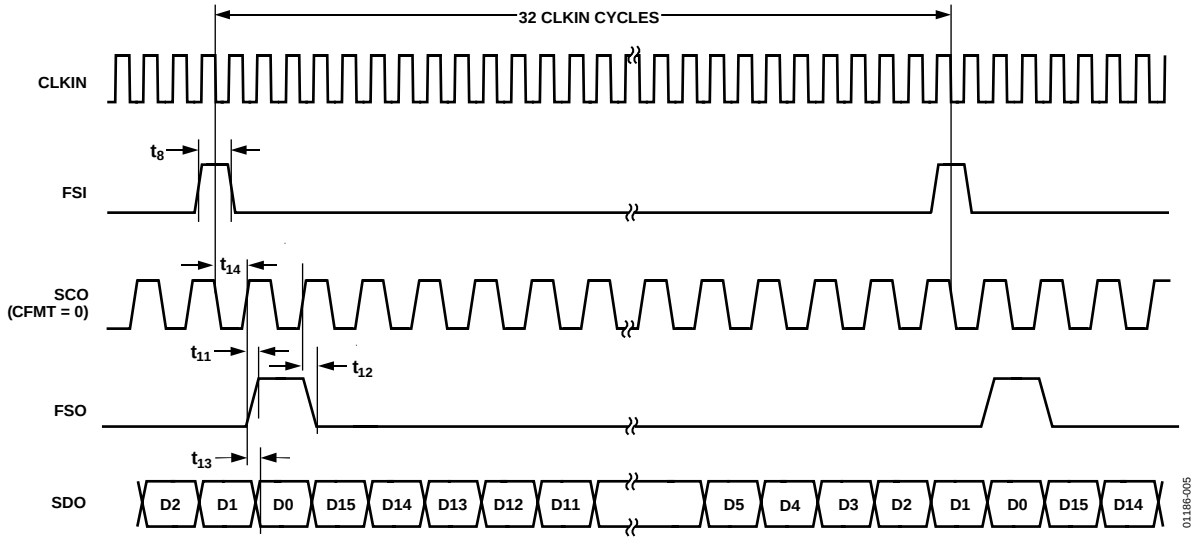


Figure 5. Serial Mode 2: Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output, and Serial Data Output (See Table 3 for Control Inputs, TSI = DOE)

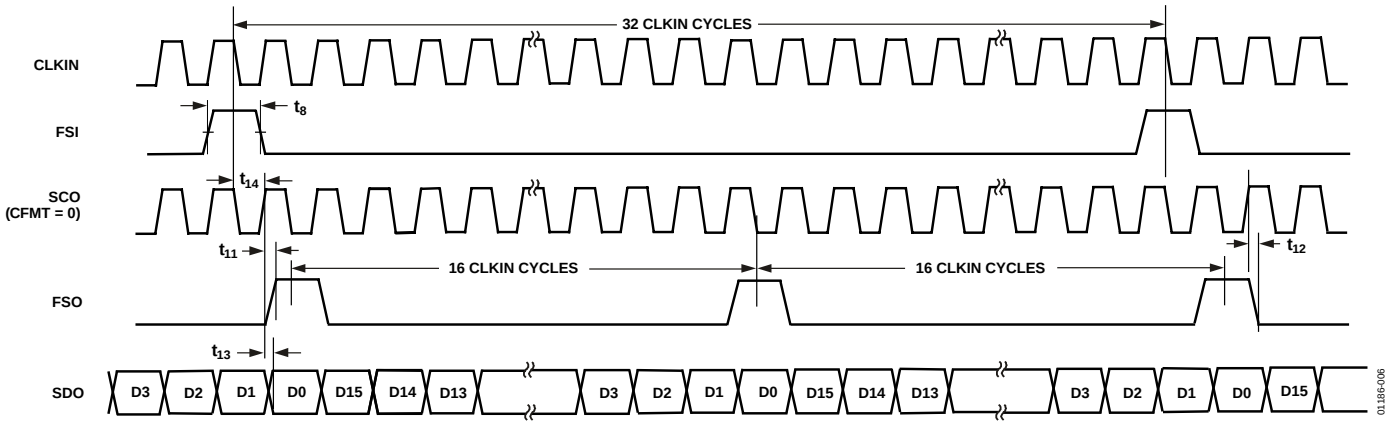


Figure 6. Serial Mode 3: Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output, and Serial Data Output (See Table 3 for Control Inputs, TSI = DOE)

Table 3. Serial Interface (MODE1 = 0, MODE2 = 0)

					Control Inputs		
Serial Mode	**Decimation Ratio (SLDR)**	**Digital Filter Mode (SLP)**	**SCO Frequency (SCR)**	**Output Data Rate**	**SLDR**	**SLP**	**SCR**
1	32	Low Pass	f_{CLKIN}	$f_{CLKIN}/32$	1	1	0
1	32	Band Pass	f_{CLKIN}	$f_{CLKIN}/32$	1	0	0
2	32	Low Pass	$f_{CLKIN}/2$	$f_{CLKIN}/32$	1	1	1
2	32	Band Pass	$f_{CLKIN}/2$	$f_{CLKIN}/32$	1	0	1
3	16	Low Pass	f_{CLKIN}	$f_{CLKIN}/16$	0	1	0

Table 4. Parallel Interface

			Control Inputs	
Digital Filter Mode	**Decimation Ratio**	**Output Data Rate**	**MODE1**	**MODE2**
Band Pass	32	$f_{CLKIN}/32$	0	1
Low Pass	32	$f_{CLKIN}/32$	1	0
Low Pass	16	$f_{CLKIN}/16$	1	1

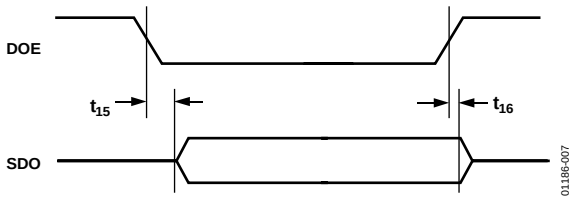


Figure 7. Serial Mode Timing for Data Output Enable and Serial Data Output

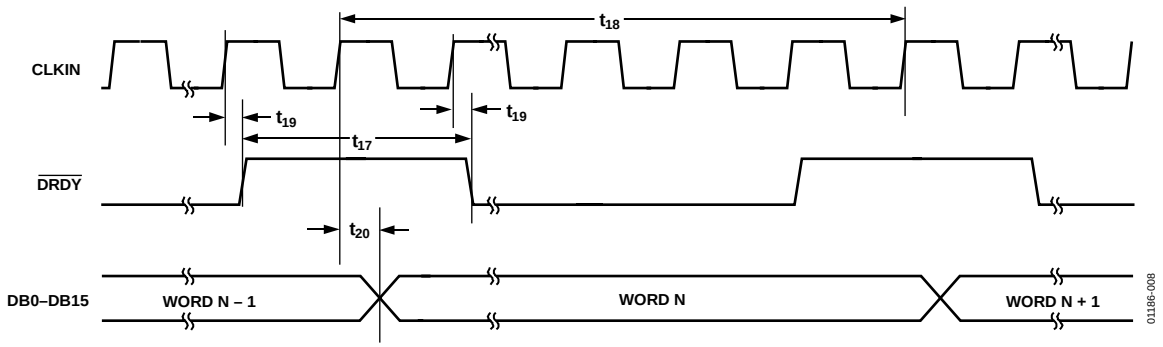


Figure 8. Parallel Mode Read Timing, $\overline{CS}$ and $\overline{RD}$ Tied Logic Low

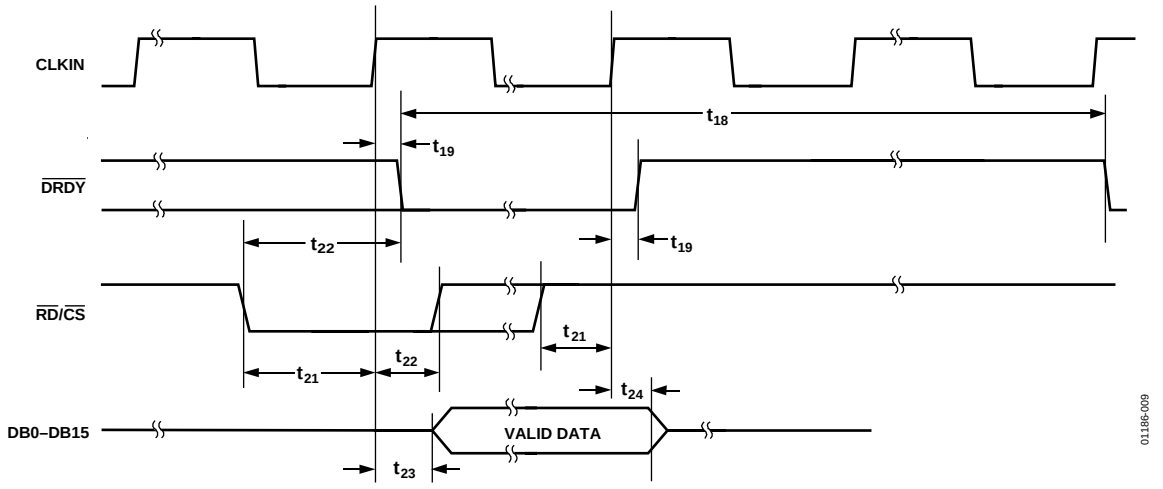


Figure 9. Parallel Mode Read Timing, $\overline{CS} = \overline{RD}$

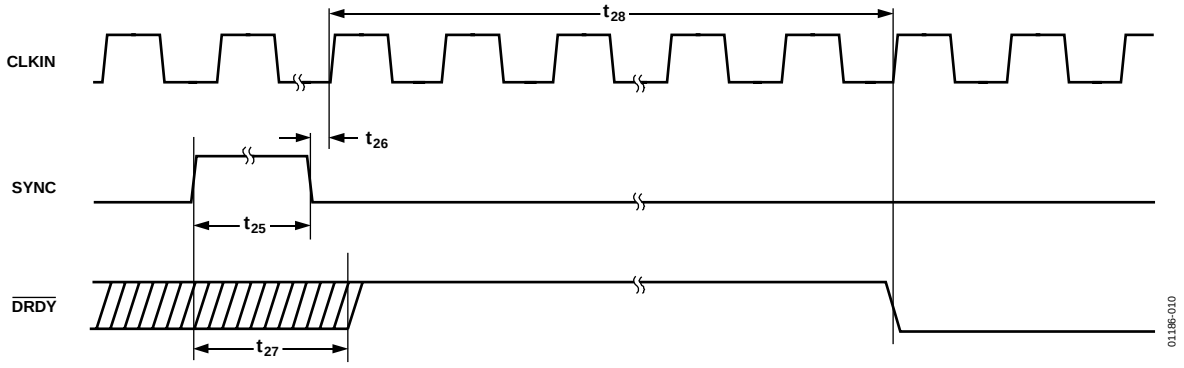


Figure 10. SYNC Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
DV_{DD} to DGND	−0.3 V to +7 V
AV_{DD}, AV_{DD1} to AGND	−0.3 V to +7 V
AV_{DD}, AV_{DD1} to DV_{DD}	−1 V to +1 V
AGND, AGND1 to DGND	−0.3 V to +0.3 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V
VIN (+), VIN(−) to AGND	−0.3 V to AV_{DD} + 0.3 V
REF1 to AGND	−0.3 V to AV_{DD} + 0.3 V
REF2 to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	95°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

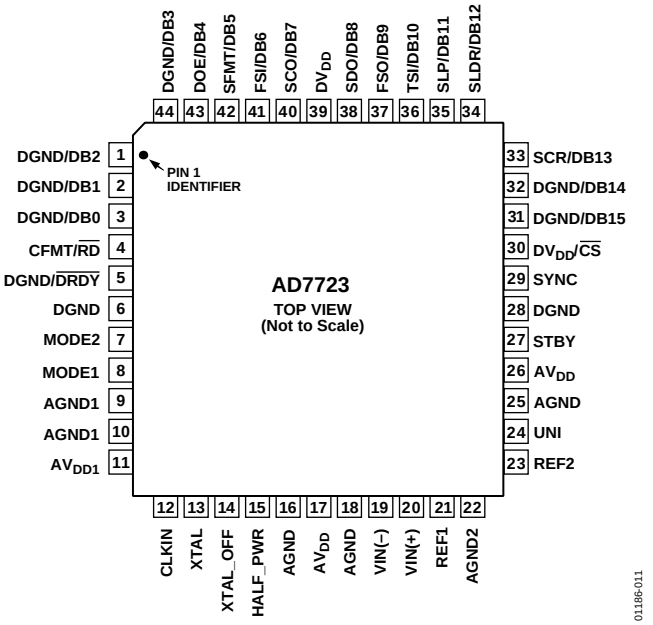


Figure 11. 44-Lead MQFP

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
6, 28	DGND	Ground Reference for Digital Circuitry.
8, 7	MODE1/MODE2	Mode Control Inputs. The MODE1 and MODE2 pins choose either parallel or serial data interface operation and select the operating mode for the digital filter in parallel mode. See Table 3 and Table 4.
9, 10	AGND1	Digital Logic Power Supply Ground for the Analog Modulator.
11	AV_{DD1}	Digital Logic Power Supply Voltage for the Analog Modulator.
12	CLKIN	Clock Input. An external clock source can be applied directly to this pin with XTAL_OFF tied high. Alternatively, a parallel resonant fundamental frequency crystal, in parallel with a 1 MΩ resistor, can be connected betweenthe XTAL pin and the CLKIN pin with XTAL_OFF tied low. External capacitors are then required from the CLKIN and XTAL pins to ground. Consult the crystal manufacturer's recommendation for the load capacitors.
13	XTAL	Input to Crystal Oscillator Amplifier. If an external clock is used, XTAL should be tied to AGND1.
14	XTAL_OFF	Oscillator Enable Input. A logic high disables the crystal oscillator amplifier to allow use of an external clock source. Set low when using an external crystal between the CLKIN and XTAL pins.
15	HALF_PWR	When set high, the power dissipation is reduced by approximately one-half, and a maximum CLKIN frequency of 10 MHz applies.
16, 18, 25	AGND	Power Supply Ground for the Analog Modulator.
17, 26	AV_{DD}	Positive Power Supply Voltage for the Analog Modulator.
19	VIN(–)	Negative Terminal of the Differential Analog Input.
20	VIN(+)	Positive Terminal of the Differential Analog Input.
21	REF1	Reference Output. REF1 connects through 3 kΩ to the output of the internal 2.5 V reference and to a buffer amplifier that drives the Σ-Δ modulator.
22	AGND2	Power Supply Ground Return to the Reference Circuitry, REF2, of the Analog Modulator.
23	REF2	Reference Input. REF2 connects to the output of an internal buffer amplifier that drives the Σ-Δ modulator. When REF2 is used as an input, REF1 must be connected to AGND to disable the internal buffer amplifier.
24	UNI	Analog Input Range Select Input. The UNI pin selects the analog input range for either bipolar or unipolar operation. A logic high input selects unipolar operation and a logic low selects bipolar operation.
27	STBY	Standby Logic Input. A logic high sets the AD7723 into the power-down state.

Pin No.	Mnemonic	Description
29	SYNC	Synchronization Logic Input. When using more than one AD7723 operated from a common master clock, SYNC allows each ADC to simultaneously sample its analog input and update its output register. A rising edge resets the AD7723 digital filter sequencer counter to 0. When the rising edge of CLKIN senses a logic low on SYNC, the reset state is released. Because the digital filter and sequencer are completely reset during this action, SYNC pulses cannot be applied continuously.
39	DV_{DD}	Digital Power Supply Voltage; 5 V ± 5%.

Table 7. Parallel Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DGND/DB2	Data Output Bit.
2	DGND/DB1	Data Output Bit.
3	DGND/DB0	Data Output Bit (LSB).
4	CFMT/$\overline{RD}$	Read Logic Input. Used in conjunction with $\overline{CS}$ to read data from the parallel bus. The output data bus is enabled when the rising edge of CLKIN senses a logic low level on $\overline{RD}$ if $\overline{CS}$ is also low. When $\overline{RD}$ is sensed high, the output data bits, DB15 to DB0, are high impedance.
5	DGND/$\overline{DRDY}$	Data Ready Logic Output. A falling edge indicates a new output word is available to be read from the output data register. $\overline{DRDY}$ returns high upon completion of a read operation. If a read operation does not occur between output updates, $\overline{DRDY}$ pulses high for two CLKIN cycles before the next output update. $\overline{DRDY}$ also indicates when conversion results are available after a SYNC sequence.
30	DV_{DD}/$\overline{CS}$	Chip Select Logic Input.
31	DGND/DB15	Data Output Bit (MSB).
32	DGND/DB14	Data Output Bit.
33	SCR/DB13	Data Output Bit.
34	SLDR/DB12	Data Output Bit.
35	SLP/DB11	Data Output Bit.
36	TSI/DB10	Data Output Bit.
37	FSO/DB9	Data Output Bit.
38	SDO/DB8	Data Output Bit.
40	SCO/DB7	Data Output Bit.
41	FSI/DB6	Data Output Bit.
42	SFMT/DB5	Data Output Bit.
43	DOE/DB4	Data Output Bit.
44	DGND/DB3	Data Output Bit.

Table 8. Serial Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DGND/DB2	Tie to DGND.
2	DGND/DB1	Tie to DGND.
3	DGND/DB0	Tie to DGND.
4	CFMT/$\overline{RD}$	Serial Clock Format Logic Input. The clock format pin selects whether the serial data, SDO, is valid on the rising or falling edge of the serial clock, SCO. When CFMT is logic low, serial data is valid on the falling edge of the serial clock, SCO. If CFMT is logic high, SDO is valid on the rising edge of SCO.
5	DGND/$\overline{DRDY}$	Tie to DGND.
30	DV_{DD}/$\overline{CS}$	Tie to DVDD.
31	DGND/DB15	Tie to DGND.
32	DGND/DB14	Tie to DGND.
33	SCR/DB13	Serial Clock Rate Select Input. With SCR set logic low, the serial clock output frequency, SCO, is equal to the CLKIN frequency. A logic high sets it equal to one-half the CLKIN frequency.
34	SLDR/DB12	Serial Mode Low/High Output Data Rate Select Input. With SLDR set logic high, the low data rate is selected. A logic low selects the high data rate. The high data rate corresponds to data at the output of the fourth decimation filter (decimate by 16). The low data rate corresponds to data at the output of the fifth decimation filter (decimate by 32).
35	SLP/DB11	Serial Mode Low-Pass/Band-Pass Filter Select Input. With SLP set logic high, the low-pass filter response is selected. A logic low selects band-pass.
36	TSI/DB10	Time Slot Logic Input. The logic level on TSI sets the active state of the DOE pin. With TSI set logic high, DOE enables the SDO output buffer when it is a logic high and vice versa. TSI is used when two AD7723s are connected to the same serial data bus. When this function is not needed, TSI and DOE should be tied low.
37	FSO/DB9	Frame Sync Output. FSO indicates the beginning of a word transmission on the SDO pin. Depending on the logic level of the SFMT pin, the FSO signal is either a positive pulse approximately one SCO period wide or a frame pulse that is active low for the duration of the 16-data bit transmission.
38	SDO/DB8	Serial Data Output. The serial data is shifted out MSB first, synchronous with the SCO. Serial Mode 1 data transmissions last 32 SCO cycles. After the LSB is output, trailing zeros are output for the remaining 16 SCO cycles. Serial Modes 2 and 3 data transmissions last 16 SCO cycles.
40	SCO/DB7	Serial Clock Output.
41	FSI/DB6	Frame Synchronization Logic Input. The FSI input is used to synchronize the AD7723 serial output data register to an external source and to allow more than one AD7723, operated from a common master clock, to simultaneously sample its analog input and update its output register.
42	SFMT/DB5	Serial Data Format Logic Input. The logic level on the SFMT pin selects the format of the FSO signal for Serial Mode 1. A logic low makes the FSO output a pulse one SCO cycle wide at the beginning of a serial data transmission. With SFMT set to a logic high, the FSO signal is a frame pulse that is active low for the duration of the 16-bit transmission. For Serial Modes 2 and 3, SFMT should be tied high.
43	DOE/DB4	Data Output Enable Logic Input. The DOE pin controls the three-state output buffer of the SDO pin. The active state of DOE is determined by the logic level on the TSI pin. When the DOE logic level equals the level on the TSI pin, the serial data output, SDO, is active. Otherwise, SDO is high impedance. SDO can be three-state after a serial data transmission by connecting DOE to FSO. In normal operations, TSI and DOE should be tied low.
44	DGND/DB3	Tie to DGND.

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all of the nonfundamental signals up to half the output data rate ($F_O/2$), excluding dc. The ADC is evaluated by applying a low noise, low distortion sine wave signal to the input pins. By generating a fast fourier transform (FFT) plot, the SNR data can then be obtained from the output spectrum.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the harmonics to the rms value of the fundamental. THD is defined as

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics. The THD is also derived from the FFT plot of the ADC output spectrum.

Spurious-Free Dynamic Range (SFDR)
Defined as the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $F_O/2$ and excluding dc) and the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the output spectrum of the FFT. For input signals whose second harmonics occur in the stop-band region of the digital filter, the spur in the noise floor limits the SFDR.

Pass-Band Ripple
The frequency response variation of the AD7723 in the defined pass-band frequency range.

Pass-Band Frequency
The frequency up to which the frequency response variation is within the pass-band ripple specification.

Cutoff Frequency
The frequency below which the AD7723's frequency response will not have more than 3 dB of attenuation.

Stop-Band Frequency
The frequency above which the AD7723's frequency response will be within its stop-band attenuation.

Stop-Band Attenuation
The AD7723's frequency response will not have less than 90 dB of attenuation in the stated frequency band.

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are minus full scale, a point 0.5 LSB below the first code transition (100 . . . 00 to 100 . . . 01 in bipolar mode, 000 . . . 00 to 000 . . . 01 in unipolar mode), and plus full scale, a point 0.5 LSB above the last code transition (011 . . . 10 to 011 . . . 11 in bipolar mode, 111 . . . 10 to 111 . . . 11 in unipolar mode). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between two adjacent codes in the ADC.

Common-Mode Rejection Ratio
The ability of a device to reject the effect of a voltage applied to both input terminals simultaneously—often through variation of a ground level—is specified as a common–mode rejection ratio. CMRR is the ratio of gain for the differential signal to the gain for the common-mode signal.

Unipolar Offset Error
Unipolar offset error is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal differential voltage (VIN(+) – VIN(–)+ 0.5 LSB) when operating in the unipolar mode.

Bipolar Offset Error
This is the deviation of the midscale transition code (111 . . . 11 to 000 . . . 00) from the ideal differential voltage (VIN(+) – VIN(–) – 0.5 LSB) when operating in the bipolar mode.

Gain Error
The first code transition should occur at an analog value ½ LSB above –full scale. The last transition should occur for an analog value 1 ½ LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TYPICAL PERFORMANCE CHARACTERISTICS

AV_{DD} = DV_{DD} = 5 V; T_A = 25°C; CLKIN = 19.2 MHz; external 2.5 V reference, unless otherwise noted.

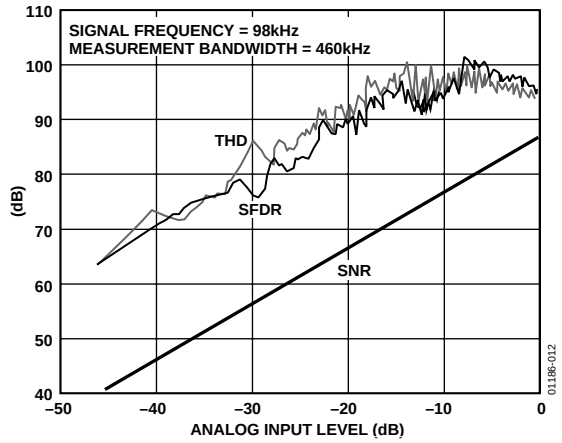


Figure 12. SNR, THD, and SFDR vs. Analog Input Level Relative to Full Scale (Output Data Rate = 1.2 MHz)

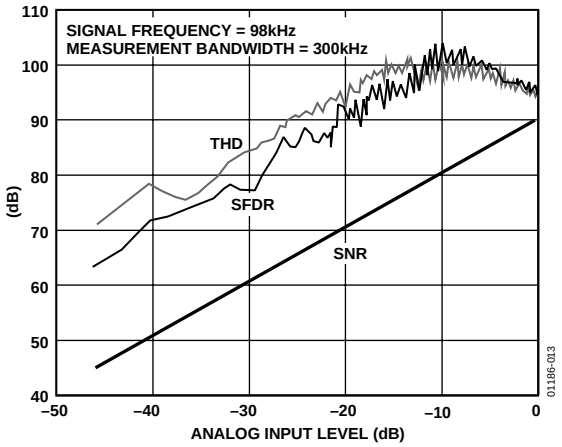


Figure 13. SNR, THD, and SFDR vs. Analog Input Level Relative to Full Scale (Output Data Rate = 600 kHz)

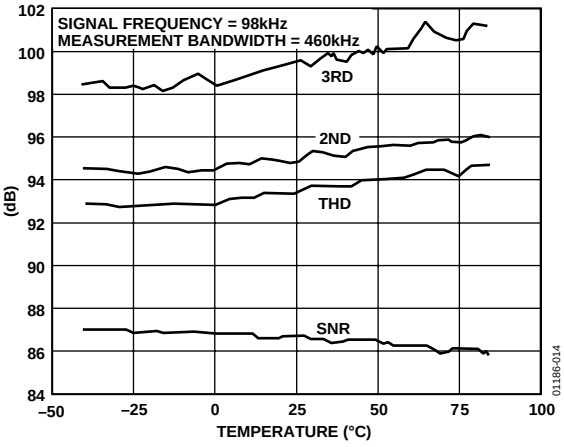


Figure 14. SNR and THD vs. Temperature (Output Data Rate = 1.2 MHz)

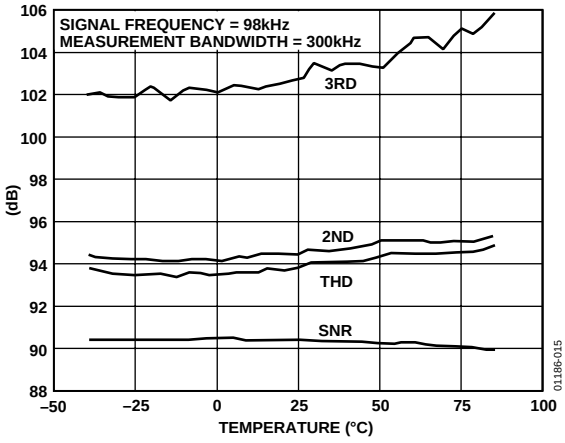


Figure 15. SNR and THD vs. Temperature (Output Data Rate = 600 kHz)

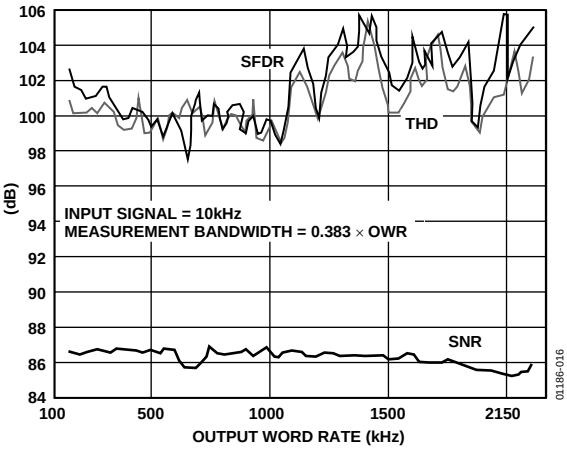


Figure 16. SNR, THD, and SFDR vs. Sampling Frequency (Decimate by 16)

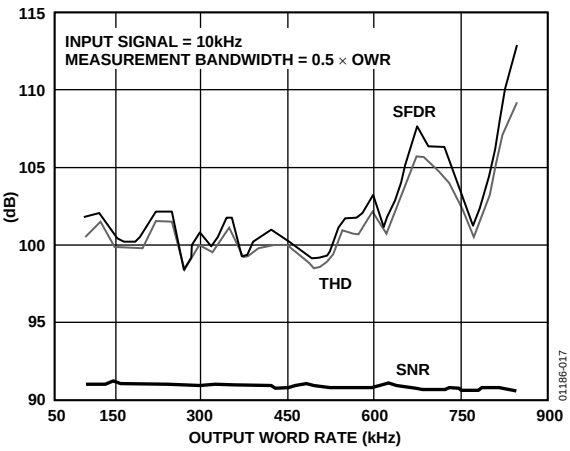


Figure 17. SNR, THD, and SFDR vs. Sampling Frequency (Decimate by 32)

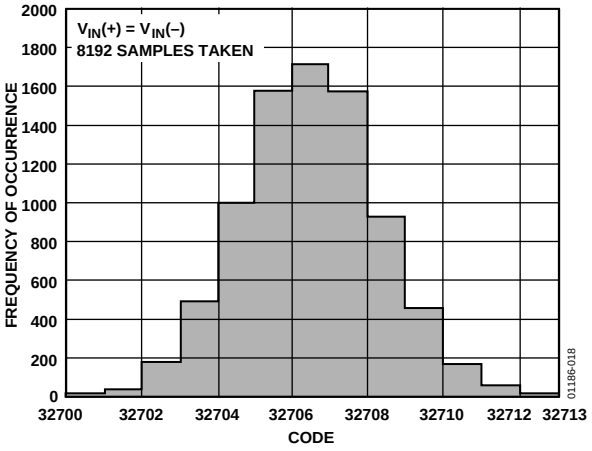


Figure 18. Histogram of Output Codes with DC Input (Output Data Rate = 1.2 MHz)

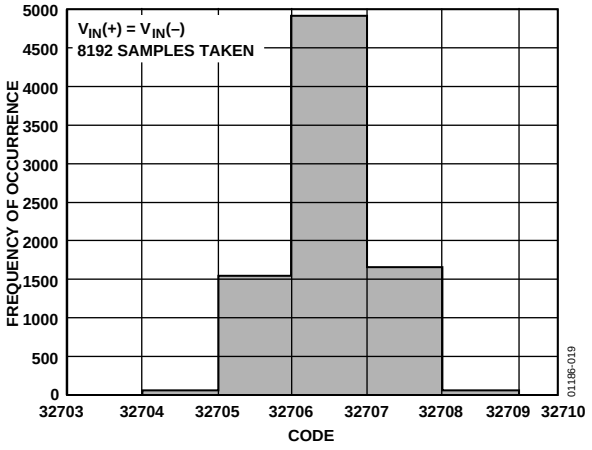


Figure 19. Histogram of Output Codes with DC Input (Output Data Rate = 600 kHz)

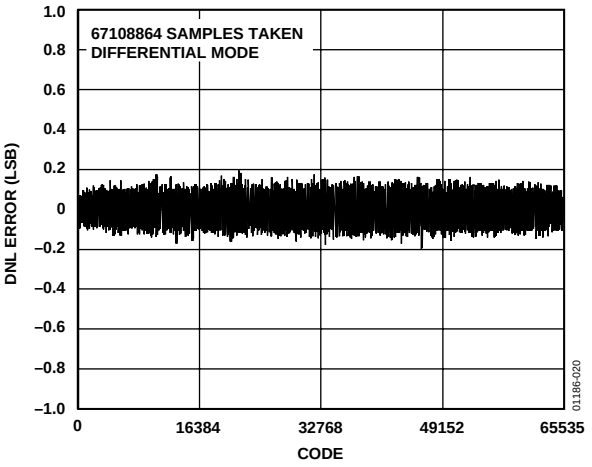


Figure 20. Differential Nonlinearity (Output Data Rate = 1.2 MHz)

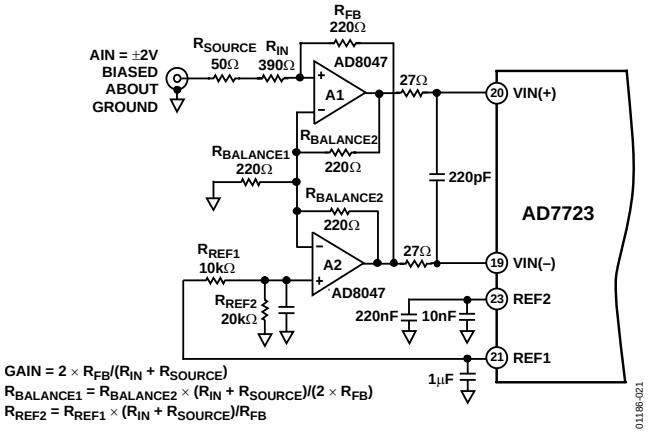


Figure 21. Differential Nonlinearity (Output Data Rate = 600 kHz)

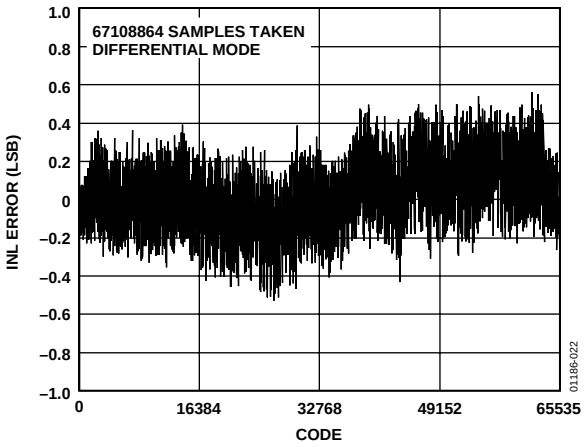


Figure 22. Integral Nonlinearity (Output Data Rate =1.2 MHz)

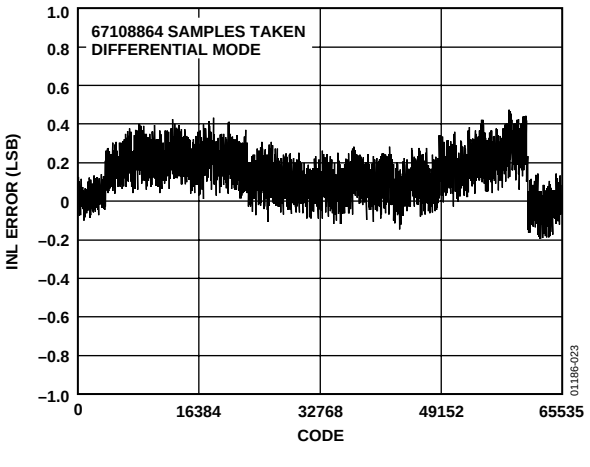


Figure 23. Integral Nonlinearity (Output Data Rate = 600 kHz)

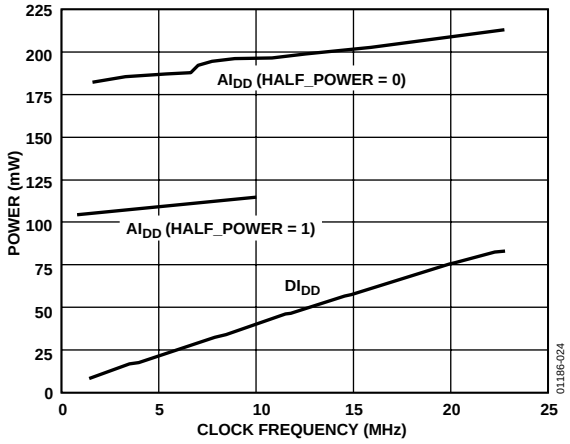


Figure 24. Power Consumption vs. CLKIN Frequency

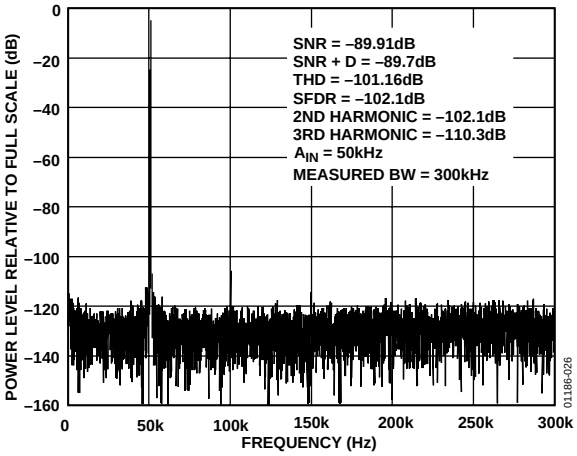


Figure 26. 16 K Point FFT (Output Data Rate = 600 kHz)

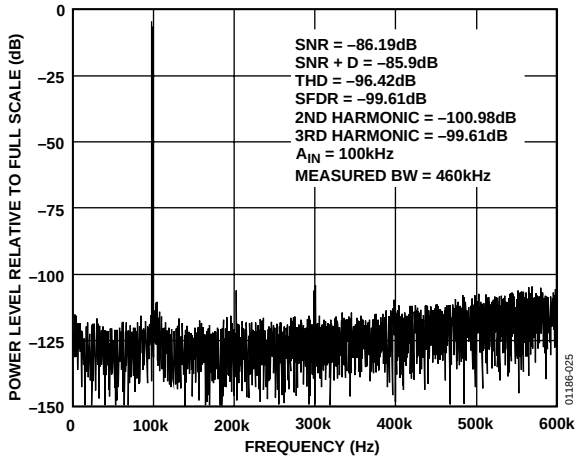


Figure 25. 16 K Point FFT (Output Data Rate = 1.2 MHz)

CIRCUIT DESCRIPTION

The AD7723 ADC employs a Σ-Δ conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word at the input clock frequency, f_{CLKIN}.

Due to the high oversampling rate that spreads the quantization noise from 0 to $f_{CLKIN}/2$, the noise energy contained in the band of interest is reduced (Figure 27A). To further reduce the quantization noise, a high-order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the band of interest (Figure 27B).

The digital filter that follows the modulator removes the large out-of-band quantization noise (Figure 27C) while also reducing the data rate from f_{CLKIN} at the input of the filter to $f_{CLKIN}/32$ or $f_{CLKIN}/16$ at the output of the filter, depending on the state on the MODE1/MODE2 pins in parallel interface mode or the SLDR pin in serial interface mode. The AD7723 output data rate is a little over twice the signal bandwidth, which guarantees that there is no loss of data in the signal band.

Digital filtering has certain advantages over analog filtering. First, since digital filtering occurs after the A/D conversion, it can remove noise injected during the conversion process. Analog filtering cannot remove noise injected during conversion. Second, the digital filter combines low pass-band ripple with a steep roll-off while also maintaining a linear phase response.

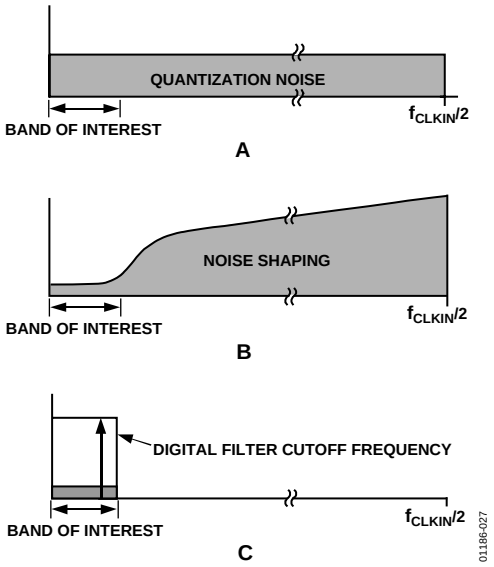


Figure 27. Sigma-Delta ADC

The AD7723 employs four or five finite impulse response (FIR) filters in series. Each individual filter's output data rate is half that of the filter's input data rate. When data is fed to the interface from the output of the fourth filter, the output data rate is $f_{CLKIN}/16$ and the resulting oversampling ratio (OSR) of the converter is 16. Data fed to the interface from the output of the fifth filter results in an output data rate of $f_{CLKIN}/32$ and a corresponding OSR for the converter of 32. When an output data rate (ODR) of $f_{CLKIN}/32$ is selected, the digital filter response can be set to either low-pass or band-pass. The band-pass response is useful when the input signal is band limited because the resulting output data rate is half that required to convert the band when the low-pass operating mode is used. To illustrate the operation of this mode, consider a band-limited signal, as shown in Figure 28A. This signal band can be correctly converted by selecting the (low-pass) ODR = $f_{CLKIN}/16$ mode, as shown in Figure 28B. Note that the output data rate is a little over twice the maximum frequency in the frequency band.

Alternatively, the band-pass mode can be selected, as shown in Figure 28C. The band-pass filter removes unwanted signals from dc to just below $f_{CLKIN}/64$. Rather than outputting data at $f_{CLKIN}/16$, the output of the band-pass filter is sampled at $f_{CLKIN}/32$. This effectively translates the wanted band to a maximum frequency of a little less than $f_{CLKIN}/64$, as shown in Figure 28D. Halving the output data rate reduces the workload of any following signal processor and also allows a lower serial clock rate to be used.

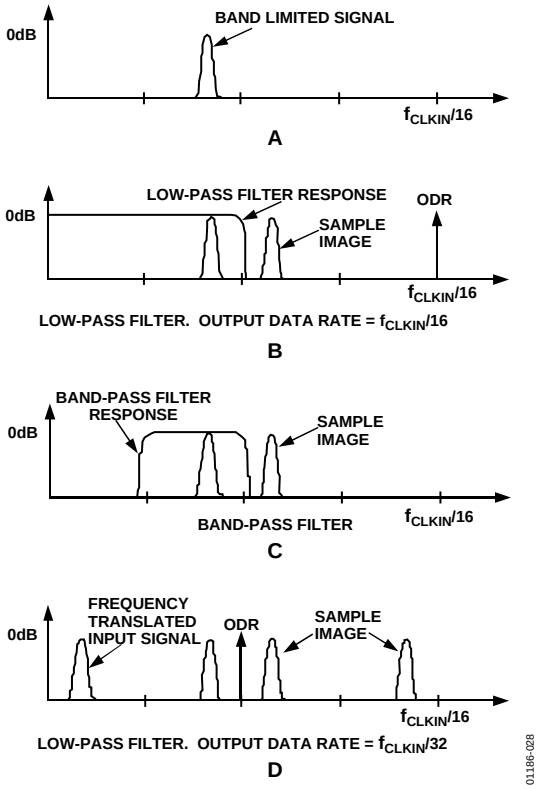


Figure 28. Band-Pass Operation

The frequency response of the three digital filter operating modes is shown in Figure 29, Figure 30, and Figure 31.

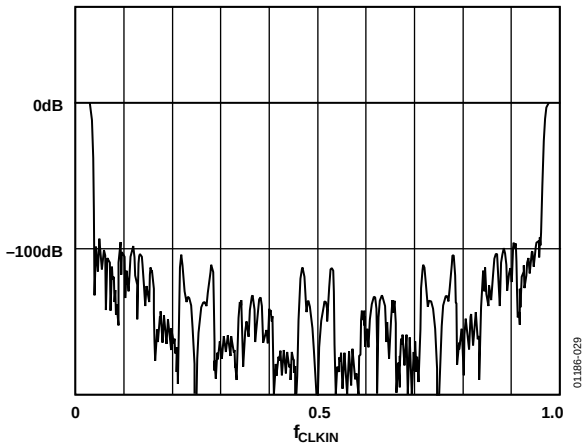


Figure 29. Low-Pass Filter Decimate by 16

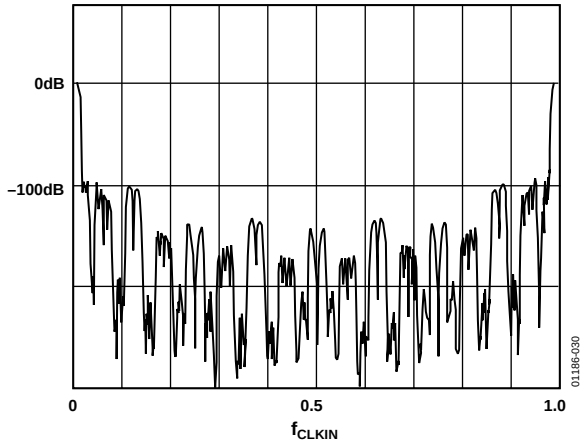


Figure 30. Low-Pass Filter Decimate by 32

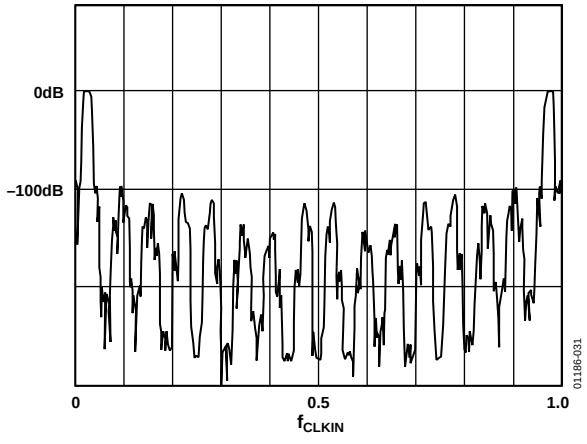


Figure 31. Band-Pass Filter Decimate by 32

Figure 32 shows the frequency response of the digital filter in both low-pass and band-pass modes. Due to the sampling nature of the converter, the pass-band response is repeated about the input sampling frequency, f_{CLKIN}, and at integer multiples of f_{CLKIN}. Out-of-band noise or signals coincident with any of the filter images are aliased down to the pass band. However, due to the AD7723's high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broadband noise is attenuated by at least 90 dB. In addition, as shown in Figure 33, with even a low-order filter, there is significant attenuation at the first image frequency. This contrasts with a normal Nyquist rate converter where a very high-order antialias filter is required to allow most of the bandwidth to be used while ensuring sufficient attenuation at multiples of f_{CLKIN}.

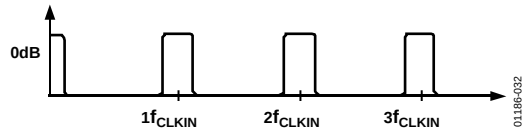


Figure 32. Digital Filter Frequency Response

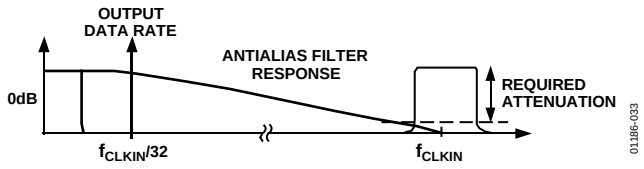


Figure 33. Frequency Response of Antialias Filter

APPLYING THE AD7723

ANALOG INPUT RANGE

The AD7723 has differential inputs to provide common-mode noise rejection. In unipolar mode, the analog input range is 0 to $8/5 \times V_{REF2}$, while in bipolar mode, the analog input range is $\pm 4/5 \times V_{REF2}$. The output code is twos complement binary in both modes with 1 LSB = 61 μV. The ideal input/output transfer characteristics for the two modes are shown in Figure 34. In both modes, the absolute voltage on each input must remain within the supply range AGND to AV_{DD}. The bipolar mode allows either single-ended or complementary input signals.

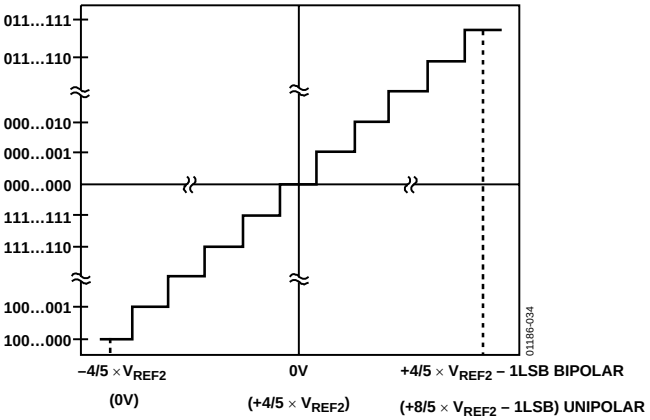


Figure 34. Bipolar (Unipolar) Mode Transfer Function

The AD7723 accepts full-scale, in-band signals. However, large scale out-of-band signals can overload the modulator inputs. Figure 35 shows the maximum input signal level as a function of frequency. A minimal single-pole, RC, antialias filter set to $f_{CLKIN}/24$ allows full-scale input signals over the entire frequency spectrum.

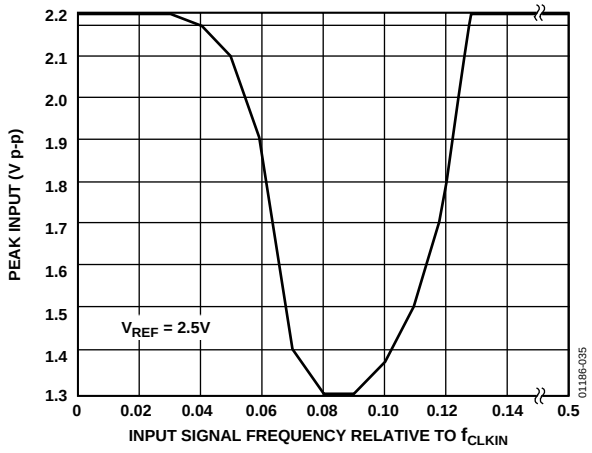


Figure 35. Peak Input Signal Level vs. Signal Frequency

ANALOG INPUT

The analog input of the AD7723 uses a switched capacitor technique to sample the input signal. For the purpose of driving the AD7723, an equivalent circuit of the analog inputs is shown in Figure 36. For each half clock cycle, two highly linear sampling capacitors are switched to both inputs, converting the input signal into an equivalent sampled charge. A signal source driving the analog inputs must be able to source this charge while also settling to the required accuracy by the end of each half-clock phase.

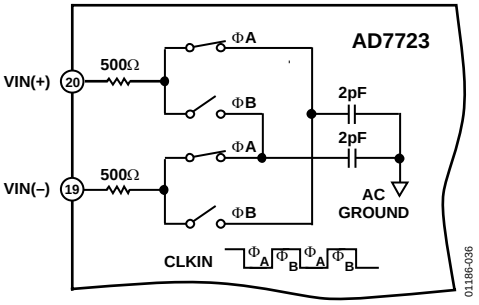


Figure 36. Analog Input Equivalent Circuit

DRIVING THE ANALOG INPUTS

To interface the signal source to the AD7723, at least one op amp is generally required. Choice of op amp is critical to achieving the full performance of the AD7723. The op amp not only has to recover from the transient loads that the ADC imposes on it, but it must also have good distortion characteristics and very low input noise. Resistors in the signal path can also add to the overall thermal noise floor, necessitating the choice of low value resistors.

Placing an RC filter between the drive source and the ADC inputs, as shown in Figure 37, has a number of beneficial effects. Transients on the op amp outputs are significantly reduced because the external capacitor now supplies the instantaneous charge required when the sampling capacitors are switched to the ADC input pins and input circuit noise at the sample images is now significantly attenuated, resulting in improved overall SNR. The external resistor serves to isolate the external capacitor from the ADC output, thus improving op amp stability while also isolating the op amp output from any remaining transients on the capacitor. By experimenting with different filter values, the optimum performance can be achieved for each application. As a guideline, the RC time constant (R × C) should be less than a quarter of the clock period to avoid nonlinear currents from the ADC inputs being stored on the external capacitor and degrading distortion. This restriction means that this filter cannot form the main antialias filter for the ADC.

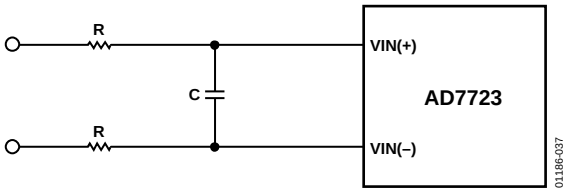


Figure 37. Input RC Network

With the unipolar input mode selected, just one op amp is required to buffer single-ended input signals. However, driving the AD7723 with complementary signals and with the bipolar input range selected has some distinct advantages: even-order harmonics in both the drive circuits and the AD7723 front end are attenuated and the peak-to-peak input signal range on both inputs is halved. Halving the input signal range allows some op amps to be powered from the same supplies as the AD7723. Although a complementary driver requires the use of two op amps per ADC, it may avoid the need to generate additional supplies just for these op amps.

Figure 38 and Figure 39 show two such circuits for driving the AD7723. Figure 38 is intended for use when the input signal is biased about 2.5 V, while Figure 39 is used when the input signal is biased about ground. While both circuits convert the input signal into a complementary signal, the circuit in Figure 39 also level shifts the signal so that both outputs are biased about 2.5 V. Suitable op amps include the AD8047, AD8044, AD8041, and its dual equivalent, the AD8042. The AD8047 has lower input noise than the AD8041/AD8042 but has to be supplied from a +7.5 V/−2.5 V supply. The AD8041/AD8042 typically degrades SNR from 90 dB to 88 dB but can be powered from the same single 5 V supply as the AD7723.

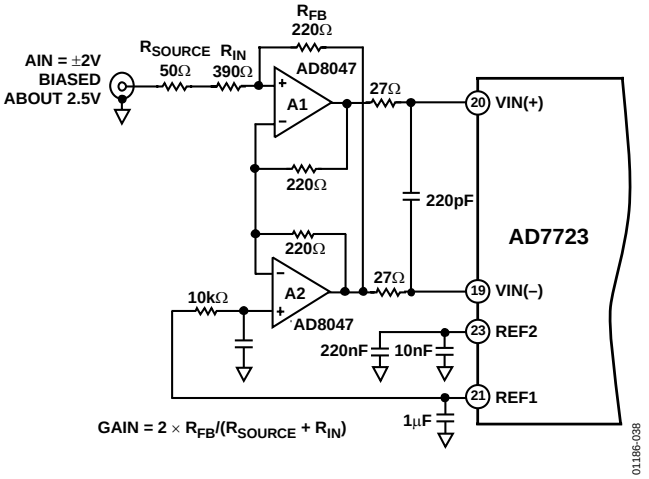


Figure 38. Single-Ended-to-Differential Input Circuit for Bipolar Mode Operation (Analog Input Biased About 2.5 V)

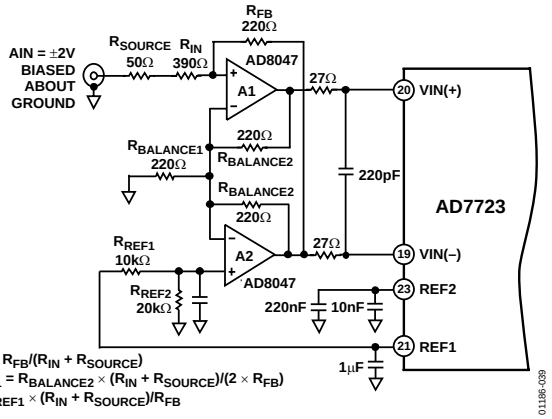


Figure 39. Single-Ended-to-Differential Input Circuit for Bipolar Mode Operation (Analog Input Biased About Ground)

APPLYING THE REFERENCE

The reference circuitry used in the AD7723 includes an on-chip 2.5 V band-gap reference and a reference buffer circuit. The block diagram of the reference circuit is shown in Figure 40. The internal reference voltage is connected to REF1 through a 3 kΩ resistor and is internally buffered to drive the analog modulator's switched cap DAC (REF2). When using the internal reference, a 1 µF capacitor is required between REF1 and AGND to decouple the band-gap noise. If the internal reference is required to bias external circuits, use an external precision op amp to buffer REF1.

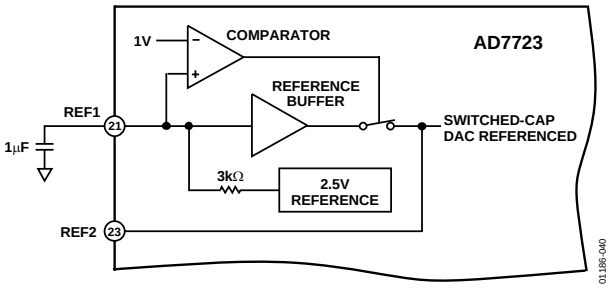


Figure 40. Reference Circuit Block Diagram

Where gain error or gain error drift requires the use of an external reference, the reference buffer in Figure 40 can be turned off by grounding the REF1 pin and the external reference can be applied directly to REF2 pin. The AD7723 accepts an external reference voltage between 1.2 V to 3.15 V. By applying a 3 V rather than a 2.5 V reference, SNR is typically improved by about 1 dB. Where the output common-mode range of the amplifier driving the inputs is restricted, the full-scale input signal span can be reduced by applying a lower than 2.5 V reference. For example, a 1.25 V reference would make the bipolar input span ±1 V but would degrade SNR.

In all cases, since the REF2 voltage connects to the analog modulator, a 220 nF and 10 nF capacitor must connect directly from REF2 to AGND. The external capacitor provides the charge required for the dynamic load presented at the REF2 pin (see Figure 41).

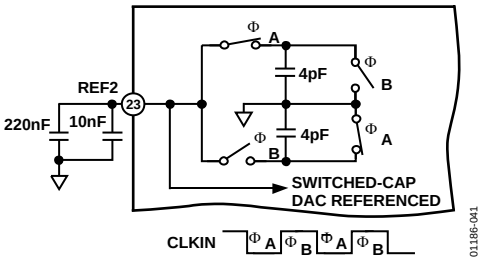


Figure 41. REF2 Equivalent Input Circuit

The AD780 is ideal to use as an external reference with the AD7723. Figure 42 shows a suggested connection diagram. Grounding Pin 8 on the AD780 selects the 3 V output mode.

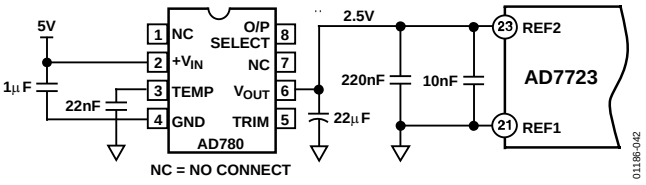


Figure 42. External Reference Circuit Connection

CLOCK GENERATION

The AD7723 contains an oscillator circuit to allow a crystal or an external clock signal to generate the master clock for the ADC. The connection diagram for use with a crystal is shown in Figure 43. Consult the manufacturer's recommendation for the load capacitors. To enable the oscillator circuit on board the AD7723, XTAL_OFF should be tied low.

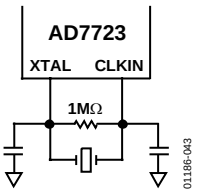


Figure 43. Crystal Oscillator Connection

When an external clock source is being used, the internal oscillator circuit can be disabled by tying XTAL_OFF high. A low phase noise clock should be used to generate the ADC sampling clock because sampling clock jitter effectively modulates the input signal and raises the noise floor. The sampling clock generator should be isolated from noisy digital circuits, grounded, and heavily decoupled to the analog ground plane.

The sampling clock generator should be referenced to the analog ground in a split ground system. However, this is not always possible because of system constraints. In many applications, the sampling clock must be derived from a higher frequency multipurpose system clock that is generated on the digital ground plane. If the clock signal is passed between its origin on a digital ground plane to the AD7723 on the analog ground plane, the ground noise between the two planes adds directly to the clock and produces excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling signal as a differential one, using either a small RF transformer or a high speed differential driver and a receiver such as PECL. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

SYSTEM SYNCHRONIZATION

The SYNC input provides a synchronization function for use in parallel or serial mode. SYNC allows the user to begin gathering samples of the analog input from a known point in time.

This allows a system using multiple AD7723s, operated from a common master clock, to be synchronized so that each ADC simultaneously updates its output register.

In a system using multiple AD7723s, a common signal to their sync inputs synchronizes their operation. On the rising edge of SYNC, the digital filter sequencer is reset to 0. The filter is held in a reset state until a rising edge on CLKIN senses SYNC low. A SYNC pulse, one CLKIN cycle long, can be applied synchronous to the falling edge of CLKIN. This way, on the next rising edge of CLKIN, SYNC is sensed low, the filter is taken out of its reset state, and multiple parts begin to gather input samples.

Following a SYNC, the modulator and filter need time to settle before data can be read from the AD7723. $\overline{\text{DRDY}}$ goes high following a synchronization and it remains high until valid data is available at the interface.

When operating in any of the serial modes, either SYNC or frame sync input (FSI) may be used to synchronize multiple AD7723 devices to a common master clock. The functionality of FSI is detailed in the Serial Interface section.

DATA INTERFACING

The AD7723 offers a choice of serial or parallel data interface options to meet the requirements of a variety of system configurations. In parallel mode, multiple AD7723s can easily be configured to share a common data bus. Serial mode is ideal when it is required to minimize the number of data interface lines connected to a host processor. In either case, careful attention to the system configuration is required to realize the high dynamic range available with the AD7723. Consult the recommendations in the Grounding and Layout section. The following recommendations for parallel interfacing also apply for the system design when using the serial mode.

PARALLEL INTERFACE

When using the AD7723, place a buffer/latch adjacent to the converter to isolate the converter's data lines from any noise that may be on the data bus. Even though the AD7723 has three state outputs, use of an isolation latch represents good design practice.

Figure 44 shows how the parallel interface of the AD7723 can be configured to interface with the system data bus of a microprocessor or a microcontroller, such as the MC68HC16 or 8XC251. With $\overline{CS}$ and $\overline{RD}$ tied permanently low, the data output bits are always active. When $\overline{DRDY}$ goes high for two clock cycles, the rising edge of $\overline{DRDY}$ is used to latch the conversion data before a new conversion result is loaded into the output data register. The falling edge of $\overline{DRDY}$ then sends an appropriate interrupt signal for interface control. Alternatively, if buffers are used instead of latches, the falling edge of $\overline{DRDY}$ provides the necessary interrupt when a new output word is available from the AD7723.

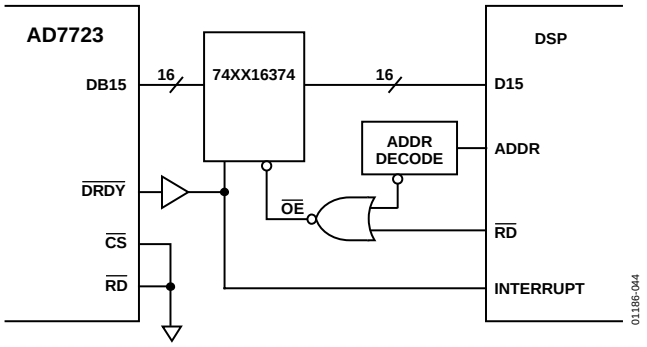


Figure 44. Parallel Interface Connection

SERIAL INTERFACE

The AD7723's serial data interface can operate in three modes, depending on the application requirements. The timing diagrams in Figure 4, Figure 5, and Figure 6 show how the AD7723 may be used to transmit its conversion results. Table 3 shows the control inputs required to select each serial mode and the digital filter operating mode. The AD7723 operates solely in the master mode, providing three serial data output pins for transfer of the conversion results. The serial data clock output, SCO, serial data output, SDO, and frame sync output, FSO, are all synchronous with CLKIN. FSO is continuously output at the conversion rate of the ADC.

Serial data shifts out of the SDO pin synchronous with SCO. The FSO is used to frame the output data transmission to an external device. An output data transmission is either 16 or 32 SCO cycles in duration (see Table 3). Serial data shifts out of the SDO pin, MSB first, LSB last, for a duration of 16 SCO cycles. In Serial Mode 1, SDO outputs 0s for the last 16 SCO cycles of the 32-cycle data transmission frame.

The clock format pin, CFMT, selects the active edge of SCO. With CFMT tied logic low, the serial interface outputs FSO and SDO change state on the SCO rising edge and are valid on the falling edge of SCO. With CFMT set high, FSO and SDO change state on the falling SCO edge and are valid on the SCO rising edge.

The frame sync input, FSI, can be used if the AD7723 conversion process must be synchronized to an external source. FSI allows the conversion data presented to the serial interface to be a filtered and decimated result derived from a known point in time. A common frame sync signal can be applied to two or more AD7723s to synchronize them to a common master clock.

When FSI is applied for the first time, the digital filter sequencer counter is reset to 0, the AD7723 interrupts the current data transmission, reloads the output shift register, resets SCO, and transmits the conversion result. Synchronization starts immediately and the following conversions are invalid while the digital filter settles. FSI can be applied once after power-up, or it can be a periodic signal, synchronous to CLKIN, occurring every 32 CLKIN cycles. Subsequent FSI inputs applied every 32 CLKIN cycles do not alter the serial data transmission and do not reset the digital filter sequencer counter. FSI is an optional signal; if synchronization is not required, FSI can be tied to a logic low and the AD7723 generates FSO outputs.

In Serial Mode 1, the control input, SFMT, can be used to select the format for the serial data transmission (see Figure 4). FSO is either a pulse, approximately one SCO cycle in duration, or a square wave with a period of 32 SCO cycles. With a logic low level on SFMT, FSO pulses high for one SCO cycle at the beginning of a data transmission frame. With a logic high level on SFMT, FSO goes low at the beginning of a data transmission frame and returns high after 16 SCO cycles.

Note that in Serial Mode 1, FSI can be used to synchronize the AD7723 if SFMT is set to a logic high. If SFMT is set low, the FSI input has no effect on synchronization.

In Serial Mode 2 and Serial Mode 3, SFMT should be tied high. TSI and DOE should be tied low in these modes. The FSO is a pulse, approximately one SCO cycle in duration, occurring at the beginning of the serial data transmission.

TWO-CHANNEL MULTIPLEXED OPERATION

Two additional serial interface control pins, DOE and TSI, are provided to allow the serial data outputs of two AD7723s, to easily share one serial data line when operating in Serial Mode 1. Figure 45 shows the connection diagram. Since a serial data transmission frame lasts 32 SCO cycles, two ADCs can share a single data line by alternating transmission of their 16-bit output data onto one SDO pin.

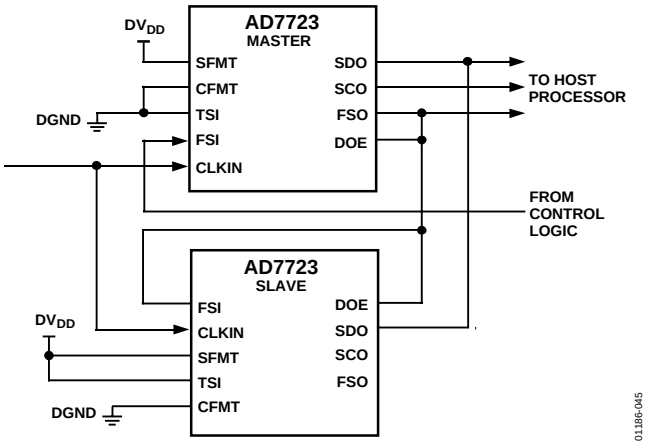


Figure 45. Serial Mode 1 Connection for Two-Channel Multiplexed Operation

The data output enable pin, DOE, controls the SDO output buffer. When the logic level on DOE matches the state of the TSI pin, the SDO output buffer drives the serial data line; otherwise, the output of the buffer goes high impedance. The serial format pin, SFMT, is set high to choose the frame sync output format. The clock format pin, CFMT, is set low so that serial data is made available on SDO after the rising edge of SCO and can be latched on the SCO falling edge.

The master device is selected by setting TSI to a logic low and connecting its FSO to DOE. The slave device is selected with its TSI pin tied high and both its FSI and DOE controlled from the master's FSO. Since the FSO of the master controls the DOE input of both the master and slave, one ADC's SDO is active while the other is high impedance (Figure 46). When the master transmits its conversion result during the first 16 SCO cycles of a data transmission frame, the low level on DOE sets the slave's SDO high impedance. Once the master completes transmitting its conversion data, its FSO goes high and triggers the slave's FSI to begin its data transmission frame.

Since FSO pulses are gated by the release of FSI (going low) and the FSI of the slave device is held high during its data transmission, the FSO from the master device must be used for connection to the host processor.

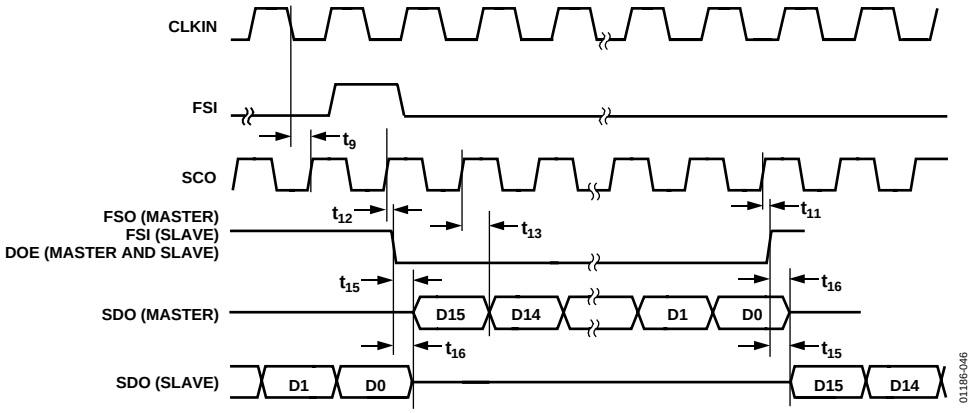


Figure 46. Serial Mode 1 Timing for Two-Channel Multiplexed Operation

SERIAL INTERFACE TO DSPs

In serial mode, the AD7723 can be directly interfaced to several industry-standard digital signal processors. In all cases, the AD7723 operates as the master with the DSP operating as the slave. The AD7723 provides its own serial clock (SCO) to transmit the digital word on the SDO pin to the DSP. The AD7723 also generates the frame synchronization signal that synchronizes the transfer of the 16-bit word from the AD7723 to the DSP. Depending on the serial mode used, SCO has a frequency equal to CLKIN or equal to CLKIN/2. When SCO equals 19.2 MHz, the AD7723 can be interfaced to the Analog Devices ADSP-2106x SHARC DSP. With a 19.2 MHz master clock and SCO equal to CLKIN/2, the AD7723 can be interfaced with the ADSP-21xx family of DSPs, the DSP56002, and the TMS320C5x-57. When the AD7723 is used in the HALF_PWR Mode, that is, CLKIN is less than 10 MHz, then the AD7723 can be used with DSPs, such as the TMS320C20/TMS320C25 and the DSP56000/DSP56001.

AD7723 TO ADSP-21xx INTERFACE

Figure 47 shows the interface between the ADSP-21xx and the AD7723. The AD7723 is operated in Mode 2 so that SCO = CLKIN/2. For the ADSP-21xx, the bits in the serial port control register should be set up as RFSR = 1 (a frame sync is needed for each transfer), SLEN = 15 (16-bit word lengths), RFSW = 0 (normal framing mode for receive operations), INVRFS = 0 (active high RFS), IRFS = 0 (external RFS), and ISCLK = 0 (external serial clock).

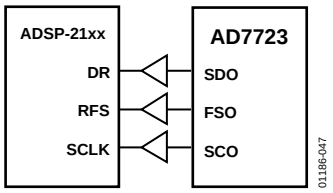


Figure 47. AD7723 to ADSP-21xx Interface

AD7723 TO SHARC INTERFACE

The interface between the AD7723 and the ADSP-2106x SHARC DSP is the same as shown in Figure 47, but the DSP is configured as follows: SLEN = 15 (16-bit word transfers), SENDN = 0 (the MSB of the 16-bit word is received by the DSP first), ICLK = 0 (an external serial clock is used), RFSR = 0 (a frame sync is required for every word transfer), IRFS = 0 (the receive frame sync signal is external), CKRE = 0 (the receive data is latched into the DSP on the falling clock edge), LAFS = 0 (the DSP begins reading the 16-bit word after the DSP has identified the frame sync signal rather than the DSP reading the word at the same instant as the frame sync signal is identified), and LRFS = 0 (RFS is active high). The AD7723 can be used in Mode 1, Mode 2, or Mode 3 when interfaced to the ADSP-2106x SHARC DSP.

AD7723 TO DSP56002 INTERFACE

Figure 48 shows the AD7723 to DSP56002 interface. To interface the AD7723 to the DSP56002, the ADC is operated in Mode 2 when the ADC is operated with a 19.2 MHz clock. The DSP56002 is configured as follows: SYN = 1 (synchronous mode), SCD1 = 0 (RFS is an input), GCK = 0 (a continuous serial clock is used), SCKD = 0 (the serial clock is external), WL1 = l, WL0 = 0 (transfers is 16 bits wide), FSL1 = 0, and FSL0 = 1 (the frame sync is active at the beginning of each transfer). Alternatively, the DSP56002 can be operated in asynchronous mode (SYN = 0).

In this mode, the serial clock for the receive section is input to the SCO pin. This is accomplished by setting Bit SCDO to 0 (external Rx clock).

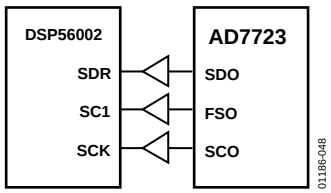


Figure 48. AD7723 to DSP56002 Interface

AD7723 TO TMS320C5x INTERFACE

Figure 49 shows the AD7723 to TMS320C5x interface. For the TMS320C5x, FSR and CLKR are automatically configured as inputs. The serial port is configured as follows: FO = 0 (16-bit word transfers) and FSM = 1 (a frame sync occurs for each transfer).

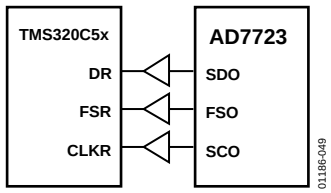


Figure 49. AD7723 to TMS320C5x Interface

GROUNDING AND LAYOUT

The analog and digital power supplies to the AD7723 are independent and separately pinned out to minimize coupling between the analog and digital sections within the device. The AD7723 AGND and DGND pins should be soldered directly to a ground plane to minimize series inductance. In addition, the ac path from any supply pin or reference pin (REF1 and REF2) through its decoupling capacitors to its associated ground must be made as short as possible (Figure 50). To achieve the best decoupling, place surface-mount capacitors as close as possible to the device, ideally right up against the device pins.

All ground planes must not overlap to avoid capacitive coupling. The AD7723's digital and analog ground planes must be connected at one place by a low inductance path, preferably right under the device. Typically, this connection is either a trace on the printed circuit board of 0.5 cm wide when the ground planes are on the same layer, or 0.5 cm wide minimum plated through holes when the ground planes are on different layers. Any external logic connected to the AD7723 should use a ground plane separate from the AD7723's digital ground plane. These two digital ground planes should also be connected at just one place.

Separate power supplies for AV_{DD} and DV_{DD} are also highly desirable. The digital supply pin DV_{DD} should be powered from a separate analog supply, but if necessary, DV_{DD} may share its power connection to AV_{DD}, as shown in the connection diagram in Figure 50. The ferrites are also recommended to filter high frequency signals from corrupting the analog power supply.

A minimum etch technique is generally best for ground planes because it gives the best shielding. Noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. In waveform sampling and reconstruction systems, the sampling clock (CLKIN) is as vulnerable to noise as any analog signal. CLKIN should be isolated from the analog and digital systems. Fast switching signals like clocks should be shielded with their associated ground to avoid radiating noise to other sections of the board, and clock signals should never be routed near the analog inputs.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD7723 to shield it from noise coupling. The power supply lines to the AD7723 should use as large a trace as possible (preferably a plane) to provide a low impedance path and reduce the effects of glitches on the power supply line. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board.

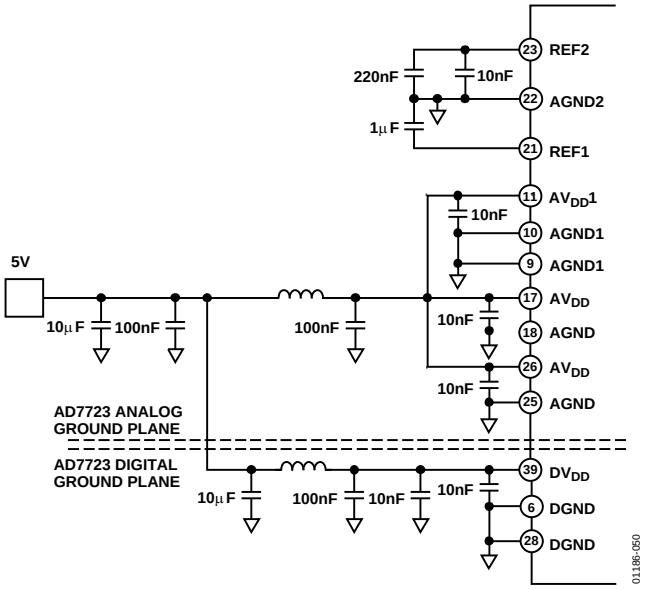
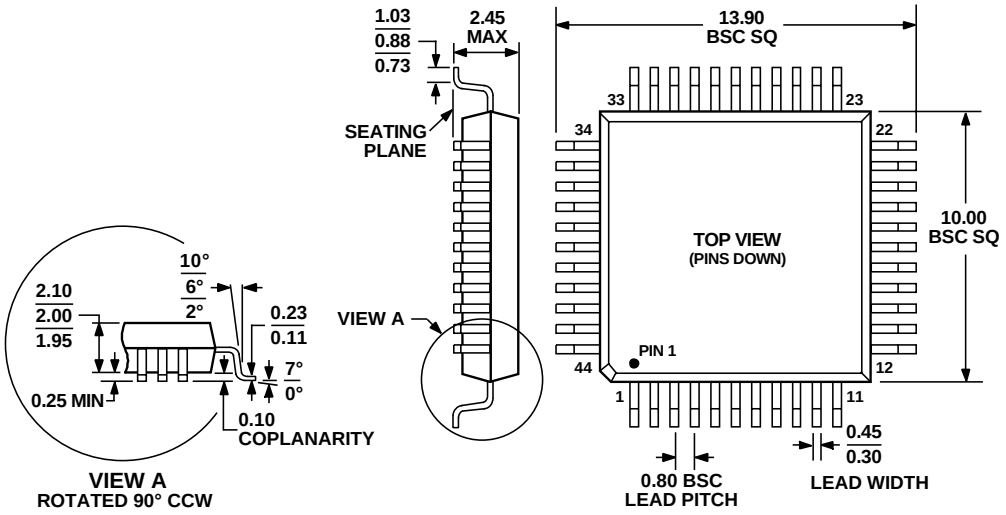


Figure 50. Reference and Power Supply Decoupling

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-112-AA-1

Figure 51. 44-Lead Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline
AD7723BS	–40°C to +85°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
AD7723BS-REEL	–40°C to +85°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
AD7723BSZ[1]	–40°C to +85°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
AD7723BSZ-REEL[1]	–40°C to +85°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
EVAL-AD7723CB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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