THE DATASHEET OF

DS125BR111RTWT

www.win-source.net 0086-755-83957316

DS125BR111 Low Power 12.5 Gbps 1-Lane Linear Repeater with Equalization

1 Features

- Low 65 mW/Channel (typ) Power Consumption
- Supports Link Training
- Supports Out-of-Band (OOB) Signaling
- Advanced Signal Conditioning I/O
  - Receive CTLE up to 10 dB at 6 GHz
  - Linear Output Driver
  - Output Voltage Range over 1200 mV
- Programmable via Pin Selection, EEPROM, or SMBus Interface
- Single Supply Voltage: 2.5 V or 3.3 V
- −40°C to 85°C Operating Temperature Range
- Flow-thru Pinout in 4 mm × 4 mm 24-pin Leadless WQFN Package

2 Applications

- SAS-1/2/3 and SATA-1/2/3
- PCI Express 1/2/3
- Other Proprietary Interfaces up to 12.5 Gbps

3 Description

The DS125BR111 is an extremely low power high performance repeater/redriver designed to support 1-lane carrying high speed interface up to 12.5 Gbps. The receiver's continuous time linear equalizer (CTLE) provides a boost of 3-10 dB at 6 GHz in each channel. When operating in SAS-3 or PCIe Gen-3 applications, the DS125BR111 preserves transmit signal characteristics allowing the host controller and the end point to negotiate transmit equalizer coefficients. Transparency to the link training protocol maximizes the flexibility of the physical placement of the device within the interconnect and improves overall channel performance.

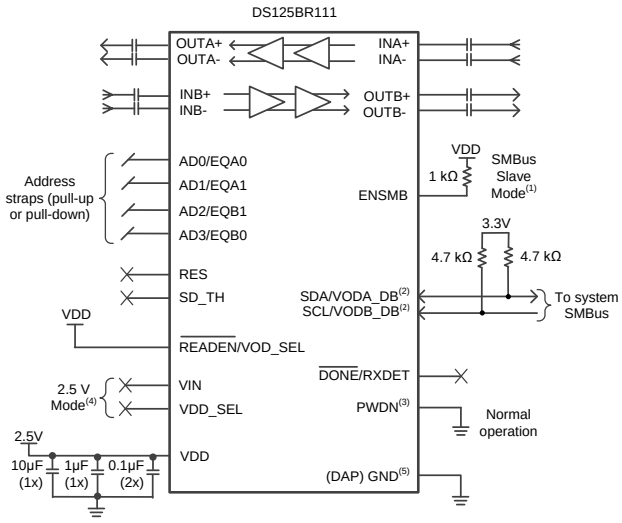
The programmable settings can be applied easily via pins, software (SMBus or I2C), or loaded via an external EEPROM. In EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS125BR111	WQFN (24)	4.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



(1) Schematic requires different connections for SMBus Master Mode and Pin Mode
(2) SMBus signals need to be pulled up elsewhere in the system
(3) PWDN pin can alternatively be driven by a control device (i.e. FPGA)
(4) Schematic requires different connections for 3.3 V mode
(5) A minimum of 4 vias are recommended for proper thermal and electrical performance

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2014) to Revision C — **Page**

- Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1

Changes from Revision A (January 2014) to Revision B — **Page**

- Changed Features ... 1

Changes from Original (April 2013) to Revision A — **Page**

- Changed layout of National Data Sheet to TI format ... 1

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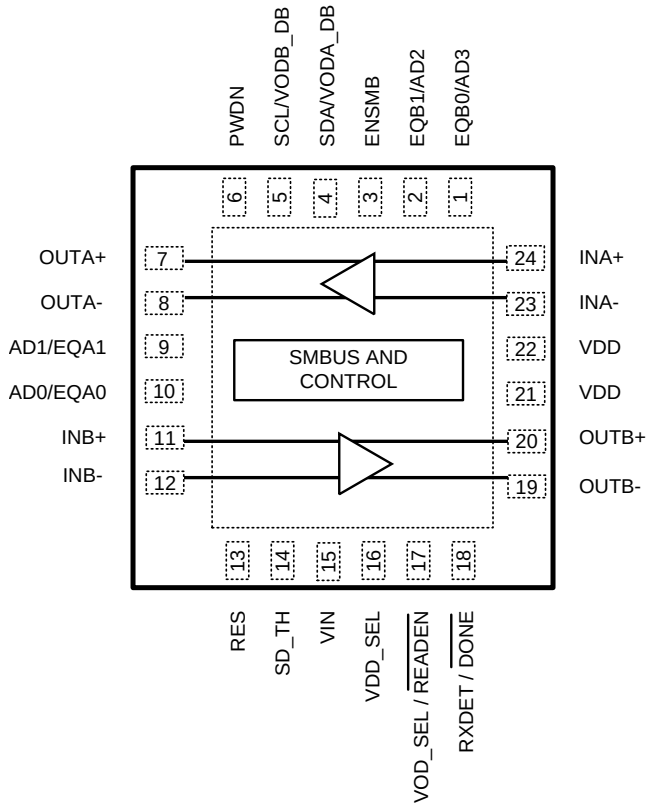
6 Pin Configuration and Functions

24 Pin
Package RTW
Top View



The center DAP on the package bottom is the only device GND connection. This pad must be connected to GND through multiple (minimum of 4) vias to ensure optimal electrical and thermal performance.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DIFFERENTIAL HIGH SPEED I/O			
INB+, INB-	11, 12	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50 Ω termination resistor connects INB+ to VDD and INB- to VDD when enabled by RXDET control logic. AC coupling required on high-speed I/O
OUTB+, OUTB-	20, 19	O	Inverting and non-inverting 50 Ω driver outputs. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
INA+, INA-	24, 23	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50 Ω termination resistor connects INA+ to VDD and INA- to VDD when enabled by RXDET control logic. AC coupling required on high-speed I/O
OUTA+, OUTA-	7, 8	O	Inverting and non-inverting 50 Ω driver outputs. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL PINS — SHARED (LVCMOS)			
ENSMB	3	I, 4-LEVEL, LVCMOS	System Management Bus (SMBus) enable Pin Tie 1 kΩ to VDD = Register Access SMBus Slave mode FLOAT = Read External EEPROM (Master SMBus Mode) Tie 1 kΩ to GND = Pin Mode
ENSMB = Float or 1 (SMBus MODEs)			
SCL	5	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode SMBus clock input Pin is enabled (slave mode). Clock output when loading EEPROM configuration (master mode).
SDA	4	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bidirectional SDA Pin is enabled. Data input or open drain output. External pull-up required as per SMBus protocol (typically in the 2 kΩ to 5 kΩ range). This pin is 3.3 V-tolerant.
AD0-AD3	10, 9, 2, 1	I, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these Pins are the user set SMBus slave address inputs.
$\overline{\text{READEN}}$	17	I, LVCMOS	ENSMB = Float: When using an External EEPROM, a logic low on this pin starts the load from the external EEPROM ENSMB = 1: When using SMBus Slave Mode the VOD_SEL/$\overline{\text{READEN}}$ pin must be tied Low for the AD[3:0] to be active. If this pin is tied High or Floated an address of 0xB0 will be used for the DS125BR111.
$\overline{\text{DONE}}$	18	O, LVCMOS	When using an External EEPROM (ENSMB = Float), Valid Register Load Status Output HIGH = External EEPROM load failed or incomplete LOW = External EEPROM load passed
ENSMB = 0 (PIN MODE)			
EQA0 EQB0	10 1	I, 4-LEVEL, LVCMOS	EQA0 and EQB0 control the level of equalization of the A/B directions. The Pins are defined as EQx0 only when ENSMB is de-asserted (low). When ENSMB goes high the SMBus registers provide independent control of each channel. See Table 4.
EQA1 EQB1	9 2	I, 4-LEVEL, LVCMOS	EQA1 and EQB1 are not used in the DS125BR111 design. These pins should always be tied to GND.
VODA_DB	4	I, 4-LEVEL, LVCMOS	VODA_DB controls the CHA output amplitude dynamic range, for SAS and PCIe applications it should be held Low. The Pin is defined as VODA_DB only when ENSMB is de-asserted (low). When ENSMB goes high the SMBus registers provide control of each channel, pin 4 is converted to SDA. See Table 5.
VODB_DB	5	I, 4-LEVEL, LVCMOS	VODB_DB controls the CHB output amplitude dynamic range, for SAS and PCIe applications it should be held Low. The Pin is defined as VODB_DB only when ENSMB is de-asserted (low). When ENSMB goes high the SMBus registers provide control of each channel, pin 5 is converted to SCL. See Table 5.
SD_TH	14	I, 4-LEVEL, LVCMOS	Controls the internal Signal Detect Threshold. This detection threshold is for system debug only and does not control the high speed datapath. See Table 3.
VOD_SEL	17	I, 4-LEVEL, LVCMOS	VOD_SEL controls the low frequency ratio of input voltage to output voltage amplitude. See Table 5.
RXDET	18	I, 4-LEVEL, LVCMOS	The RXDET Pin controls the receiver detect function. Depending on the input level, a 50 Ω or > 50 kΩ termination to the power rail is enabled. In a SAS/SATA system RXDET should be set to a Logic "1" state to keep the termination always enabled. **The RXDET pin only controls the RXDET function in PIN MODE. PCIe applications which require SMBus Mode functionality must utilize a specific register write sequence documented in PCIe Applications . If this sequence is not utilized, SMBus configuration modes will default the input terminations to active (50 Ω). See Table 2 .**

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL PINS — BOTH PIN AND SMBus MODES (LVCMOS)			
RES	13	I, 4-LEVEL, LVCMOS	Reserved: This input must be left Floating.
VDD_SEL	16	I, FLOAT	Controls the internal regulator Float = 2.5 V mode Tie GND = 3.3 V mode
PWDN	6	I, LVCMOS	Tie High = Low power - power down Tie GND = Normal Operation See Table 2.
POWER (See Figure 11)			
VIN	15	Power	In 3.3 V mode, feed 3.3 V to VIN In 2.5 V mode, leave floating.
VDD	21, 22	Power	Power supply pins CML/analog 2.5 V mode, connect to 2.5 V 3.3 V mode, decouple each VDD pin with 0.22 µF cap to GND
GND	DAP	Power	Ground pad (DAP - die attach pad).

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply Voltage (VDD - 2.5 V)	-0.5	+2.75	V
Supply Voltage (VIN - 3.3 V)	-0.5	+4.0	V
LVCMOS Input/Output Voltage	-0.5	+4.0	V
CML Input Voltage	-0.5	VDD + 0.5	V
CML Input Current	-30	+30	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-40	125	°C
T_{solder}	Lead Temperature Range Soldering (4 sec.) (1)			260	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	-5000	5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	-1250	1250	

(1) For soldering specifications: See application note SNOA549.
(2) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (2.5 V mode)	2.375	2.5	2.625	V
Supply Voltage (3.3 V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V
Supply Noise up to 50 MHz (1)			100	mVp-p

(1) Allowed supply noise (mVp-p sine wave) under typical conditions.

7.4 Thermal Information

THERMAL METRIC (1)		DS125BR111 RTW 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	13.4	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	13.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{DD}	Current Consumption	VODx_DB = 0, EQ = 0, VOD_SEL = 1, RXDET = 1, PWDN = 0 V_{IN} = 2.625 or 3.6 V		40	60	mA
	Power Down Current Consumption	PWDN = 1		7	13	mA
V_{DD}	Integrated LDO Regulator	V_{IN} = 3.0 - 3.6 V	2.375	2.5	2.625	V
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{ih25}	High Level Input Voltage	2.5 V Supply Mode	1.7		V_{DD}	V
V_{ih33}	High Level Input Voltage	3.3 V Supply Mode	1.7		V_{IN}	V
V_{il}	Low Level Input Voltage		0		0.7	V
V_{oh}	High Level Output Voltage ($\overline{DONE}$ pin)	I_{oh} = −4 mA	2.0			V
V_{ol}	Low Level Output Voltage ($\overline{DONE}$ pin)	I_{ol} = 4 mA			0.4	V
I_{ih}	Input High Current (PWDN pin)	V_{IN} = 3.6 V, LVCMOS = 3.6 V	-15		+15	µA
I_{il}	Input Low Current (PWDN pin)	V_{IN} = 3.6 V, LVCMOS = 0 V	-15		+15	µA
4-LEVEL INPUT DC SPECIFICATIONS						
I_{ih}	Input High Current with internal resistors (4–level input pin)	V_{IN} = 3.6 V, LVCMOS = 3.6 V	+20		+80	µA
I_{il}	Input Low Current with internal resistors (4–level input pin)	V_{IN} = 3.6 V, LVCMOS = 0 V	-160		-40	µA
V_{th}	Threshold 0 / R	V_{DD} = 2.5 V (2.5 V supply mode) Internal LDO Disabled See Table 1 for details		0.40		V
	Threshold R / Float			1.25		
	Threshold Float / 1			2.1		
	Threshold 0 / R	V_{IN} = 3.3 V (3.3 V supply mode) Internal LDO Enabled See Table 1 for details.		0.55		V
	Threshold R / Float			1.65		
	Threshold Float / 1			2.7		
CML RECEIVER INPUTS (IN_n+, IN_n-)						
$RL_{RX-diff}$	RX Differential return loss	SDD11 10 MHz		-19		dB
		SDD11 2 GHz		-14		
		SDD11 6-11.1 GHz		-8		
RL_{RX-cm}	RX Common mode return loss	0.05 - 5 GHz		-10		dB
Z_{RX-dc}	RX DC common mode impedance	Tested at VDD = 2.5 V	40	50	60	Ω
$Z_{RX-diff-dc}$	RX DC differential mode impedance	Tested at VDD = 2.5 V	80	100	120	Ω
$V_{RX-signal-det-diff-pp}$	Signal detect assert level	SD_TH = F (float), 0101 pattern at 12 Gbps		50		mVp-p
$V_{RX-idle-det-diff-pp}$	Signal detect de-assert level	SD_TH = F (float), 0101 pattern at 12 Gbps		37		mVp-p
HIGH SPEED OUTPUTS						
$T_{TX-RISE-FALL}$	Transmitter rise/fall time (1)	20% to 80% of differential output voltage		40		ps
$T_{RF-MISMATCH}$	Transmitter rise/fall mismatch (2)	20% to 80% of differential output voltage		0.01		UI

(1) Rise / Fall time measurements will vary based on EQ setting, Input Amplitude, and input edge rate.
(2) Mismatch between rise time and fall time for a given channel.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$RL_{TX-DIFF}$	TX Differential return loss	SDD22 10 MHz - 2 GHz		-15		dB
		SDD22 5.5 GHz		-12		
		SDD22 11.1 GHz		-10		dB
RL_{TX-CM}	TX Common mode return loss	0.05 - 5 GHz		-10		dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance			100		Ω
$I_{TX-SHORT}$	Transmitter short circuit current limit	Total current, output shorted to VDD or GND		20		mA
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle				100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltage between TX+ and TX-				25	mV
HIGH SPEED OUTPUTS						
$V_{TX-diff1-pp}$	Output Voltage Differential Swing	Differential measurement with OUTx+ and OUTx-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, VODx_DB = 0 dB, VID = 600 mVp-p VOD = 001'b (0.7*VID)	440	500	550	mVp-p
$V_{TX-diff2-pp}$	Output Voltage Differential Swing	Differential measurement with OUTx+ and OUTx-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, VODx_DB = 0 dB, VID = 1000 mVp-p VOD = 001'b (0.7*VID) (3)	630	700	740	mVp-p
$V_{TX-diff3-pp}$	Output Voltage Differential Swing	Differential measurement with OUTx+ and OUTx-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, VODx_DB = 0 dB, VID = 600 mVp-p VOD = 111'b (1.05*VID) (3)	570	650	740	mVp-p
$V_{TX-diff4-pp}$	Output Voltage Differential Swing	Differential measurement with OUTx+ and OUTx-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, VODx_DB = 0 dB, VID = 1000 mVp-p VOD = 111'b (1.05*VID) (3)	800	1010	1215	mVp-p
$T_{TX-IDLE-DATA}$	Time to transition to valid differential signal after idle	VID = 1.0 Vp-p, 3 Gbps		0.04		ns
$T_{TX-DATA-IDLE}$	Time to transition to idle after differential signal	VID = 1.0 Vp-p, 3 Gbps		0.70		ns
T_{PD}	Differential Propagation Delay	EQ = Level 1 to Level 4		70		ps

(3) The output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level and the frequency content. The DS125BR111 repeater is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support handshake negotiation link training.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EQUALIZATION						
DJE1	Residual Deterministic Jitter at 6 Gbps	Input: 5" Differential Stripline, 5mil trace width, FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 0x01,** VOD = 111'b, VODx_DB = 0 dB		0.06		UI
DJE2	Residual Deterministic Jitter at 12 Gbps	Input: 5" Differential Stripline, 5mil trace width, FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 0x01,** VOD = 111'b, VODx_DB = 0 dB		0.12		UI
RJ_{ADD1}	Additive Random Jitter (4)	Evaluation Module (EVM) only, FR4, VID = 0.8 Vp-p, PRBS7, **EQ = 0x00,** VOD = 111'b, VODx_DB = 0 dB		< 300		fs RMS
RJ_{ADD2}	Additive Random Jitter (4)	Input: 10" Differential Stripline, 5 mil trace width, FR4, VID = 0.8 Vp-p, PRBS7, **EQ = 0x03,** VOD = 111'b, VODx_DB = 0 dB		< 400		fs RMS

(4) Additive random jitter is given in RMS value by the following equation: $RJ_{ADD} = \sqrt{[(\text{Output Jitter})^2 - (\text{Input Jitter})^2]}$. The typical source input jitter for these measurements is 150 fs RMS.

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7.6 Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
V_{OL}	Output Low Voltage	SDA or SCL, I_{OL} = 1.25 mA	0		0.36	V
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{IH\text{-}pin}$	Input Leakage Per Device pin		+20		+150	µA
$I_{IL\text{-}pin}$	Input Leakage Per Device pin		-160		-40	µA
C_I	Capacitance for SDA and SCL	See (1)(2)		< 5		pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5 V ± 5% OR 3.3 V ± 10%	Pullup V_{DD} = 3.3 V (1)(2)(3)		2000		Ω
		Pullup V_{DD} = 2.5 V (1)(2)(3)		1000		Ω

(1) Typical value.
(2) Recommended maximum capacitance load per bus segment is 400 pF.
(3) Maximum termination voltage should be identical to the device supply voltage.

7.7 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode) (1)	280	400	520	kHz
t_{FALL}	SCL or SDA Fall Time	Read operation RPU = 4.7 kΩ, Cb < 50 pF		60		ns
t_{RISE}	SCL or SDA Rise Time	Read operation RPU = 4.7 kΩ, Cb < 50 pF		140		ns
t_F	Clock/Data Fall Time	See (2)			300	ns
t_R	Clock/Data Rise Time	See (2)			1000	ns

(1) The external EEPROM device address byte must be 0xA0 and capable of 1 MHz operation at 2.5 V and 3.3 V.
(2) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

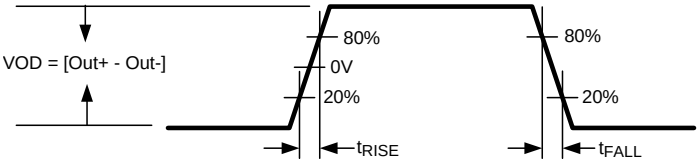

Figure 1. Output Rise And Fall Transition Time

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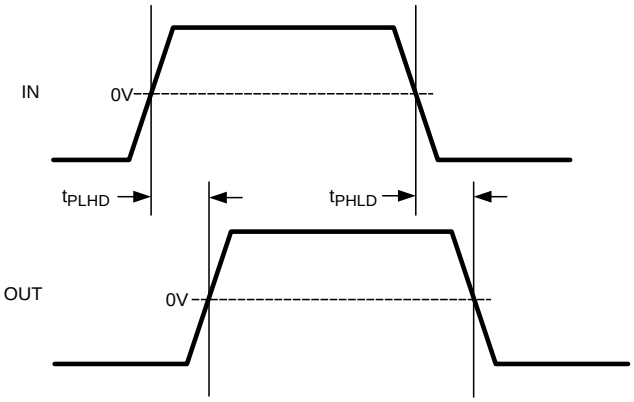


Figure 2. Propagation Delay Timing Diagram

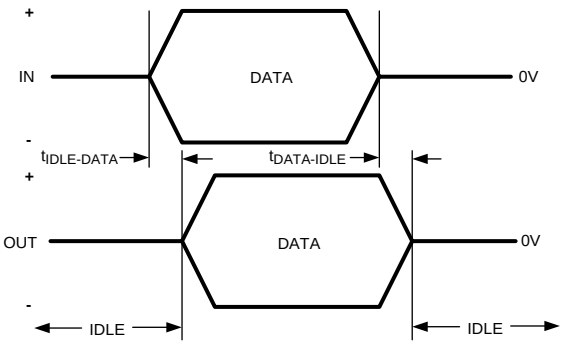


Figure 3. Transmit Idle-Data and Data-Idle Response Time

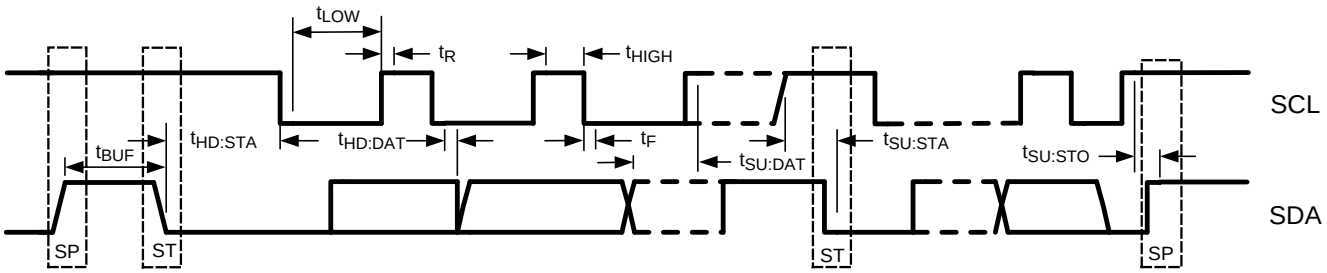
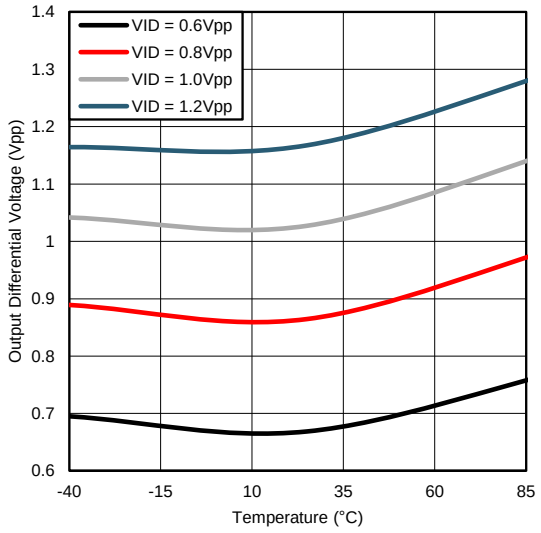


Figure 4. SMBus Timing Parameters

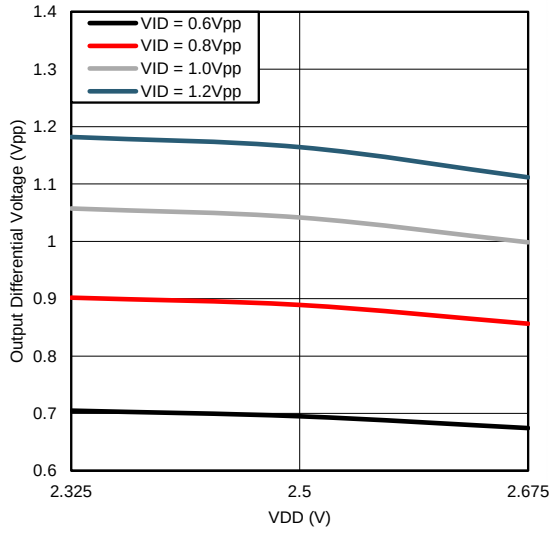
7.8 Typical Characteristics



Test Conditions

Data Rate/Test Pattern:	1.5625 Gbps / 101010 Repeating Pattern
VOD:	Level 6
EQ:	Level 1
VOD_DB:	000'b
VDD:	2.5 V

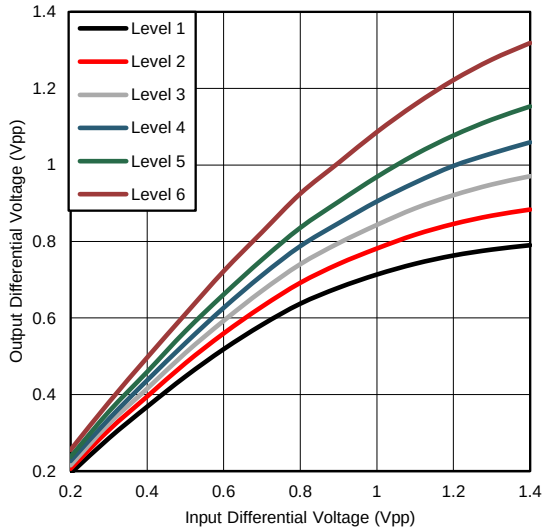
Figure 5. Typical VOD vs. VDD



Test Conditions

Data Rate/Test Pattern:	1.5625 Gbps / 101010 Repeating Pattern
VOD:	Level 6
EQ:	Level 1
VOD_DB:	000'b
Temperature:	25°C

Figure 6. Typical VOD vs. Temperature



Test Conditions

Data Rate/Test Pattern:	1.5625 Gbps / 101010 Repeating Pattern
EQ:	Minimum
VOD_DB:	000'b
Temperature:	25°C
VDD:	2.5 V

Figure 7. Typical VOD Level vs. VID

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8 Detailed Description

8.1 Overview

The DS125BR111 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS125BR111 operates in 3 modes: pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register information from external EEPROM; please refer to SMBus Master Mode for additional information.

8.2 Functional Block Diagram

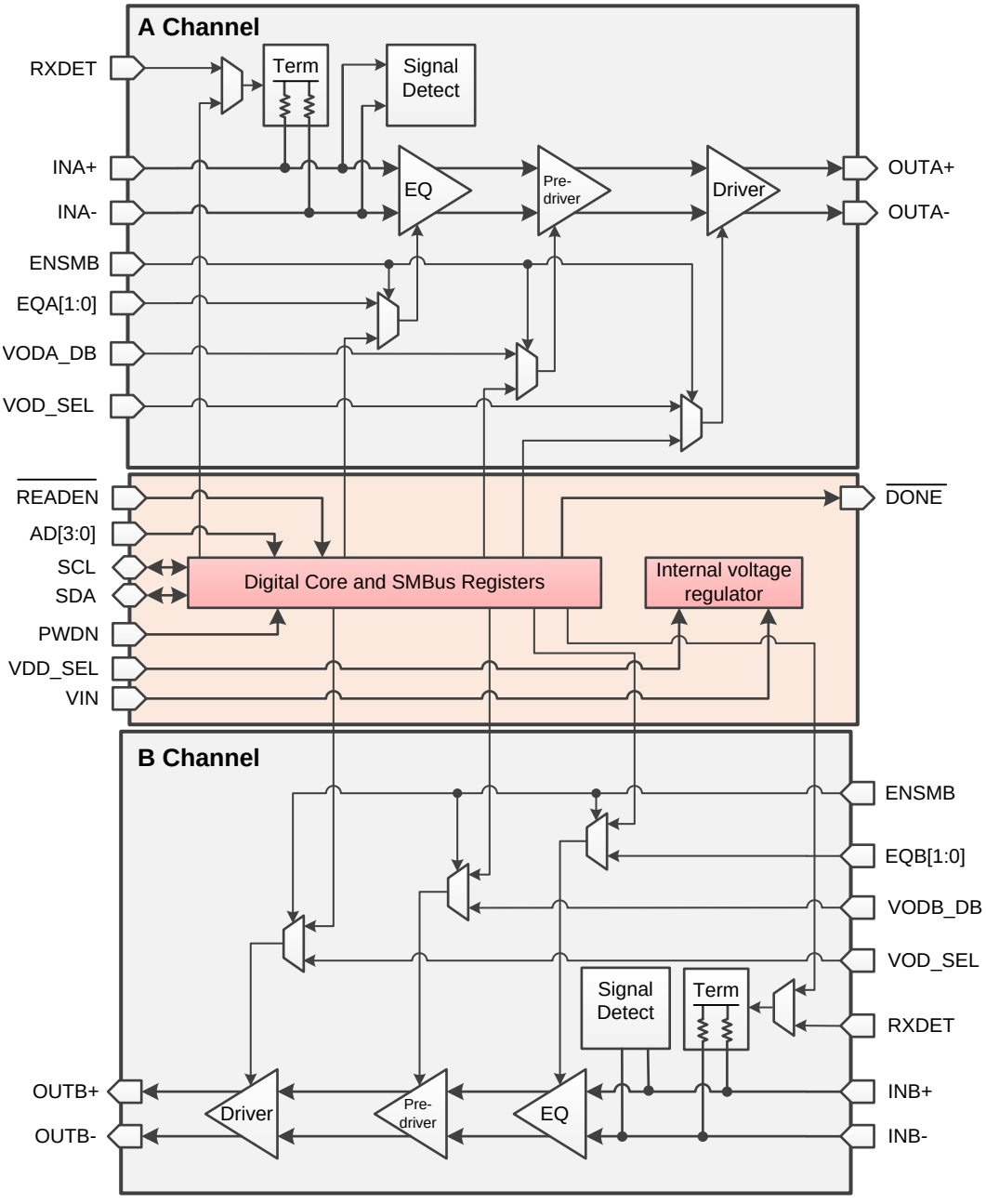

Figure 8. Channel A/B Datapath

Functional Block Diagram (continued)

8.2.1 Functional Datapath Blocks

The DS125BR111 datapath is designed to provide transparency for Rx-Tx training in SAS-3, PCIe Gen3, and other standards. The datapath includes input continuous time linear equalization coupled with a linear driver. This combination has a high level of transparency, achieving greater drive distance in applications which utilize Rx-Tx training.

The DS125BR111 datapath is optimized to work as a transparent driver and a transparent receiver. The typical DS125BR111 system placement breaks a long transmission line into two pieces. This often leads to one short and one long piece. While the DS125BR111 can be placed anywhere in the channel, to maximize channel extension placement with some attenuation on the DS125BR111 inputs works best. Refer to *Application and Implementation* for more application information regarding device placement.

8.3 Feature Description

The 4-level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30 kΩ pull-up and a 60 kΩ pull-down connected to the package Pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1 kΩ pull-up, 1 kΩ pull-down, no connect, and 20 kΩ pull-down provide the optimal voltage levels for each of the four input states.

Table 1. 4–Level Control Pin Settings

LEVEL	SETTING	RESULTING PIN VOLTAGE	
		3.3 V MODE	2.5 V MODE
0	Tie 1 kΩ to GND	0.10 V	0.08 V
R	Tie 20 kΩ to GND	1/3 x V_{IN}	1/3 x V_{DD}
Float	Float (leave pin open)	2/3 x V_{IN}	2/3 x V_{DD}
1	Tie 1 kΩ to V_{IN} or V_{DD}	V_{IN} - 0.05 V	V_{DD} - 0.04 V

Typical 4-Level Input Thresholds

- Level 1 - 2 = 0.16 * V_{IN} or V_{DD}
- Level 2 - 3 = 0.5 * V_{IN} or V_{DD}
- Level 3 - 4 = 0.83 * V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5 V regulator the 1 kΩ pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1 kΩ resistors into a single lower value resistor. As an example; combining two inputs with a single 500 Ω resistor is a good way to save board space.

8.4 Device Functional Modes

8.4.1 Pin Control Mode

When in Pin mode (ENSMB = 0), equalization can be selected via pins for each side independently. For PCIe applications, the RXDET pin provides automatic and manual control for input termination (50 Ω or > 50 kΩ). The receiver electrical signal detect threshold is also adjustable via the SD_TH pin. The signal detect status can only be used for system debug.

8.4.2 SMBus Mode

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, and termination disable features are all programmable on a individual channel basis. Upon assertion of ENSMB = 1, the EQx, VOD, and VODx_DB functions revert to register control immediately. The EQx pins are converted to AD0-AD3 SMBus address inputs. SD_TH remains active unless their respective registers are written to and the appropriate override bit is set, in which case it is ignored until ENSMB is driven low (Pin mode). On power-up or when ENSMB is driven low all registers are reset to their default state. If PWDN is asserted while ENSMB is high, the registers retain their current state.

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Device Functional Modes (continued)

Equalization settings accessible via the Pin controls were chosen to meet the needs of most high speed applications. If ongoing adjustment is needed, equalization settings can be accessed via the SMBus registers. Each input has a total of 4 possible equalization settings. The tables show the 4 settings when the device is in Pin mode. When using SMBus mode, the equalization, VOD and VOD_DB levels are set by registers.

The 4-level input Pins utilize a resistor divider to help set the 4 valid levels and provide a wide range of control settings when ENSMB = 0. There is an internal 30 kΩ pull-up and a 60 kΩ pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1 kΩ pull-up, 1 kΩ pull-down, no connect, and 20 kΩ pull-down provide the optimal voltage levels for each of the four input states.

Table 2. RX-Detect Settings

PWDN (Pin 6)	RXDET (Pin 18)	SMBus REG 0x0E and 0X15[3:2]	INPUT TERMINATION	RECOMMENDED USE	COMMENTS
0	0	00'b	Hi-Z		Manual RX-Detect, input is high impedance mode
0	Tie 20 kΩ to GND	01'b	Pre Detect: Hi-Z Post Detect: 50 Ω	PCIe only	Auto RX-Detect, outputs test every 12 ms for 600 ms then stops; termination is Hi-Z until RX detection; once detected input termination is 50 Ω Reset function by pulsing PWDN high for 5 µs then low again
0	Float (PCIe Default)	10'b	Pre Detect: Hi-Z Post Detect: 50 Ω	PCIe only	Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until RX detection; once detected input termination is 50 Ω
0	1 (SAS Default)	11'b	50 Ω	All Others	Manual RX-Detect, input is 50 Ω
1	X		High Impedance		Power down mode, input is Hi-Z, output drivers are disabled Used to reset RX-Detect State Machine when held high for 5 µsec

When SMBus is used to control the DS125BR111 in a PCIe application, a specific register write sequence detailed in PCIe Applications is required on power-up to properly enable and control the RX_Detect process.

Table 3. Signal Detect Status Threshold Level (1) (2)

SD_TH (Pin 14)	SMBus REG BIT [3:2] and [1:0]	[3:2] ASSERT LEVEL (mVp-p)		[1:0] DE-ASSERT LEVEL (mVp-p)	
		3 Gbps	12 Gbps	3 Gbps	12 Gbps
0	10	18	75	14	55
R	01	12	40	8	22
F (default)	00	15	50	11	37
1	11	16	58	12	45

(1) VDD = 2.5 V, 25°C, 11 00 11 00 pattern at 3 Gbps and 101010 pattern at 12 Gbps
(2) Signal Detect Threshold (SD_TH) is for debugging purposes only, outputs are enabled unless the channel is set to PWDN

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8.4.3 Signal Conditioning Settings

Table 4. Equalizer Settings

EQUALIZATION BOOST RELATIVE TO DC									
Level	**EQx1**	**EQx0**	**EQ – 8 bits [7:0]**	**dB at 1.5 GHz**	**dB at 2.5 GHz**	**dB at 4 GHz**	**dB at 5 GHz**	**dB at 6 GHz**	**Suggested Use(1)**
1	0	0	xxxx xx00 = 0x00	2.1	2.5	2.7	2.9	3.0	
2	0	R	xxxx xx01 = 0x01	4.0	5.1	6.4	6.8	7.4	
3	0	Float	xxxx xx10 = 0x02	5.5	7.0	8.3	8.6	8.9	
4	0	1	xxxx xx11 = 0x03	6.8	8.3	9.5	9.6	9.8	SAS-3

(1) For SAS3 applications the best performance is achieved with Equalization Level 4. For non SAS applications, optimal EQ setting should be determined via simulation and prototype verification.

Table 5. Output Voltage Pin Settings

Channel A Level	**Channel B Level**	**VOD_SEL**	**VID Vp-p**	**VODx_DB Setting(1)**	**VOD Vp-p**
	0	0	1.0	0	0.65
1		0	1.0	0	0.70
3	3	R	1.0	0	0.83
5	5	Float	1.0	0	0.91
7	7	1	1.0	0	1.05

(1) The VOD output amplitude is set with the VOD_SEL Pin. For SAS-3 and PCIe operation the VOD_DB level is typically left at 0 dB (SMBus control = 000'b) in order to keep the output dynamic range as large as possible. VOD_DB settings other than 0 dB or 000'b will decrease the output dynamic range and act to limit the output VOD. When operating in Pin Mode in a SAS3 environment it is recommended to use VOD_SEL = 1.

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8.5 Programming

The DS125BR111 device supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS125BR111 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Maximum EEPROM size is 8 kbits (1024 x 8-bit).
- Set ENSMB = Float — enable the SMBus master mode.
- The external EEPROM device address byte must be 0xA0 and capable of 1 MHz operation at 2.5 V and 3.3 V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is 0xB0. The VOD_SEL/$\overline{\text{READEN}}$ pin must be tied Low for the AD[3:0] to be active. If this pin is tied High or Floated an address of 0xB0 will be used for the DS125BR111.

When tying multiple DS125BR111 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 devices. The first device in the sequence must be address 0xB0, subsequent devices must follow the address order listed below.
  - U1: AD[3:0] = 0000 = 0xB0,
  - U2: AD[3:0] = 0001 = 0xB2,
  - U3: AD[3:0] = 0010 = 0xB4,
  - U4: AD[3:0] = 0011 = 0xB6
- Use a pull-up resistor on SDA and SCL; typical value = 2 kΩ - 5 kΩ
- Daisy-chain $\overline{\text{READEN}}$ (Pin 17) and $\overline{\text{DONE}}$ (Pin 18) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie $\overline{\text{READEN}}$ of the 1st device in the chain (U1) to GND
  2. Tie $\overline{\text{DONE}}$ of U1 to $\overline{\text{READEN}}$ of U2
  3. Tie $\overline{\text{DONE}}$ of U2 to $\overline{\text{READEN}}$ of U3
  4. Tie $\overline{\text{DONE}}$ of U3 to $\overline{\text{READEN}}$ of U4
  5. Optional: Tie $\overline{\text{DONE}}$ output of U4 to a LED to show the devices have been loaded successfully

Below is an example using the default register values of a 2 kbit (256 x 8-bit) EEPROM in hex format for the DS125BR111 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS125BR111 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS125BR111 device.

```
:20000000000010000000407002FED4002FED4002FAD4002FAD400005F5A8005F5A8005F5A15
:20002000 8005F5A800005454 0000000000000000000000000000000000000000000000F6
:2000600000000000000000000000000000000000000000000000000000000000000000080
:2000800000000000000000000000000000000000000000000000000000000000000000060
:2000A0000000000000000000000000000000000000000000000000000000000000000040
:2000C0000000000000000000000000000000000000000000000000000000000000000020
:2000E0000000000000000000000000000000000000000000000000000000000000000000
:20004000000000000000000000000000000000000000000000000000000000000000000A0
```

Note: The maximum EEPROM size supported is 8 kbits (1024 x 8 bits).

Note: Default register values. These should be changed as indicated in the datasheet to support PCIe and SAS/SATA

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Table 6. EEPROM Register Map - Single Device With SAS Values

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		0	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Value	00		0	0	0	0	0	0	0	0
Description		1	RES	RES	RES	RES	RES	RES	RES	RES
Value	00		0	0	0	0	0	0	0	0
Description		2	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Value	00		0	0	0	0	0	0	0	0
Description		3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$\overline{\text{ENABLE}}$_CHB	$\overline{\text{ENABLE}}$_CHA
SMBus Register			0x01 [7]	0x01 [6]	0x01 [5]	0x01 [4]	0x01 [3]	0x01 [2]	0x01 [1]	0x01 [0]
Value	00		0	0	0	0	0	0	0	0
Description		4	Reserved	Reserved	Reserved	Reserved	Ovrd_$\overline{\text{ENABLE}}$	Reserved	Reserved	Reserved
SMBus Register			0x02 [5]	0x02 [4]	0x02 [3]	0x02 [2]	0x02 [0]	0x04 [7]	0x04 [6]	0x04 [5]
Value	00		0	0	0	0	0	0	0	0
Description		5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Ovrd_SD_TH	Reserved
SMBus Register			0x04 [4]	0x04 [3]	0x04 [2]	0x04 [1]	0x04 [0]	0x06 [4]	0x08 [6]	0x08 [5]
Value	04		0	0	0	0	0	1	0	0
Description		6	Reserved	Ovrd_RX_Detect	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x08 [4]	0x08 [3]	0x08 [2]	0x08 [1]	0x08 [0]	0x0B [6]	0x0B [5]	0x0B [4]
Value	07		0	0	0	0	0	1	1	1
Description		7	rate_delay_3	rate_delay_2	rate_delay_1	rate_delay_0	Reserved	Reserved	RXDET_A_1	RXDET_A_0
SMBus Register			0x0B [3]	0x0B [2]	0x0B [1]	0x0B [0]	0x0E [5]	0x0E [4]	0x0E [3]	0x0E [2]
Value	00		0	0	0	0	0	0	0	0
Description		8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHA_EQ_1	CHA_EQ_0
SMBus Register			0x0F [7]	0x0F [6]	0x0F [5]	0x0F [4]	0x0F [3]	0x0F [2]	0x0F [1]	0x0F [0]
Value	2F		0	0	1	0	1	1	1	1
Description		9	CHA_SCP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x10 [7]	0x10 [6]	0x10 [5]	0x10 [4]	0x10 [3]	0x10 [2]	0x10 [1]	0x10 [0]
Value	ED		1	1	1	0	1	1	0	1

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Table 6. EEPROM Register Map - Single Device With SAS Values (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		A	CHA_VOD_DB_2	CHA_VOD_DB_1	CHA_VOD_DB_0	Reserved	CHA_THa_1	CHA_THa_0	CHA_THd_1	CHA_THd_0
SMBus Register			0x11 [2]	0x11 [1]	0x11 [0]	0x12 [7]	0x12 [3]	0x12 [2]	0x12 [1]	0x12 [0]
Value	40		0	1	0	0	0	0	0	0
Description		B	Reserved	Reserved	RXDET_B_1	RXDET_B_0	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x15 [5]	0x15 [4]	0x15 [3]	0x15 [2]	0x16 [7]	0x16 [6]	0x16 [5]	0x16 [4]
Value	02		0	0	0	0	0	0	1	0
Description		C	Reserved	Reserved	CHB_EQ_1	CHB_EQ_0	CHB_SCP	Reserved	Reserved	Reserved
SMBus Register			0x16 [3]	0x16 [2]	0x16 [1]	0x16 [0]	0x17 [7]	0x17 [6]	0x17 [5]	0x17 [4]
Value	FE		1	1	1	1	1	1	1	0
Description		D	Reserved	Reserved	Reserved	Reserved	CHB_VOD_DB_2	CHB_VOD_DB_1	CHB_VOD_DB_0	Reserved
SMBus Register			0x17 [3]	0x17 [2]	0x17 [1]	0x17 [0]	0x18 [2]	0x18 [1]	0x18 [0]	0x19 [7]
Value	D4		1	1	0	1	0	1	0	0
Description		E	CHB_THa_1	CHB_THa_0	CHB_THd_1	CHB_THd_0	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x19 [3]	0x19 [2]	0x19 [1]	0x19 [0]	0x1C [5]	0x1C [4]	0x1C [3]	0x1C [2]
Value	00		0	0	0	0	0	0	0	0
Description		F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1D [7]	0x1D [6]	0x1D [5]	0x1D [4]	0x1D [3]	0x1D [2]	0x1D [1]	0x1D [0]
Value	2F		0	0	1	0	1	1	1	1
Description		10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1E [7]	0x1E [6]	0x1E [5]	0x1E [4]	0x1E [3]	0x1E [2]	0x1E [1]	0x1E [0]
Value	AD		1	0	1	0	1	1	0	1
Description		11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1F [2]	0x1F [1]	0x1F [0]	0x20 [7]	0x20 [3]	0x20 [2]	0x20 [1]	0x20 [0]
Value	40		0	1	0	0	0	0	0	0
Description		12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x23 [5]	0x23 [4]	0x23 [3]	0x23 [2]	0x24 [7]	0x24 [6]	0x24 [5]	0x24 [4]
Value	02		0	0	0	0	0	0	1	0
Description		13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHA_VOD_2
SMBus Register			0x24 [3]	0x24 [2]	0x24 [1]	0x24 [0]	0x25 [7]	0x25 [6]	0x25 [5]	0x25 [4]
Value	FA		1	1	1	1	1	0	1	0

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Table 6. EEPROM Register Map - Single Device With SAS Values (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		14	CHA_VOD_1	CHA_VOD_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x25 [3]	0x25 [2]	0x25 [1]	0x25 [0]	0x26 [2]	0x26 [1]	0x26 [0]	0x27 [7]
Value	D4		1	1	0	1	0	1	0	0
Description		15	Reserved	Reserved	Reserved	Reserved	ovrd_fast_idle	hi_idle_th CHA	hi_idle_th CHB	fast_idle CHA
SMBus Register			0x27 [3]	0x27 [2]	0x27 [1]	0x27 [0]	0x28 [6]	0x28 [5]	0x28 [4]	0x28 [3]
Value	00		0	0	0	0	0	0	0	0
Description		16	fast_idle CHB	low_gain CHA	low_gain CHB	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x28 [2]	0x28 [1]	0x28 [0]	0x2B [5]	0x2B [4]	0x2B [3]	0x2B [2]	0x2C [7]
Value	00		0	0	0	0	0	0	0	0
Description		17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x2C [6]	0x2C [5]	0x2C [4]	0x2C [3]	0x2C [2]	0x2C [1]	0x2C [0]	0x2D [7]
Value	5F		0	1	0	1	1	1	1	1
Description		18	Reserved	Reserved	CHB_VOD_2	CHB_VOD_1	CHB_VOD_0	Reserved	Reserved	Reserved
SMBus Register			0x2D [6]	0x2D [5]	0x2D [4]	0x2D [3]	0x2D [2]	0x2D [1]	0x2D [0]	0x2E [2]
Value	5A		0	1	0	1	1	0	1	0
Description		19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x2E [1]	0x2E [0]	0x2F [7]	0x2F [3]	0x2F [2]	0x2F [1]	0x2F [0]	0x32 [5]
Value	80		1	0	0	0	0	0	0	0
Description		1A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x32 [4]	0x32 [3]	0x32 [2]	0x33 [7]	0x33 [6]	0x33 [5]	0x33 [4]	0x33 [3]
Value	05		0	0	0	0	0	1	0	1
Description		1B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x33 [2]	0x33 [1]	0x33 [0]	0x34 [7]	0x34 [6]	0x34 [5]	0x34 [4]	0x34 [3]
Value	F5		1	1	1	1	0	1	0	1
Description		1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x34 [2]	0x34 [1]	0x34 [0]	0x35 [2]	0x35 [1]	0x35 [0]	0x36 [7]	0x36 [3]
Value	A8		1	0	1	0	1	0	0	0
Description		1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x36 [2]	0x36 [1]	0x36 [0]	0x39 [5]	0x39 [4]	0x39 [3]	0x39 [2]	0x3A [7]
Value	00		0	0	0	0	0	0	0	0

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Table 6. EEPROM Register Map - Single Device With SAS Values (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		1E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3A [6]	0x3A [5]	0x3A [4]	0x3A [3]	0x3A [2]	0x3A [1]	0x3A [0]	0x3B [7]
Value	5F		0	1	0	1	1	1	1	1
Description		1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3B [6]	0x3B [5]	0x3B [4]	0x3B [3]	0x3B [2]	0x3B [1]	0x3B [0]	0x3C [2]
Value	5A		0	1	0	1	1	0	1	0
Description		20	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3C [1]	0x3C [0]	0x3D [7]	0x3D [3]	0x3D [2]	0x3D [1]	0x3D [0]	0x40 [5]
Value	80		1	0	0	0	0	0	0	0
Description		21	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x40 [4]	0x40 [3]	0x40 [2]	0x41 [7]	0x41 [6]	0x41 [5]	0x41 [4]	0x41 [3]
Value	05		0	0	0	0	0	1	0	1
Description		22	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x41 [2]	0x41 [1]	0x41 [0]	0x42 [7]	0x42 [6]	0x42 [5]	0x42 [4]	0x42 [3]
Value	F5		1	1	1	1	0	1	0	1
Description		23	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x42 [2]	0x42 [1]	0x42 [0]	0x43 [2]	0x43 [1]	0x43 [0]	0x44 [7]	0x44 [3]
Value	A8		1	0	1	0	1	0	0	0
Description		24	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x44 [2]	0x44 [1]	0x44 [0]	0x47 [3]	0x47 [2]	0x47 [2]	0x47 [0]	0x48 [7]
Value	00		0	0	0	0	0	0	0	0
Description		25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x48 [6]	0x4C [7]	0x4C [6]	0x4C [5]	0x4C [4]	0x4C [3]	0x4C [0]	0x59 [0]
Value	00		0	0	0	0	0	0	0	0
Description		26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5A [7]	0x5A [6]	0x5A [5]	0x5A [4]	0x5A [3]	0x5A [2]	0x5A [1]	0x5A [0]
Value	54		0	1	0	1	0	1	0	0
Description		27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5B [7]	0x5B [6]	0x5B [5]	0x5B [4]	0x5B [3]	0x5B [2]	0x5B [1]	0x5B [0]
Value	54		0	1	0	1	0	1	0	0

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Table 7. Example of EEPROM For Four Devices Using Two Address Maps

EEPROM ADDRESS		EEPROM DATA	COMMENTS
DECIMAL	HEX		
0	00	0x43	CRC_EN = 0, Address Map = 1, > 256 bytes = 0, Device Count[3:0] = 3
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x0B	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x30	Device 3 Address Location
11	0B	0x00	Begin Device 0, 1 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x03	EQ CHA = 03
17	11	0xED	
18	12	0x00	VOD_DB CHA = 0 (0dB)
19	13	0x00	
20	14	0xFE	EQ CHB = 03
21	15	0xD0	VOD_DB CHB = 0 (0dB)
22	16	0x00	
23	17	0x2F	
24	18	0xAD	
25	19	0x40	
26	1A	0x02	
27	1B	0xFB	VOD CHA = 1.4 V
28	1C	0xD4	VOD CHA = 1.4 V
29	1D	0x00	Signal Detect Status Threshold Control
30	1E	0x00	Signal Detect status Threshold Control
31	1F	0x5F	
32	20	0x7A	VOD CHB = 1.4 V
33	21	0x80	
34	22	0x05	
35	23	0xF5	
36	24	0xA8	
37	25	0x00	
38	26	0x5F	
39	27	0x5A	
40	28	0x80	
41	29	0x05	
42	2A	0xF5	
43	2B	0xA8	
44	2C	0x00	
45	2D	0x00	

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Table 7. Example of EEPROM For Four Devices Using Two Address Maps (continued)

EEPROM ADDRESS		EEPROM DATA	COMMENTS
DECIMAL	HEX		
46	2E	0x54	
47	2F	0x54	End Device 0, 1 - Address Offset 39
48	30	0x00	Begin Device 2, 3 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x01	EQ CHA = 01
54	36	0xED	
55	37	0x00	VOD_DB CHA = 0 (0dB)
56	38	0x00	
57	39	0xFE	EQ CHB = 03
58	3A	0xD0	VOD_DB CHB1 = 0 (0dB)
59	3B	0x00	
60	3C	0x2F	
61	3D	0xAD	
62	3E	0x40	
63	3F	0x02	
64	40	0xFB	VOD CHA = 1.4 V
65	41	0xD4	VOD CHA = 1.4 V
66	42	0x00	Signal Detect status Threshold Control
67	43	0x00	Signal Detect status Threshold Control
68	44	0x5F	
69	45	0x7A	VOD CHB = 1.4 V
70	46	0x80	
71	47	0x05	
72	48	0xF5	
73	49	0xA8	
74	4A	0x00	
75	4B	0x5F	
76	4C	0x5A	
77	4D	0x80	
78	4E	0x05	
79	4F	0xF5	
80	50	0xA8	
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 2, 3 - Address Offset 39

Note: CRC_EN = 0, Address Map = 1, > 256 byte = 0, Device Count[3:0] = 3. Multiple devices can point to the same address map. Maximum EEPROM size is 8 kbits (1024 x 8-bits). EEPROM must support 1 MHz operation.

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8.6 Register Maps

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. Tie ENSMB = 1 kΩ to VDD (2.5 V mode) or VIN (3.3 V mode) to enable SMBus slave mode and allow access to the configuration registers.

The DS125BR111 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBus slave address inputs. The AD[3:0] Pins have internal pull-down. Based on the SMBus 2.0 specification, the DS125BR111 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). When AD[3:0] pins are left floating or pulled low, AD[3:0] = 0000'b, the device default address byte is 0xB0.The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses. Use the address listed in the Slave Address Byte column to address.

Table 8. Device Slave Address Bytes

AD[3:0] SETTINGS	FULL SLAVE ADDRESS BYTE (HEX)	7-BIT SLAVE ADDRESS (HEX)
0000	B0	58
0001	B2	59
0010	B4	5A
0011	B6	5B
0100	B8	5C
0101	BA	5D
0110	BC	5E
0111	BE	5F
1000	C0	60
1001	C2	61
1010	C4	62
1011	C6	63
1100	C8	64
1101	CA	65
1110	CC	66
1111	CE	67

The SDA, SCL Pins are 3.3 V tolerant, but are not 5 V tolerant. External pull-up resistor is required on the SDA line. The resistor value can be from 2 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

8.6.1 Transfer Of Data Via The SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus transfers to the IDLE state.

8.6.2 SMBus Transactions

The device supports WRITE and READ transactions. See Table 9 for register address, type (Read/Write, Read Only), default value and function information.

8.6.3 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).

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3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

8.6.4 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1” indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

8.6.5 SMBus Register Information

Table 9. SMBus Register Map

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x00	Device ID	7	Reserved	R/W	0x00		Set bit to 0
		6:3	I2C Address [3:0]	R			[6:3] SMBus strap observation
		2	EEPROM reading done	R			1 = EEPROM Done Loading 0 = EEPROM Loading
		1:0	Reserved	RWSC			Set bits to 0
0x01	Control 1	7:2	Reserved	R/W	0x00	Yes	Set bits to 0
		1:0	$\overline{\text{ENABLE}}$ A/B				[1]: Disable Channel B (1); Normal Operation (0) [0]: Disable Channel A (1); Normal Operation (0) Note: Must set $\overline{\text{ENABLE}}$ override in Reg 0x02[0]
0x02	Control 2	7	Override PWDN	R/W	0x00		[1]: Override PWDN (1); PWDN pin control (0)
		6	PWDN Pin value				Override value for PWDN pin [1]: PWDN - Low Power (1); Normal Operation (0) Note: Must set PWDN override in Reg 0x02[7]
		5:4	Reserved			Yes	Set bits to 0
		3	PWDN Inputs			Yes	Set bit to 0
		2	PWDN Oscillator			Yes	Set bit to 0
		1	Reserved				Set bit to 0
		0	Override $\overline{\text{ENABLE}}$			Yes	1 = Enables Reg 0x01[1:0] 0 = Normal Operation

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Table 9. SMBus Register Map (continued)

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x04	Reserved	7:0	Reserved	R/W	0x00	Yes	Set bits to 0
0x05	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x06	**SMBus Control**	7:5	Reserved	R/W	**0x10**		Set bits to 0
		4	Reserved			Yes	Set bit to 1
		3	**Register Mode Enable**				**1 = Enable SMBus Slave Mode Register Control** 0 = Disable Register Control **Note: With register control "Enabled" register updates take immediate effect on high speed data path. When "Disabled", SMBus registers are still R/W, but changes will not be sent to the high speed controls until this register is "Enabled".**
		2:0	Reserved				Set bits to 0
0x07	Digital Reset and Control	7	Reserved	R/W	0x01		Set bit to 0
		6	Reset Regs	RWSC			Self clearing reset for registers. Writing a [1] will return register settings to default values.
		5	Reset SMBus Master	RWSC			Self clearing reset to SMBus master state machine
		4:0	Reserved	R/W			Set bits to 0001'b
0x08	Pin Override	7	Reserved	R/W	0x00		Set bit to 0
		6	Override SD_TH Threshold			Yes	1 = Override by Channel - see Reg 0x12 and 0x19 0 = SD_TH pin control
		5:4	Reserved			Yes	Set bits to 0
		3	Override RXDET			Yes	1 = Override by Channel - see Reg 0x0E and 0x15 0 = RXDET pin control
		2:0	Reserved			Yes	Set bits to 0
0x0A	Signal Detect Status	7:2	Reserved	R	0x00		
		1	Internal Idle B	R			1 = LOS (No Signal Present) 0 = Signal present Note: RES Pin = Float for these bits to function.
		0	Internal Idle A				
0x0B	Reserved	7:0	Reserved	R/W	0x70	Yes	
0x0C	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x0E	CH A RXDET Control	7:5	Reserved	R/W	0x00		Set bits to 0
		4	Reserved			Yes	Set bit to 0
		3:2	RXDET			Yes	CHA RXDET register control 00'b = Input is high-z impedance 01'b = Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10'b = Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: override RXDET pin in 0x08[3]. **Note: Can only be used with the register write sequence described in .***PCIe Applications*
		1:0	Reserved				Set bits to 0

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Table 9. SMBus Register Map (continued)

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x0F	CH A EQ Control	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Control - total of 4 levels See Table 4
0x10	CH A Control	7	Select Short Circuit Protection	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Reserved			Yes	Set bit to 0
		5:3	Reserved			Yes	Set bits to 0
		2:0	Reserved			Yes	Set bits to 101'b
0x11	CH A VOD_DB Control	7	Reserved	R	0x82		
		6:5	Reserved				
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control [2:0]			Yes	OUTA VOD_DB Control (010'b Default). **Based on system interoperability testing it is recommended to set these bits to 000'b for SAS, PCIe, and other non-limiting applications.** 000'b = 0 dB (Recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD gain by a factor of the corresponding amount of dB reduction.
0x12	CH A SD Threshold	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Tassert			Yes	Assert Thresholds (1010 pattern 12 Gbps) Use only if register 0x08 [6] = 1 00'b = 50 mV (Default) 01'b = 40 mV 10'b = 75 mV 11'b = 58 mV Note: Override the SD_TH pin using 0x08[6]. Note: This threshold adjustment is for SD status indication only.
		1:0	Signal Detect Status Tde-assert			Yes	De-assert Thresholds (1010 pattern 12 Gbps) Use only if register 0x08 [6] = 1 00'b = 37 mV (Default) 01'b = 22 mV 10'b = 55 mV 11'b = 45 mV Note: Override the SD_TH pin using 0x08[6]. Note: This threshold adjustment is for SD status indication only.
0x13	Reserved	7:2	Reserved	R/W	0x00		Set bits to 0
		1:0		R			
0x14	CH B	7:3	Reserved	R/W	0x00		Set bits to 0
		2	Signal Detect Reset				1 = Override Signal Detect, hold "Off"
		1	Signal Detect Preset				1 = Override Signal Detect, hold "On"
		0	Reserved				Set bit to 0

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Table 9. SMBus Register Map (continued)

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x15	CH B RXDET Control	7:5	Reserved	R/W	0x00		Set bits to 0
		4	Reserved			Yes	Set bit to 0
		3:2	RXDET			Yes	CHB RXDET register control 00'b = Input is high-z impedance 01'b = Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10'b = Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: override RXDET pin in 0x08[3]. **Note: Can only be used with the register write sequence described in PCIe Applications .**
		1:0	Reserved				Set bits to 0
0x16	CH B EQ Control	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Control - total of 4 levels See Table 4
0x17	CH B RATE Control	7	Select Short Circuit Protection	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Reserved				Set bit to 0
		5:3	Reserved				Set bits to 0
		2:0	Reserved				Set bits to 101'b
0x18	CH B VOD_DB Control	7	Reserved	R	0x82		
		6:5	Reserved				
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control [2:0]			Yes	OUTB VOD_DB Control (010'b Default). **Based on system interoperability testing it is recommended to set these bits to 000'b for SAS, PCIe, and other non-limiting applications.** 000'b = 0 dB (Recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD gain by a factor of the corresponding amount of dB reduction.

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Table 9. SMBus Register Map (continued)

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x19	CH B SD Threshold	7	Reserved	R/W	0x00	Yes	Set bits to 0
		6:4	Reserved				
		3:2	Signal Detect Status Tassert			Yes	Assert Thresholds (1010 pattern 12 Gbps) Use only if register 0x08 [6] = 1 00'b = 50 mV (Default) 01'b = 40 mV 10'b = 75 mV 11'b = 58 mV Note: Override the SD_TH pin using 0x08[6]. Note: This threshold adjustment is for SD status indication only.
		1:0	Signal Detect Status Tde-assert			Yes	De-assert Thresholds (1010 pattern 12 Gbps) Use only if register 0x08 [6] = 1 00'b = 37 mV (Default) 01'b = 22 mV 10'b = 55 mV 11'b = 45 mV Note: Override the SD_TH pin using 0x08[6]. Note: This threshold adjustment is for SD status indication only.
0x1C		7:6	Reserved	R/W	0x00		Set bits to 0
		5:2				Yes	
		1:0					
0x1D		7:0	Reserved	R/W	0x2F	Yes	
0x1E		7:0	Reserved	R/W	0xAD	Yes	
0x1F		7:3	Reserved	R/W	0x02		
		2:0				Yes	
0x20		7	Reserved	R/W	0x00	Yes	
		6:4					
		3:0				Yes	
0x23		7:6	Reserved	R/W	0x00		
		5:2				Yes	
		1:0					
0x24		7:0	Reserved	R/W	0x2F	Yes	
0x25	CH A VOD	7:5	Reserved	R/W	0xAD	Yes	Set bits to 101'b
		4:2	VOD CHA Control				VOD Control CHA: VOD / VID Ratio 000'b = 0.65 001'b = 0.70 010'b = 0.78 011'b = 0.83 100'b = 0.88 101'b = 0.91 (Default) 110'b = 1.00 (Recommended for SAS/SATA/PCIe) 111'b = 1.05 (Recommended for SAS/SATA/PCIe)
		1:0	Reserved				Set bits to 01'b
0x26		7:6	Reserved	R	0x02		
		4:3		R/W			
		2:0				Yes	

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Table 9. SMBus Register Map (continued)

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x27		7	Reserved	R/W	0x00	Yes	
		6:4					
		3:0				Yes	
0x28	Signal Detect Control	7	Reserved	R/W	0x00		Set bit to 0
		6	Override Fast IDLE			Yes	Override Fast IDLE 1 = Use value in 0x28[3:2] 0 = Based on MODE pin
		5:4	High IDLE			Yes	Enable higher SD Threshold range [1]: CH A [0]: CH B
		3:2	Fast IDLE			Yes	Enable Fast SD response [1]: CH A [0]: CH B
		1:0	Reduced SD Gain			Yes	Enable reduced SD Gain [1]: CH A [0]: CH B
0x2B		7:6	Reserved	R/W	0x00		
		5:2				Yes	
		1:0					
0x2C		7:0	Reserved	R/W	0x2F	Yes	
0x2D	CH B VOD	7:5	Reserved	R/W	0xAD	Yes	Set bits to 101'b
		4:2	VOD CHB Control				VOD Control CHB: VOD / VID Ratio 000'b = 0.65 001'b = 0.70 010'b = 0.78 011'b = 0.83 100'b = 0.88 101'b = 0.91 (Default) 110'b = 1.00 (Recommended for SAS/SATA/PCIe) 111'b = 1.05 (Recommended for SAS/SATA/PCIe)
		1:0	Reserved				Set bits to 01'b
0x2E		7:5	Reserved	R	0x02		
		4:3		R/W			
		2:0				Yes	
0x2F		7	Reserved	R/W	0x00	Yes	
		6:4					
		3:0				Yes	
0x32		7:6	Reserved	R/W	0x00		
		5:2				Yes	
		1:0					
0x33		7:0	Reserved	R/W	0x2F	Yes	
0x34		7:0	Reserved	R/W	0xAD	Yes	
0x35		7:5	Reserved	R	0x02		
		4:3		R/W			
		2:0				Yes	
0x36		7	Reserved	R/W	0x00	Yes	
		6:4					
		3:0				Yes	

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Table 9. SMBus Register Map (continued)

ADDRESS	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	EEPROM REG BIT	DESCRIPTION
0x39		7:6	Reserved	R/W	0x00		
		5:2				Yes	
		1:0					
0x3A		7:0	Reserved	R/W	0x2F	Yes	
0x3B		7:0	Reserved	R/W	0xAD	Yes	
0x3C		7:5	Reserved	R	0x02		
		4:3		R/W			
		2:0				Yes	
0x3D		7	Reserved	R/W	0x00	Yes	
		6:4					
		3:0				Yes	
0x40		7:6	Reserved	R/W	0x00		
		5:2				Yes	
		1:0					
0x41		7:0	Reserved	R/W	0x2F	Yes	
0x42		7:0	Reserved	R/W	0xAD	Yes	
0x43		7:5	Reserved	R	0x02		
		4:3		R/W			
		2:0				Yes	
0x44		7	Reserved	R/W	0x00	Yes	
		6:4					
		3:0				Yes	
0x47		7:4	Reserved	R/W	0x00		
		3:0				Yes	
0x48		7:6	Reserved	R/W	0x05	Yes	
		5:0					
0x4C		7:3	Reserved	R/W	0x00	Yes	
		2:1					
		0				Yes	
0x51	Device Information	7:5	Version	R	0x97		100'b
		4:0	Device ID				1 0111'b
0x59		7:1	Reserved	R/W	0x00		
		0				Yes	
0x5A		7:0	Reserved	R/W	0x54	Yes	
0x5B		7:0	Reserved	R/W	0x54	Yes	

Legend:

RWSC: Read / Write / Self Clearing on Read

R/W: Read / Write

R: Read Only

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9 Application and Implementation

9.1 Application Information

9.1.1 Signal Integrity

In SAS and PCIe applications, specifications require Rx-Tx link training to establish and optimize signal conditioning settings for data rates up to 12 Gbps. In link training, the Rx partner requests a series of FIR coefficients from the TX partner at speed. This polling sequence is designed to pre-condition the signal path with an optimized link between the endpoints. Link training occurs at the following data-rates:

Table 10. Link Training Data-Rates

PROTOCOL	MAXIMUM DATA-RATE (Gbps)	ALTERNATIVE DATA RATES (Gbps)
SAS	12.0	6.0, 3.0
PCIe	8.0	5.0, 2.5

The DS125BR111 works to extend the reach possible by using active linear equalization to the channel, boosting attenuated signals so that they can be more easily recovered at the Rx. The repeater outputs are specially designed to be transparent to TX FIR signaling in order to pass information critical for optimal link training to the Rx. Suggested settings for the A-channels and B-channels in a SAS or PCIe environment are given in the table below. Further adjustments to EQ and VOD settings may optimize signal margin on the link for different system applications:

Table 11. Pin Mode Device Settings

CHANNEL SETTINGS	PIN MODE
EQx	Level 4
VOD_SEL	Level 7 (1)
VODx_DB	0 dB (0)

Table 12. SMBus Mode Device Settings

CHANNEL SETTINGS	SMBus REGISTER VALUE
EQ	0x03
VOD	110'b or 111'b
VODx_DB	000'b

9.1.2 RX-Detect in SAS/SATA Applications

Unlike PCIe systems, SAS/SATA systems use a low speed Out-Of-Band or OOB communications sequence to detect and communicate between SAS Controllers/Expanders and target drives. This communication eliminates the need to detect for endpoints like PCIe. For SAS systems, it is recommended to tie the RXDET pin high. This will ensure any OOB sequences sent from the Controller/Expander will reach the target drive without any additional latency due to the termination detection sequence defined by PCIe.

9.1.3 PCIe Applications

9.1.3.1 RXDET When Using SMBus Modes

PCIe systems use an input termination polling and detection sequence to begin the PCIe bus configuration process. When using PIN MODE configuration the RXDET pin should be left Floating to allow for this process to begin upon power-up of the DS125BR111 device. If SMBus Slave MODE configuration is required, the SMBus register write sequence in Table 13 should be initiated upon power-up of the DS125BR111.

- Pin Settings for DS125BR111 in a PCIe Application (SMBus Slave Mode)
  - ENSMB = H
  - RXDET = Float
  - PWDN = System control (Hold HIGH until Register Write process is completed)

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Table 13. PCIe RX-Detect Programming Sequence

STEP	SMBus REGISTER ADDRESS	REGISTER DATA (Hex)	COMMENTS
1	0x08	0x08	Give RXDET control to SMBus Registers
2	0x0E	0x04 or 0x08	Channel A: 0x04: Auto RX-Detect, outputs test every 12 ms for 600 ms then stops; termination is Hi-Z until RX detection; once detected input termination is 50 Ω 0x08: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until RX detection; once detected input termination is 50 Ω
3	0x15	0x04 or 0x08	Channel B: 0x04: Auto RX-Detect, outputs test every 12 ms for 600 ms then stops; termination is Hi-Z until RX detection; once detected input termination is 50 Ω 0x08: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until RX detection; once detected input termination is 50 Ω
4	0x06	0x18	Enable SMBus register control. Register updates in Steps 1-3 are applied to high speed channels.

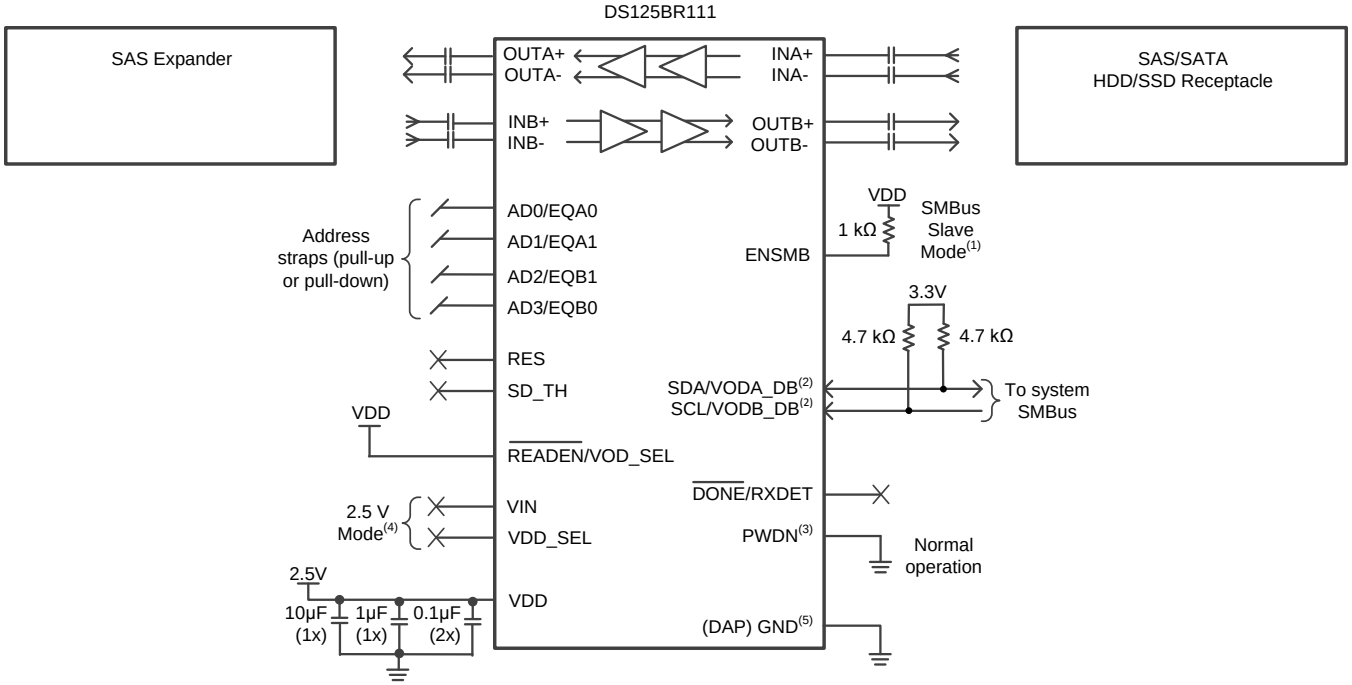
- Pin Settings for DS125BR111 in a PCIe Application (SMBus Master Mode - EEPROM Configuration)
  - ENSMB = Float
  - RXDET = Float
  - PWDN = System control (Hold PWDN HIGH until $\overline{\text{DONE}}$ = 0, EEPROM Write process is completed)

The highlighted bits for RXDET in the Table 6 show the equivalent RXDET control locations to the SMBus Register write sequence shown in Table 13.

9.2 Typical Application

SAS-3 specifications have fully specified Rx-Tx training as a means to establish and optimize signal conditioning settings at the 12.0 Gbps data-rate. The DS125BR111 works to extend the reach possible by adding active linear equalization to the channel, boosting attenuated signals so that they can be more easily recovered at the SAS-3 Rx. The outputs are specially designed to be transparent to TX FIR signaling passing this information critical for optimal link training to the SAS-3 Rx. The typical device settings used in most SAS-3 environments are EQ = Level 4, VOD_DB = 0 and VOD_SEL = 1 in Pin mode or EQ = 0x03, VOD = 111'b, and VOD_DB = 000'b in SMBus mode.

The maximum channel attenuation for a single DS125BR111 in a SAS-3 application utilizing link training is -34 dB @ 6 GHz. Other system variables such as crosstalk and channel topology can have an impact on the link extension possible using the DS125BR111.



(1) Schematic requires different connections for SMBus Master Mode and Pin Mode
(2) SMBus signals need to be pulled up elsewhere in the system
(3) PWDN pin can alternatively be driven by a control device (i.e. FPGA)
(4) Schematic requires different connections for 3.3 V mode
(5) A minimum of 4 vias are recommended for proper thermal and electrical performance

Figure 9. DS125BR111 Typical Application

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Typical Application (continued)

9.2.1 Design Requirements

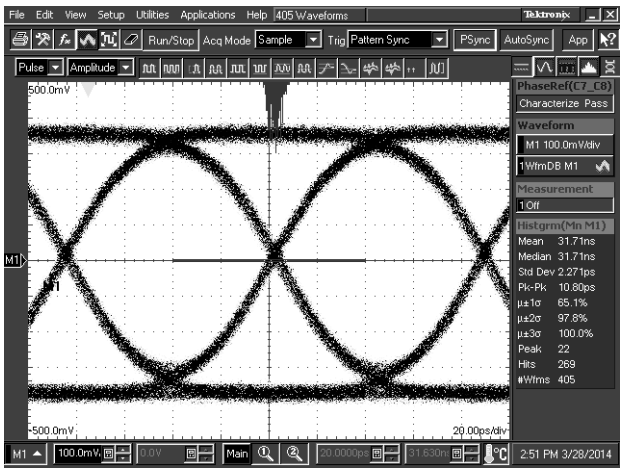
As with any high speed design, there are many factors which influence the overall performance, this section lists some critical areas for consideration and study.

- **Limit the maximum attenuation to -34 dB @ 6 GHz for the entire channel.**
- Utilize 100 Ω impedance traces. Generally these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length
- Use Reference plane vias to ensure a low inductance path for the return current.

9.2.2 Detailed Design Procedure

The DS125BR111 is designed to be placed almost anywhere within the channel, maximum channel extension requires the DS125BR111 be placed with attenuation of at least 10 dB on its inputs. The device settings used in a SAS-3 environment are EQ = Level 4, VOD_SEL = 1, and VOD_DB = 0 in Pin mode or EQ = 0x03, VOD = 110'b or 111'b, and VOD_DB = 000'b in SMBus mode. This setting has proven to give the best overall SAS-3 extension for all configurations tested.

9.2.3 Application Curves



DS125BR111 settings: EQ = 0x01, VOD = 110'b, VOD_DB = 000'b

Figure 10. TLine = 5 Inch 5–Mil FR4 Trace, 12 Gbps

10 Power Supply Recommendations

Two approaches are recommended to ensure that the DS125BR111 is provided with an adequate power supply. First, the supply (V_{DD}) and ground (GND) Pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} Pin such that the capacitor is placed as close as possible to the DS125BR111. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

The DS125BR111 has an optional internal voltage regulator to provide the 2.5 V supply to the device. In 3.3 V mode operation, the V_{IN} Pin = 3.3 V is used to supply power to the device. The internal regulator will provide the 2.5 V to the V_{DD} Pins of the device and a 0.1 µF cap is needed at each of the 2 V_{DD} Pins for power supply de-coupling (total capacitance should equal 0.2 µF). The VDD_SEL Pin must be tied to GND to enable the internal regulator. In 2.5 V mode operation, the VIN Pin should be left open and 2.5 V supply must be applied to the 2 V_{DD} Pins to power the device. The VDD_SEL Pin must be left open (no connect) to disable the internal regulator.

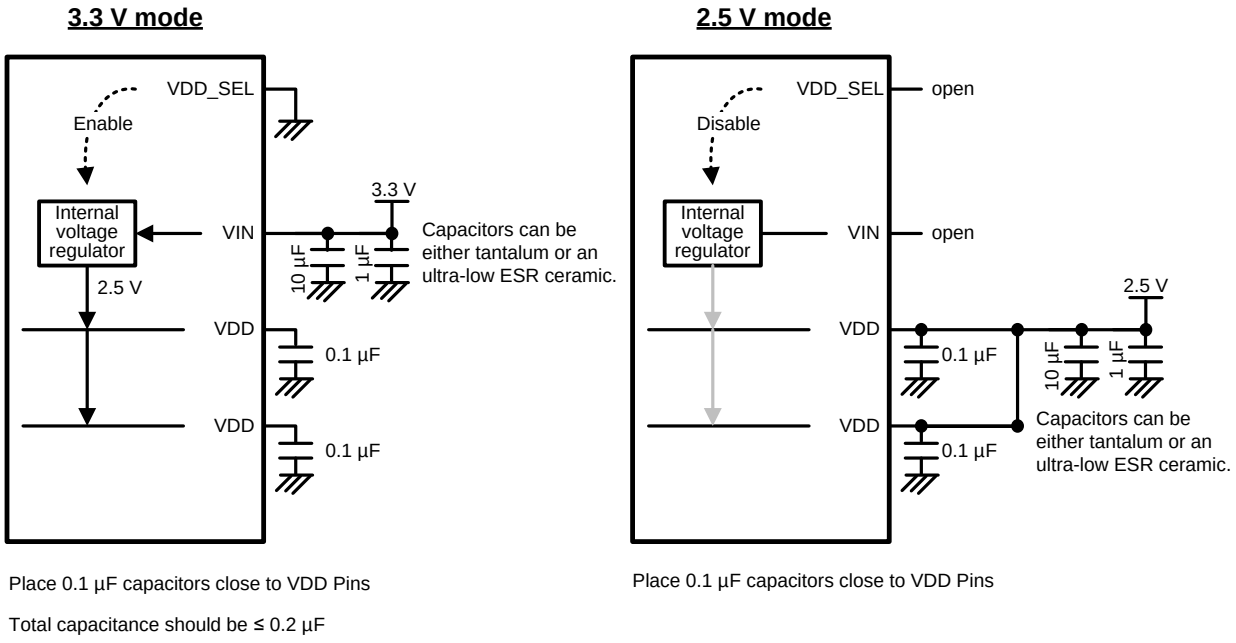


Figure 11. 3.3 V or 2.5 V Supply Connection Diagram

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11 Layout

11.1 Layout Guidelines

The DS125BR111 pinout promotes makes for easy high speed routing and layout. To optimize DS125BR111 performance refer to the following guidelines;

1. Differential pairs going into or out of the DS125BR111 should have adequate pair - pair spacing to minimize crosstalk. Keep a 5x spacing ratio as shown on the Blue pairs in the layout example.
2. Place local V_{IN} and V_{DD} capacitors as close as possible to the device supply pins to ensure a low inductance layout. Often the best location is directly under the DS125BR111 pins.
3. Use return current via connections to link reference planes locally. This ensures a low inductance return current path when the differential signal changes layers.
4. Open up the supply planes around differential vias to better match the trace impedance.
5. Place GND vias around the DAP perimeter to ensure optimal electrical and thermal performance.
6. Use 0201 body size coupling capacitors whenever possible, 0402 body size capacitors can also be used if they are placed closer to the Rx on the channel.

11.2 Layout Example

In most cases DS125BR111 layouts will fit neatly into a single or 1-lane application. The example layout shows how to "flip" one of the DS125BR111 channels to produce a 2-channel unidirectional layout.

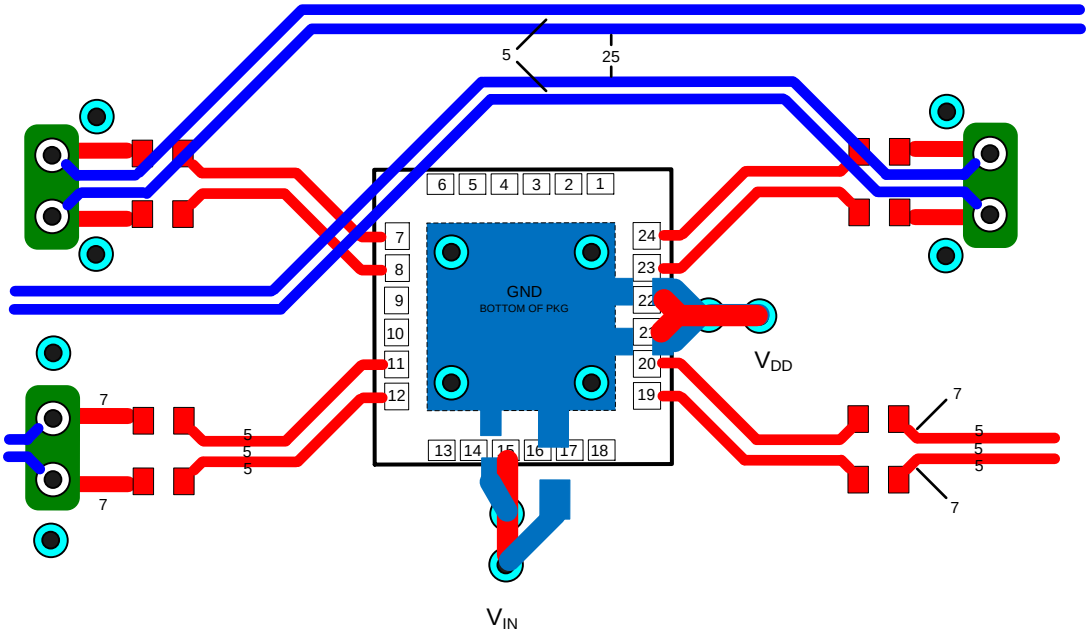

Figure 12. DS125BR111 Example Unidirectional Layout

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS125BR111RTWR	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2B111A0	Samples
DS125BR111RTWT	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2B111A0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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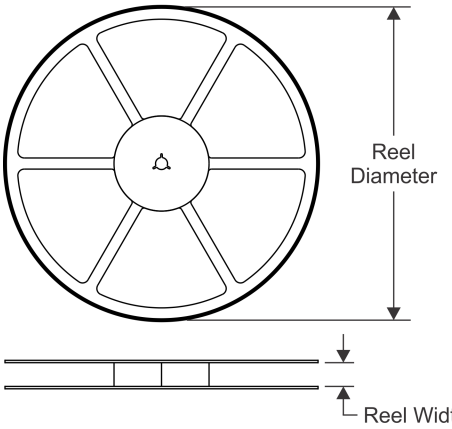
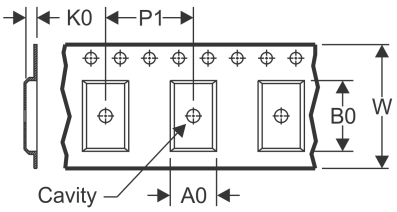
TAPE AND REEL INFORMATION

REEL DIMENSIONS

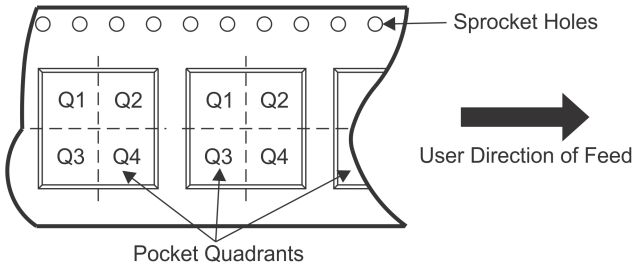


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

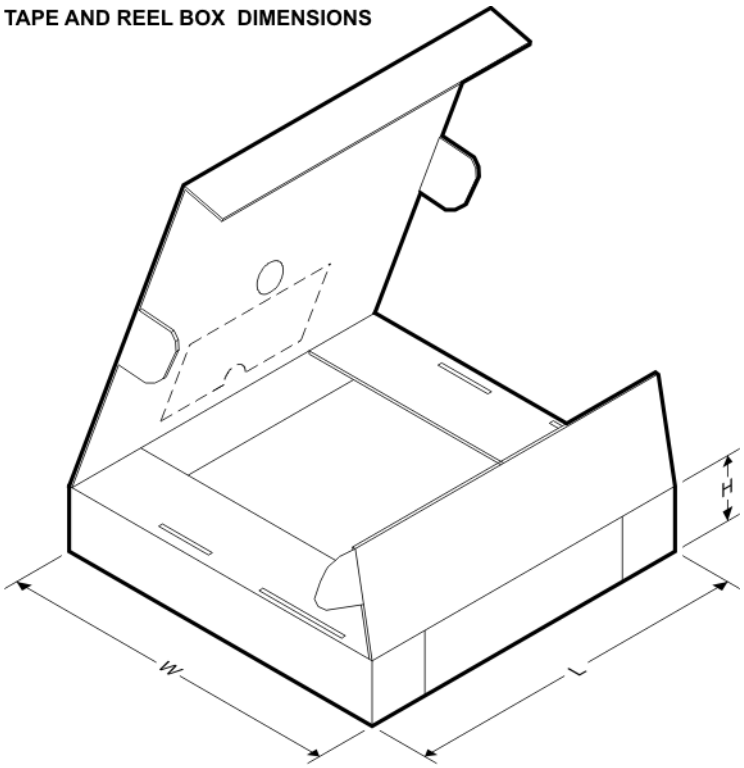
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS125BR111RTWR	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS125BR111RTWT	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

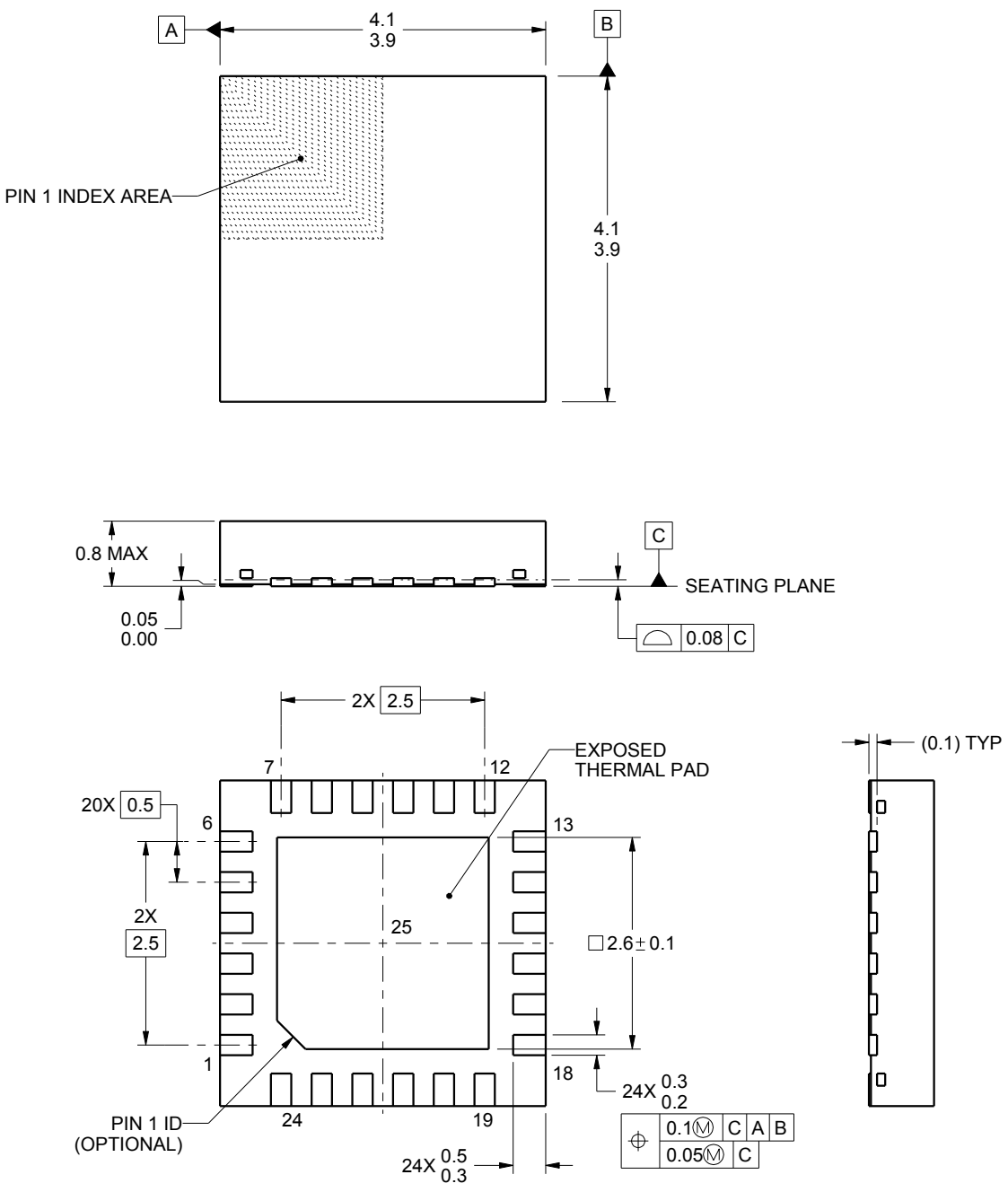
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS125BR111RTWR	WQFN	RTW	24	1000	210.0	185.0	35.0
DS125BR111RTWT	WQFN	RTW	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RTW0024A

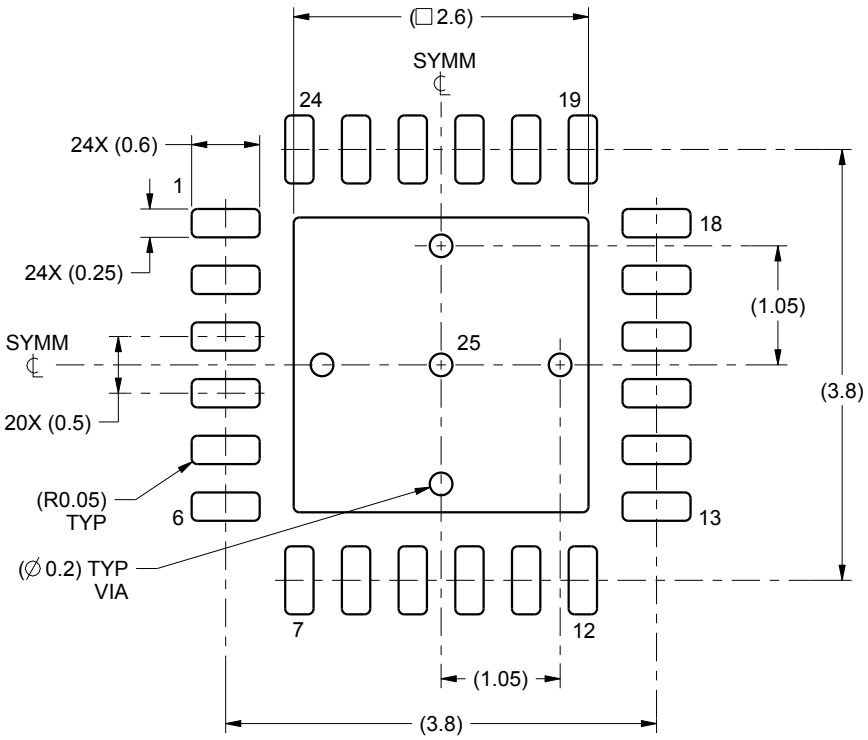
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

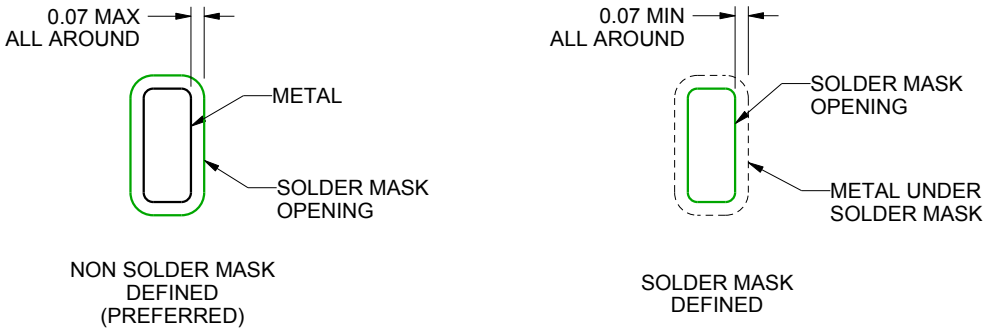


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

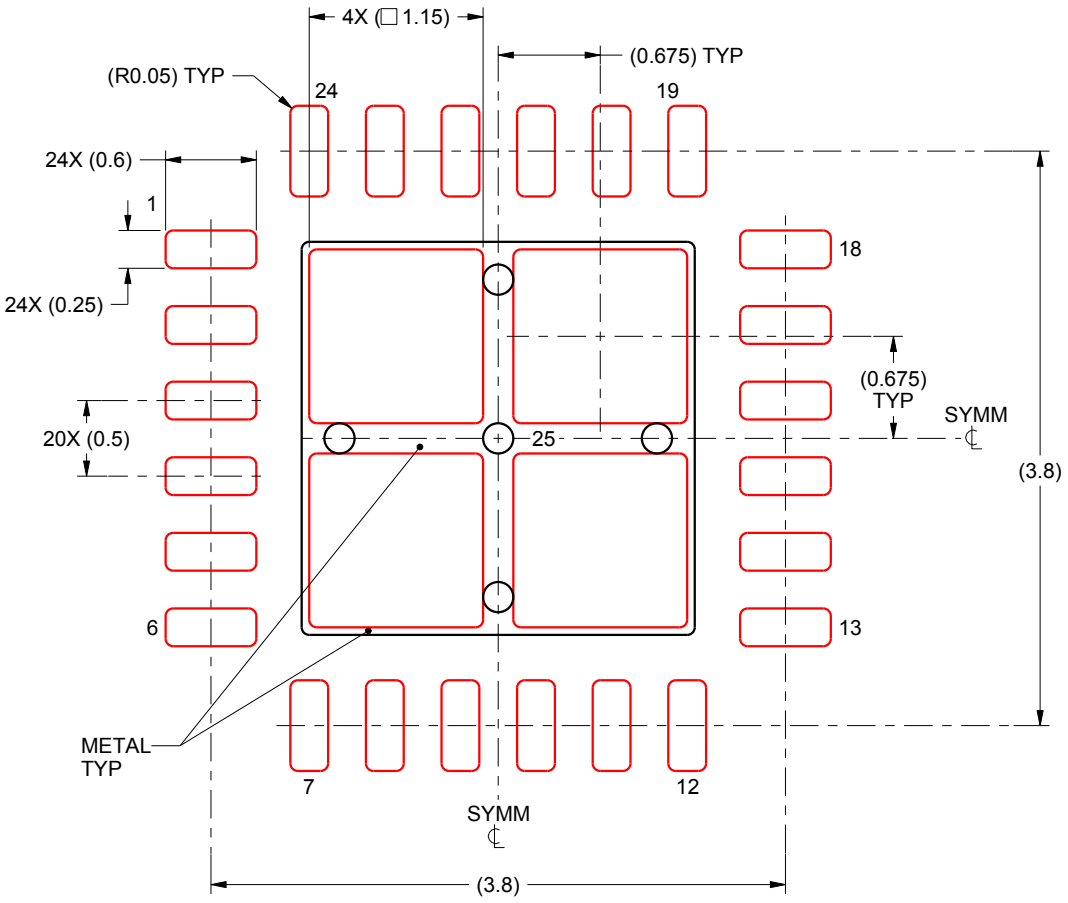


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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