



**THE DATASHEET OF
TLE2037QDRQ1**

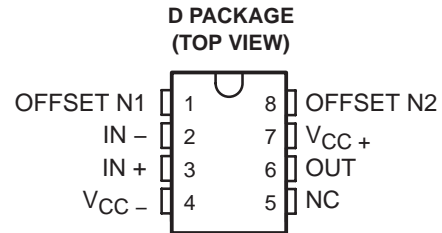


TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1 EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Outstanding Combination of DC Precision and AC Performance:
- Available in Standard-Pinout Small-Outline Package
- Output Features Saturation Recovery Circuitry
- Macromodels and Statistical information

Unity-Gain Bandwidth . . . 15 MHz Typ
 V_n 3.3 nV/ $\sqrt{\text{Hz}}$ at $f = 10$ Hz Typ,
 2.5 nV/ $\sqrt{\text{Hz}}$ at $f = 1$ kHz Typ
 V_{IO} 25 μV Max
 A_{VD} . . . 45 V/ μV Typ With $R_L = 2$ k Ω ,
 19 V/ μV Typ With $R_L = 600$ Ω



description

The TLE20x7 and TLE20x7A contain innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Manufactured using Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

In the area of dc precision, the TLE20x7 and TLE20x7A offer maximum offset voltages of 100 μV and 25 μV , respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/ μV (typ).

The ac performance of the TLE2027 and TLE2037 is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/ $\sqrt{\text{Hz}}$ and 2.5 nV/ $\sqrt{\text{Hz}}$ at frequencies of 10 Hz and 1 kHz, respectively. The TLE2037 and TLE2037A have been decompensated for faster slew rate (–7.5 V/ μs , typical) and wider bandwidth (50 MHz). To ensure stability, the TLE2037 and TLE2037A should be operated with a closed-loop gain of 5 or greater.

ORDERING INFORMATION†

T_A	$V_{IO\text{max}}$ AT 25°C	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	25 μV	SOIC (D)	Tape and reel	TLE2027AQDRQ1	2027AQ
				TLE2037AQDRQ1	2037AQ
	100 μV	SOIC (D)	Tape and reel	TLE2027QDRQ1	2027Q1
				TLE2037QDRQ1	2037Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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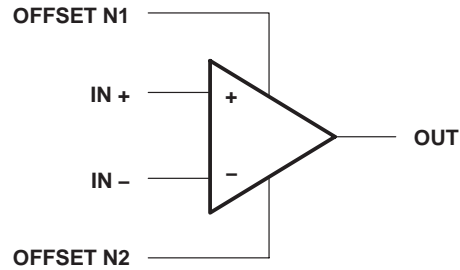
TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1 EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

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description (continued)

Both the TLE20x7 and TLE20x7A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The Q-suffix devices are characterized for operation from -40°C to 125°C .

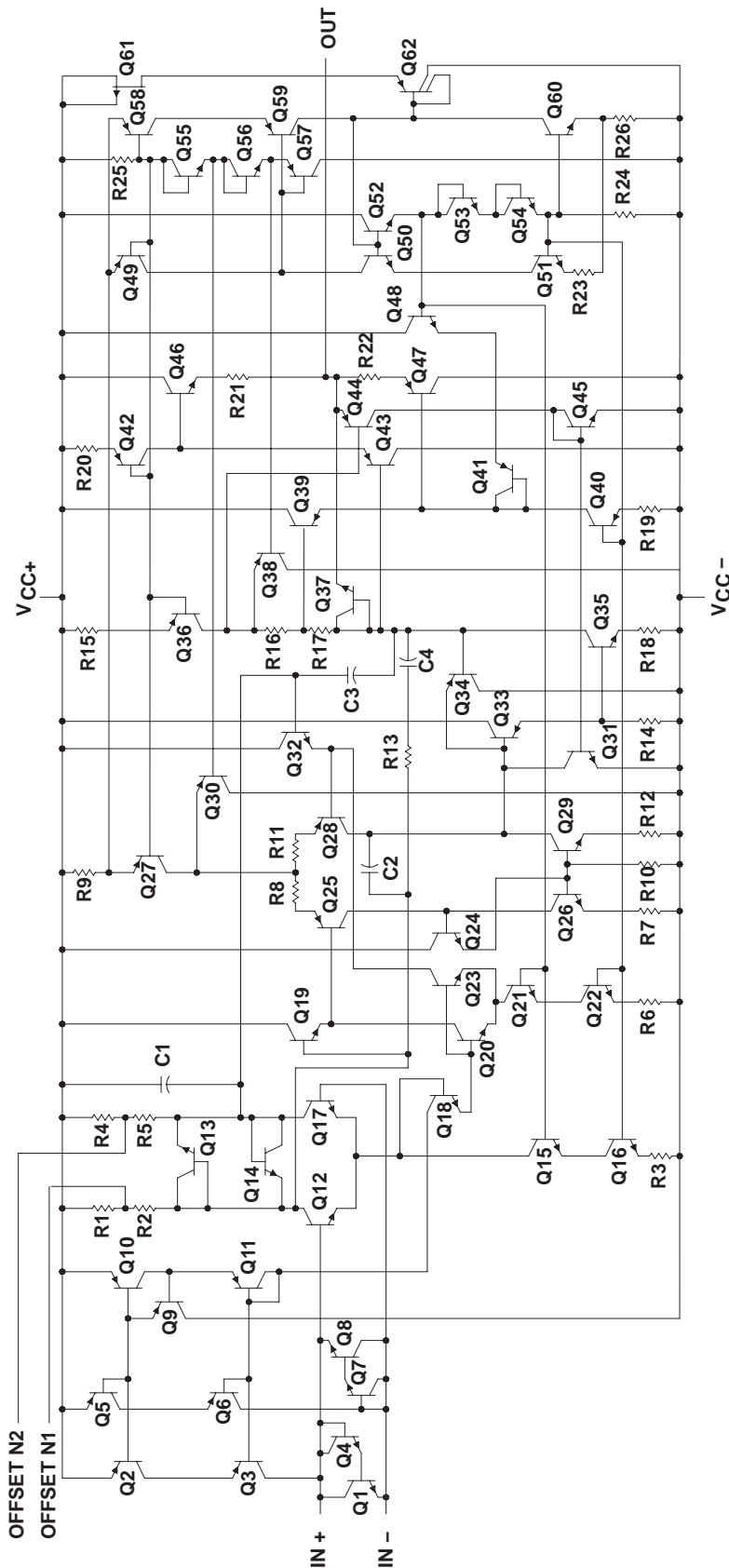
symbol



TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1 EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

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equivalent schematic



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	TLE2027	TLE2037
Transistors	61	61
Resistors	26	26
epiFET	1	1
Capacitors	4	4

TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1 EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	19 V
Supply voltage, V_{CC-}	-19 V
Differential input voltage, V_{ID} (see Note 2)	± 1.2 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each Input)	± 1 mA
Output current, I_O	± 50 mA
Total current into V_{CC+}	50 mA
Total current out of V_{CC-}	50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Junction temperature, T_J	142°C
Operating free-air temperature range, T_A : Q suffix	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Package thermal impedance, θ_{JA} (D Package) (0 LFPM) (see Note 4)	101°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if a differential input voltage in excess of approximately ± 1.2 V is applied between the inputs, unless some limiting resistance is used.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 4. The thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		± 4	± 19	V
Common-mode input voltage, V_{IC}	$T_A = 25^\circ\text{C}$	-11	11	V
	$T_A = \text{Full range}^\ddagger$	-10.2	10.2	
Operating free-air temperature, T_A		-40	125	°C

‡ Full range is -40°C to 125°C for Q-suffix devices.



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TLE20x7-Q1 electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE20x7-Q1			TLE20x7A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	20	100		10	25	μV	
		Full range			200		105		
α_{VIO} Temperature coefficient of input offset voltage		Full range	0.4	1		0.2	1	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.006	1		0.006	1	$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	6	90		6	90	nA	
		Full range			150		150		
I_{IB} Input bias current		25°C	15	90		15	90	nA	
		Full range			150		150		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-11 to 11	-13 to 13		-11 to 11	-13 to 13	V	
		Full range	-10.3 to 10.3			-10.4 to 10.4			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5	12.9		10.5	12.9	V	
		Full range	10			10			
	$R_L = 2\ \text{k}\Omega$	25°C	12	13.2		12	13.2		
		Full range	11			11			
V_{OM-} Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	-10.5	-13		-10.5	-13	V	
		Full range	-10			-10			
	$R_L = 2\ \text{k}\Omega$	25°C	-12	-13.5		-12	-13.5		
		Full range	-11			-11			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 11\ \text{V}, R_L = 2\ \text{k}\Omega$	25°C	5	45		10	45	V/ μV	
	$V_O = \pm 10\ \text{V}, R_L = 2\ \text{k}\Omega$	Full range	2.5			3.5			
	$V_O = \pm 10\ \text{V}, R_L = 1\ \text{k}\Omega$	25°C	3.5	38		8	38		
		Full range	1.8			2.2			
$V_O = \pm 10\ \text{V}, R_L = 600\ \Omega$	25°C	2	19		5	19			
C_i Input capacitance		25°C	8			8	pF		
z_o Open-loop output impedance	$I_O = 0$	25°C	50			50	Ω		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	100	131		117	131	dB	
		Full range	96			113			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4\ \text{V to } \pm 18\ \text{V}, R_S = 50\ \Omega$	25°C	94	144		110	144	dB	
		Full range	90			105			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C	3.8	5.3		3.8	5.3	mA	
		Full range			5.6		5.6		

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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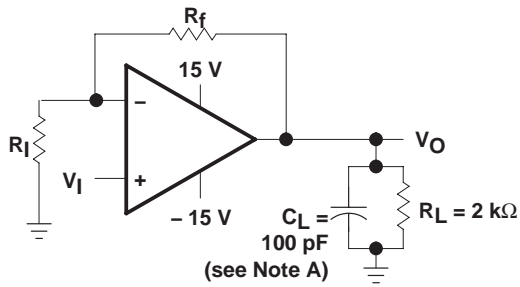
TLE20x7-Q1 operating characteristics at specified free-air temperature, $V_{CC \pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS		TLE20x7-Q1			TLE20x7A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Figure 1	TLE2027	1.7	2.8		1.7	2.8	V/ μs
			TLE2037	6	7.5		6	7.5	
	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_A = -55^\circ\text{C}$ to 125°C , See Figure 1	TLE2027	1			1			
		TLE2037	4.4			4.4			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\ \Omega$, $f = 10\text{ Hz}$		3.3	8		3.3	4.5	nV/ $\sqrt{\text{Hz}}$
			$R_S = 20\ \Omega$, $f = 1\text{ kHz}$		2.5	4.5		2.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 10 Hz		50	250		50	130	nV
I_n	Equivalent input noise current	$f = 10\text{ Hz}$		10			10		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.8			0.8		
THD	Total harmonic distortion	$V_O = +10\text{ V}$, $A_{VD} = 1$, See Note 5	TLE2027	<0.002			<0.002		%
		$V_O = +10\text{ V}$, $A_{VD} = 5$, See Note 5	TLE2037	<0.002			<0.002		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$	TLE2027	7	13		9	13	MHz
			TLE2037	35	50		35	50	
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\text{ k}\Omega$	TLE2027	30			30		kHz
			TLE2037	80			80		
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$	TLE2027	55			55		°
			TLE2037	50			50		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.



PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

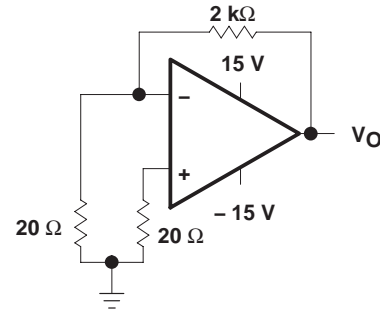
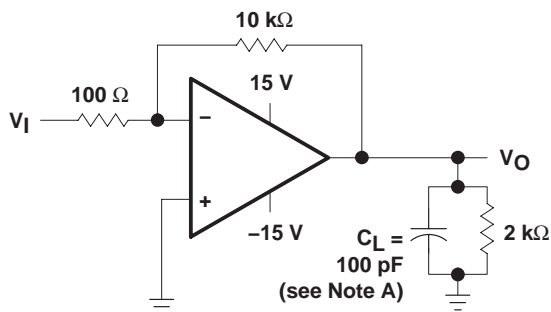
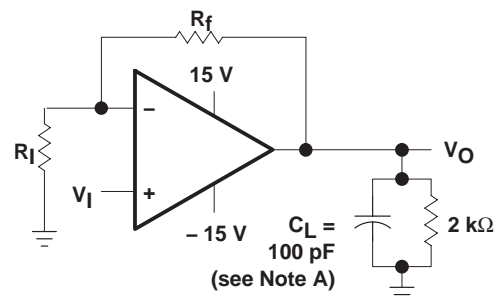


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit (TLE2027 Only)



NOTES: A. C_L includes fixture capacitance.
 B. For the TLE2037 and TLE2037A, A_{VD} must be ≥ 5 .

Figure 4. Small-Signal Pulse-Response Test Circuit

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typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the ongoing program of improving data sheets and supplying more information to our customers, Texas Instruments has added an estimate of not only the typical values, but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from the characterization of the initial wafer lots of this new device type (see Figure 5). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ± 3 sigma, since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 5, there were a total of 835 units from two wafer lots. In this case, there is a good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This is always the case on newly released products, since there can only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. While 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

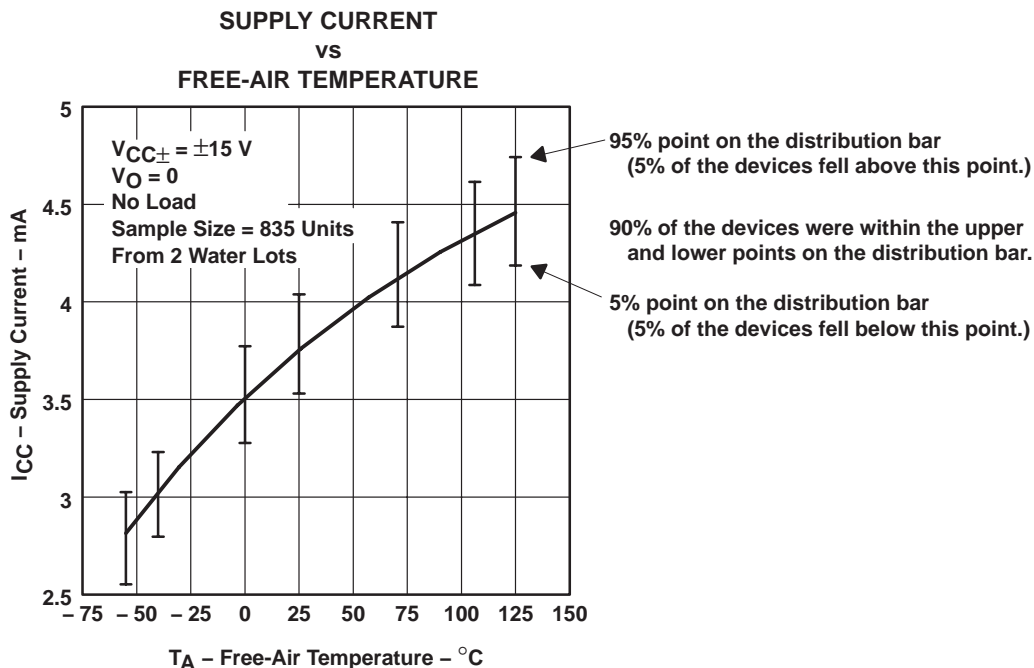


Figure 5. Sample Graph With Distribution Bars



TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1
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TYPICAL CHARACTERISTICS

Table of Graphs

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I_{IO}	Input offset current	vs Free-air temperature	10
I_{IB}	Input bias current	vs Free-air temperature	11
		vs Common-mode input voltage	12
I_I	Input current	vs Differential input voltage	13
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	14, 15
V_{OM}	Maximum (positive/negative) peak output voltage	vs Load resistance	16, 17
		vs Free-air temperature	18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	20
		vs Load resistance	21
		vs Frequency	22 – 25
		vs Free-air temperature	26
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ϕ_m	Phase margin	vs Supply voltage	50, 51
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	Phase shift	vs Frequency	22 – 25

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TYPICAL CHARACTERISTICS

**DISTRIBUTION
INPUT OFFSET VOLTAGE**

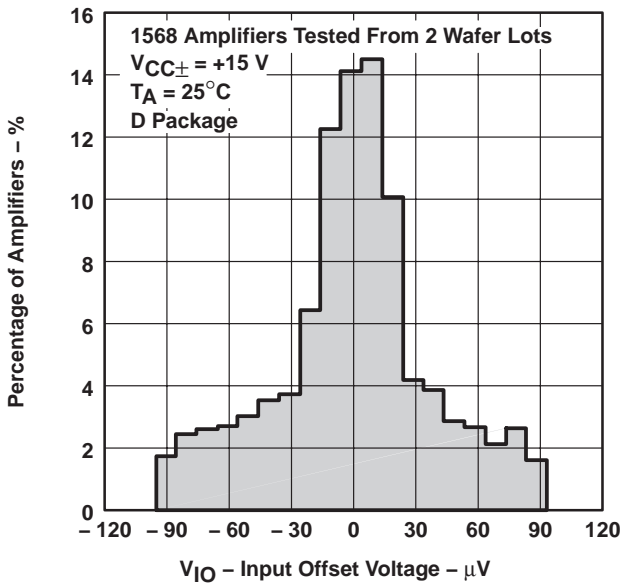


Figure 6

**INPUT OFFSET VOLTAGE CHANGE
VS
TIME AFTER POWER ON**

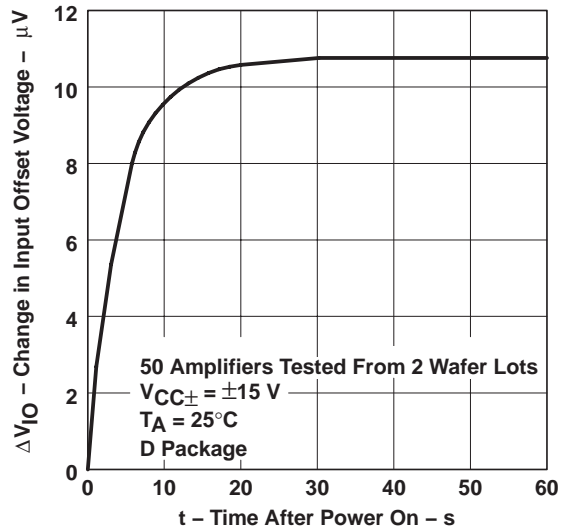


Figure 7

**INPUT OFFSET VOLTAGE CHANGE
VS
TIME AFTER POWER ON**

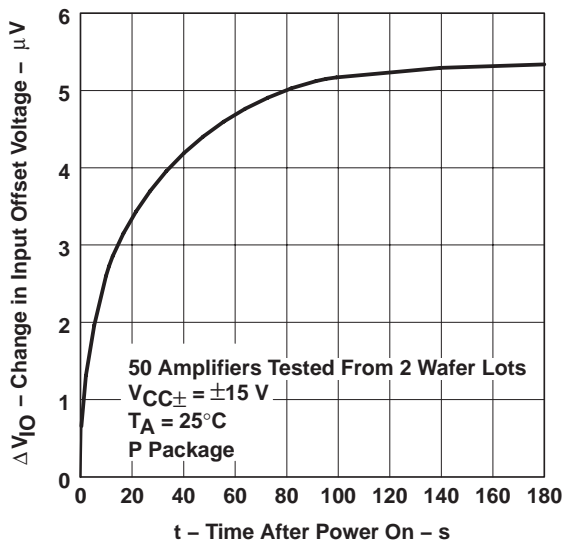


Figure 8

**INPUT OFFSET CURRENT†
VS
FREE-AIR TEMPERATURE**

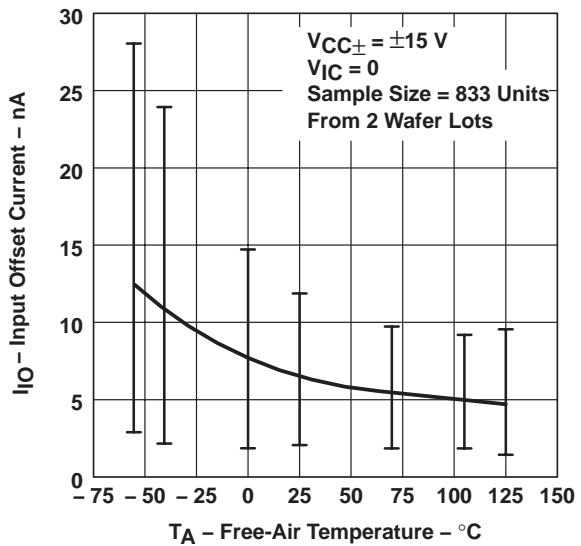


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**INPUT BIAS CURRENT †
 vs
 FREE-AIR TEMPERATURE**

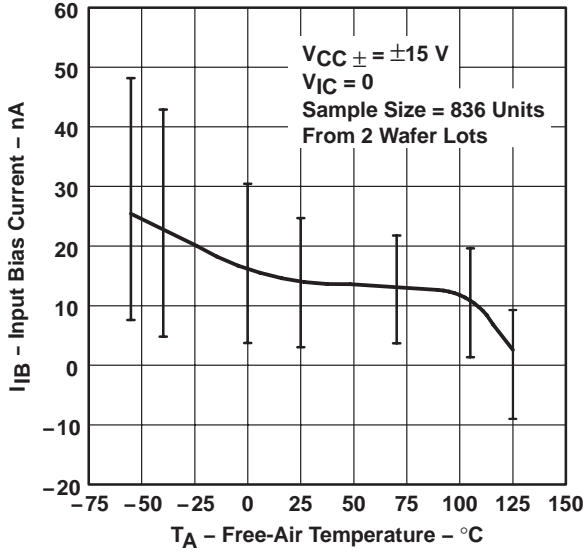


Figure 10

**INPUT BIAS CURRENT
 vs
 COMMON-MODE INPUT VOLTAGE**

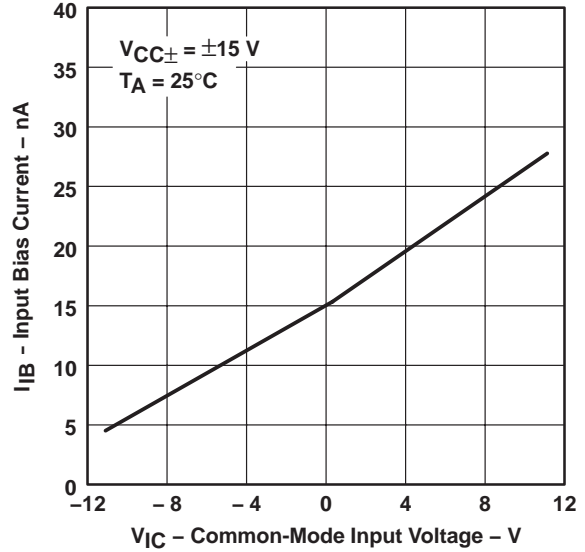


Figure 11

**INPUT CURRENT
 vs
 DIFFERENTIAL INPUT VOLTAGE**

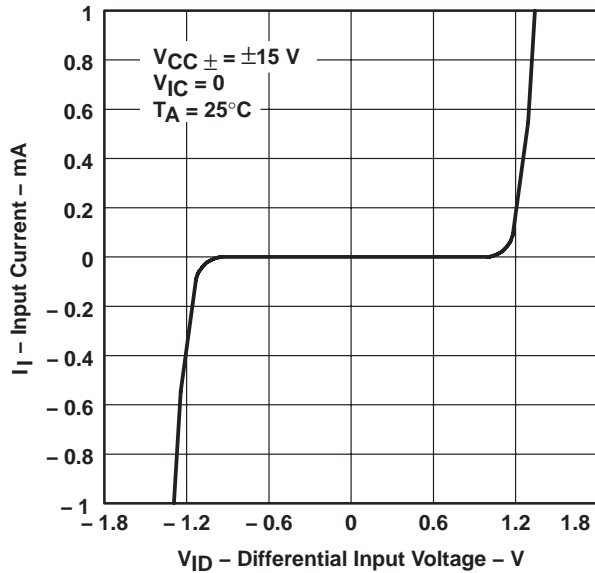


Figure 12

**TLE2027
 MAXIMUM PEAK-TO-PEAK
 OUTPUT VOLTAGE †
 vs
 FREQUENCY**

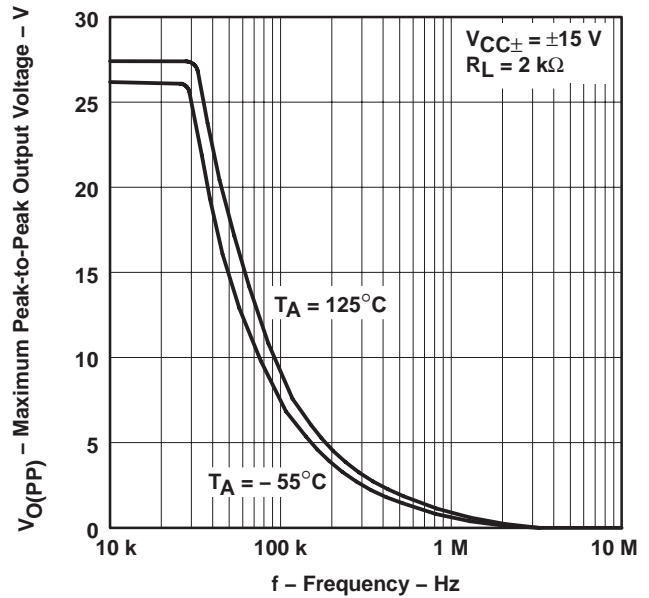


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

TLE2037
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE†
vs
FREQUENCY

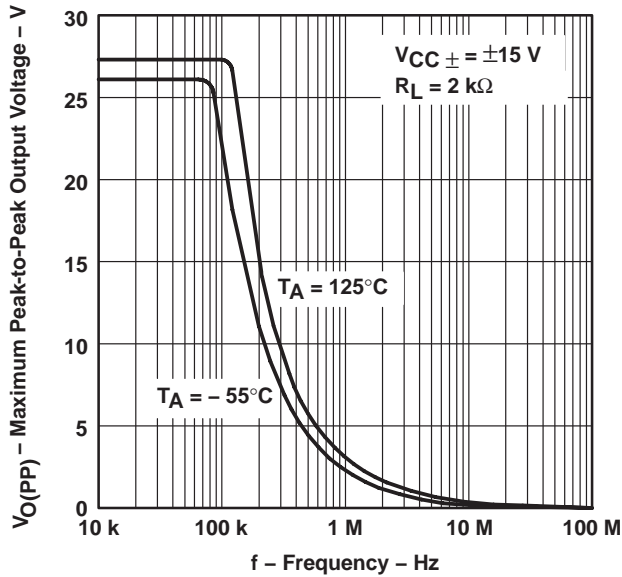


Figure 14

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

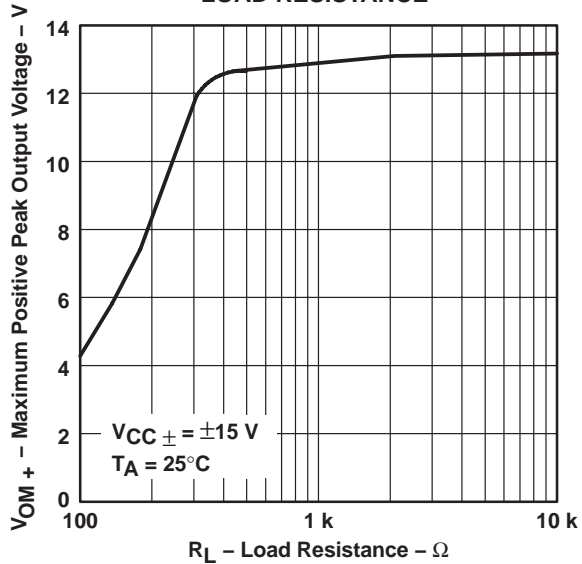


Figure 15

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

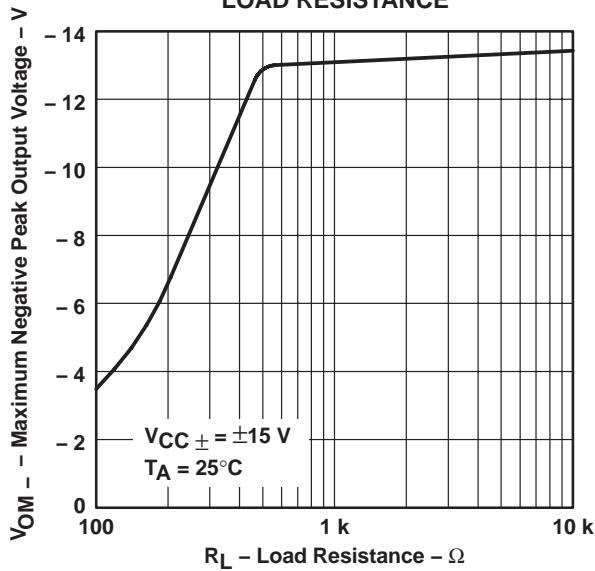


Figure 16

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

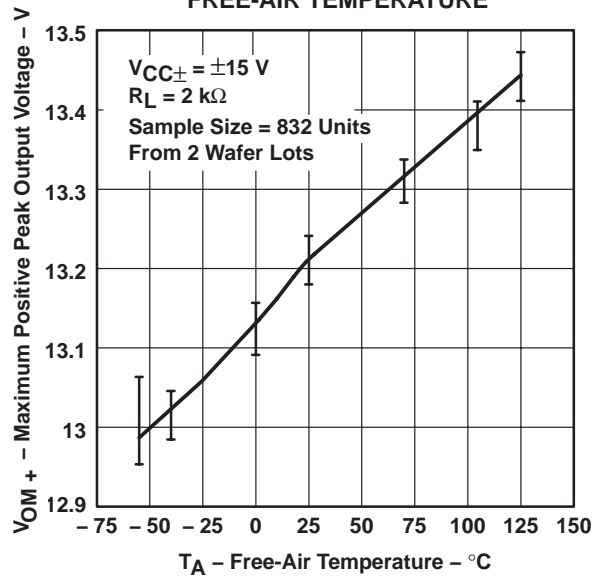
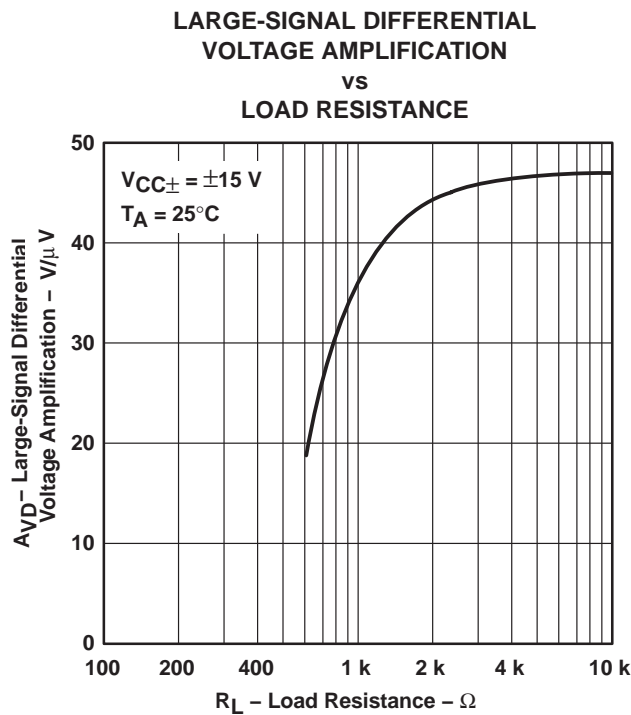
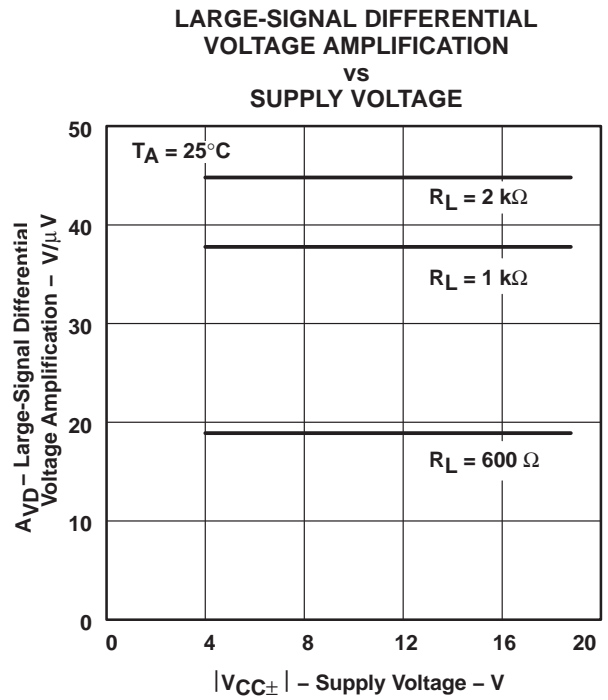
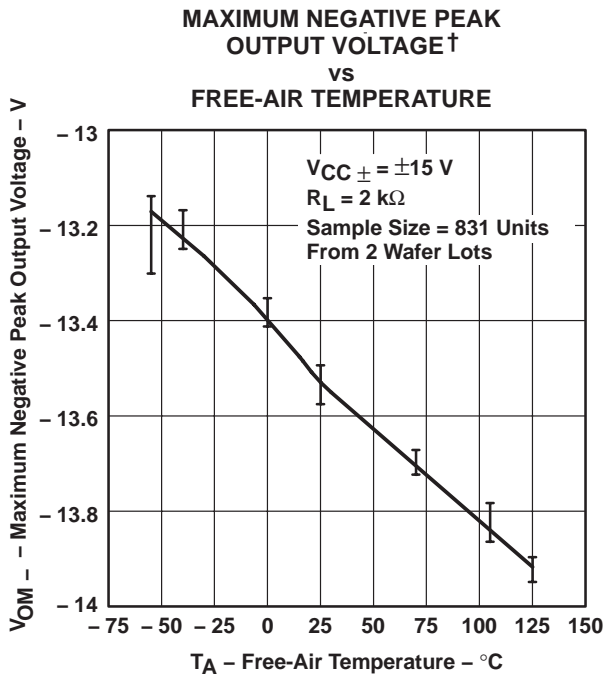


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

TLE2027
LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

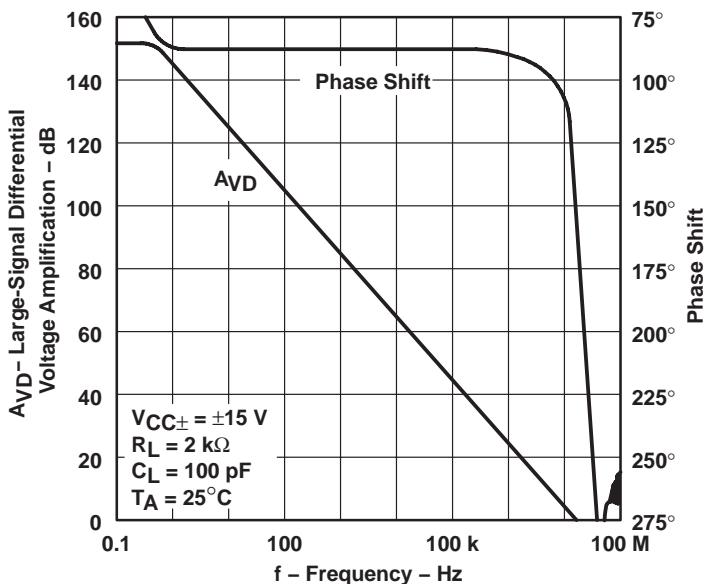


Figure 21

TLE2037
LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

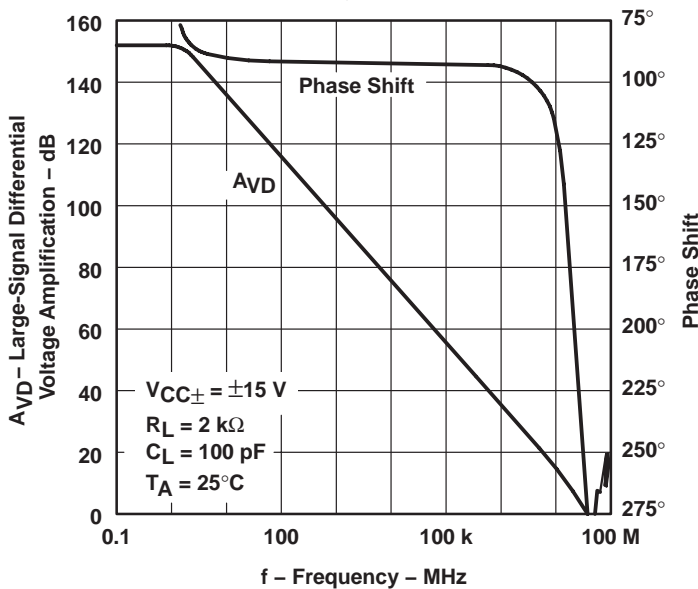


Figure 22



TYPICAL CHARACTERISTICS

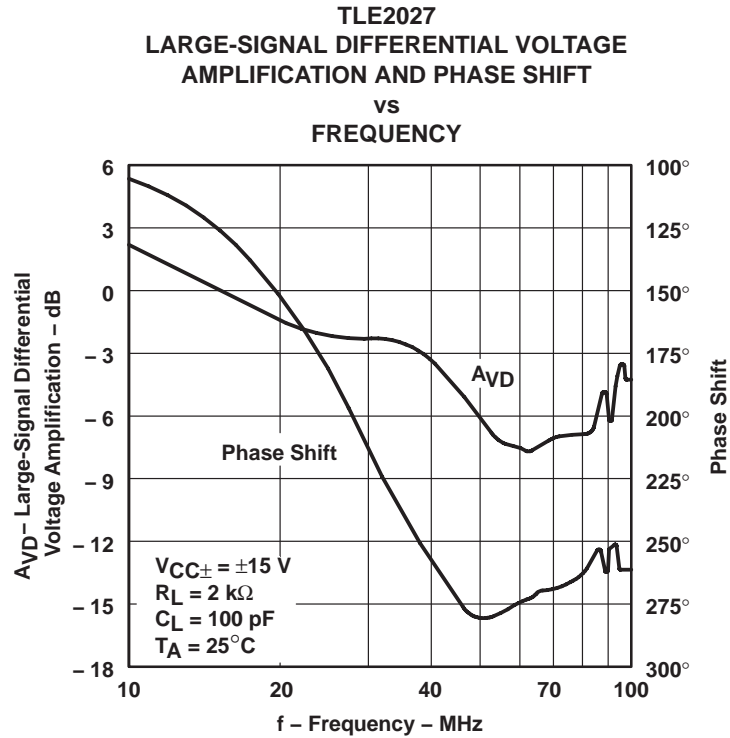


Figure 23

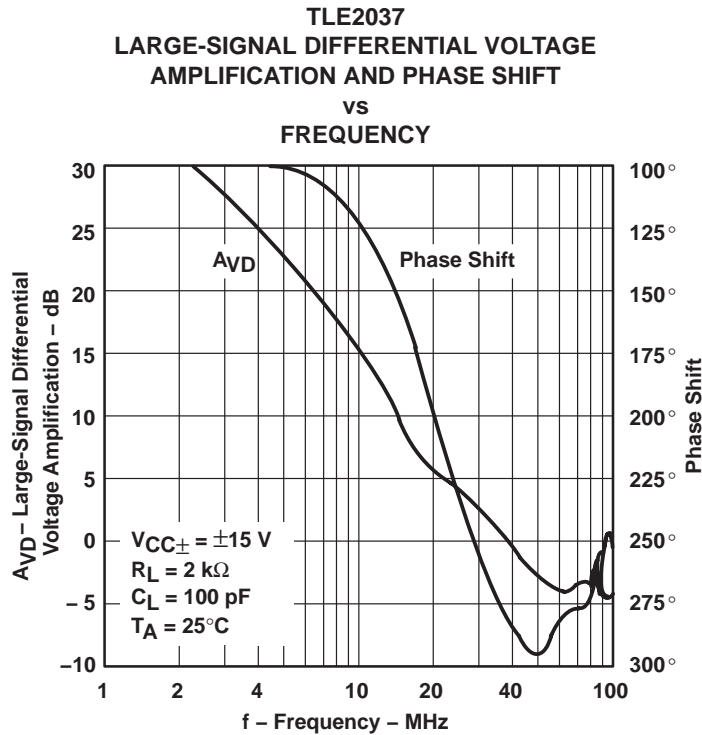


Figure 24

TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1
EXCALIBUR LOW-NOISE HIGH-SPEED
PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†
VS
FREE-AIR TEMPERATURE

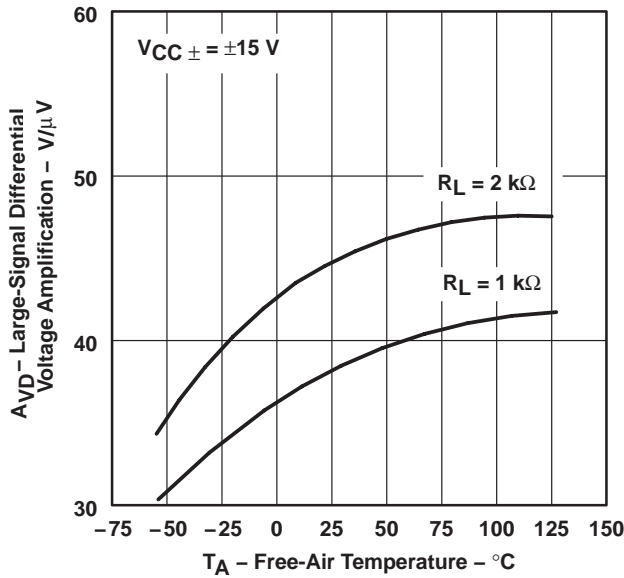
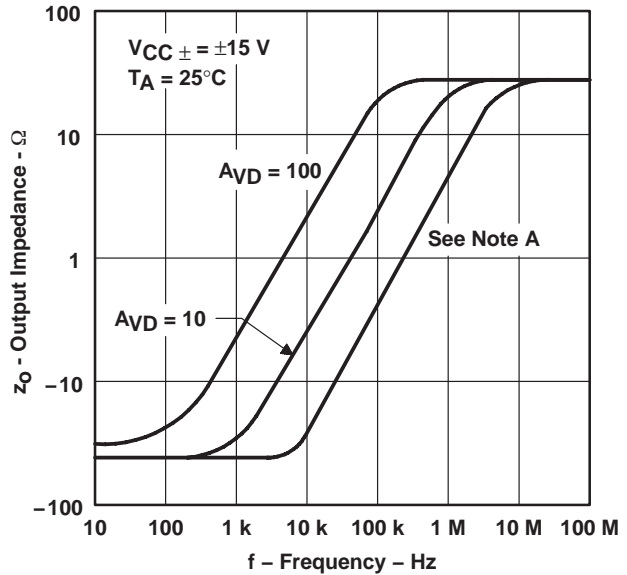


Figure 25

OUTPUT IMPEDANCE
VS
FREQUENCY



NOTE A: For this curve, the TLE2027 is $A_{VD} = 1$ and the TLE2037 is $A_{VD} = 5$.

Figure 26

COMMON-MODE REJECTION RATIO
VS
FREQUENCY

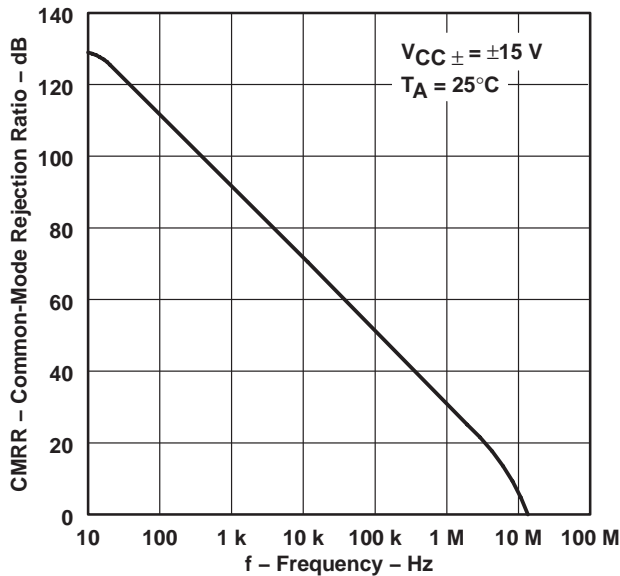


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO
VS
FREQUENCY

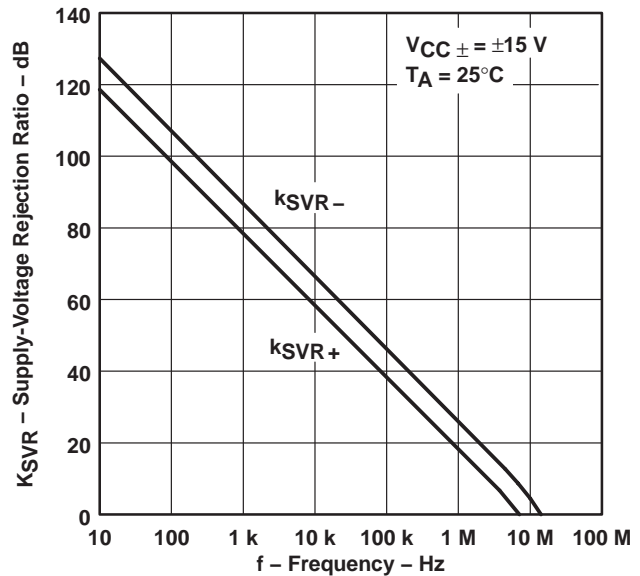


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 SUPPLY VOLTAGE

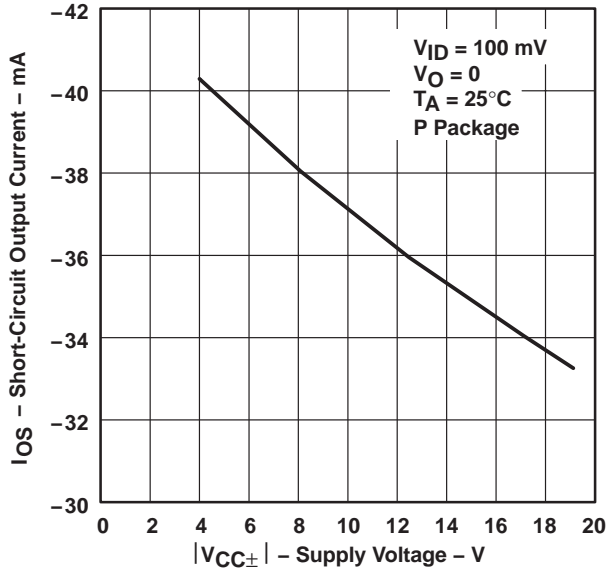


Figure 29

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 SUPPLY VOLTAGE

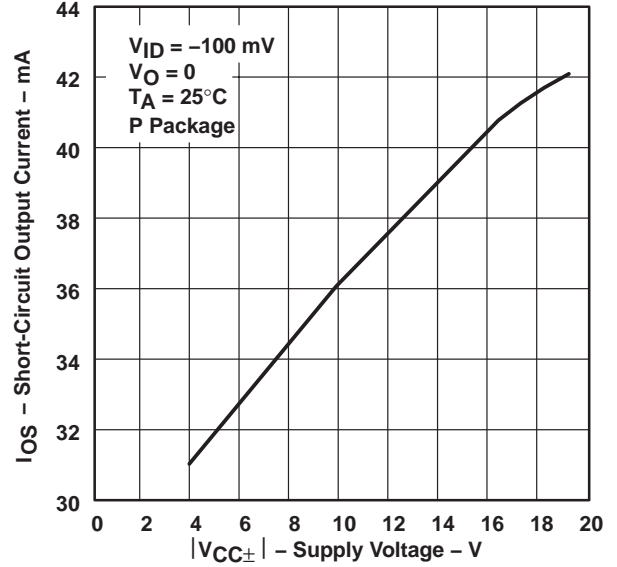


Figure 30

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 ELAPSED TIME

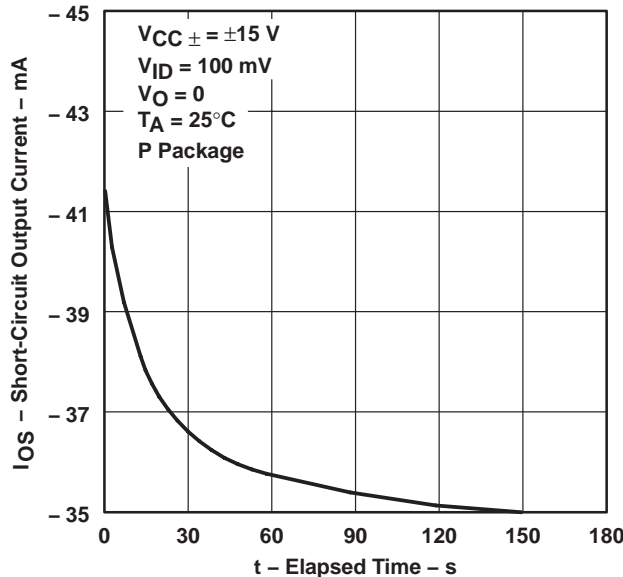


Figure 31

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 ELAPSED TIME

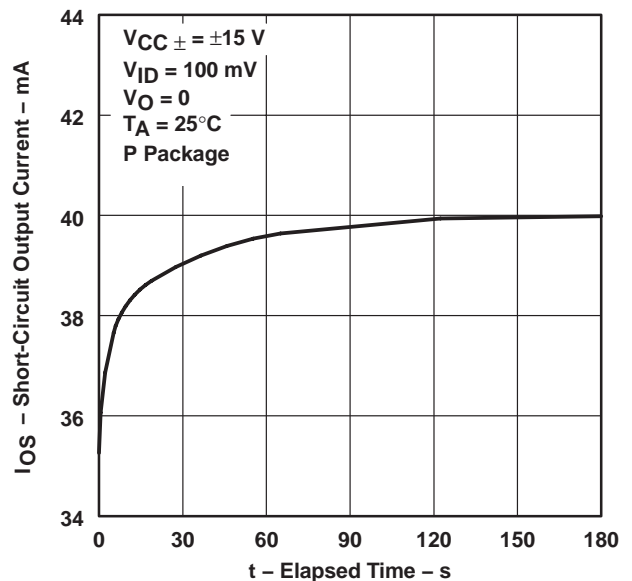


Figure 32

TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1
EXCALIBUR LOW-NOISE HIGH-SPEED
PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

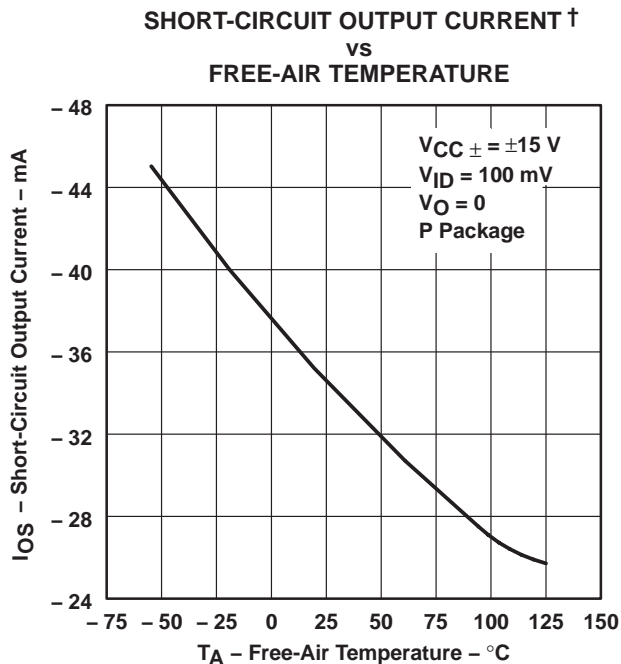


Figure 33

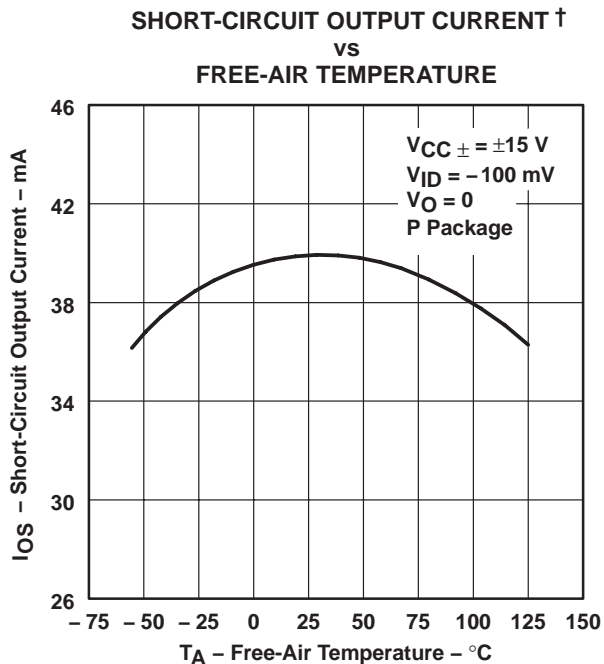


Figure 34

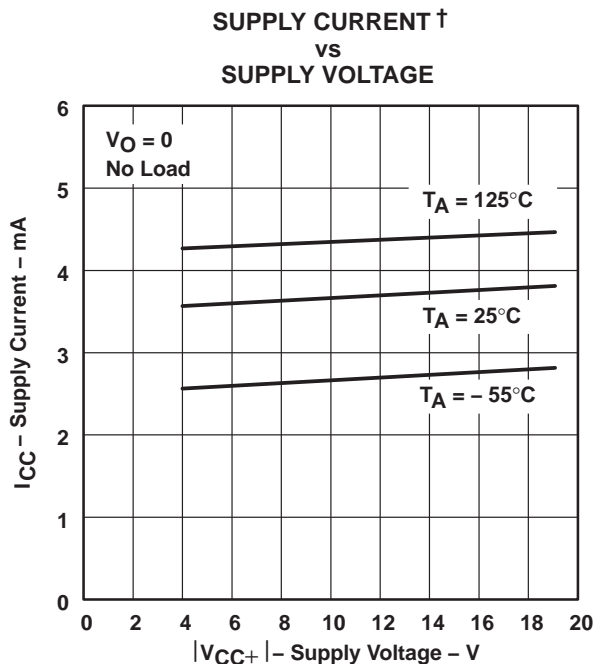


Figure 35

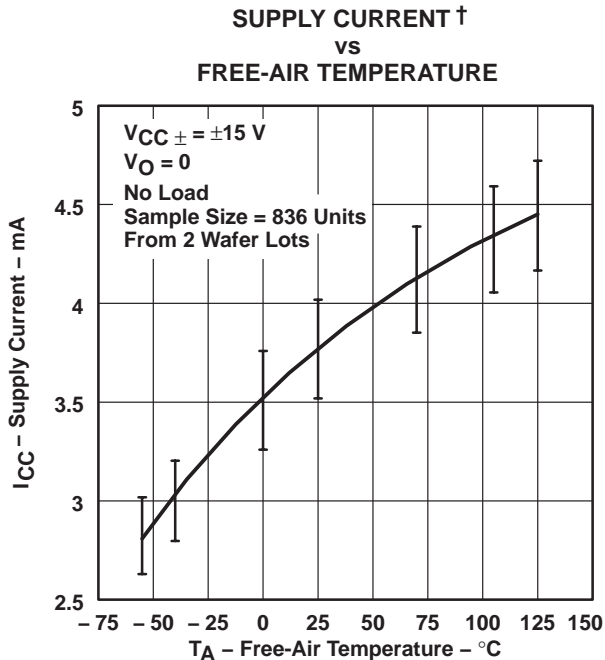


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS

TLE2027
 VOLTAGE-FOLLOWER
 SMALL-SIGNAL
 PULSE RESPONSE

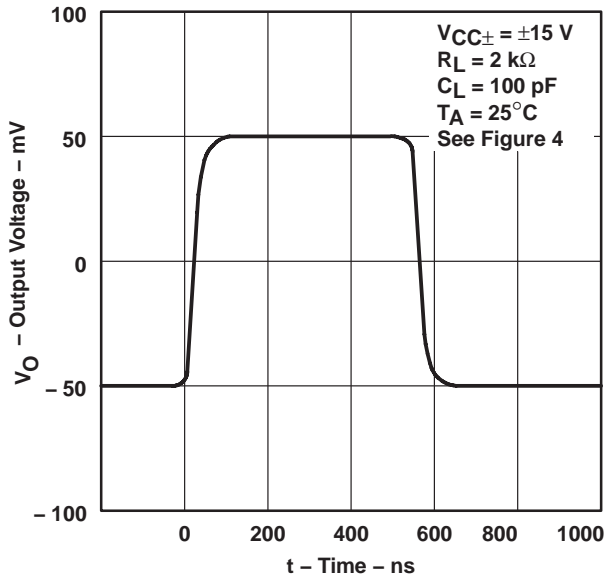


Figure 37

TLE2027
 VOLTAGE-FOLLOWER
 LARGE-SIGNAL
 PULSE RESPONSE

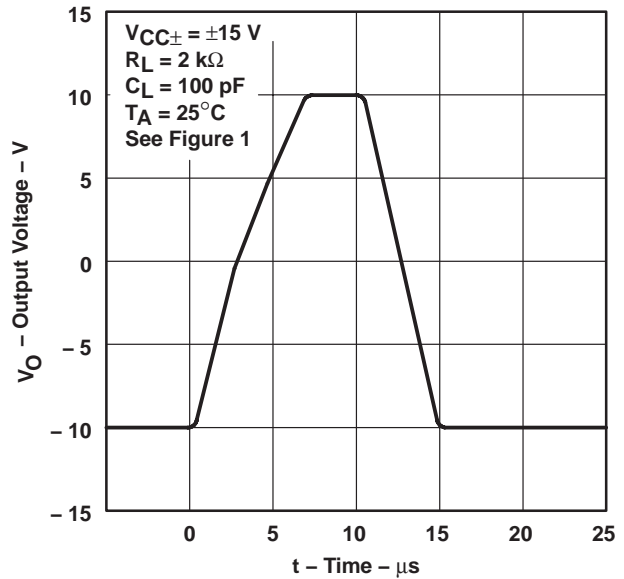


Figure 38

TLE2037
 VOLTAGE-FOLLOWER
 SMALL-SIGNAL
 PULSE RESPONSE

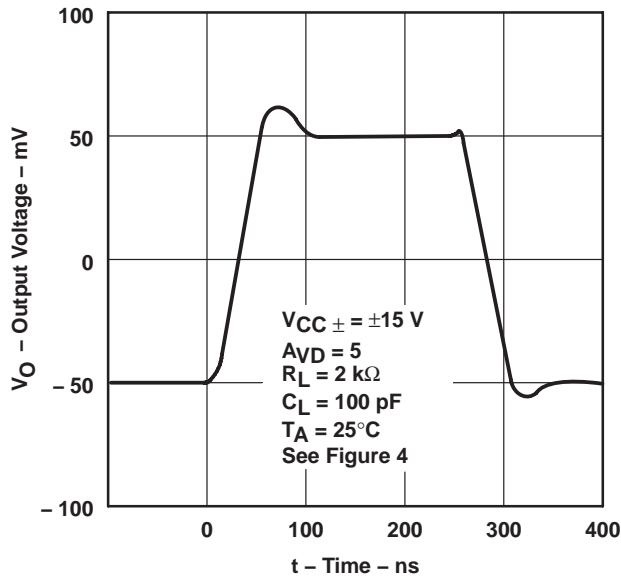


Figure 39

TLE2037
 VOLTAGE-FOLLOWER
 LARGE-SIGNAL
 PULSE RESPONSE

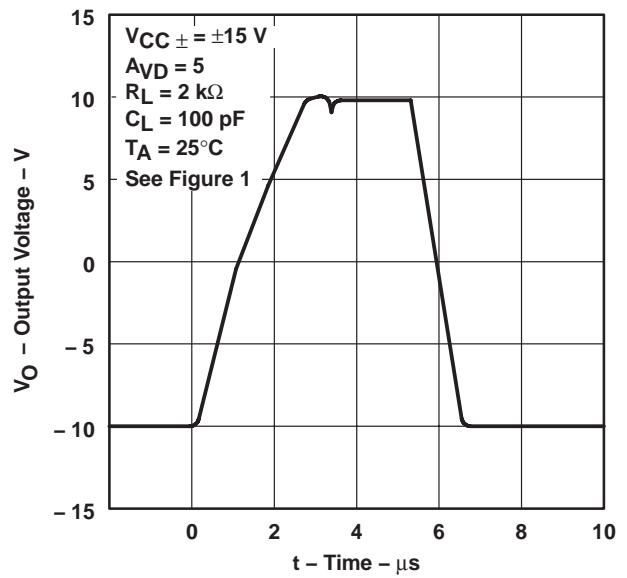


Figure 40

TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1
EXCALIBUR LOW-NOISE HIGH-SPEED
PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**EQUIVALENT INPUT NOISE VOLTAGE
 vs
 FREQUENCY**

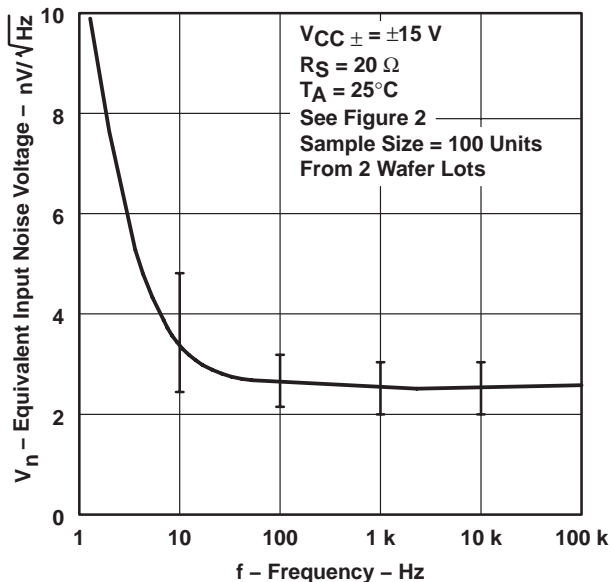


Figure 41

**NOISE VOLTAGE
 (REFERRED TO INPUT)
 OVER A 10-SECOND INTERVAL**

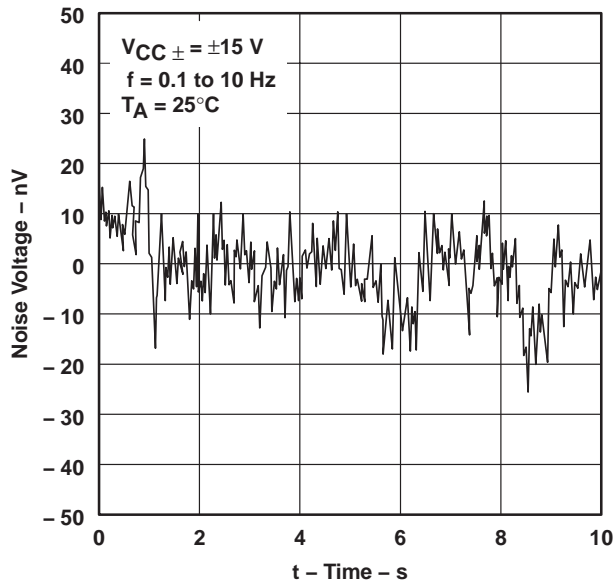


Figure 42

**TLE2027
 UNITY-GAIN BANDWIDTH
 vs
 SUPPLY VOLTAGE**

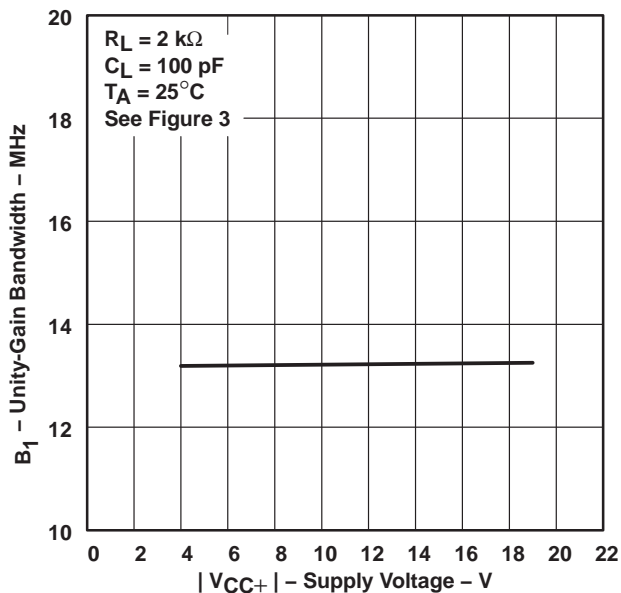


Figure 43

**TLE2037
 GAIN-BANDWIDTH PRODUCT
 vs
 SUPPLY VOLTAGE**

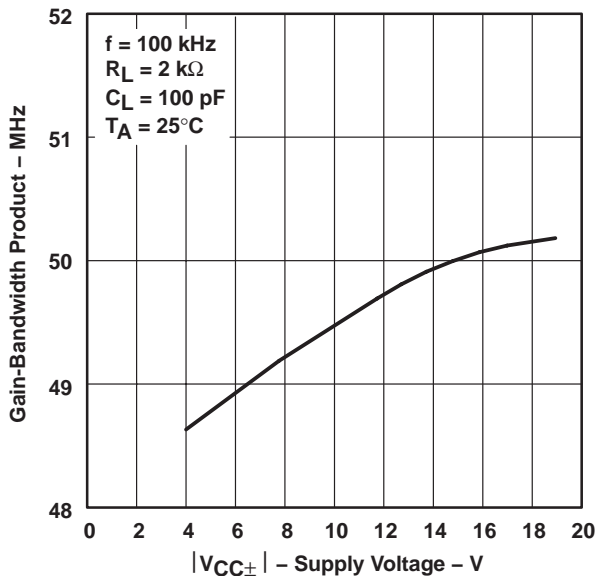
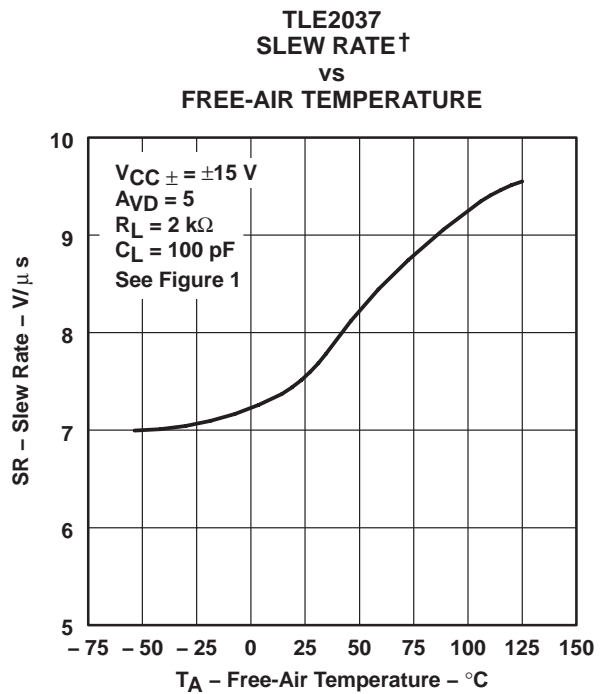
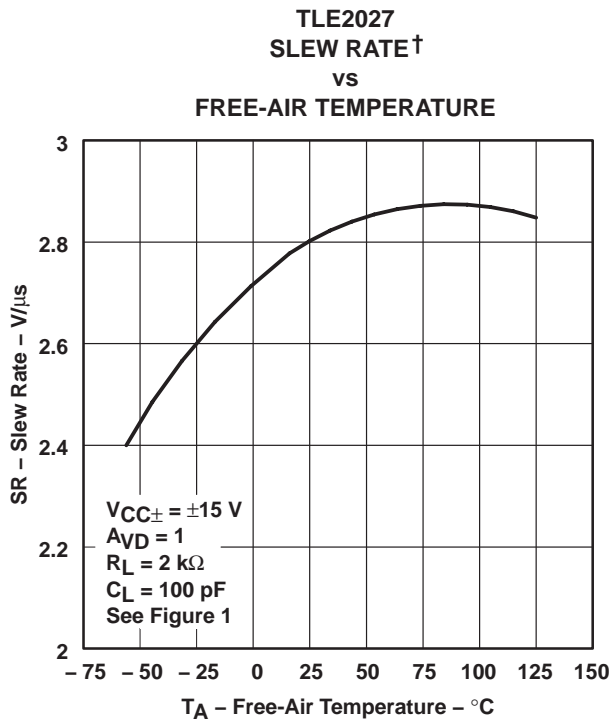
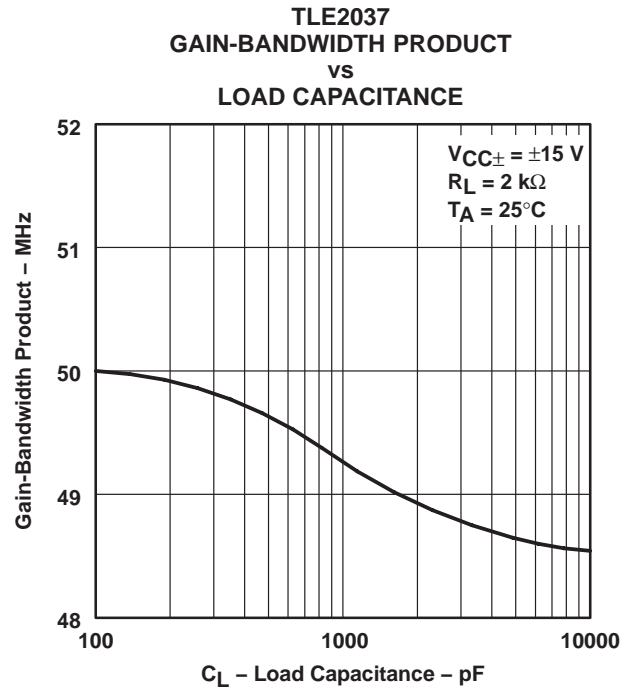
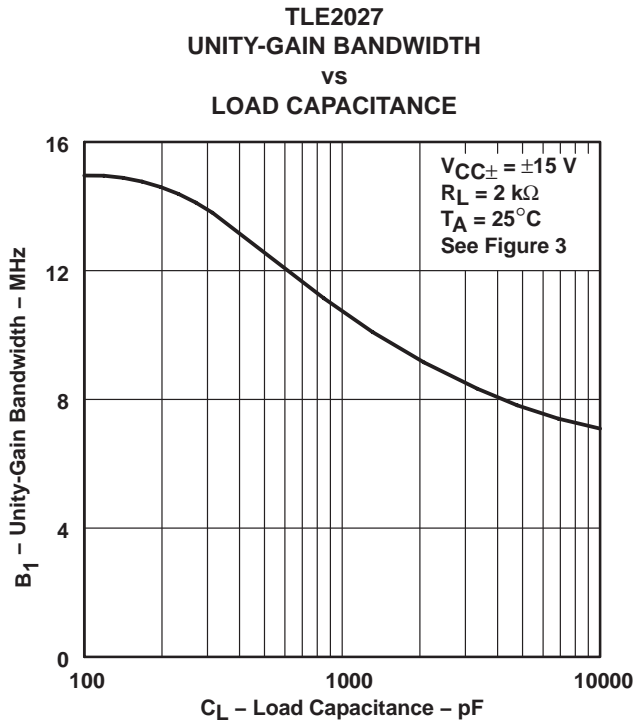


Figure 44



TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1
EXCALIBUR LOW-NOISE HIGH-SPEED
PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

TLE2027
PHASE MARGIN
vs
SUPPLY VOLTAGE

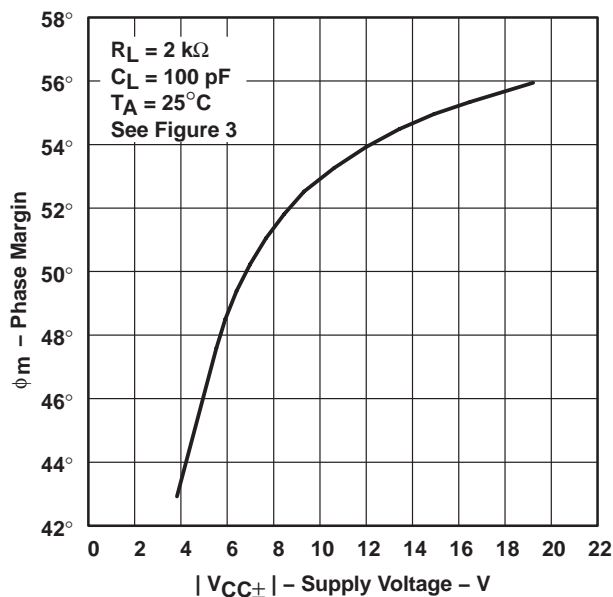


Figure 49

TLE2037
PHASE MARGIN
vs
SUPPLY VOLTAGE

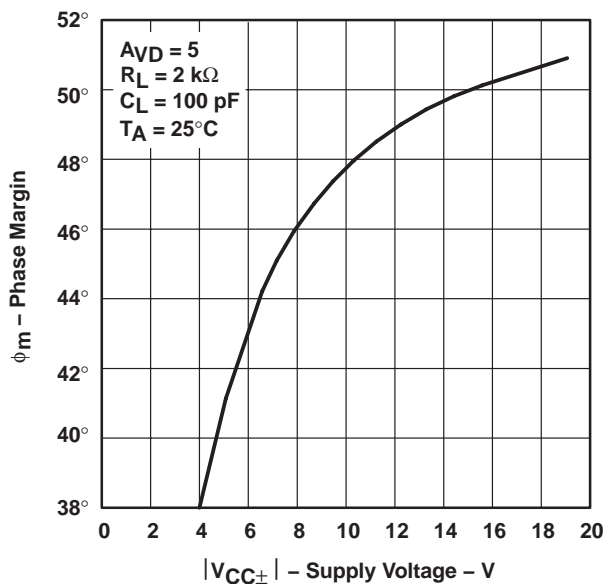


Figure 50

TLE2027
PHASE MARGIN
vs
LOAD CAPACITANCE

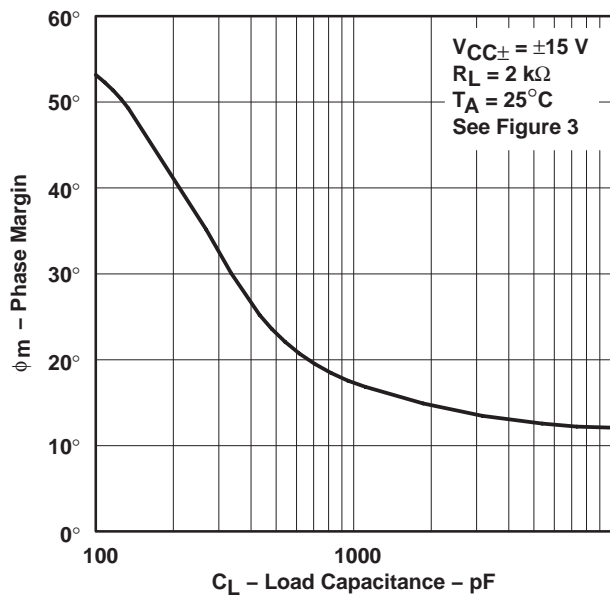


Figure 51

TLE2037
PHASE MARGIN
vs
LOAD CAPACITANCE

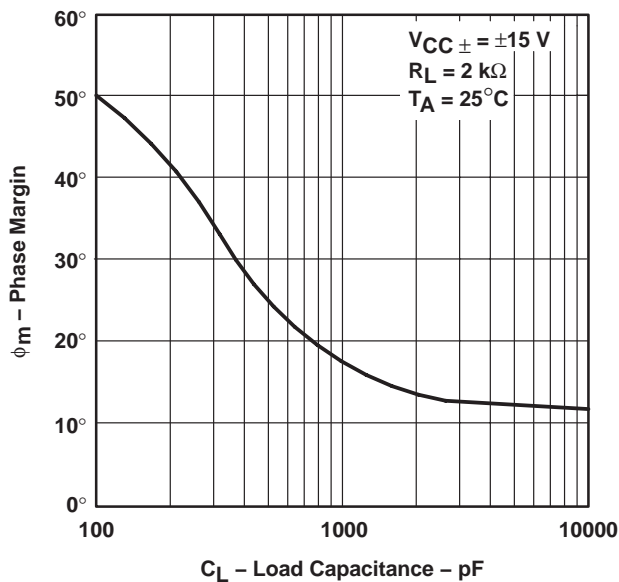


Figure 52



TYPICAL CHARACTERISTICS

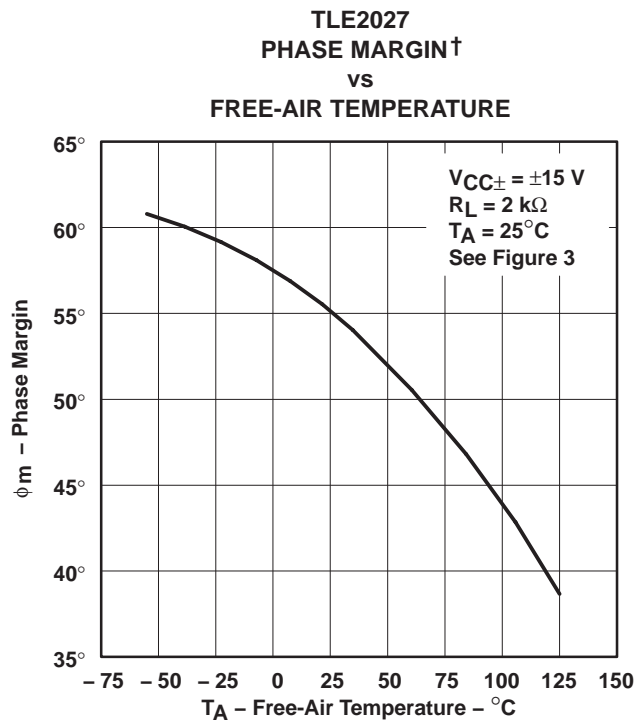


Figure 53

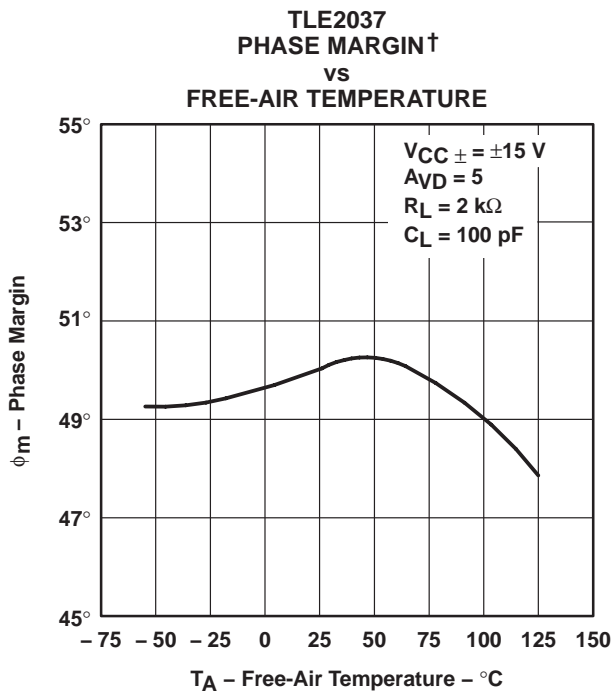


Figure 54

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input offset voltage nulling

The TLE2027 and TLE2037 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 55 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

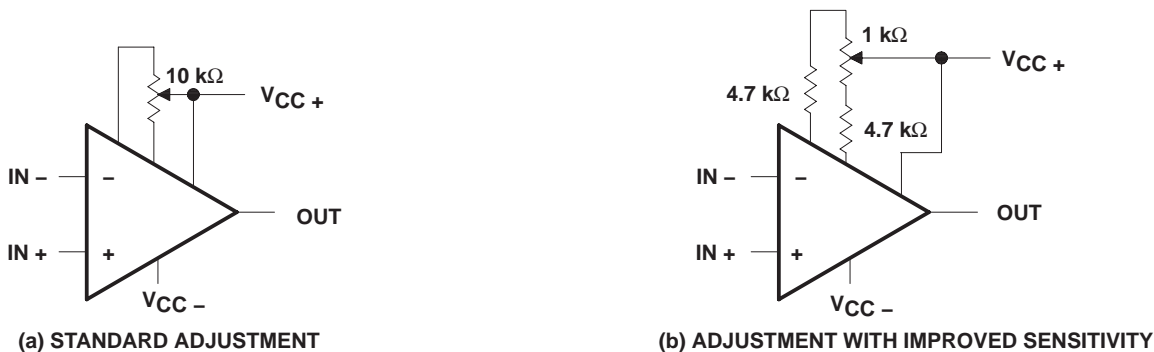


Figure 55. Input Offset Voltage Nulling Circuits

voltage-follower applications

The TLE2027 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 56).

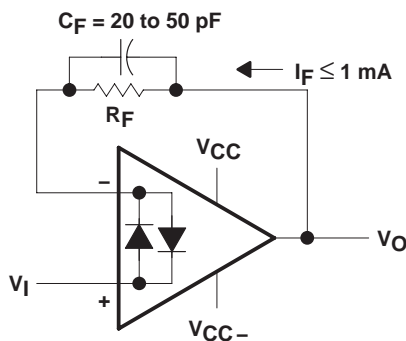


Figure 56. Voltage Follower

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*[™], the model generation software used with Microsim *PSpice*[™]. The Boyle macromodel (see Note 6) and subcircuit in Figure 57, Figure 58, and Figure 59 were generated using the TLE20x7 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

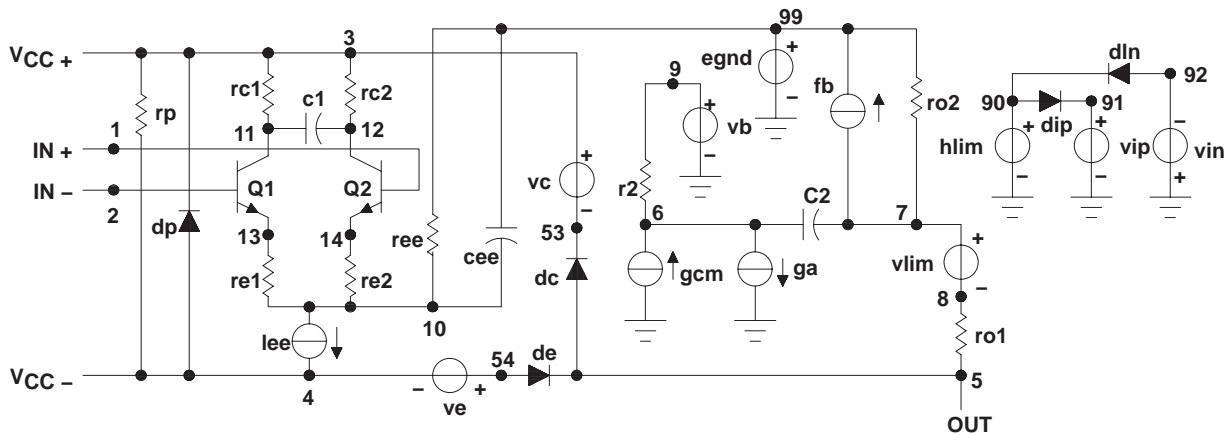


Figure 57. Boyle Macromodel

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TLE2027-Q1, TLE2037-Q1, TLE2027A-Q1, TLE2037A-Q1
EXCALIBUR LOW-NOISE HIGH-SPEED
PRECISION OPERATIONAL AMPLIFIERS

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APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2027 1 2 3 4 5
*
c1      11  12  4.003E-12
c2      6   7   20.00E-12
dc      5   53  dz
de      54  5   dz
dlp     90  91  dz
dln     92  90  dx
dp      4   3   dz
egnd    99  0   poly(2) (3,0)
(4,0)  0  5   .5
fb      7   99  poly(5) vb vc
ve vlp vln 0 954.8E6 -1E9 1E9 1E9
-1E9
ga      6   0   11  12
2.062E-3
gcm     0   6   10  99
531.3E-12
iee     10  4   dc  56.01E-6
hlim    90  0   vlim 1K
q1      11  2   13 qx
q2      12  1   14 qx
r2      6   9   100.0E3
rc1     3   11  530.5
rc2     3   12  530.5
re1     13  10  -393.2
re2     14  10  -393.2
ree     10  99  3.571E6
ro1     8   5   25
ro2     7   99  25
rp      3   4   8.013E3
vb      9   0   dc  0
vc      3   53  dc  2.400
ve      54  4   dc  2.100
vlim    7   8   dc  0
vlp     91  0   dc  40
vln     0   92  dc  40
.modeldx D(Is=800.0E-18)
.modelqx NPN(Is=800.0E-18
Bf=7.000E3)
.ends
```

Figure 58. TLE2027 Macromodel Subcircuit

```
.subckt TLE2037 1 2 3 4 5
*
c1      11  12  4.003E-12
c2      6   7   7.500E-12
dc      5   53  dz
de      54  5   dz
dlp     90  91  dz
dln     92  90  dx
dp      4   3   dz
egnd    99  0   poly(2) (3,0)
(4,0)  0  .5  .5
fb      7   99  poly(5) vb vc
ve vip vln 0 923.4E6 A800E6
800E6 800E6 A800E6
ga      6   0   11  12  2.121E-3
gcm     0   6   10  99  597.7E-12
iee     10  4   dc  56.26E-6
hlim    90  0   vlim 1K
q1      11  2   13 qx
q2      12  1   14 qz
r2      6   9   100.0E3
rc1     3   11  471.5
rc2     3   12  471.5
re1     13  10  A448
re2     14  10  A448
ree     10  99  3.555E6
ro1     8   5   25
ro2     7   99  25
rp      3   4   8.013E3
vb      9   0   dc  0
vc      3   53  dc  2.400
ve      54  4   dc  2.100
vlim    7   8   dc  0
vlp     91  0   dc  40
vln     0   92  dc  40
.model  dxD(Is=800.0E-18)
.model  qxNPN(Is=800.0E-18
Bf=7.031E3)
.ends
```

Figure 59. TLE2037 Macromodel Subcircuit



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2037AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2037AQ1	Samples
TLE2037AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2037AQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLE2037A-Q1 :

- Catalog: [TLE2037A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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