THE DATASHEET OF

IR3637ASPBF

IR3637ASPbF

1% ACCURATE SYNCHRONOUS PWM CONTROLLER

FEATURES

- 0.8V Reference Voltage
- Operates with a single 5V Supply
- Internal 600KHz Oscillator
- Soft-Start Function
- Fixed Frequency Voltage Mode
- Short Circuit Protection

APPLICATIONS

- Computer Peripheral Voltage Regulator
- Memory Power supplies
- Graphics Card
- Low cost on-board DC to DC

DESCRIPTION

The IR3637A controller IC is designed to provide a simple synchronous Buck regulator for on-board DC to DC applications in a small 8-pin SOIC. The output voltage can be precisely regulated using the internal 0.8V reference voltage for low voltage applications.

The IR3637A operates at a fixed internal 600KHz switching frequency to reduce the component size.

The device features under-voltage lockout for both input supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

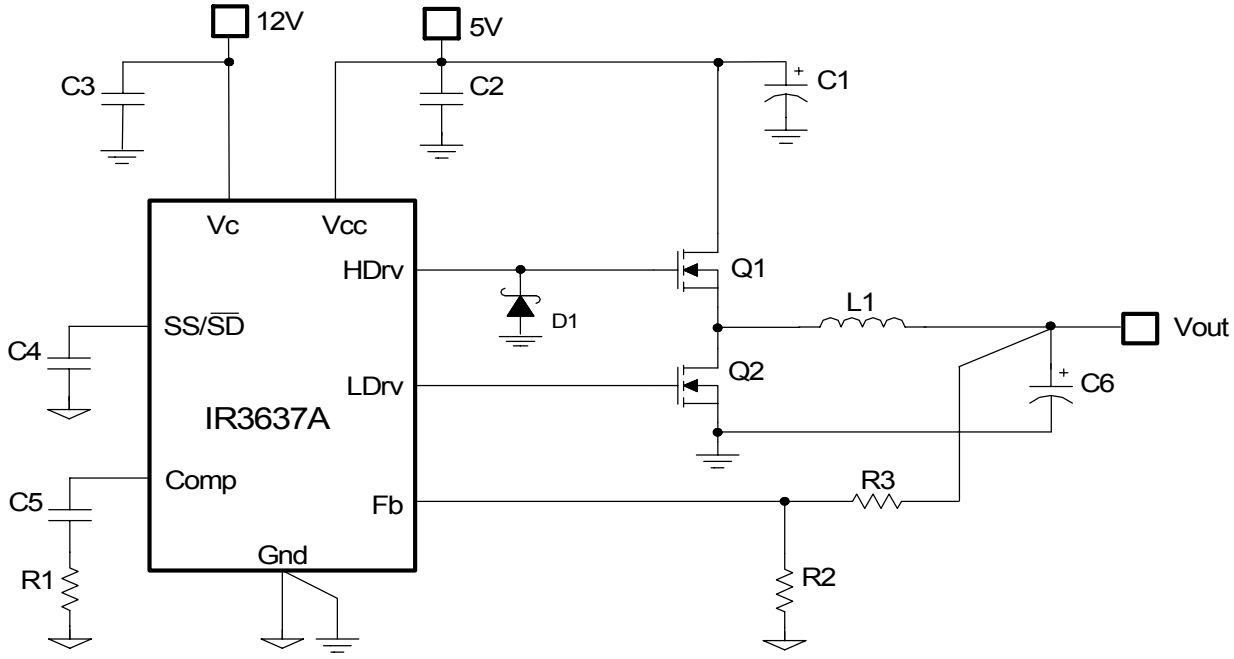


Figure 1 - Typical application of IR3637A.

ORDERING INFORMATION

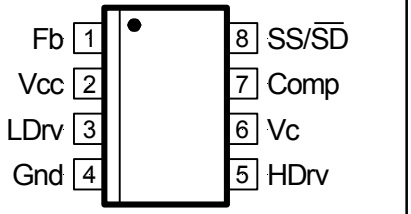
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Oriantation
S	IR3637ASPbF	8	95	------	Fig A
S	IR3637ASTRPbF	8	-------	2500	

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 16V
Vc Supply Voltage 25V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C
ESD Classification ..... HBM Class 2 (2KV) JEDEC Standard
Moisture Sensitivity Level ..... JEDEC Level 1 @ 260°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

PACKAGE INFORMATION



θ_{JA}=154°C/W
θ_{JC}=41.2°C/W

Recommended Operating Conditions

Parameter	Min	Max	Units
Vcc	4.5	5.5	V
Vc	8	14	V

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and 0°C<Tj<125°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
Fb Voltage	V_{FB}	25°C<Tj<75°C	0.792	0.800	0.808	V
		0°C<Tj<125°C	0.789	0.800	0.811	V
Fb Voltage Line Regulation	L_{REG}	4.5<Vcc<5.5			0.1	%
UVLO						
UVLO Threshold - Vcc	UVLO Vcc	Supply Ramping Up	4.0	4.2	4.4	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO Vc	Supply Ramping Up	3.1	3.3	3.5	V
UVLO Hysteresis - Vc				0.2		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.3	0.4	0.5	V
Supply Current						
Vcc Dynamic Supply Current	Dyn Icc	Freq=600KHz, C_L=1500pF	4	7	16	mA
Vc Dynamic Supply Current	Dyn Ic	Freq=600KHz, C_L=1500pF	6	15	20	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V	1	3.3	6	mA
Vc Static Supply Current	I_{CQ}	SS=0V	0.5	1	4.7	mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	-15	-25	-35	µA
Shutdown Threshold	SD				0.4	V

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V, Fb=0.6V		-0.1		μA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V, Fb=0.6V		-64		μA
Transconductance	gm		450	600	800	μmho
Oscillator						
Frequency	Freq		540	600	660	KHz
Ramp-Amplitude Voltage	V_{RAMP}			1.25		V
Output Drivers						
Rise Time, Hdrv, Ldrv	Tr	C_L=1500pF, Vcc=12V,2V to 9V		30	60	ns
Fall Time,Hdrv, Ldrv	Tf	C_L=1500pF, Vcc=12V, 9V to 2V		30	60	ns
Dead Band Time	T_{DB}	Vcc=12V, 2V to 2V	40	150	200	ns
Max Duty Cycle	T_{ON}	Fb=0.6V, Freq=600KHz	76			%
Min Duty Cycle	T_{OFF}	Fb=1V	0	0		%

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	Vcc	This pin provides biasing for the internal blocks of the IC as well as powers the low side driver. A minimum of 0.1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
3	LDrv	Output driver for the synchronous power MOSFET.
4	Gnd	IC's ground pin, this pin must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from Vcc and Vc pins to this pin for noise free operation.
5	HDrv	Output driver for the high side power MOSFET. The negative voltage at this pin may cause instability for the gate drive circuit. To prevent this, a low forward voltage drop diode (e.g. BAT54 or 1N4148) is required between this pin and ground.
6	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 0.1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
7	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
8	SS / $\overline{SD}$	This pin provides user programmable soft-start function. Connect an extrnal capacitor from this pin to ground to set the start up time of the output. The converter can be shut-down by pulling this pin below 0.4V. During shutdown both drivers turn off.

BLOCK DIAGRAM

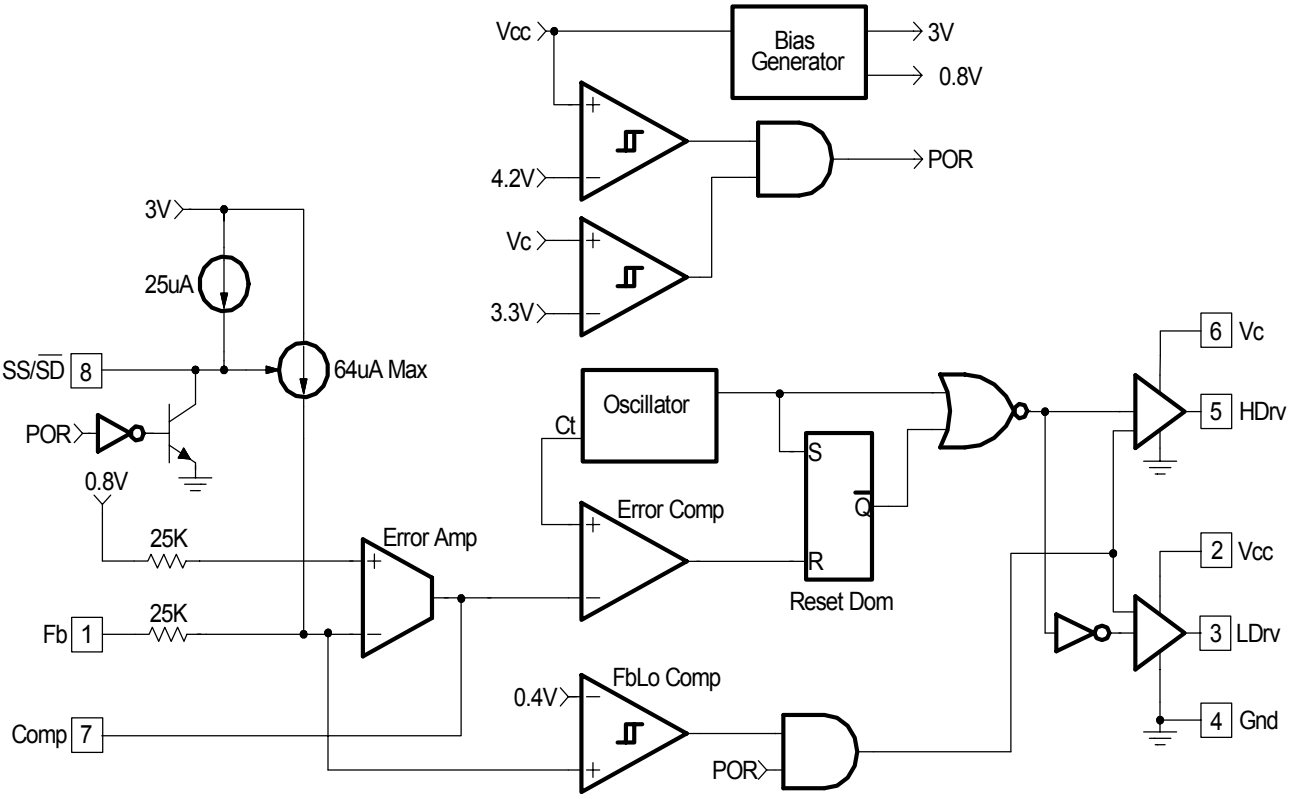


Figure 2 - Simplified block diagram of the IR3637A.

THEORY OF OPERATION

Introduction

The IR3637A is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an error amplifier, an internal oscillator, a PWM comparator, 0.5A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the reference voltage.

This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor to set the oscillation frequency to 600 KHz.

Short-Circuit Protection

The output is protected against the short-circuit. The IR3637A protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The IR3637A shuts down the PWM signals, when the output voltage drops below 0.4V.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc or Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.4V. This can be easily done by using an external small signal transistor. During shutdown both drivers turn off.

THEORY OF OPERATION

Soft-Start

The IR3637A has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter and disables the short circuit protection. During the power up, the output starts at zero and voltage at Fb is below 0.4V. The feedback UVLO is disabled during this time by injecting a current (64μA) into the Fb. This generates a voltage about 1.6V (64μA × 25K) across the negative input of E/A and positive input of the feedback UVLO comparator (see Figure 3).
The magnitude of this current is inversely proportional to the voltage at soft-start pin.

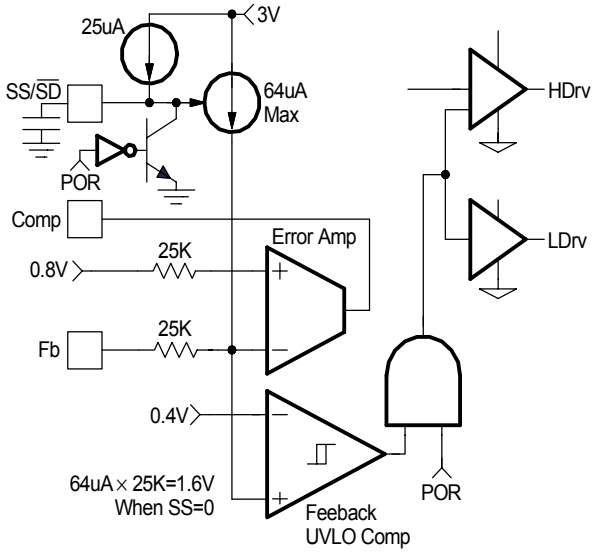


Figure 3 - Soft-start circuit for IR3637A.

The 20μA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at the positive pin of feedback UVLO comparator and the voltage negative input of E/A.

When the soft-start capacitor is around 1V, the current flowing into the Fb pin is approximately 32μA. The voltage at the positive input of the E/A is approximately:

$$32\mu A \times 25K = 0.8V$$

The E/A will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing. Because the voltage at pin of E/A is regulated to reference voltage 0.8V, the voltage at the Fb is:

$$V_{FB} = 0.8\text{-}25K \times (\text{Injected Current})$$

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 2V and the output voltage goes into steady state.

As shown in Figure 4, the positive pin of feedback UVLO comparator is always higher than 0.4V, therefore, feedback UVLO is not functional during soft-start.

The output start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$25\mu A \times T_{START}/C_{SS} = 2V\text{-}1V$$

For a given start up time, the soft-start capacitor can be estimated as:

$$C_{SS} \cong 25\mu A \times T_{START}/1V$$

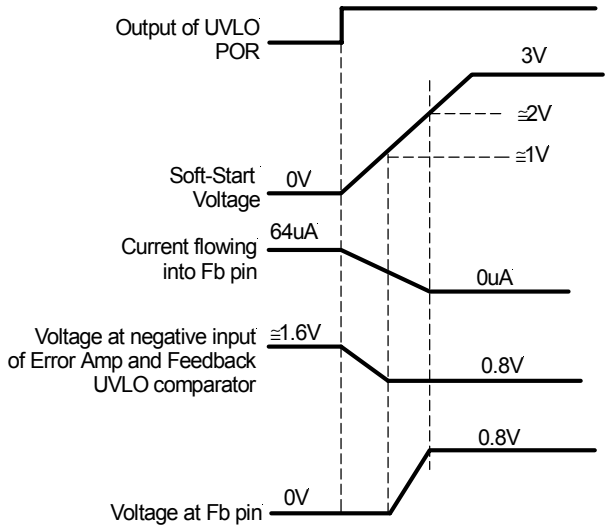


Figure 4 - Theoretical operational waveforms during soft-start.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IR3637A. Appliaction circuit is shown in page 12.

V_{IN} = Vcc = 5V
Vc=12V
V_{OUT} = 1.8V
I_{OUT} = 6A
ΔV_{OUT} = 50mV
F_S = 600KHz

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.8V. The divider is ratioed to provide 0.8V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 5.

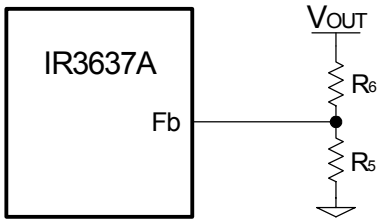


Figure 5 - Typical application of the IR3637A for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Choose R_5 = 1KΩ
This will result to R_6 = 1.25KΩ

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$Css \cong 25 \times t_{START} \ (\mu F) \qquad ---(2)$$

Where t_{START} is the desired start-up time (ms)

For a start-up time of 4ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Boost Supply for Single 5V appliaction
To drive the high side switch, it is necessary to supply a gate voltage at least 4V grater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 6. This method is simple and inexpensive. The operation of the circuit is as follows: when the lower MOSFET is turned on, the capacitor (C1) is pulled down to ground and charges, up to V_{BUS} value, through the diode (D1). The bus voltage will be added to this voltage when upper MOSFET turns on in next cycle, and providing supply voltage (Vc) through diode (D2). Vc is approximately:

$$Vc \cong 2V_{BUS} - (V_{D1} + V_{D2})$$

Capacitors in the range of 0.1μF and 1μF are generally adequate for most applications. The diode must be a fast recovery device to minimize the amount of charge fed back from the charge pump capacitor into V_{BUS}. The diodes need to be able to block the full power rail voltage, which is seen when the high side MOSFET is switched on. For low voltage application, schottky diodes can be used to minimize forward drop across the diodes at start up.

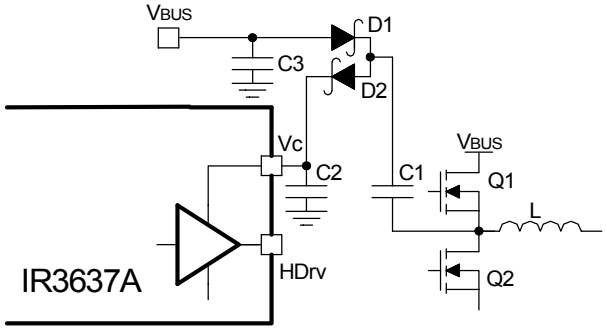


Figure 6 - Charge pump circuit.

Input Capacitor Selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$I_{RMS} = I_{OUT} \sqrt{D \times (1-D)}$ ---(3)

Where:
D is the Duty Cycle, $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For I_{OUT}=6A and D=0.36, the I_{RMS}=2.8A

For higher efficiency, low ESR capacitor is recommended. Two capacitors of Sanyo's TPB series PosCap with 150µF, 6.3V, 40mΩ ESR and 1.4A ripple current will meet the ripple current requirement.

Inductor Selection
The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \quad ---(5)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If Δi = 32%(I_O), then the output inductor will be:
L = 1.0µH
The Coilcraft DO3316P series provides a range of inductors in different values, low profile suitable for large currents, 1.0µH, 9A(Isat) is a good choice for this application.

Output Capacitor Selection
The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements.

The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \quad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Inductor Ripple Current
ΔV_O=50mV and ΔI_O=1.92A
Results to ESR=26.8mΩ

The Sanyo TPB series, PosCap capacitor is a good choice. The 6TPB150M 150µF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of ≅ 20mΩ which achieves our low ESR goal.

Power MOSFET Selection
The IR3637A uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

P_{COND} (Upper Switch) = $I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$

P_{COND} (Lower Switch) = $I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF8910 is a good choice. The device provides two N-MOSFETs in a compact SOIC 8-Pin package.

The IRF8910 has the following data:

V_{DSS} = 20V
I_D = 10A
$R_{DS(ON)}$ =18.3Ω @ V_{GS}=4.5V (Lower FET)
$R_{DS(ON)}$ =13.4Ω @ V_{GS}=10V (Upper FET)

The total conduction losses will be:

$P_{CON(TOTAL)}=P_{CON}$(Upper Switch)+P_{CON}(Lower Switch)

ϑ = 1.4 according to the IRF8910 data sheet for 150°C junction temperature

$P_{CON(TOTAL)}$ =0.83W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(6)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

The switching time waveform is shown in figure 7.

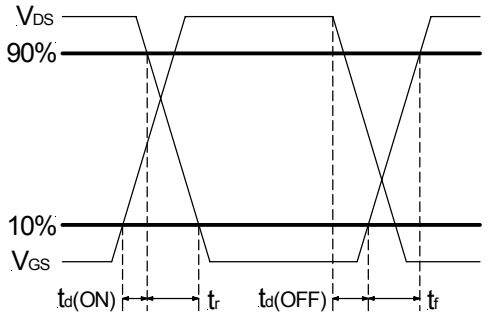


Figure 7 - Switching time waveforms.

From IRF8910 data sheet: t_r = 10ns
t_f = 4.1ns

These values are taken under a certain condition test. For more detail please refer to the IRF8915 data sheet.

By using equation (6), we can calculate the switching losses.

P_{SW} = 0.127mW

Feedback Compensation

The IR3637A is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 8). The Resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad ---(7)$$

Figure 8 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

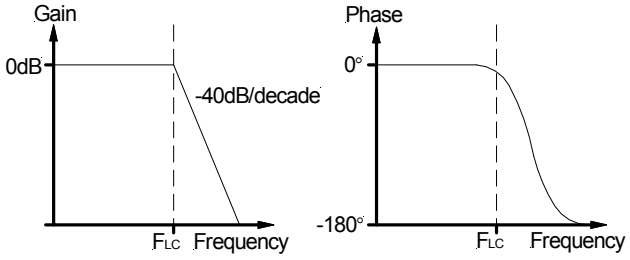


Figure 8 - Gain and phase of LC filter.

The IIR3637A's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 9.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \quad ---(8)$$

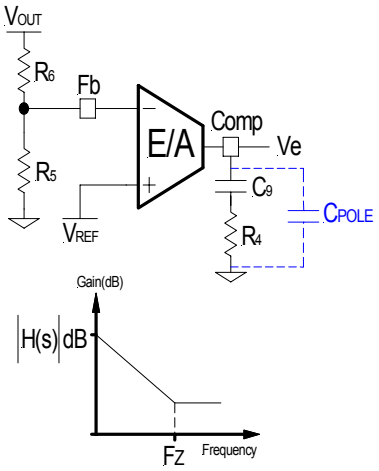


Figure 9 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \quad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \quad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \quad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$$Fo > F_{ESR} \text{ and } F_O \leq (1/5 \sim 1/10) \times f_S$$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \quad ---(12)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:
V_{IN} = 5.5V
V_{OSC} = 1.25V
Fo = 60KHz
F_{ESR} = 26.5KHz
F_{LC} = 9.20KHz
R_5 = 1K
R_6 = 1.25K
g_m = 600μmho

This results to R_4=16.06KΩ. Choose R_4=16KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z \cong 75\% F_{LC}$$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \quad ---(13)$$

For:
Lo = 1.0μH
Co = 300μF
F_Z = 6.9KHz
R_4 = 16KΩ

Using equations (11) and (13) to calculate C_9, we get:

C_9 = 1.44nF
Choose C_9 = 1.5nF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 10.

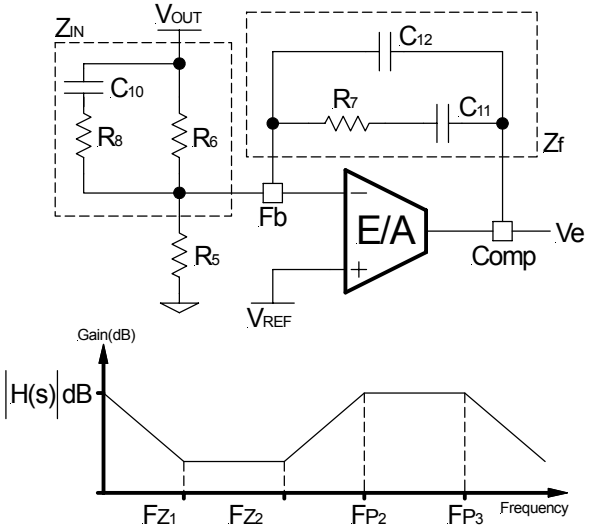


Figure 10 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(14)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (14) regarding transconductance error amplifier.

1) Select the crossover frequency:
$F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.
$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times Fo \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at the ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C_{10} \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C_{10} \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5.

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Based on the frequency of the zero generated by ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation type and location of crossover frequency.

Compensator Type	Location of Zero Crossover Frequency (F_O)	Typical Output Capacitor
Type II (PI)	$F_{LC} < F_{ESR} < F_O < f_S/2$	Electrolytic, Tantalum
Type III (PID) Method A	$F_{LC} < F_O < F_{ESR} < f_S/2$	Tantalum, Ceramic
Type III (PID) Method B	$F_{LC} < F_O < f_S/2 < F_{ESR}$	Ceramic

Table - The compensation type and location of zero crossover frequency.

Detail information is dicussed in application Note AN-1043 which can be downloaded from the IR Web-Site.

All design should be tested for stability to verify the calculated values.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

Two Supplies Application: Vc=12V, Vin=Vcc=5V to 1.8V @ 6A

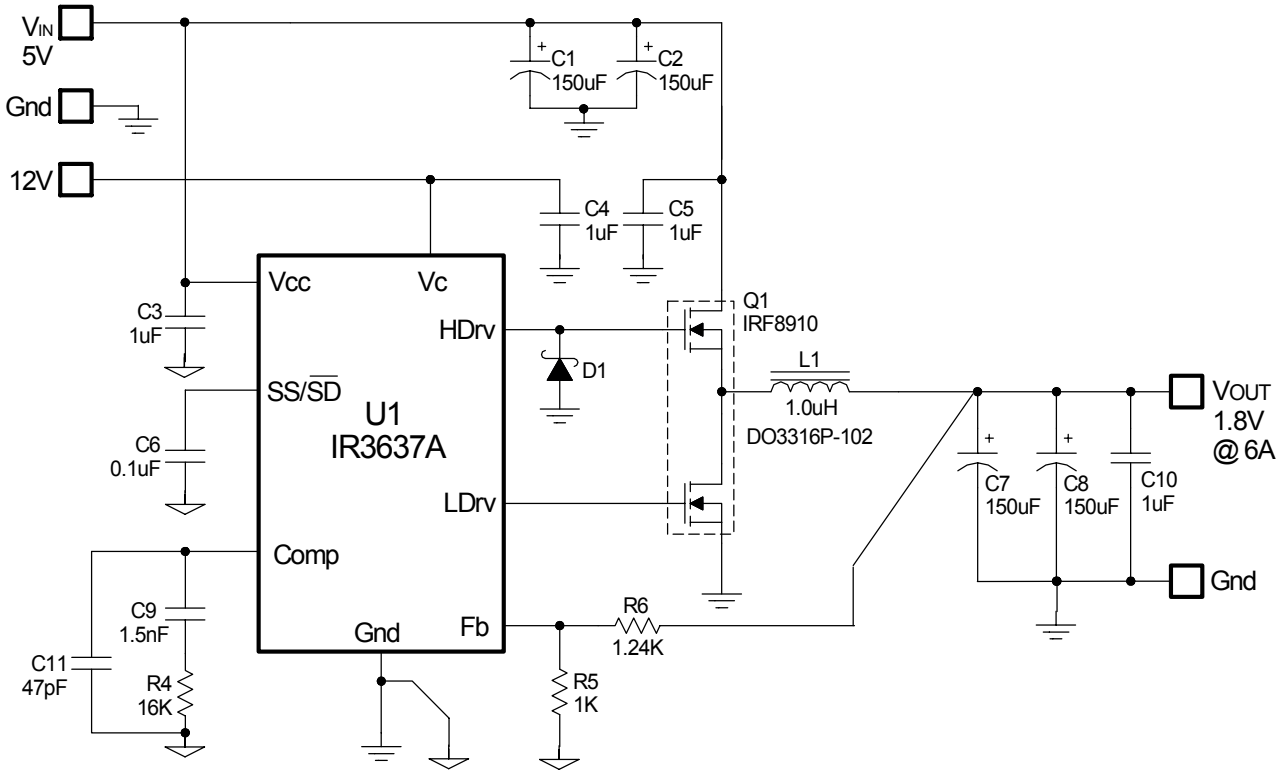


Figure 11 - Typical Application for IR3637A.

TYPICAL APPLICATION

Single 5V Application

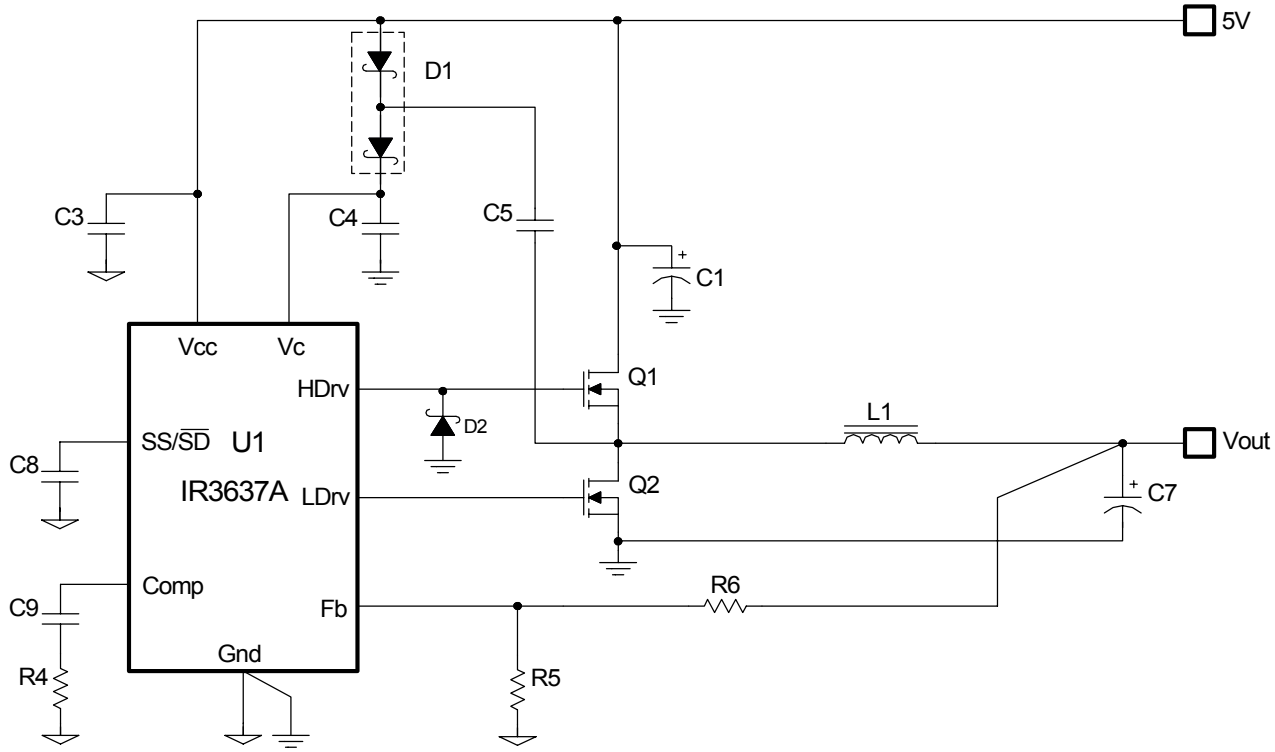


Figure 12 - Typical application for single 5V

TYPICAL APPLICATION

Two Supplies Application, Vcc=Vc=12V, Vin=5V

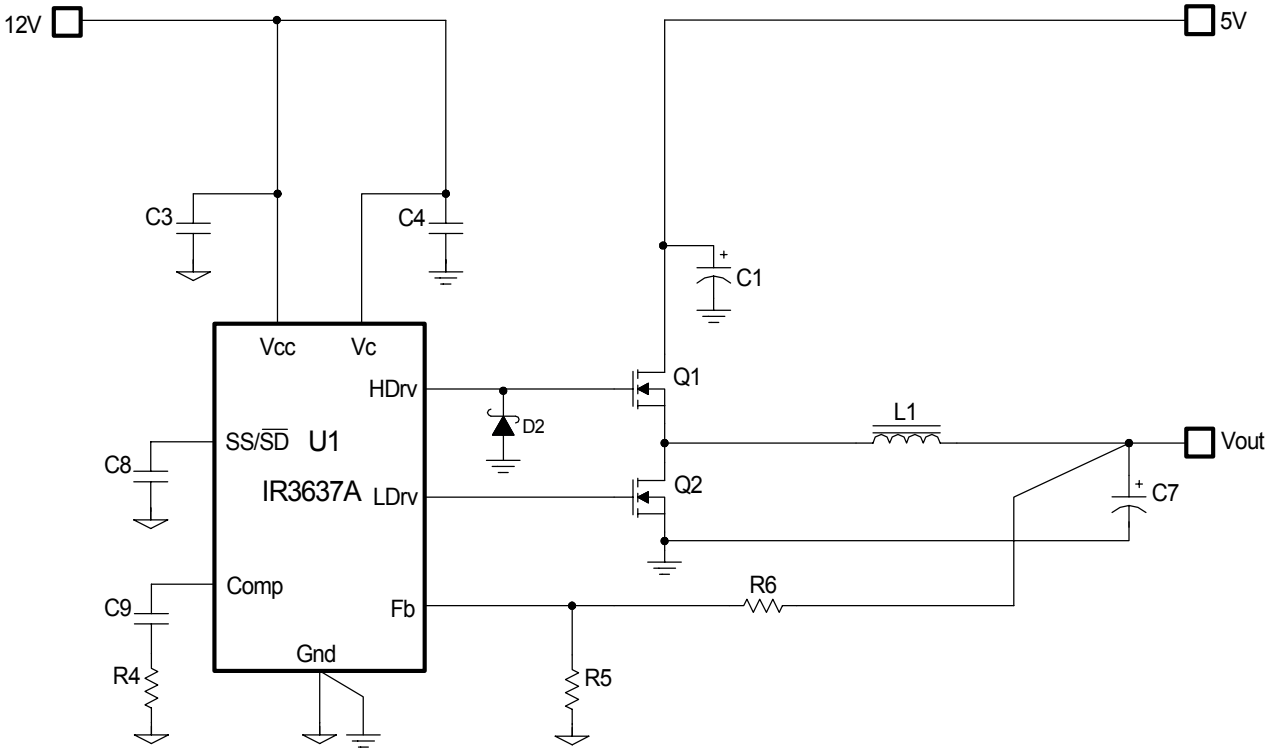
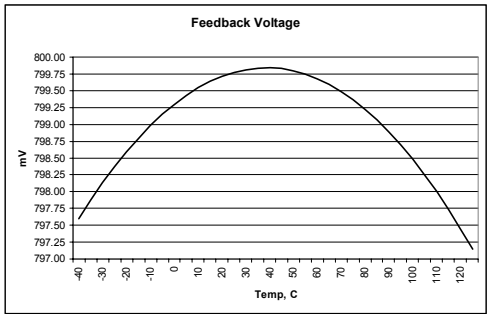
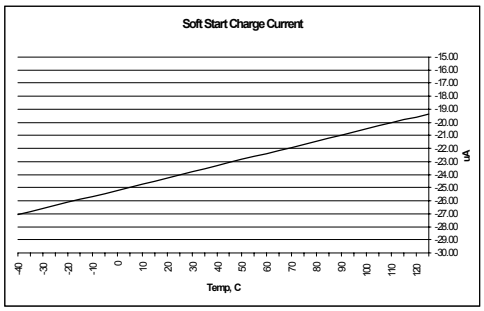


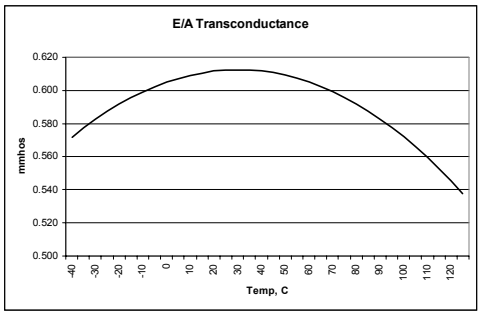
Figure 13 - Typical application using 12V for biasing both Vcc and Vc and 5V for Bus Voltage

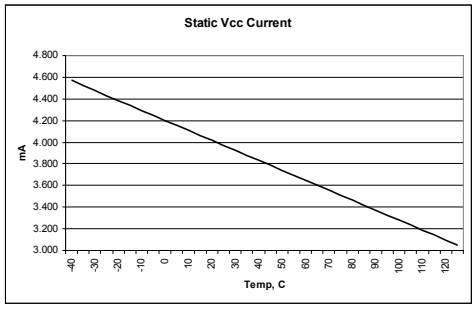
For proper start up the 5V rail needs to start before 12V

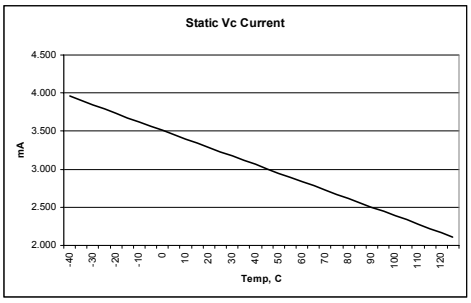
TYPICAL OPERATING CHARACTERISTICS

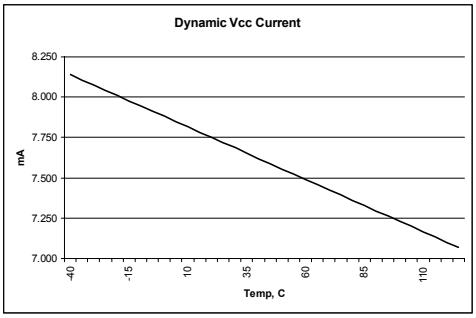












TYPICAL PERFORMANCE CURVES

Test Conditions:
Vcc=Vin=5V, Vc=12V, Vout=1.8V, Iout=0-7A, Ta=Room Temp, No Air Flow. Unless otherwise specified.

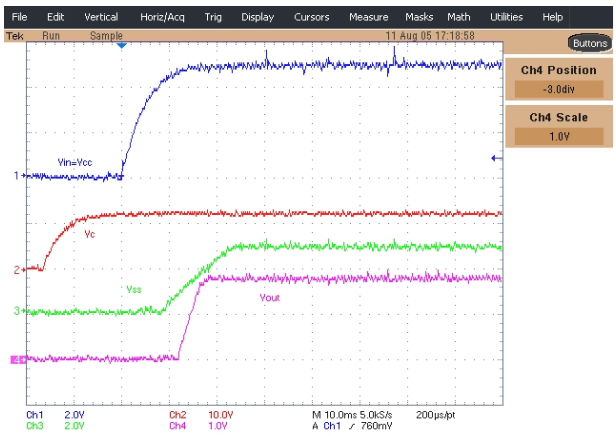


Figure 14 - Start up waveforms
Ch1: Vin=Vcc, Ch2:Vc, Ch3:Vss, Ch4: Vout

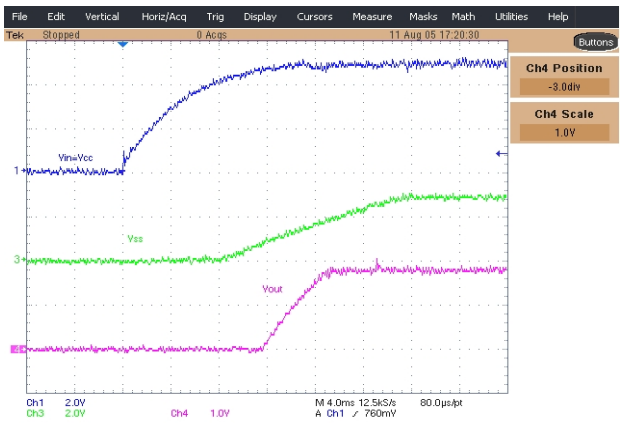


Figure 15 - Start up waveforms
Ch1:Vin=Vcc, Ch3:Vss, Ch4:Vout

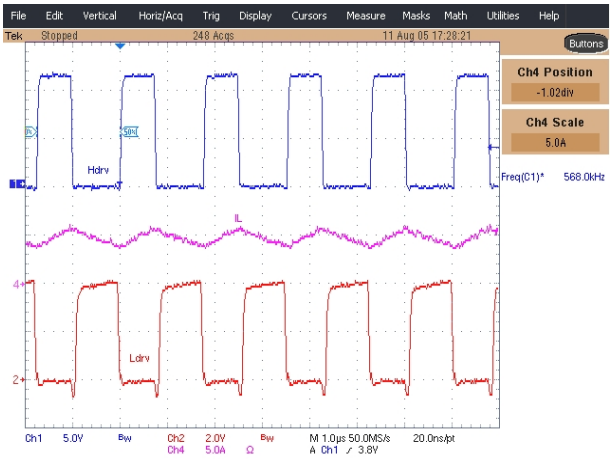


Figure 16 - Gates waveforms
Ch1:Hdrv, Ch2:Ldrv, Ch4:Inductor Current
ILoad=5A

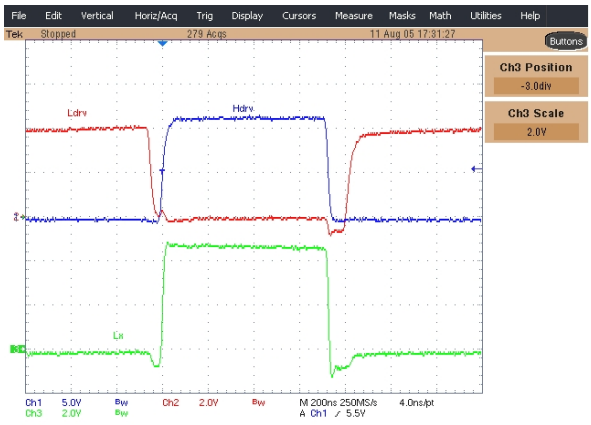


Figure 17 - Gates waveforms
Ch1:Hdrv, Ch2:Ldrv, Ch3:Inductor Point
ILoad=5A

TYPICAL OPERATING WAVEFORMS

Test Conditions:
Vcc=Vin=5V, Vc=12V, Vout=1.8V, Iout=0-7A, Ta=Room Temp, No Air Flow. Unless otherwise specified.

Figure 18 - Shutdown by shorting the SS pin
Ch1:Hdrv, Ch2:Ldrv, Ch3:SS
ILoad=5A

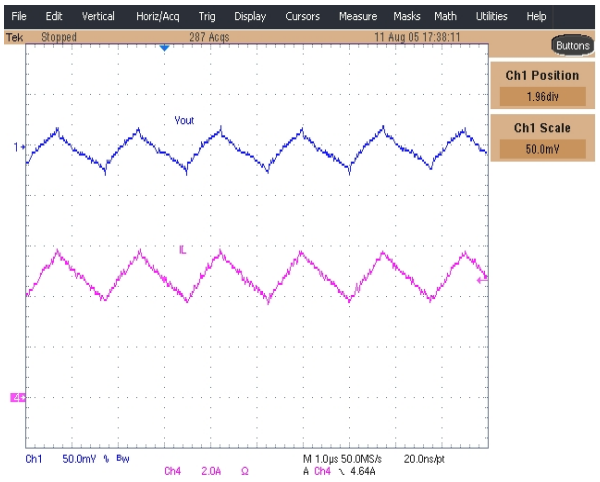


Figure 19 - Output Voltage Ripple
Ch1:Vout, Ch4:Inductor Current
ILoad=5A

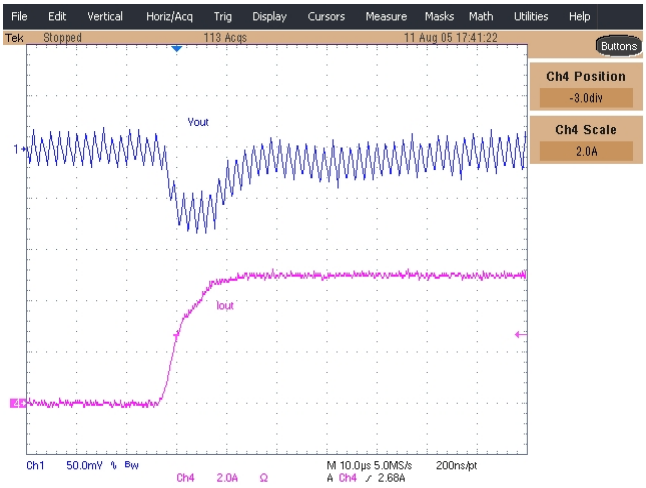


Figure 20 - Load Transient (0-5A)
Ch1:Vout, Ch4:Step Load Current

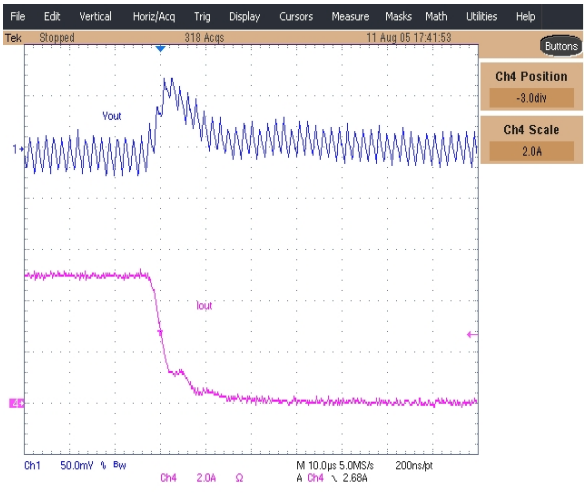
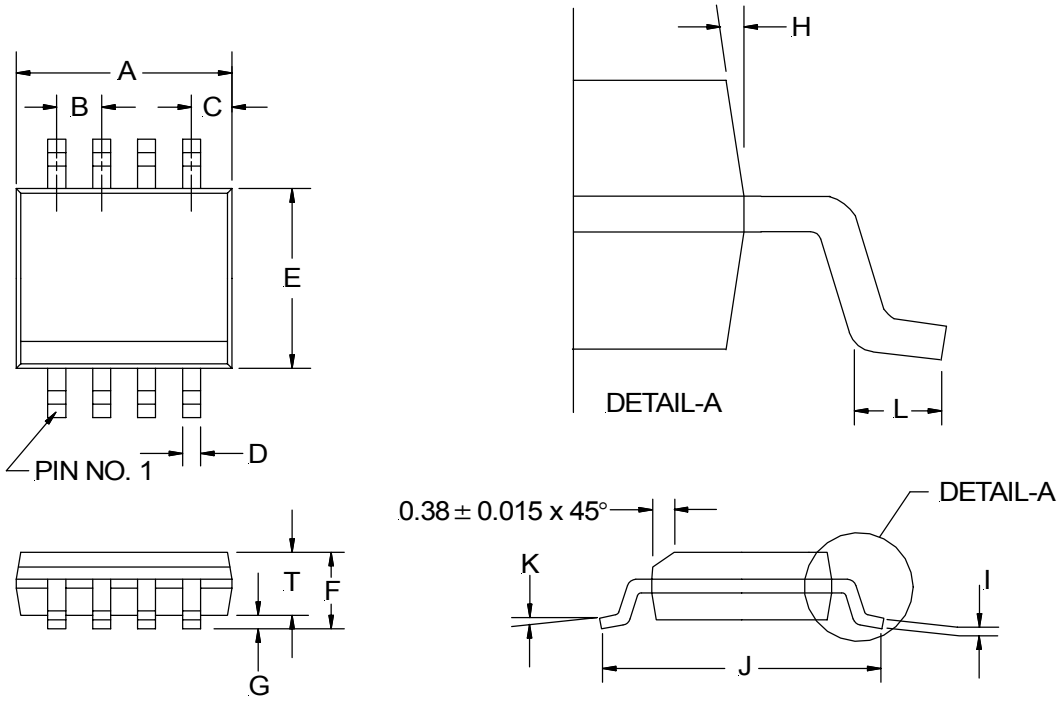


Figure 21 - Load Transient (5-0A)
Ch1:Vout, Ch4:Step Load Current

(S) SOIC Package
8-Pin Surface Mount, Narrow Body

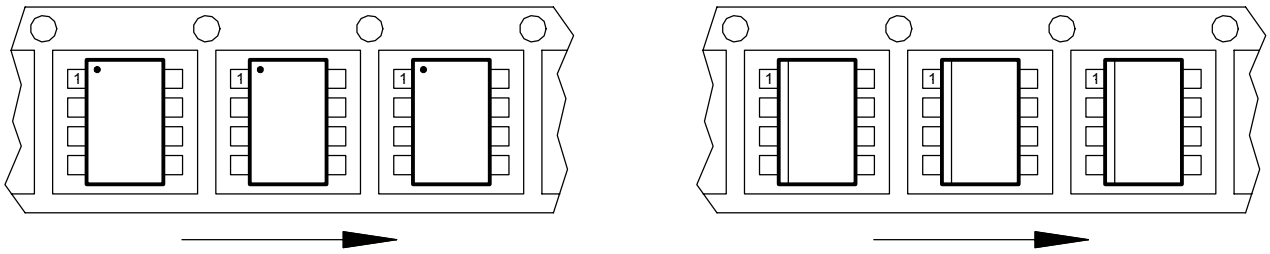


8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
S	SOIC, Narrow Body	8	95	2500	Fig A



Feed Direction
Figure A

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