



# THE DATASHEET OF AOWF7S65



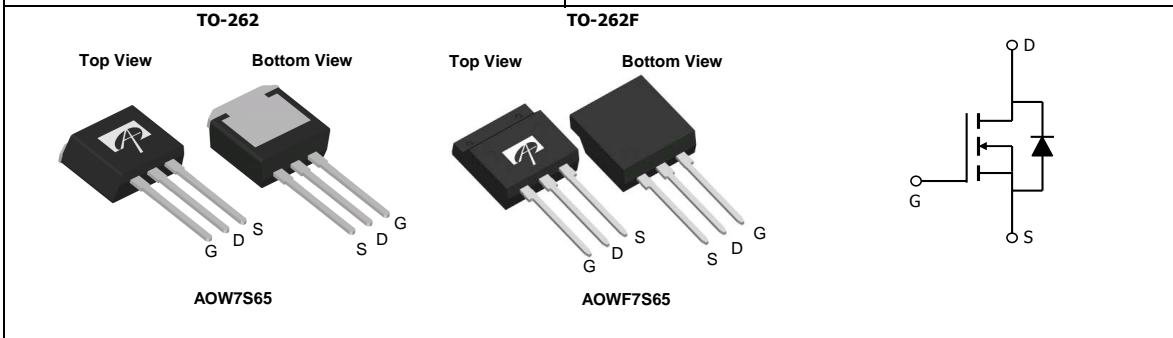
**General Description**

The AOW7S65 & AOWF7S65 have been fabricated using the advanced  $\alpha$ MOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications. By providing low  $R_{DS(on)}$ ,  $Q_g$  and  $E_{OSS}$  along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

**Product Summary**

$V_{DS} @ T_{j,max}$	750V
$I_{DM}$	30A
$R_{DS(ON),max}$	0.65 $\Omega$
$Q_{g,typ}$	9.2nC
$E_{oss} @ 400V$	2 $\mu$ J

100% UIS Tested  
 100%  $R_g$  Tested


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	AOW7S65	AOWF7S65	Units
Drain-Source Voltage	$V_{DS}$	650		V
Gate-Source Voltage	$V_{GS}$	$\pm 30$		V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	7	7*
		$T_C=100^\circ\text{C}$	5	5*
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30		A
Avalanche Current <sup>C</sup>	$I_{AR}$	1.7		A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	43		mJ
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	86		mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	104	25
		Derate above $25^\circ\text{C}$	0.8	0.2
MOSFET dv/dt ruggedness	dv/dt		100	V/ns
Peak diode recovery dv/dt <sup>H</sup>			20	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds <sup>J</sup>	$T_L$	300		$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	AOW7S65	AOWF7S65	Units
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	65	65	$^\circ\text{C}/\text{W}$
Maximum Case-to-sink <sup>A</sup>	$R_{\theta CS}$	0.5	--	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	5	$^\circ\text{C}/\text{W}$

\* Drain current limited by maximum junction temperature.

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	650	-	-	V
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	700	750	-	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =520V, T <sub>J</sub> =150°C	-	10	-	
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	2.6	3.3	4	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A, T <sub>J</sub> =25°C	-	0.54	0.65	Ω
		V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A, T <sub>J</sub> =150°C	-	1.48	1.64	Ω
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =3.5A, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	-	0.82	-	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current		-	-	7	A
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current <sup>C</sup>		-	-	30	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	-	434	-	pF
C <sub>OSS</sub>	Output Capacitance		-	30	-	pF
C <sub>o(er)</sub>	Effective output capacitance, energy related <sup>H</sup>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0 to 480V, f=1MHz	-	23	-	pF
C <sub>o(tr)</sub>	Effective output capacitance, time related <sup>I</sup>		-	80	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	-	1	-	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	-	17.5	-	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =480V, I <sub>D</sub> =3.5A	-	9.2	-	nC
Q <sub>gs</sub>	Gate Source Charge		-	2.5	-	nC
Q <sub>gd</sub>	Gate Drain Charge		-	2.7	-	nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =400V, I <sub>D</sub> =3.5A, R <sub>G</sub> =25Ω	-	21	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	14	-	ns
t <sub>D(off)</sub>	Turn-Off Delay Time		-	55	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	15	-	ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =3.5A, di/dt=100A/μs, V <sub>DS</sub> =400V	-	224	-	ns
I <sub>rm</sub>	Peak Reverse Recovery Current	I <sub>F</sub> =3.5A, di/dt=100A/μs, V <sub>DS</sub> =400V	-	19	-	A
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =3.5A, di/dt=100A/μs, V <sub>DS</sub> =400V	-	2.8	-	μC

A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I<sub>AS</sub>=1.7A, V<sub>DD</sub>=150V, Starting T<sub>J</sub>=25°C

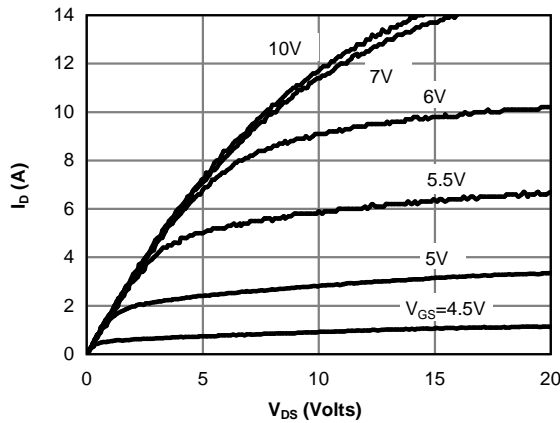
H. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

I. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

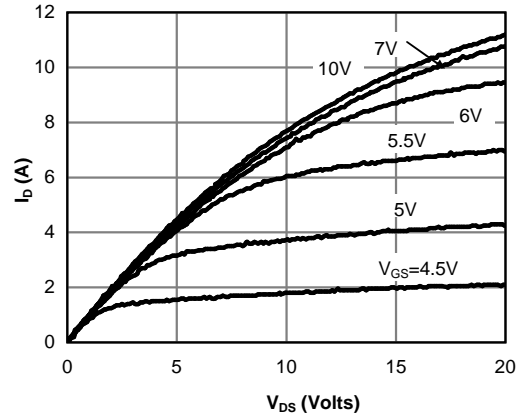
J. Wavesoldering only allowed at leads.

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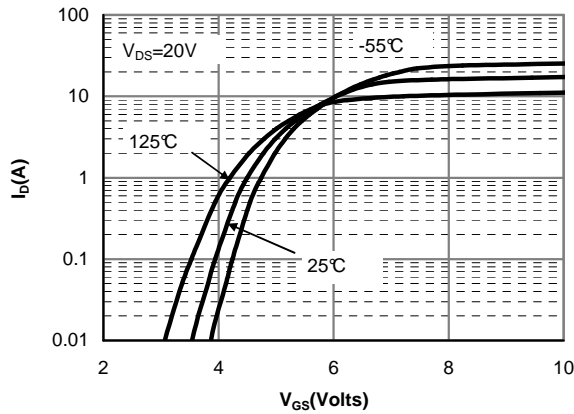
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



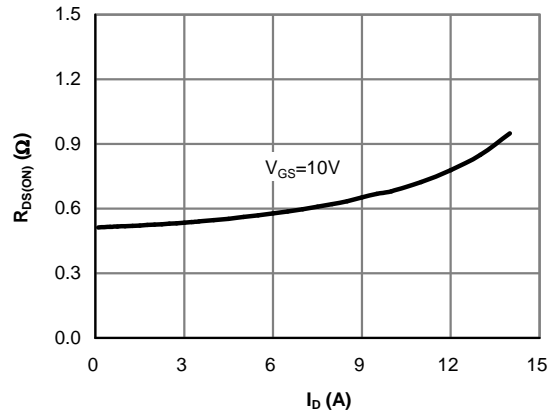
**Figure 1: On-Region Characteristics @ 25°C**



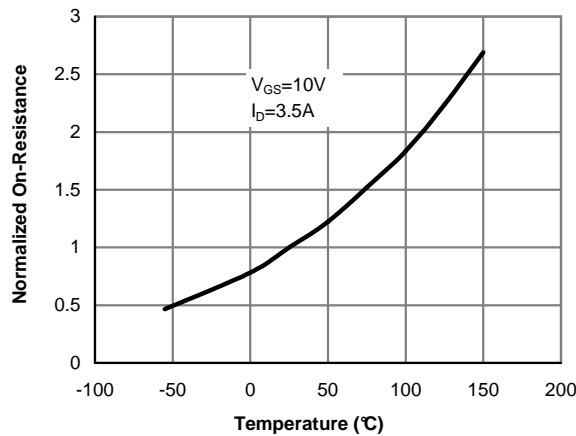
**Figure 2: On-Region Characteristics @ 125°C**



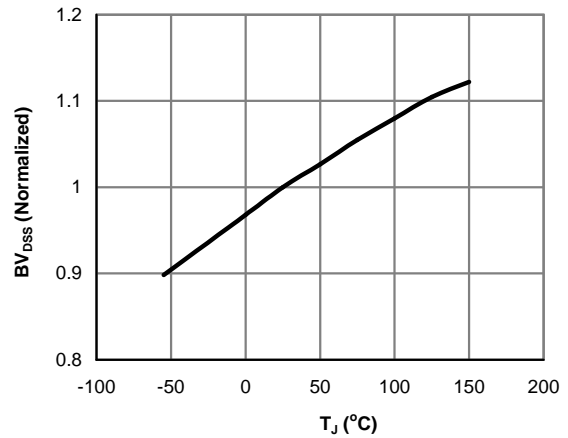
**Figure 3: Transfer Characteristics**



**Figure 4: On-Resistance vs. Drain Current and Gate Voltage**

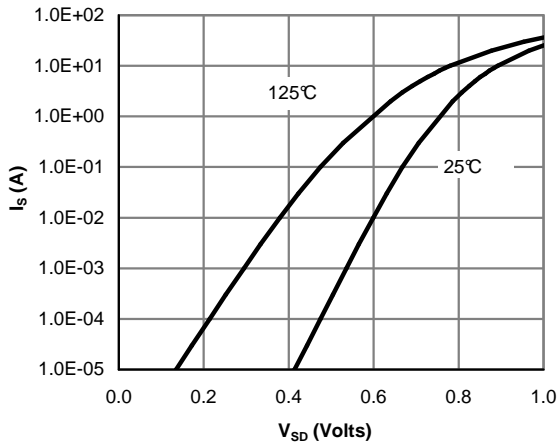


**Figure 5: On-Resistance vs. Junction Temperature**

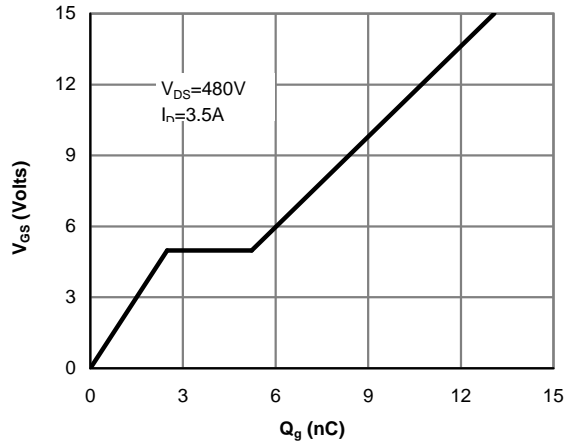


**Figure 6: Break Down vs. Junction Temperature**

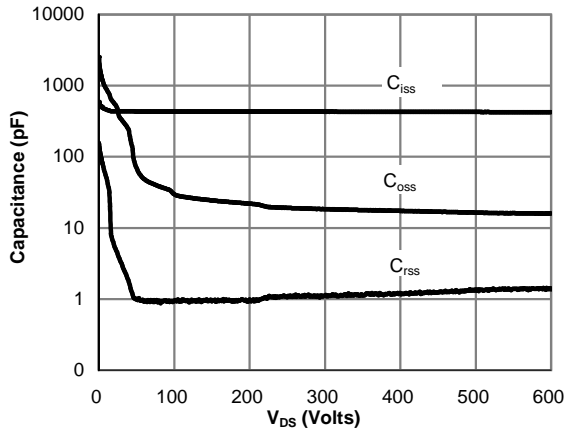
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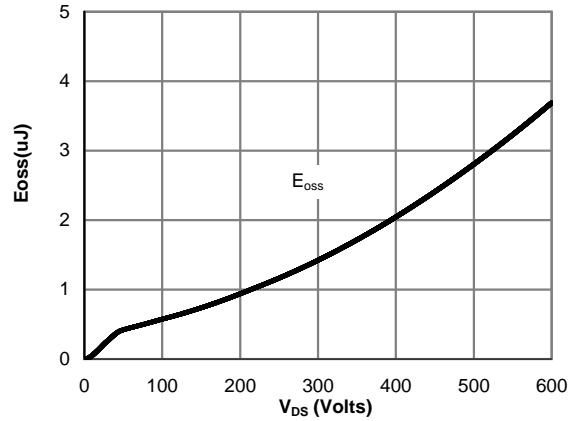
**Figure 7: Body-Diode Characteristics (Note E)**



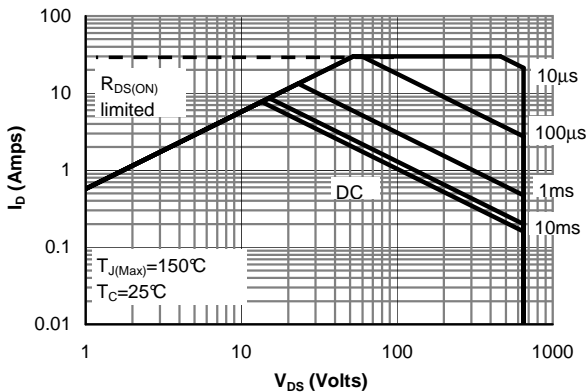
**Figure 8: Gate-Charge Characteristics**



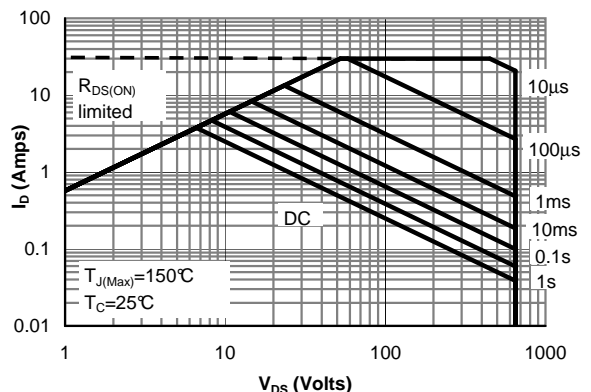
**Figure 9: Capacitance Characteristics**



**Figure 10: Coss stored Energy**

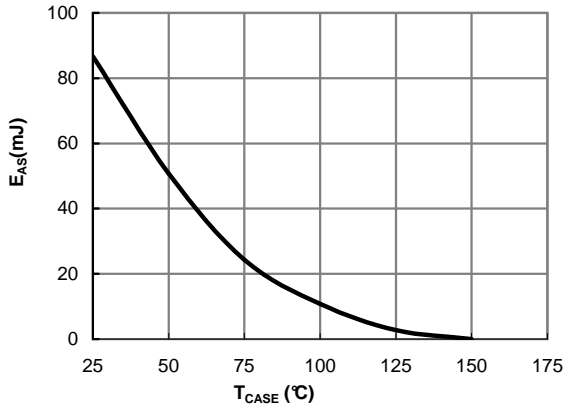


**Figure 11: Maximum Forward Biased Safe Operating Area for AOW7S65 (Note F)**

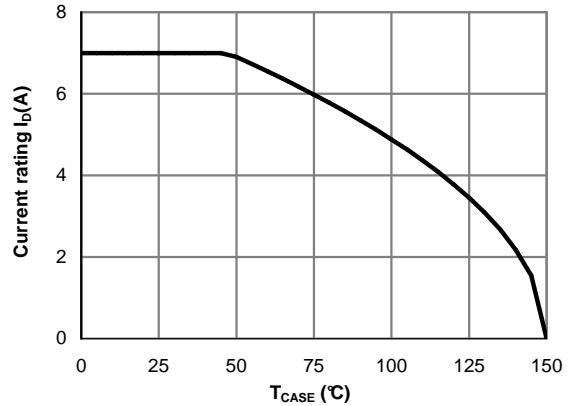


**Figure 12: Maximum Forward Biased Safe Operating Area for AOWF7S65 (Note F)**

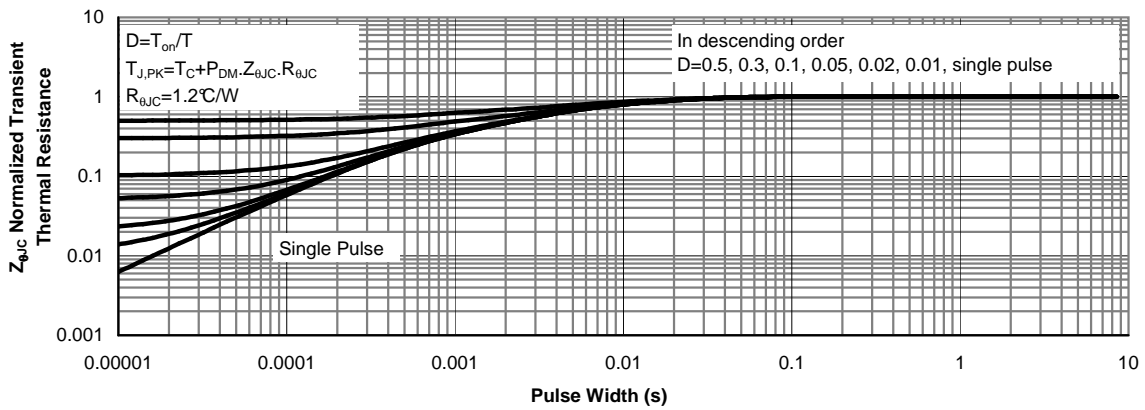
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



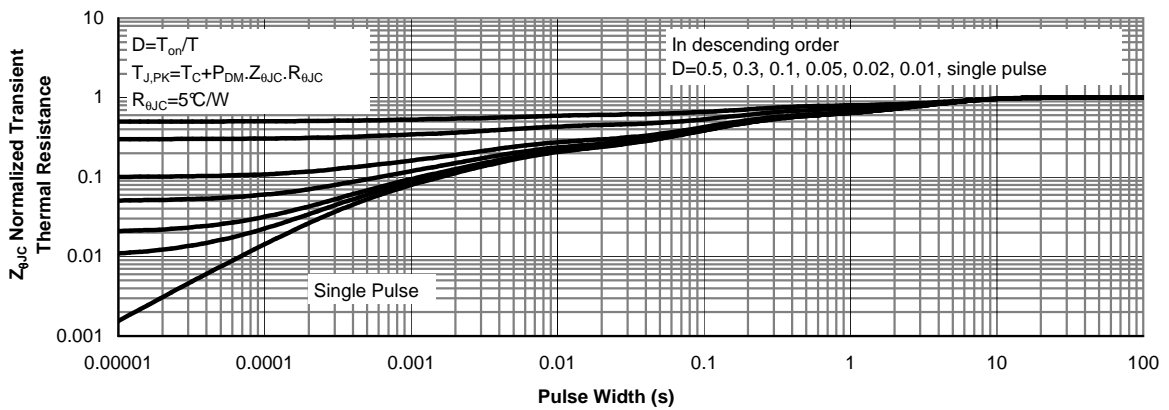
**Figure 13: Avalanche energy**



**Figure 14: Current De-rating (Note B)**

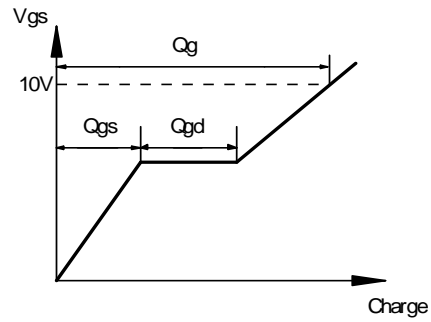
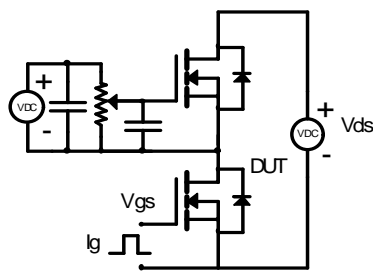


**Figure 15: Normalized Maximum Transient Thermal Impedance for AOW7S65 (Note F)**

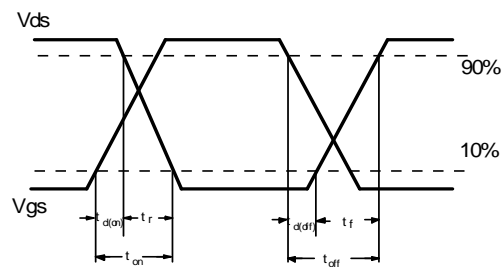
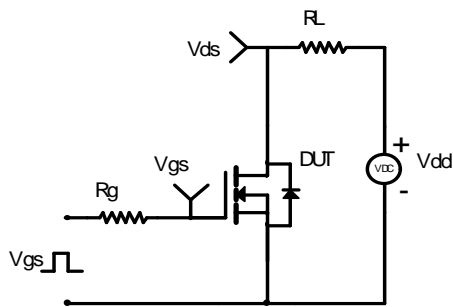


**Figure 16: Normalized Maximum Transient Thermal Impedance for AOWF7S65 (Note F)**

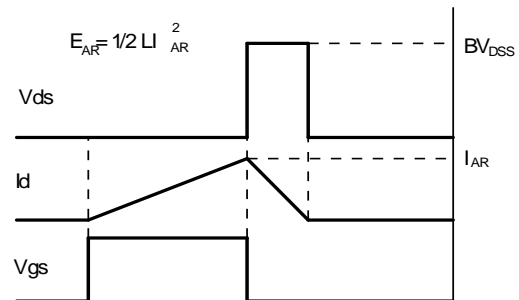
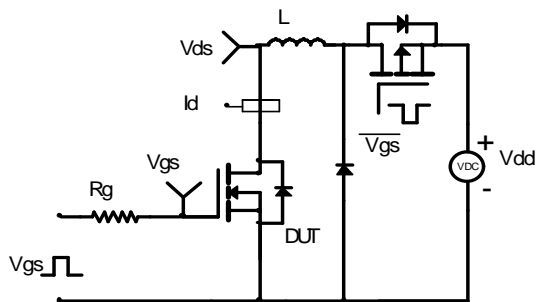
Gate Charge Test Circuit & Waveform



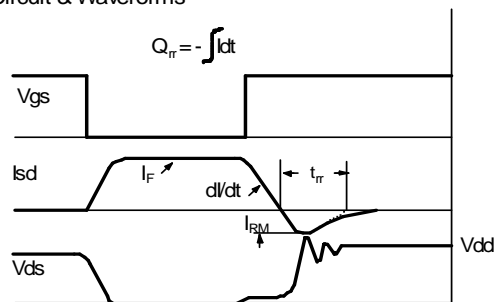
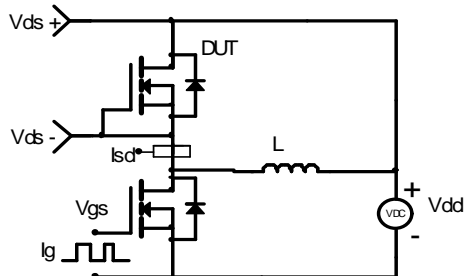
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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