THE DATASHEET OF

AD8531ARZ-REEL

Low Cost, 250 mA Output, Single-Supply Amplifiers

AD8531/AD8532/AD8534

FEATURES

Single-supply operation: 2.7 V to 6 V
High output current: ±250 mA
Low supply current: 750 µA/amplifier
Wide bandwidth: 3 MHz
Slew rate: 5 V/µs
No phase reversal
Low input currents
Unity gain stable
Rail-to-rail input and output

APPLICATIONS

Multimedia audio
LCD drivers
ASIC input or output amplifiers
Headphone drivers

GENERAL DESCRIPTION

The AD8531, AD8532, and AD8534 are single, dual, and quad rail-to-rail input/output single-supply amplifiers featuring 250 mA output drive current. This high output current makes these amplifiers excellent for driving either resistive or capacitive loads. AC performance is very good with 3 MHz bandwidth, 5 V/µs slew rate, and low distortion. All are guaranteed to operate from a 3 V single supply as well as a 5 V supply.

The very low input bias currents enable the AD853x to be used for integrators, diode amplification, and other applications requiring low input bias current. Supply current is only 750 µA per amplifier at 5 V, allowing low current applications to control high current loads.

Applications include audio amplification for computers, sound ports, sound cards, and set-top boxes. The AD853x family is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs.

The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

The AD8531/AD8532/AD8534 are specified over the extended industrial temperature range (−40°C to +85°C). The AD8531 is available in 8-lead SOIC, 5-lead SC70, and 5-lead SOT-23 packages. The AD8532 is available in 8-lead SOIC, 8-lead MSOP, and 8-lead TSSOP surface-mount packages. The AD8534 is available in narrow 14-lead SOIC and 14-lead TSSOP surface-mount packages.

PIN CONFIGURATIONS

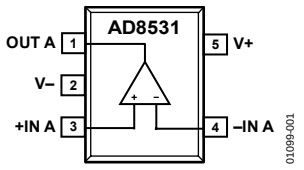


Figure 1. 5-Lead SC70 and 5-Lead SOT-23 (KS and RJ Suffixes)

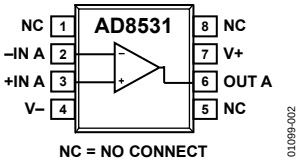


Figure 2. 8-Lead SOIC (R Suffix)

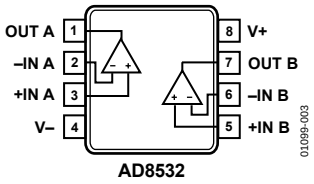


Figure 3. 8-Lead SOIC, 8-Lead TSSOP, and 8-Lead MSOP (R, RU, and RM Suffixes)

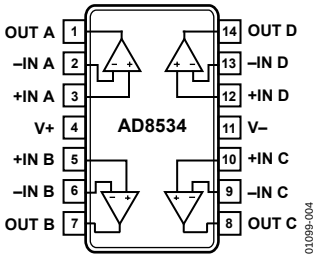


Figure 4. 14-Lead SOIC and 14-Lead TSSOP (R and RU Suffixes)

Rev. F

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©1996–2008 Analog Devices, Inc. All rights reserved.**

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Pin Configurations ... 1
Revision History ... 2
Specifications ... 3
Electrical Characteristics ... 3
Absolute Maximum Ratings ... 5
Thermal Resistance ... 5
ESD Caution ... 5
Typical Performance Characteristics ... 6
Theory of Operation ... 11
Short-Circuit Protection ... 11
Power Dissipation ... 11
Power Calculations for Varying or Unknown Loads ... 12
Calculating Power by Measuring Ambient and Case Temperature ... 12
Calculating Power by Measuring Supply Current ... 12
Input Overvoltage Protection ... 12
Output Phase Reversal ... 13
Capacitive Load Drive ... 13
Applications Information ... 14
High Output Current, Buffered Reference/Regulator ... 14
Single-Supply, Balanced Line Driver ... 14
Single-Supply Headphone Amplifier ... 15
Single-Supply, 2-Way Loudspeaker Crossover Network ... 15
Direct Access Arrangement for Telephone Line Interface ... 16
Outline Dimensions ... 17
Ordering Guide ... 20

REVISION HISTORY

1/08—Rev. E to Rev. F

Changes to Layout ... 5
Changes to Figure 12 and Figure 13 ... 7
Changes to Figure 38 ... 11
Changes to Input Overvoltage Protection Section ... 12
Changes to Figure 43 ... 14
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 20

4/05—Rev. D to Rev. E

Updated Format ... Universal
Changes to Pin Configurations ... 1
Changes to Table 4 ... 5
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 19

10/02—Rev. C to Rev. D

Deleted 8-Lead PDIP (N-8) ... Universal
Deleted 14-Lead PDIP (N-14) ... Universal
Edits to Figure 34 ... 9
Updated Outline Dimensions ... 15

8/96—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				25	mV
		−40°C ≤ T_A ≤ +85°C			30	mV
Input Bias Current	I_B			5	50	pA
		−40°C ≤ T_A ≤ +85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	38	45		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2.5 V		25		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	2.85	2.92		V
		−40°C ≤ T_A ≤ +85°C	2.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA		60	100	mV
		−40°C ≤ T_A ≤ +85°C			125	mV
Output Current	I_{OUT}			±250		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		60		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 6 V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		0.70	1	mA
		−40°C ≤ T_A ≤ +85°C			1.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			2.2		MHz
Phase Margin	ϕo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				25	mV
		−40°C ≤ T_A ≤ +85°C			30	mV
Input Bias Current	I_B			5	50	pA
		−40°C ≤ T_A ≤ +85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	38	47		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	15	80		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	4.9	4.94		V
		−40°C ≤ T_A ≤ +85°C	4.85			V
Output Voltage Low	V_{OL}	I_L = 10 mA		50	100	mV
		−40°C ≤ T_A ≤ +85°C			125	mV
Output Current	I_{OUT}			±250		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 6 V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		0.75	1.25	mA
		−40°C ≤ T_A ≤ +85°C			1.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Full-Power Bandwidth	BW_p	1% distortion		350		kHz
Settling Time	t_S	To 0.01%		1.4		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	ϕo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (V_S)	7 V
Input Voltage	GND to V_S
Differential Input Voltage[1]	±6 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supplies less than 6 V, the differential input voltage is equal to ±V_S.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS)	376	126	°C/W
5-Lead SOT-23 (RJ)	230	146	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

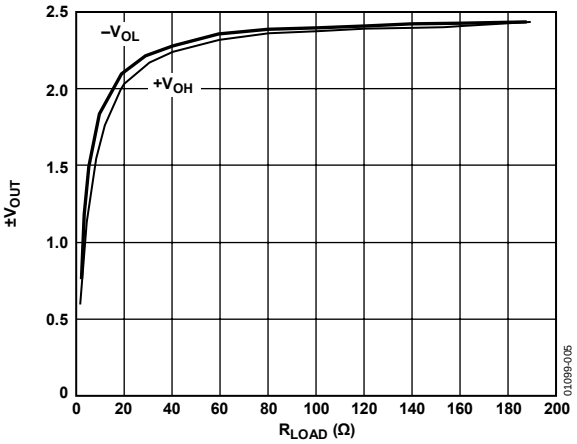


Figure 5. Output Voltage vs. Load, V_S = ±2.5 V, R_{LOAD} Is Connected to GND (0 V)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

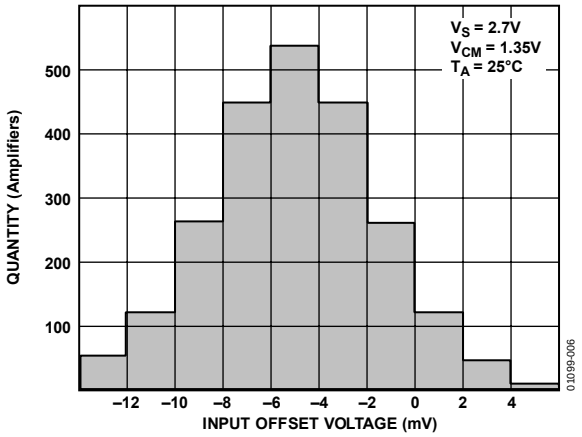


Figure 6. Input Offset Voltage Distribution

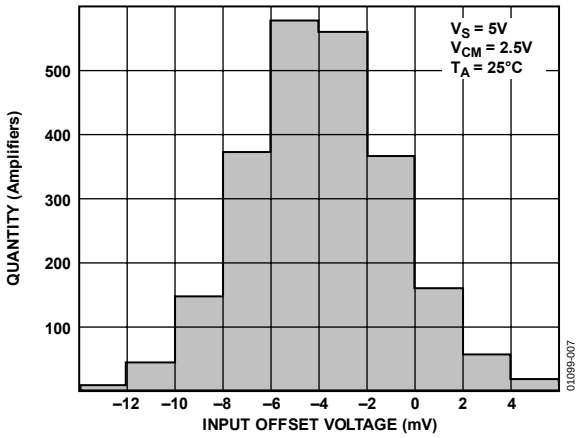


Figure 7. Input Offset Voltage Distribution

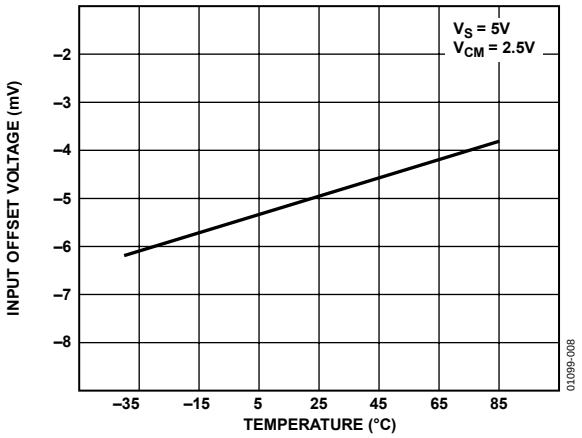


Figure 8. Input Offset Voltage vs. Temperature

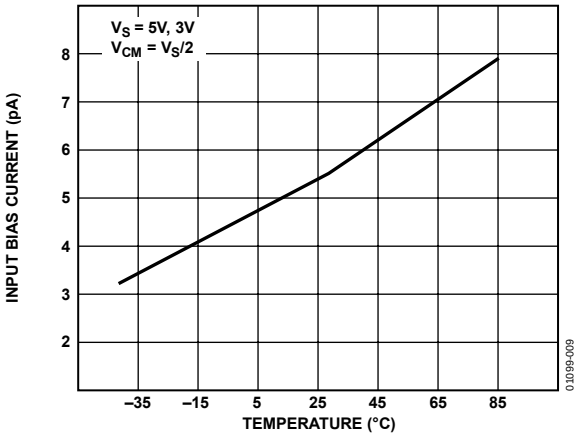


Figure 9. Input Bias Current vs. Temperature

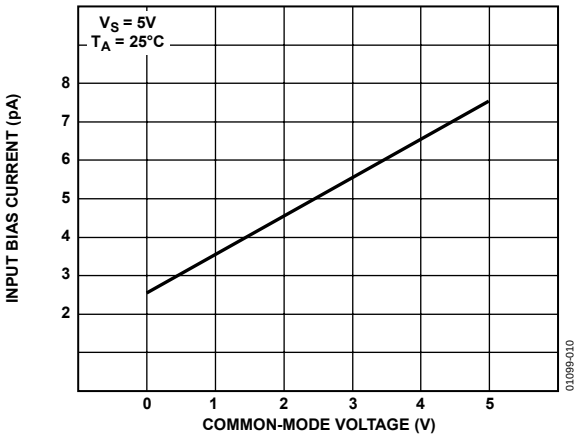


Figure 10. Input Bias Current vs. Common-Mode Voltage

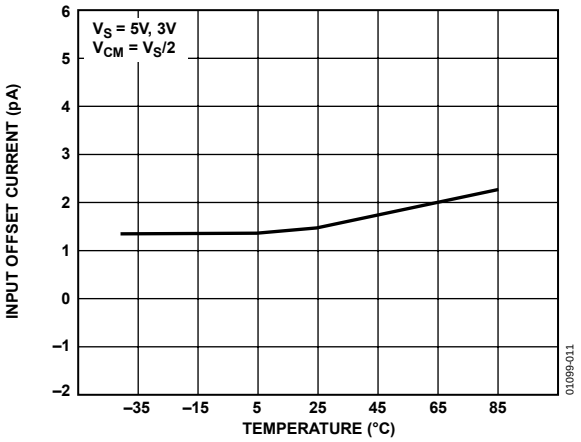


Figure 11. Input Offset Current vs. Temperature

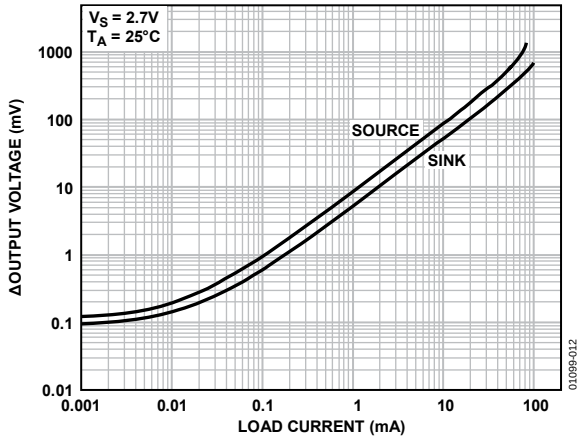


Figure 12. Output Voltage to Supply Rail vs. Load Current

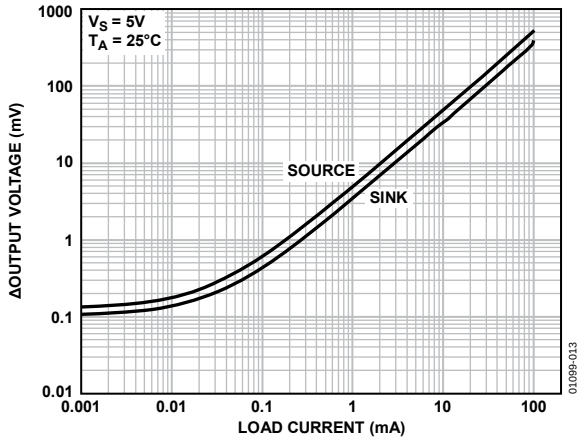


Figure 13. Output Voltage to Supply Rail vs. Load Current

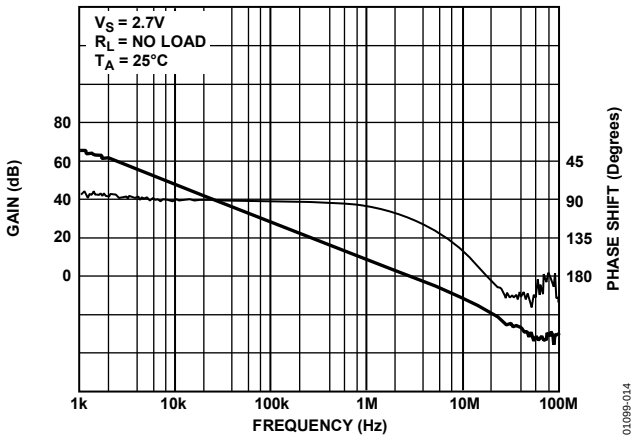


Figure 14. Open-Loop Gain and Phase Shift vs. Frequency

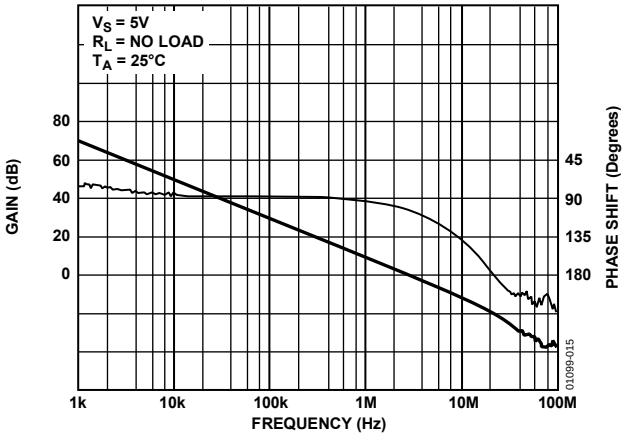


Figure 15. Open-Loop Gain and Phase Shift vs. Frequency

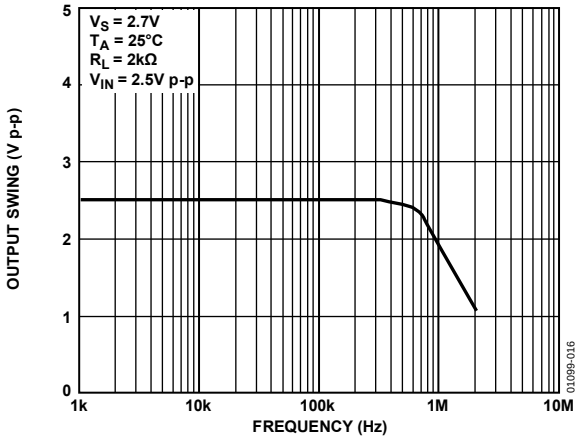


Figure 16. Closed-Loop Output Swing vs. Frequency

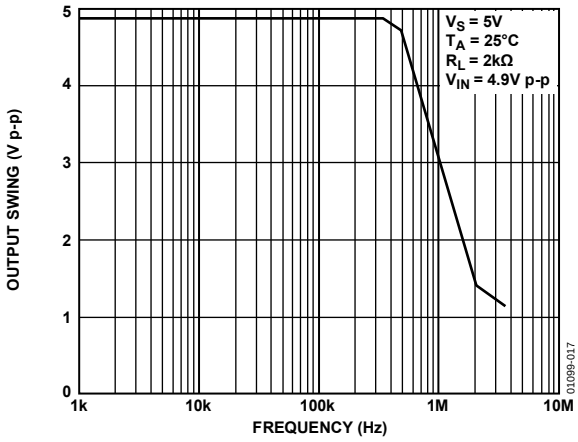


Figure 17. Closed-Loop Output Swing vs. Frequency

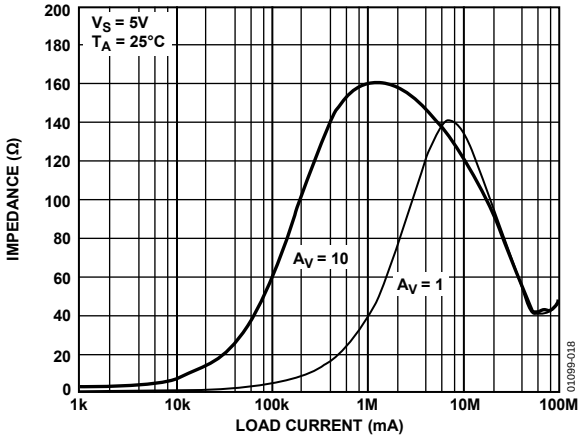


Figure 18. Closed-Loop Output Impedance vs. Frequency

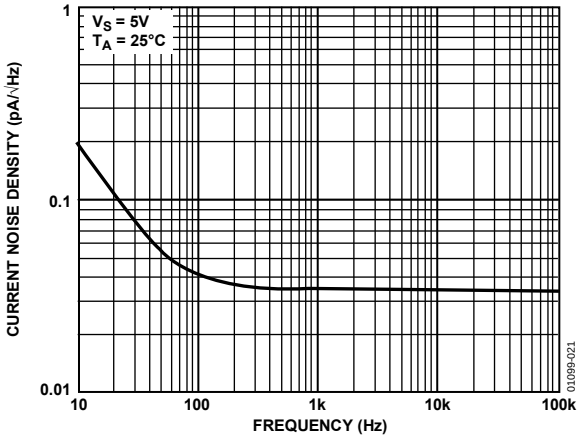


Figure 21. Current Noise Density vs. Frequency

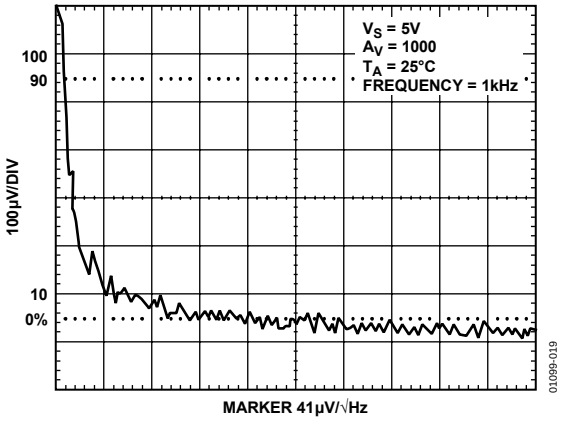


Figure 19. Voltage Noise Density vs. Frequency (1 kHz)

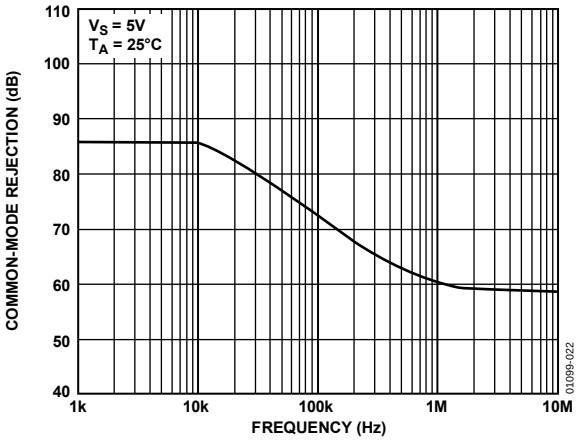


Figure 22. Common-Mode Rejection vs. Frequency

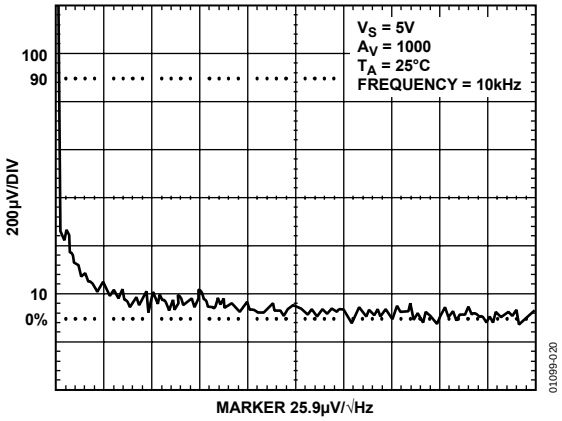


Figure 20. Voltage Noise Density vs. Frequency (10 kHz)

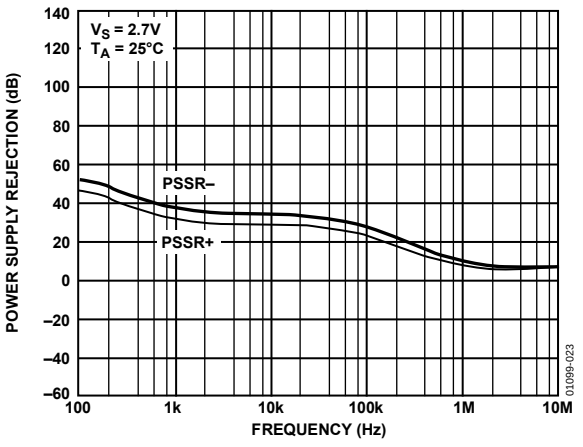


Figure 23. Power Supply Rejection vs. Frequency

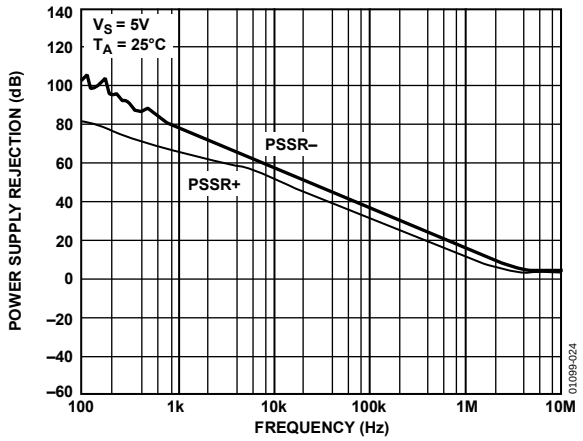


Figure 24. Power Supply Rejection vs. Frequency

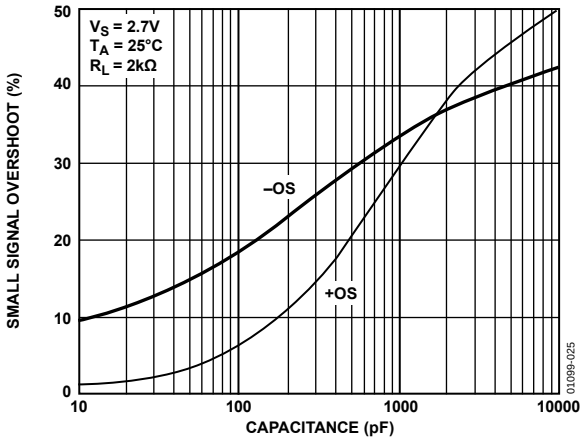


Figure 25. Small Signal Overshoot vs. Load Capacitance

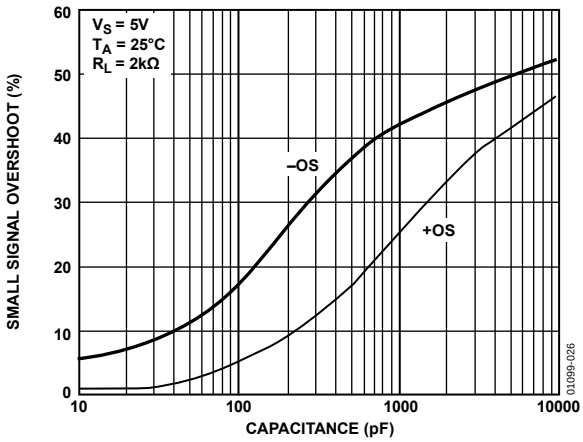


Figure 26. Small Signal Overshoot vs. Load Capacitance

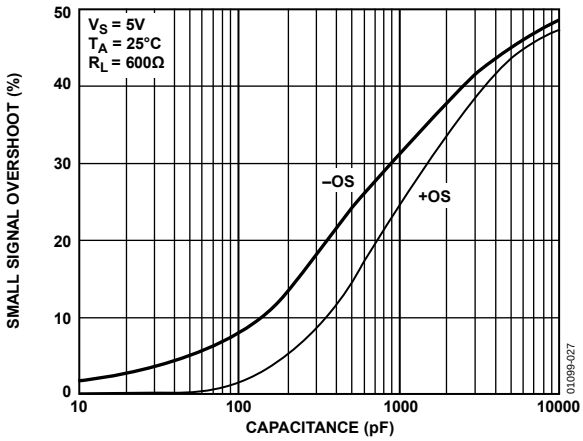


Figure 27. Small Signal Overshoot vs. Load Capacitance

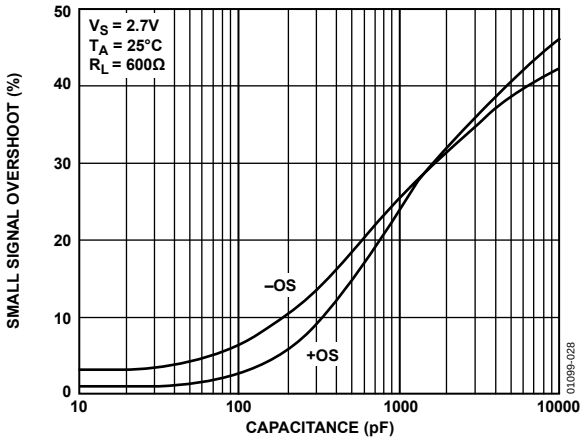


Figure 28. Small Signal Overshoot vs. Load Capacitance

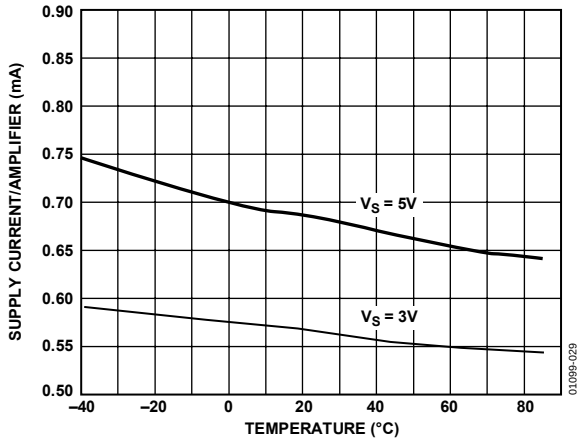


Figure 29. Supply Current per Amplifier vs. Temperature

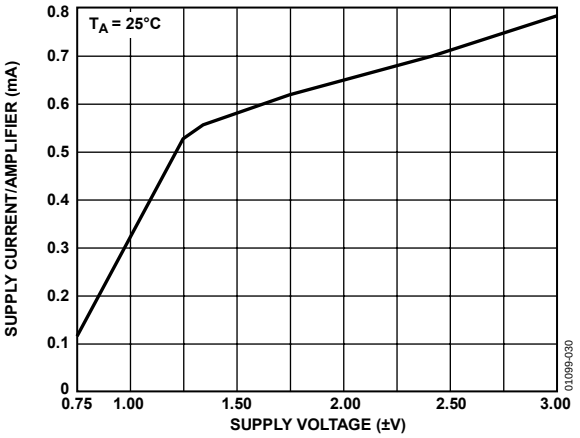


Figure 30. Supply Current per Amplifier vs. Supply Voltage

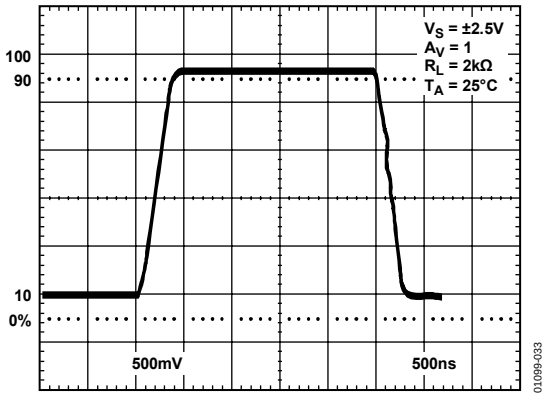


Figure 33. Large Signal Transient Response

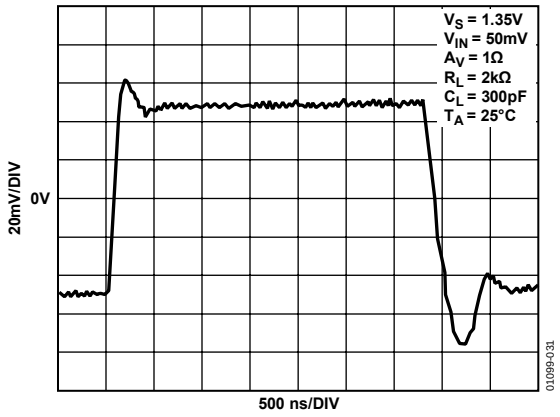


Figure 31. Small Signal Transient Response

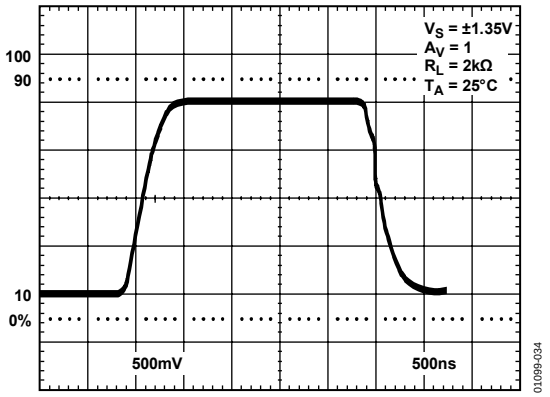


Figure 34. Large Signal Transient Response

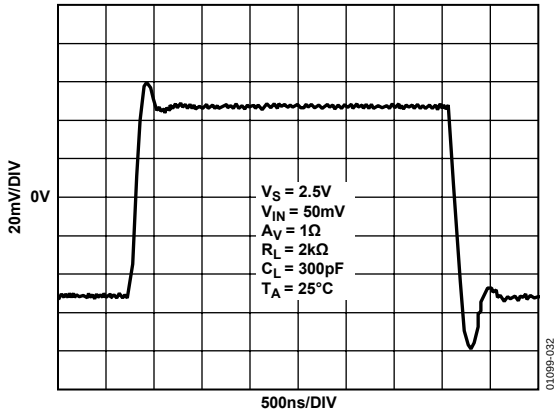


Figure 32. Small Signal Transient Response

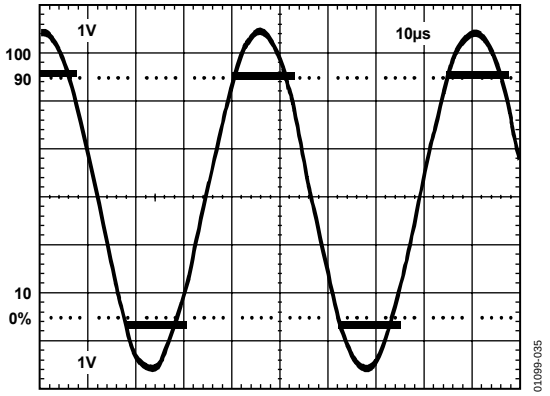


Figure 35. No Phase Reversal

THEORY OF OPERATION

The AD8531/AD8532/AD8534 are all CMOS, high output current drive, rail-to-rail input/output operational amplifiers. Their high output current drive and stability with heavy capacitive loads make the AD8531/AD8532/AD8534 excellent choices as drive amplifiers for LCD panels.

Figure 36 illustrates a simplified equivalent circuit for the AD8531/AD8532/AD8534. Like many rail-to-rail input amplifier configurations, it comprises two differential pairs, one N-channel (M1 to M2) and one P-channel (M3 to M4). These differential pairs are biased by 50 μA current sources, each with a compliance limit of approximately 0.5 V from either supply voltage rail. The differential input voltage is then converted into a pair of differential output currents. These differential output currents are then combined in a compound folded-cascade second gain stage (M5 to M9). The outputs of the second gain stage at M8 and M9 provide the gate voltage drive to the rail-to-rail output stage. Additional signal current recombination for the output stage is achieved using M11 to M14.

To achieve rail-to-rail output swings, the AD8531/AD8532/AD8534 design employs a complementary, common source output stage (M15 to M16). However, the output voltage swing is directly dependent on the load current because the difference between the output voltage and the supply is determined by the AD8531/AD8532/AD8534's output transistors on channel resistance (see Figure 12 and Figure 13). The output stage also exhibits voltage gain by virtue of the use of common source amplifiers; as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a strong dependence on the total load resistance at the output of the AD8531/AD8532/AD8534.

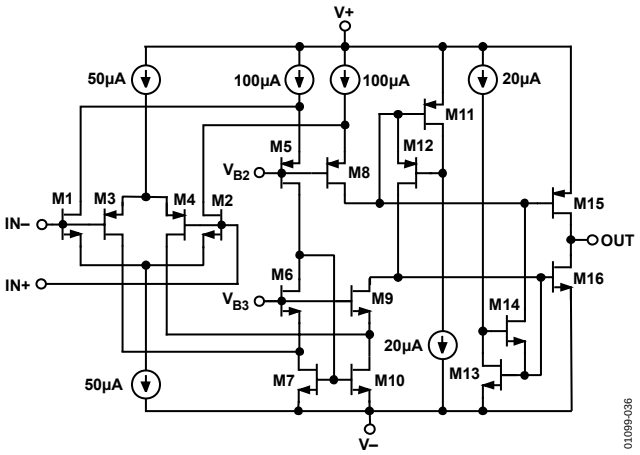


Figure 36. Simplified Equivalent Circuit

SHORT-CIRCUIT PROTECTION

As a result of the design of the output stage for the maximum load current capability, the AD8531/AD8532/AD8534 do not have any internal short-circuit protection circuitry. Direct connection of the output of the AD8531/AD8532/AD8534 to the positive supply in single-supply applications destroys the device. In applications where some protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output, as shown in Figure 37, can be used. The resistor, connected within the feedback loop of the amplifier, has very little effect on the performance of the amplifier other than limiting the maximum available output voltage swing. For single 5 V supply applications, resistors less than 20 Ω are not recommended.

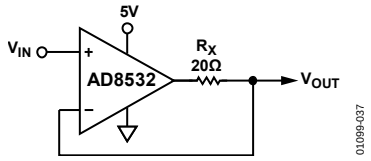


Figure 37. Output Short-Circuit Protection

POWER DISSIPATION

Although the AD8531/AD8532/AD8534 are capable of providing load currents to 250 mA, the usable output load current drive capability is limited to the maximum power dissipation allowed by the device package used. In any application, the absolute maximum junction temperature for the AD8531/AD8532/AD8534 is 150°C. The maximum junction temperature should never be exceeded because the device could suffer premature failure. Accurately measuring power dissipation of an integrated circuit is not always a straightforward exercise; therefore, Figure 38 is provided as a design aid for either setting a safe output current drive level or selecting a heat sink for the package options available on the AD8531/AD8532/AD8534.

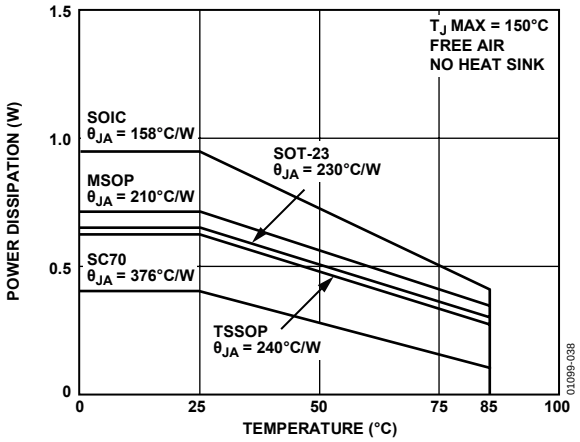


Figure 38. Maximum Power Dissipation vs. Ambient Temperature

The thermal resistance curves were determined using the AD8531/AD8532/AD8534 thermal resistance data for each package and a maximum junction temperature of 150°C. The following formula can be used to calculate the internal junction temperature of the AD8531/AD8532/AD8534 for any application:

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

where:
T_J is the junction temperature.
P_{DISS} is the power dissipation.
θ_{JA} is the package thermal resistance, junction-to-case.
T_A is the ambient temperature of the circuit.

To calculate the power dissipated by the AD8531/AD8532/AD8534, the following equation can be used:

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where:
I_{LOAD} is the output load current.
V_S is the supply voltage.
V_{OUT} is the output voltage.

The quantity within the parentheses is the maximum voltage developed across either output transistor. As an additional design aid in calculating available load current from the AD8531/AD8532/AD8534, Figure 5 illustrates the output voltage of the AD8531/AD8532/AD8534 as a function of load resistance.

POWER CALCULATIONS FOR VARYING OR UNKNOWN LOADS

Often, calculating power dissipated by an integrated circuit to determine if the device is being operated in a safe range is not as simple as it may seem. In many cases, power cannot be directly measured, which may be the result of irregular output waveforms or varying loads; indirect methods of measuring power are required.

There are two methods to calculate power dissipated by an integrated circuit. The first can be done by measuring the package temperature and the board temperature, and the other is to directly measure the supply current of the circuit.

CALCULATING POWER BY MEASURING AMBIENT AND CASE TEMPERATURE

Given the two equations for calculating junction temperature

$$T_J = T_A + P_{DISS}\,\theta_{JA}$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
θ_{JA} is the junction to ambient thermal resistance.

$$T_J = T_C + P_{DISS}\,\theta_{JA}$$

where:
T_C is the case temperature.
θ_{JA} and θ_{JC} are given in the data sheet.

The two equations can be solved for P (power)

$$T_A + P_{DISS}\,\theta_{JA} = T_C + P\theta_{JC}$$

$$P_{DISS} = (T_A - T_C)/(\theta_{JC} - \theta_{JA})$$

Once power is determined, it is necessary to go back and calculate the junction temperature to ensure that it has not been exceeded.

The temperature measurements should be directly on the package and on a spot on the board that is near the package but not touching it. Measuring the package could be difficult. A very small bimetallic junction glued to the package can be used, or measurement can be done using an infrared sensing device if the spot size is small enough.

CALCULATING POWER BY MEASURING SUPPLY CURRENT

Power can be calculated directly, knowing the supply voltage and current. However, supply current may have a dc component with a pulse into a capacitive load, which can make rms current very difficult to calculate. It can be overcome by lifting the supply pin and inserting an rms current meter into the circuit. For this to work, be sure the current is being delivered by the supply pin being measured. This is usually a good method in a single-supply system; however, if the system uses dual supplies, both supplies may need to be monitored.

INPUT OVERVOLTAGE PROTECTION

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, the input overvoltage characteristic of the device must be considered. When an overvoltage occurs, the amplifier can be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current. Although not shown here, when the input voltage exceeds either supply by more than 0.6 V, pn junctions internal to the AD8531/AD8532/AD8534 energize, allowing current to flow from the input to the supplies. As illustrated in the simplified equivalent input circuit (see Figure 36), the AD8531/AD8532/AD8534 do not have any internal current limiting resistors; therefore, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, as long as it is limited to 5 mA or less. For the AD8531/AD8532/AD8534, once the input voltage exceeds the supply by more than 0.6 V, the input current quickly exceeds 5 mA. If this condition continues to exist, an external series resistor should be added. The size of the resistor is calculated by dividing the maximum overvoltage by 5 mA. For example, if the input voltage could reach 10 V, the external resistor should be (10 V/5 mA) = 2 kΩ.

This resistance should be placed in series with either or both inputs if they are exposed to an overvoltage condition.

OUTPUT PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. The AD8531/AD8532/AD8534 are free from reasonable input voltage range restrictions, provided that input voltages no greater than the supply voltage rails are applied. Although the output of the device does not change phase, large currents can flow through internal junctions to the supply rails, which was described in the Input Overvoltage Protection section. Without limit, these fault currents can easily destroy the amplifier. The technique recommended in the Input Overvoltage Protection section should therefore be applied in those applications where the possibility of input voltages exceeding the supply voltages exists.

CAPACITIVE LOAD DRIVE

The AD8531/AD8532/AD8534 exhibit excellent capacitive load driving capabilities. They can drive up to 10 nF directly, as shown in Figure 25 through Figure 28. However, even though the device is stable, a capacitive load does not come without a penalty in bandwidth. As shown in Figure 39, the bandwidth is reduced to less than 1 MHz for loads greater than 10 nF. A snubber network on the output does not increase the bandwidth, but it does significantly reduce the amount of overshoot for a given capacitive load. A snubber consists of a series RC network (R_S, C_S), as shown in Figure 40, connected from the output of the device to ground. This network operates in parallel with the load capacitor, C_L, to provide phase lag compensation. The actual value of the resistor and capacitor is best determined empirically.

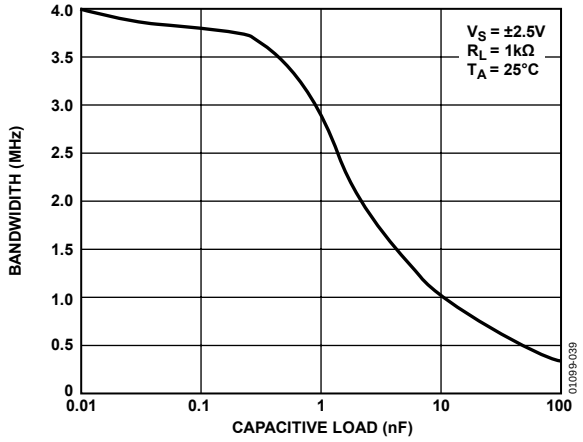


Figure 39. Unity-Gain Bandwidth vs. Capacitive Load

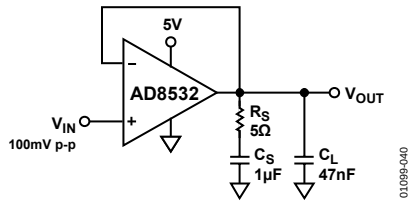


Figure 40. Snubber Network Compensates for Capacitive Loads

The first step is to determine the value of the resistor, R_S. A good starting value is 100 Ω. This value is reduced until the small signal transient response is optimized. Next, C_S is determined; 10 µF is a good starting point. This value is reduced to the smallest value for acceptable performance (typically, 1 µF). For the case of a 47 nF load capacitor on the AD8531/AD8532/AD8534, the optimal snubber network is 5 Ω in series with 1 µF. The benefit is immediately apparent, as seen in Figure 41. The top trace was taken with a 47 nF load, and the bottom trace was taken with the 5 Ω in series with a 1 µF snubber network in place. The amount of overshoot and ringing is dramatically reduced. Table 5 illustrates a few sample snubber networks for large load capacitors.

Table 5. Snubber Networks for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (R_S, C_S)
0.47 nF	300 Ω, 0.1 µF
4.7 nF	30 Ω, 1 µF
47 nF	5 Ω, 1 µF

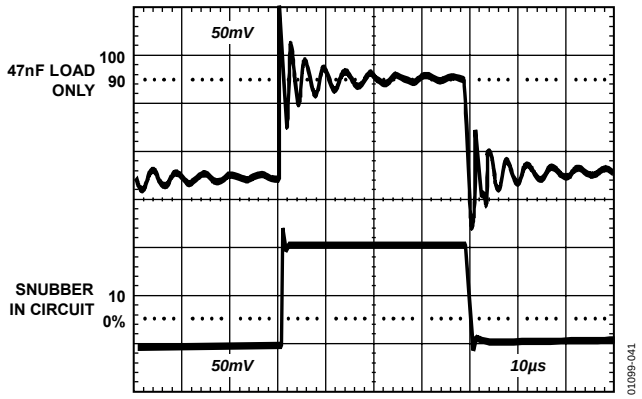


Figure 41. Overshoot and Ringing Are Reduced by Adding a Snubber Network in Parallel with the 47 nF Load

APPLICATIONS INFORMATION

HIGH OUTPUT CURRENT, BUFFERED REFERENCE/REGULATOR

Many applications require stable voltage outputs relatively close in potential to an unregulated input source. This low dropout type of reference/regulator is readily implemented with a rail-to-rail output op amp and is particularly useful when using a higher current device, such as the AD8531/AD8532/AD8534. A typical example is the 3.3 V or 4.5 V reference voltage developed from a 5 V system source. Generating these voltages requires a three terminal reference, such as the REF196 (3.3 V) or the REF194 (4.5 V), both of which feature low power, with sourcing outputs of 30 mA or less. Figure 42 shows how such a reference can be outfitted with an AD8531/AD8532/AD8534 buffer for higher currents and/or voltage levels, plus sink and source load capability.

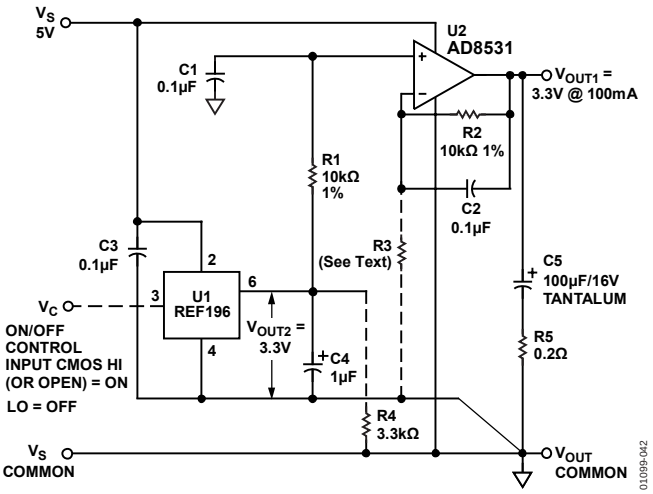


Figure 42. High Output Current Reference/Regulator

The low dropout performance of this circuit is provided by stage U2, an AD8531 connected as a follower/buffer for the basic reference voltage produced by U1. The low voltage saturation characteristic of the AD8531/AD8532/AD8534 allows up to 100 mA of load current in the illustrated use, as a 5 V to 3.3 V converter with good dc accuracy. In fact, the dc output voltage change for a 100 mA load current delta measures less than 1 mV. This corresponds to an equivalent output impedance of < 0.01 Ω. In this application, the stable 3.3 V from U1 is applied to U2 through a noise filter, R1 to C1. U2 replicates the U1 voltage within a few millivolts, but at a higher current output at V_{OUT1}, with the ability to both sink and source output current(s), unlike most IC references. R2 and C2 in the feedback path of U2 provide additional noise filtering.

Transient performance of the reference/regulator for a 100 mA step change in load current is also quite good and is largely determined by the R5 to C5 output network. With values as shown, the transient is about 20 mV peak and settles to within 2 mV in less than 10 µs for either polarity. Although room exists for optimizing the transient response, any changes to the R5 to C5 network should be verified by experiment to preclude the possibility of excessive ringing with some capacitor types.

To scale V_{OUT2} to another (higher) output level, the optional resistor R3 (shown dotted in Figure 42) is added, causing the new V_{OUT1} to become

$$V_{OUT1} = V_{OUT2} \times \left(1 + \frac{R2}{R3}\right)$$

The circuit can either be used as shown, as a 5 V to 3.3 V reference/regulator, or with on/off control. By driving Pin 3 of U1 with a logic control signal as noted, the output is switched on/off. Note that when on/off control is used, R4 must be used with U1 to speed on/off switching.

SINGLE-SUPPLY, BALANCED LINE DRIVER

The circuit in Figure 43 is a unique line driver circuit topology used in professional audio applications. It was modified for automotive and multimedia audio applications. On a single 5 V supply, the line driver exhibits less than 0.7% distortion into a 600 Ω load from 20 Hz to 15 kHz (not shown) with an input signal level of 4 V p-p. In fact, the output drive capability of the AD8531/AD8532/AD8534 maintains this level for loads as small as 32 Ω. For input signals less than 1 V p-p, the THD is less than 0.1%, regardless of load. The design is a transformer-less, balanced transmission system where output common-mode rejection of noise is of paramount importance. As with the transformer-based system, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. Other circuit gains can be set according to the equation in the diagram. This allows the design to be easily configured for inverting, noninverting, or differential operation.

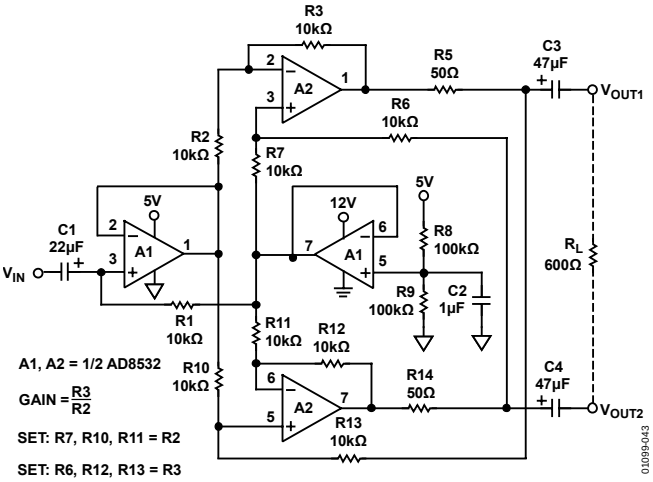


Figure 43. Single-Supply, Balanced Line Driver for Multimedia and Automotive Applications

SINGLE-SUPPLY HEADPHONE AMPLIFIER

Because of its speed and large output drive, the AD8531/AD8532/AD8534 make an excellent headphone driver, as illustrated in Figure 44. Its low supply operation and rail-to-rail inputs and outputs give a maximum signal swing on a single 5 V supply. To ensure maximum signal swing available to drive the headphone, the amplifier inputs are biased to V+/2, which in this case is 2.5 V. The 100 kΩ resistor to the positive supply is equally split into two 50 kΩ resistors, with their common point bypassed by 10 µF to prevent power supply noise from contaminating the audio signal.

The audio signal is then ac-coupled to each input through a 10 µF capacitor. A large value is needed to ensure that the 20 Hz audio information is not blocked. If the input already has the proper dc bias, the ac coupling and biasing resistors are not required. A 270 µF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of the headphones, which can range from 32 Ω to 600 Ω. An additional 16 Ω resistor is used in series with the output capacitor to protect the output stage of the op amp by limiting the capacitor discharge current. When driving a 48 Ω load, the circuit exhibits less than 0.3% THD+N at output drive levels of 4 V p-p.

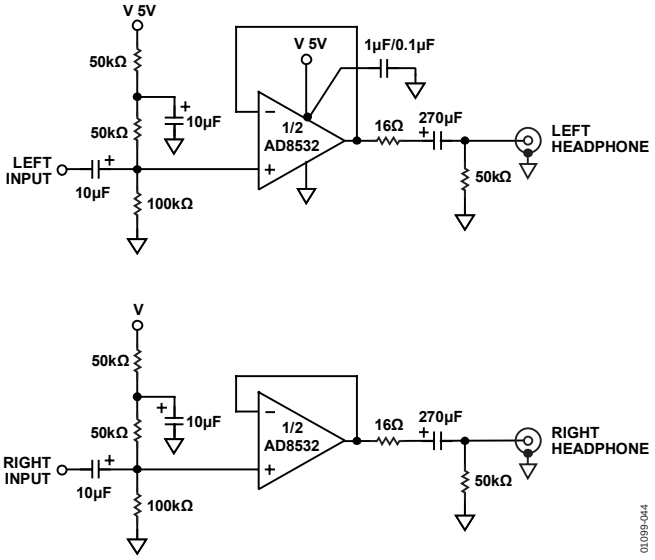


Figure 44. Single-Supply, Stereo Headphone Driver

SINGLE-SUPPLY, 2-WAY LOUDSPEAKER CROSSOVER NETWORK

Active filters are useful in loudspeaker crossover networks because of small size, relative freedom from parasitic effects, the ease of controlling low/high channel drive, and the controlled driver damping provided by a dedicated amplifier. Both Sallen-Key (SK) and multiple-feedback (MFB) filter architectures are useful in implementing active crossover networks. The circuit shown in Figure 45 is a single-supply, 2-way active crossover that combines the advantages of both filter topologies.

This active crossover exhibits less than 0.4% THD+N at output levels of 1.4 V rms using general-purpose, unity-gain HP/LP stages.

In this 2-way example, the LO signal is a dc-to-500 Hz LP woofer output, and the HI signal is the HP (>500 Hz) tweeter output. U1B forms an LP section at 500 Hz, while U1A provides an HP section, covering frequencies ≥500 Hz.

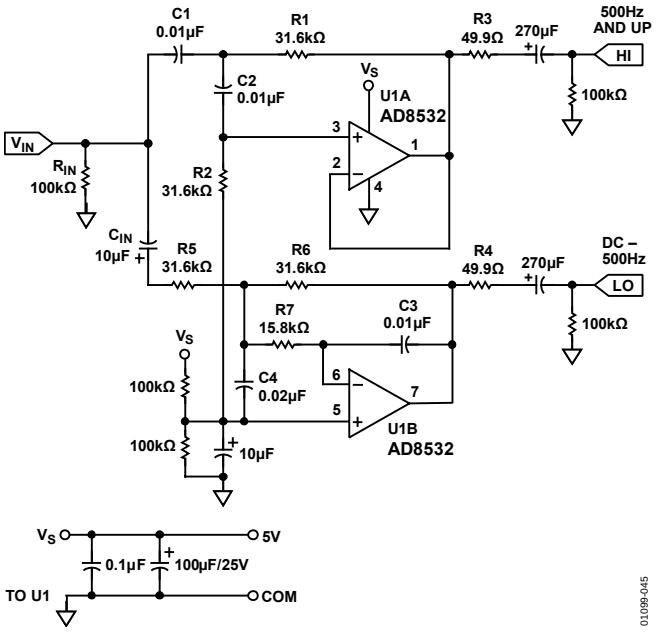


Figure 45. A Single-Supply, 2-Way Active Crossover

The crossover example frequency of 500 Hz can be shifted lower or higher by frequency scaling of either resistors or capacitors. In configuring the circuit for other frequencies, complementary LP/HP action must be maintained between sections, and component values within the sections must be in the same ratio. Table 6 provides a design aid to adaptation, with suggested standard component values for other frequencies.

For additional information on the active filters and active crossover networks, refer to the data sheet for the OP279, a dual rail-to-rail, high output current, operational amplifier.

Table 6. RC Component Selection for Various Crossover Frequencies[1]

Crossover Frequency (Hz)	R1/C1 (U1A)[2], R5/C3 (U1B)[3]
100	160 kΩ/0.01 µF
200	80.6 kΩ/0.01 µF
319	49.9 kΩ/0.01 µF
500	31.6 kΩ/0.01 µF
1 k	16 kΩ/0.01 µF
2 k	8.06 kΩ/0.01 µF
5 k	3.16 kΩ/0.01 µF
10 k	1.6 kΩ/0.01 µF

[1] Applicable for Filter A = 2.
[2] For Sallen-Key stage U1A: R1 = R2, and C1 = C2, and so on.
[3] For multiple feedback stage U1B: R6 = R5, R7 = R5/2, and C4 = 2C3.

DIRECT ACCESS ARRANGEMENT FOR TELEPHONE LINE INTERFACE

Figure 46 illustrates a 5 V only transmit/receive telephone line interface for 600 Ω transmission systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line in a differential manner. A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Because of the high output current drive and low dropout voltage of the AD8531/AD8532/AD8534, the largest signal available on a single 5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. A3 is configured as a difference amplifier for two reasons: it prevents the transmit signal from interfering with the receive signal, and it extracts the receive signal from the transmission line for amplification by A4. The gain of A4 can be adjusted in the same manner as that of A1 to meet the input signal requirements of the modem. Standard resistor values permit the use of single in-line package (SIP) format resistor arrays.

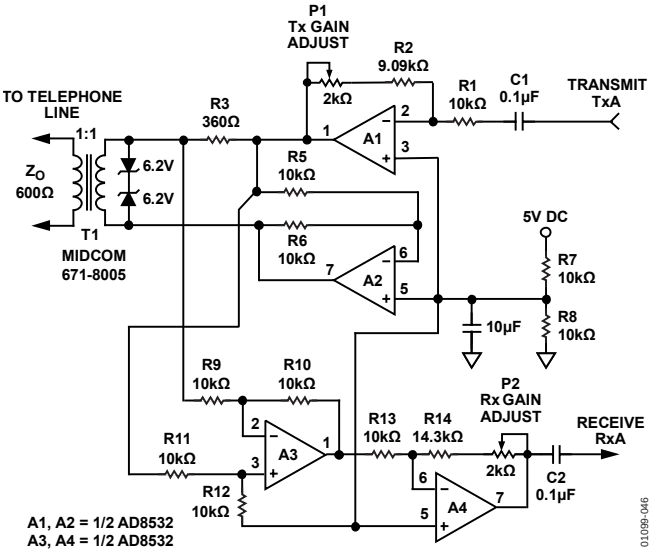
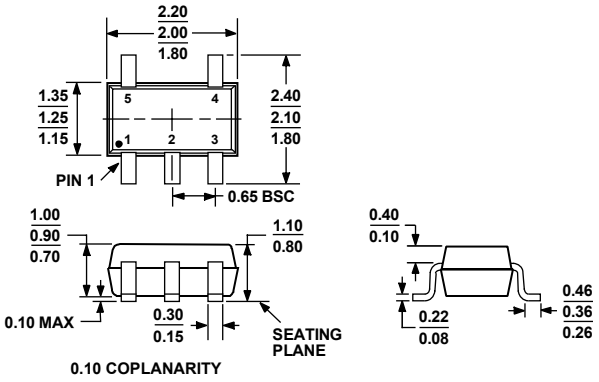


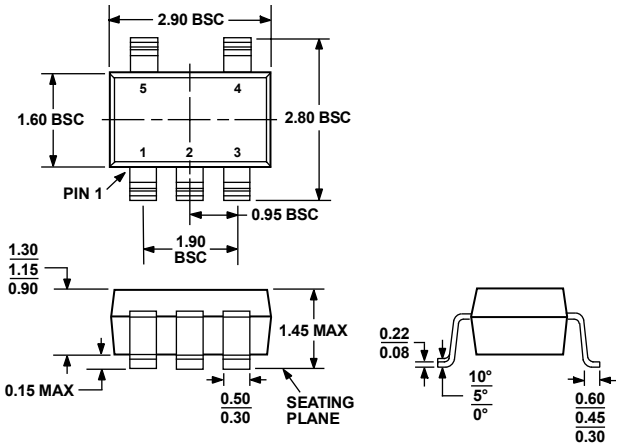
Figure 46. Single-Supply Direct Access Arrangement for Modems

OUTLINE DIMENSIONS



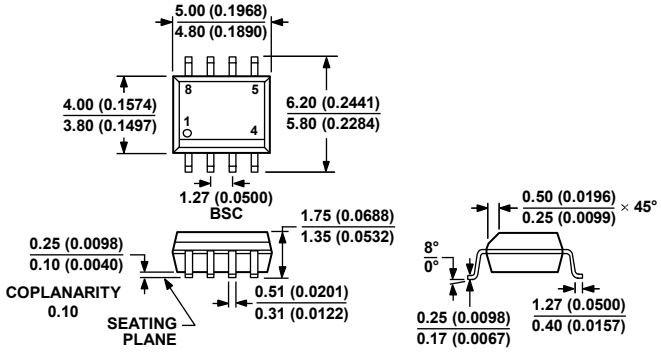
COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 47. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AA

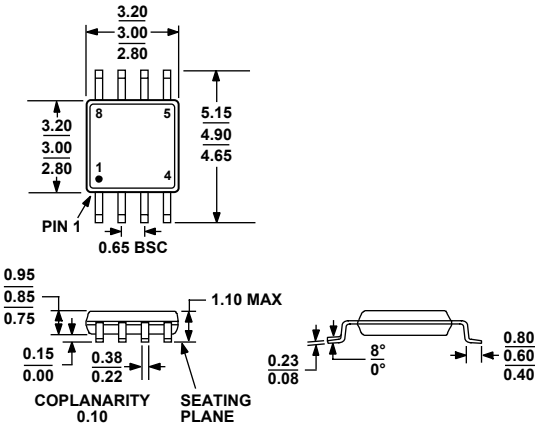
Figure 48. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

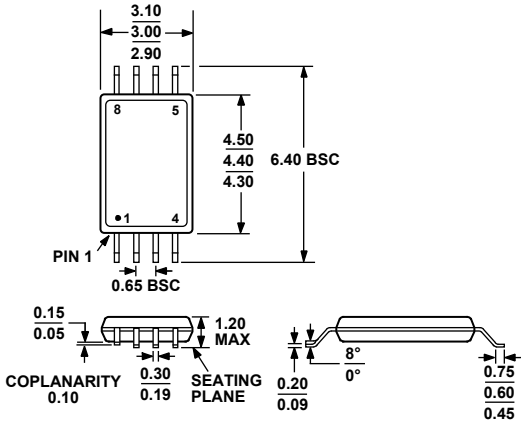
012407-A

Figure 49. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



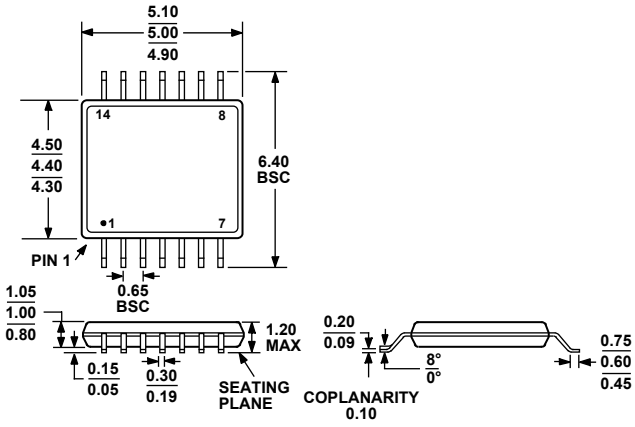
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 50. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



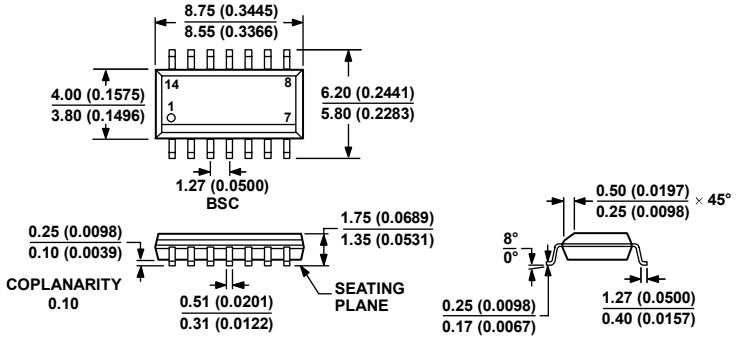
COMPLIANT TO JEDEC STANDARDS MO-153-AA

Figure 51. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 52. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 53. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8531AKS-R2	−40°C to +85°C	5-Lead SC70	KS-5	A7B
AD8531AKS-REEL7	−40°C to +85°C	5-Lead SC70	KS-5	A7B
AD8531AKSZ-R2[1]	−40°C to +85°C	5-Lead SC70	KS-5	A0Q
AD8531AKSZ-REEL7[1]	−40°C to +85°C	5-Lead SC70	KS-5	A0Q
AD8531ART-REEL	−40°C to +85°C	5-Lead SOT-23	RJ-5	A7A
AD8531ART-REEL7	−40°C to +85°C	5-Lead SOT-23	RJ-5	A7A
AD8531ARTZ-REEL[1]	−40°C to +85°C	5-Lead SOT-23	RJ-5	A0P
AD8531ARTZ-REEL7[1]	−40°C to +85°C	5-Lead SOT-23	RJ-5	A0P
AD8531AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8531AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8531ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8531ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8532ARM-R2	−40°C to +85°C	8-Lead MSOP	RM-8	ARA
AD8532ARM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	ARA
AD8532ARMZ-R2[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A0R
AD8532ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A0R
AD8532ARU	−40°C to +85°C	8-Lead TSSOP	RU-8	
AD8532ARU-REEL	−40°C to +85°C	8-Lead TSSOP	RU-8	
AD8532ARUZ[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	
AD8532ARUZ-REEL[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	
AD8534AR	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8534AR-REEL	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8534ARZ[1]	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8534ARZ-REEL[1]	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8534ARU	−40°C to +85°C	14-Lead TSSOP	RU-14	
AD8534ARU-REEL	−40°C to +85°C	14-Lead TSSOP	RU-14	
AD8534ARUZ[1]	−40°C to +85°C	14-Lead TSSOP	RU-14	
AD8534ARUZ-REEL[1]	−40°C to +85°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part.

©1996–2008 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D01099-0-1/08(F)

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AD8531ARZ-REEL on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management