THE DATASHEET OF

LT3011EDD#TRPBF

50mA, 3V to 80V Low Dropout Micropower Linear Regulator with PWRGD

FEATURES

- **Wide Input Voltage Range: 3V to 80V**
- **Low Quiescent Current: 46µA**
- **Low Dropout Voltage: 300mV**
- **Output Current: 50mA**
- **PWRGD Flag with Programmable Delay**
- No Protection Diodes Needed
- Adjustable Output from 1.24V to 60V
- 1µA Quiescent Current in Shutdown
- Stable with 1µF Output Capacitor
- Stable with Ceramic, Tantalum, and Aluminum Capacitors
- Reverse-Battery Protection
- No Reverse Current Flow from Output to Input
- Thermal Limiting
- Thermally Enhanced 12-Lead MSOP and 10-Pin (3mm × 3mm) DFN Packages

APPLICATIONS

- Low Current High Voltage Regulators
- Regulator for Battery-Powered Systems
- Telecom Applications
- Automotive Applications

DESCRIPTION

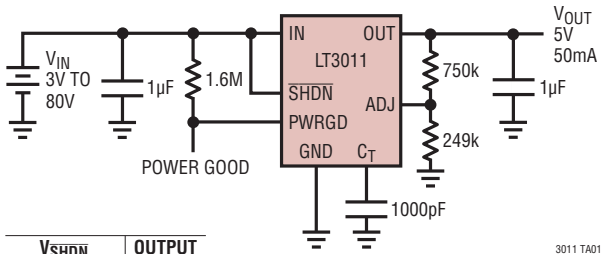
The LT®3011 is a high voltage, micropower, low dropout linear regulator. The device is capable of supplying 50mA of output current with a dropout voltage of 300mV. Designed for use in battery-powered high voltage systems, the low quiescent current (46µA operating and 1µA in shutdown) is well controlled in dropout, making the LT3011 an ideal choice.

The LT3011 includes a PWRGD flag to indicate output regulation. The delay between regulated output level and flag indication is programmable with a single capacitor. The LT3011 also has the ability to operate with very small output capacitors; it is stable with only 1µF on the output. Small ceramic capacitors can be used without the addition of any series resistance (ESR) as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse current protection.

The LT3011 features an adjustable output with a 1.24V reference voltage. The device is available in the thermally enhanced 12-lead MSOP and the low profile (0.75mm) 10-pin (3mm × 3mm) DFN package, both providing excellent thermal characteristics.

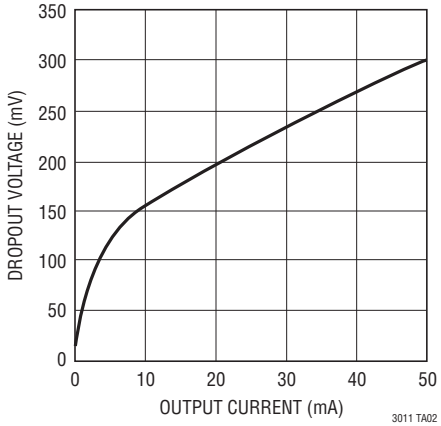
TYPICAL APPLICATION

5V Supply with Shutdown



$V_{\overline{SHDN}}$	OUTPUT
<0.3V	OFF
>2.0V	ON

Dropout Voltage

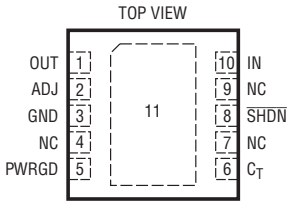


ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage ..... ±80V
OUT Pin Voltage ..... ±60V
Input-to-Output Differential Voltage ..... ±80V
ADJ Pin Voltage ..... ±7V
$\overline{SHDN}$ Pin Voltage ..... ±80V
C_T Pin Voltage ..... 7V, –0.5V
PWRGD Pin Voltage ..... 80V, –0.5V
Output Short-Circuit Duration ..... Indefinite

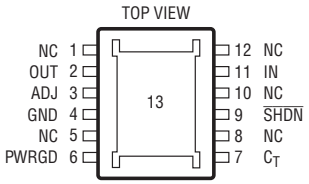
Storage Temperature Range ..... –65°C to 150°C
Operating Junction Temperature
(Notes 3, 10, 11)
LT3011E, LT3011I ..... –40°C to 125°C
LT3011H ..... –40°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Package Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 16°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 16°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3011EDD#PBF	LT3011EDD#TRPBF	LDKQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3011IDD#PBF	LT3011IDD#TRPBF	LDKQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3011EMSE#PBF	LT3011EMSE#TRPBF	3011	12-Lead Plastic MSOP	–40°C to 125°C
LT3011HMSE#PBF	LT3011HMSE#TRPBF	3011	12-Lead Plastic MSOP	–40°C to 150°C
LT3011IMSE#PBF	LT3011IMSE#TRPBF	3011	12-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3011EDD	LT3011EDD#TR	LDKQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3011IDD	LT3011IDD#TR	LDKQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3011EMSE	LT3011EMSE#TR	3011	12-Lead Plastic MSOP	–40°C to 125°C
LT3011HMSE	LT3011HMSE#TR	3011	12-Lead Plastic MSOP	–40°C to 150°C
LT3011IMSE	LT3011IMSE#TR	3011	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (LT3011E, LT3011I)

The ● denotes the specifications which apply over the –40°C to 125°C operating temperature range, otherwise specifications are T_J = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	I_{LOAD} = 50mA	●		2.8	4	V
ADJ Pin Voltage (Notes 2, 3)	V_{IN} = 3V, I_{LOAD} = 1mA 4V < V_{IN} < 80V, 1mA < I_{LOAD} < 50mA	 ●	1.228 1.215	1.24 1.24	1.252 1.265	V V
Line Regulation (Note 2)	ΔV_{IN} = 3V to 80V, I_{LOAD} = 1mA	●		1	12	mV
Load Regulation (Note 2)	V_{IN} = 4V, ΔI_{LOAD} = 1mA to 50mA V_{IN} = 4V, ΔI_{LOAD} = 1mA to 50mA	 ●		6	15 25	mV mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 4, 5)	I_{LOAD} = 1mA I_{LOAD} = 1mA	 ●		100	150 190	mV mV
	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		200	260 350	mV mV
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		300	370 550	mV mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 4, 6)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 10mA I_{LOAD} = 50mA	● ● ● ●		46 105 410 1.9	90 200 700 3.3	µA µA µA mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 50mA, BW = 10Hz to 100kHz, V_{OUT} = 1.24V			100		μV_{RMS}
ADJ Pin Bias Current	(Note 7)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.3	1.3 1.1	2	V V
$\overline{SHDN}$ Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 6V			0.5 0.1	2 0.5	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			1	5	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	85	90	94	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1.1		%
PWRGD Output Low Voltage	I_{PWRGD} = 50µA	●		140	250	mV
C_T Pin Charging Current		●		3	6	µA
C_T Pin Voltage Differential	$V_{CT(PWRGD\ High)} - V_{CT(PWRGD\ Low)}$			1.67		V
Ripple Rejection	V_{IN} = 7V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 50mA		65	85		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0V V_{IN} = 4V, ΔV_{OUT} = –0.1V (Note 2)	 ●	 60	140		mA mA
Input Reverse Leakage Current	V_{IN} = –80V, V_{OUT} = 0V	●			6	mA
Reverse Output Current (Note 9)	V_{OUT} = 1.24V, V_{IN} < 1.24V (Note 2)			8	15	µA

ELECTRICAL CHARACTERISTICS (LT3011H)

The ● denotes the specifications which apply over the –40°C to 150°C operating temperature range, otherwise specifications are T_J = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	I_{LOAD} = 50mA	●		2.8	4	V
ADJ Pin Voltage (Notes 2, 3)	V_{IN} = 3V, I_{LOAD} = 1mA 4V < V_{IN} < 80V, 1mA < I_{LOAD} < 50mA	 ●	1.228 1.215	1.24 1.24	1.252 1.265	V V
Line Regulation (Note 2)	ΔV_{IN} = 3V to 80V, I_{LOAD} = 1mA	●		1	12	mV
Load Regulation (Note 2)	V_{IN} = 4V, ΔI_{LOAD} = 1mA to 50mA V_{IN} = 4V, ΔI_{LOAD} = 1mA to 50mA	 ●		6	15 25	mV mV

ELECTRICAL CHARACTERISTICS (LT3011H)

The ● denotes the specifications which apply over the –40°C to 150°C operating temperature range, otherwise specifications are at T_J = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 5)	I_{LOAD} = 1mA I_{LOAD} = 1mA	 ●		100	150 220	mV mV
	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		200	260 380	mV mV
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		300	370 575	mV mV
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 6)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 10mA I_{LOAD} = 50mA	● ● ● ●		46 105 410 1.9	125 225 750 3.5	µA µA µA mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 50mA, BW = 10Hz to 100kHz, V_{OUT} = 1.24V			100		μV_{RMS}
ADJ Pin Bias Current	(Note 7)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.3	1.3 1.1	2	V V
$\overline{SHDN}$ Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 6V			0.5 0.1	2 0.5	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			1	5	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	85	90	95	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1.1		%
PWRGD Output Low Voltage	I_{PWRGD} = 50µA	●		140	250	mV
C_T Pin Charging Current		●		3	6	µA
C_T Pin Voltage Differential	$V_{CT(PWRGD\ High)} - V_{CT(PWRGD\ Low)}$			1.67		V
Ripple Rejection	V_{IN} = 7V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 50mA		65	85		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0V V_{IN} = 4V, ΔV_{OUT} = –0.1V (Note 2)	 ●	 60	140		mA mA
Input Reverse Leakage Current	V_{IN} = –80V, V_{OUT} = 0V	●			6	mA
Reverse Output Current (Note 9)	V_{OUT} = 1.24V, V_{IN} < 1.24V (Note 2)			8	15	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3011 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 3: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 4: To satisfy requirements for minimum input voltage, the LT3011 is tested and specified for these conditions with an external resistor divider (249k bottom, 409k top) for an output voltage of 3.3V. The external resistor divider will add a 5µA DC load on the output.

Note 5: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to ($V_{IN} - V_{DROPOUT}$).

Note 6: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. This means the device is tested while operating close to its dropout region. This is the worst-case GND pin current. The GND pin current will decrease slightly at higher input voltages.

Note 7: ADJ pin bias current flows into the ADJ pin.

Note 8: $\overline{SHDN}$ pin current flows out of the $\overline{SHDN}$ pin.

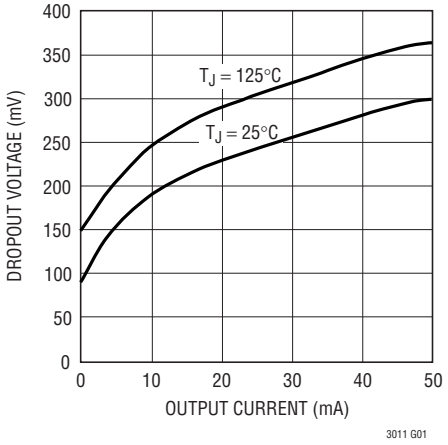
Note 9: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

Note 10: The LT3011 regulators are tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3011E regulators are 100% tested at T_A = 25°C. Performance of the LT3011E over the full –40°C to 125°C operating junction temperature range is assured by design, characterization and correlation with statistical process controls. The LT3011I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3011H is tested to the LT3011H Electrical Characteristics table at 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

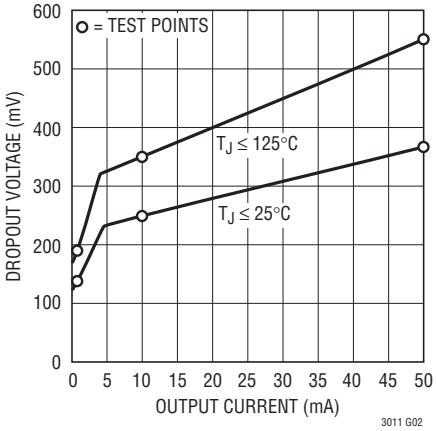
Note 11: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C (LT3011E/LT3011I) or 150°C (LT3011H) when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

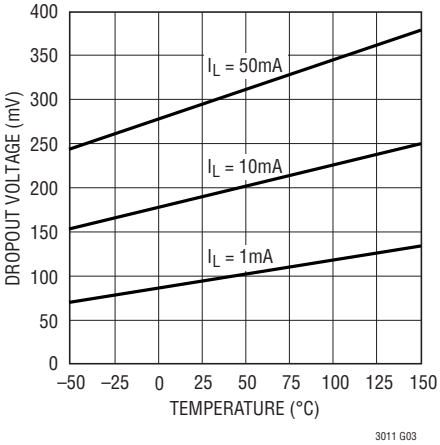
Dropout Voltage



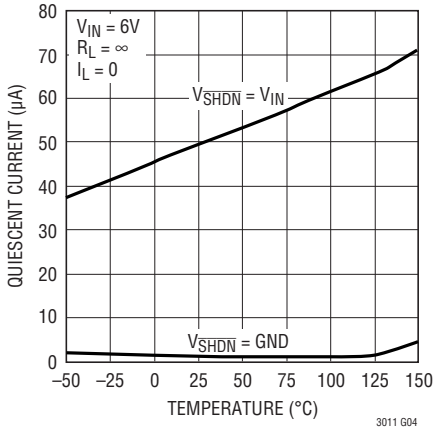
Guaranteed Dropout Voltage



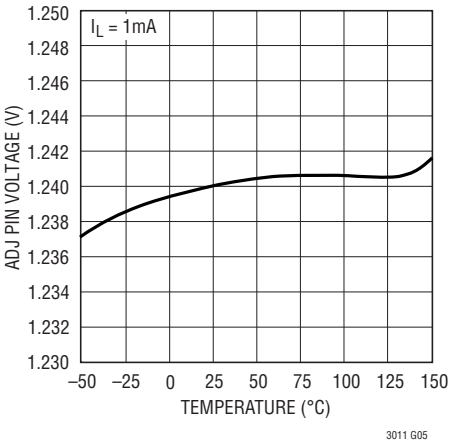
Dropout Voltage



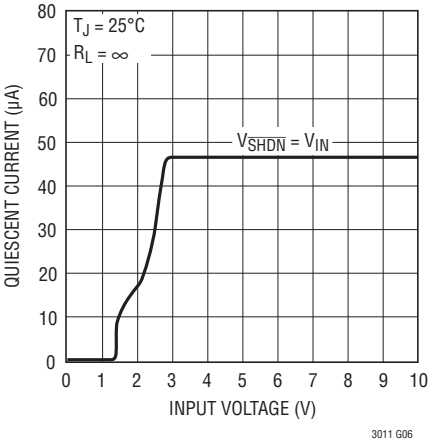
Quiescent Current



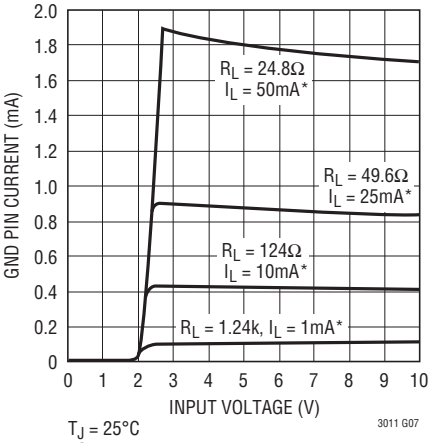
ADJ Pin Voltage



Quiescent Current

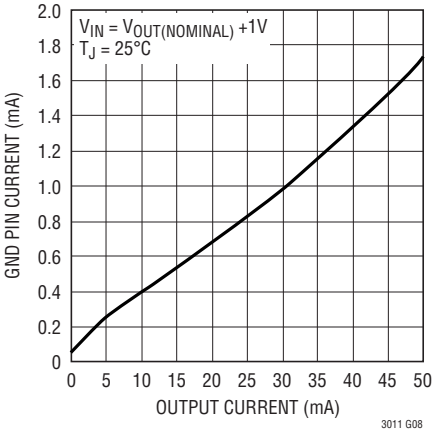


GND Pin Current

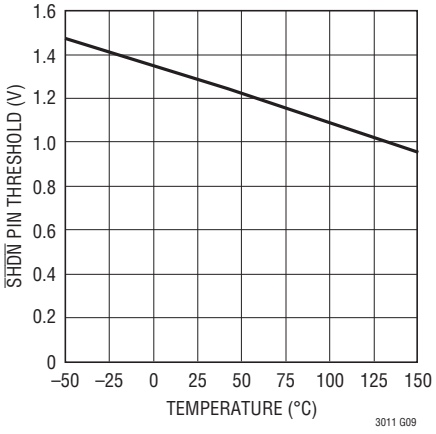


TJ = 25°C
*FOR V_{OUT} = 1.24V

GND Pin Current vs I_{OUT}

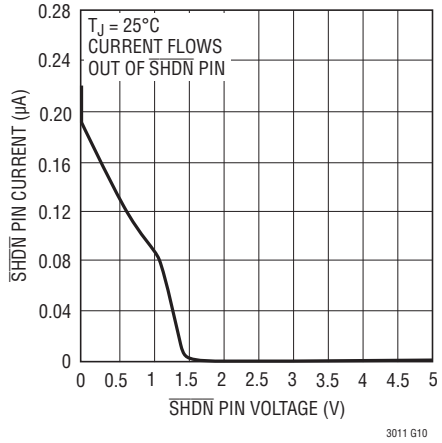


$\overline{SHDN}$ Pin Threshold

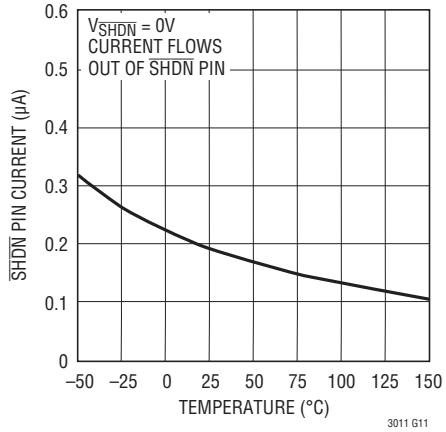


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

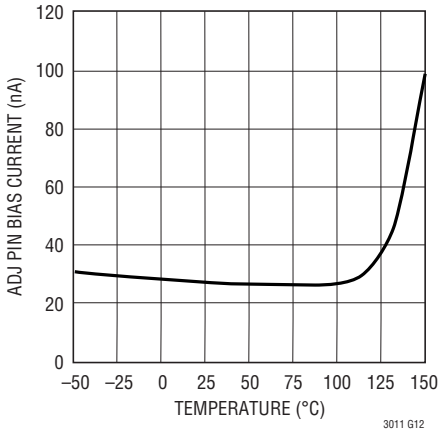
$\overline{SHDN}$ Pin Current



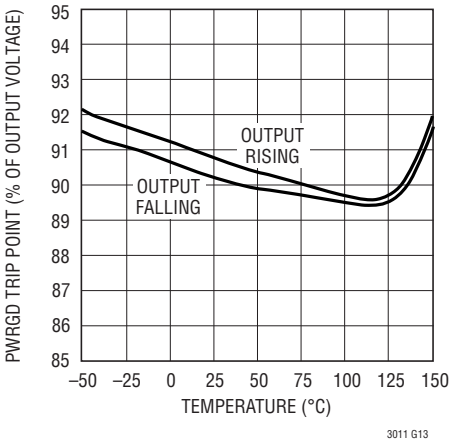
$\overline{SHDN}$ Pin Current



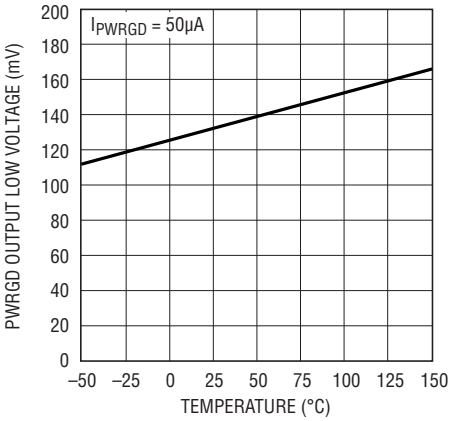
ADJ Pin Bias Current



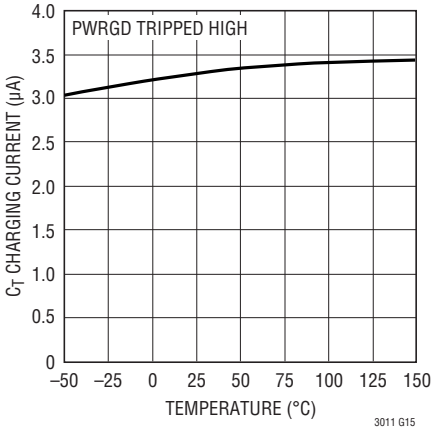
PWRGD Trip Point



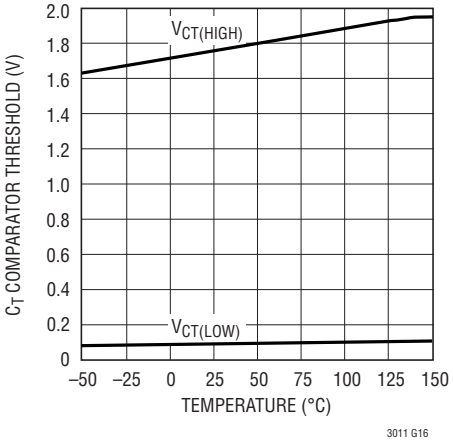
PWRGD Output Low Voltage



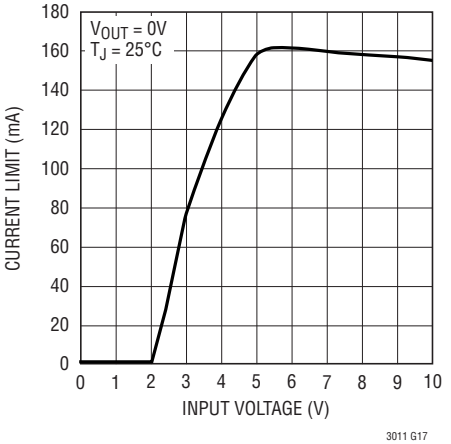
C_T Charging Current



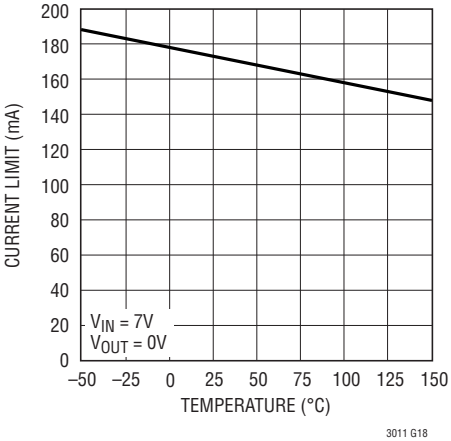
C_T Comparator Threshold



Current Limit

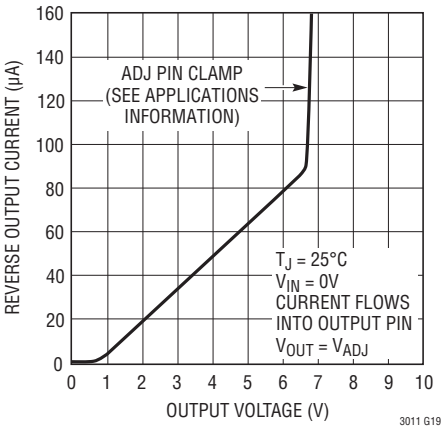


Current Limit

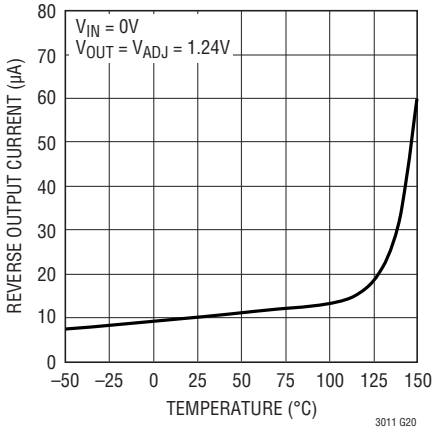


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

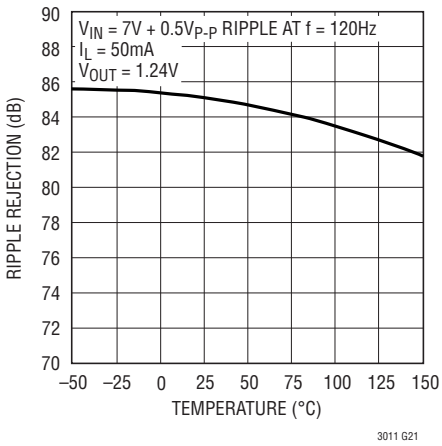
Reverse Output Current



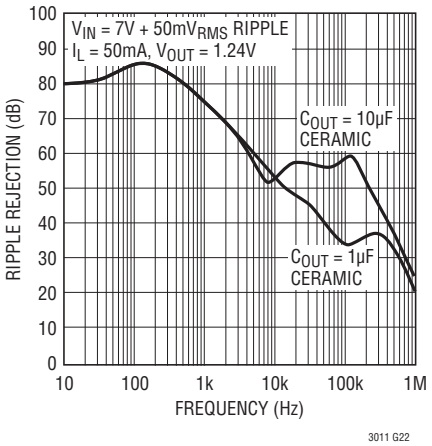
Reverse Output Current



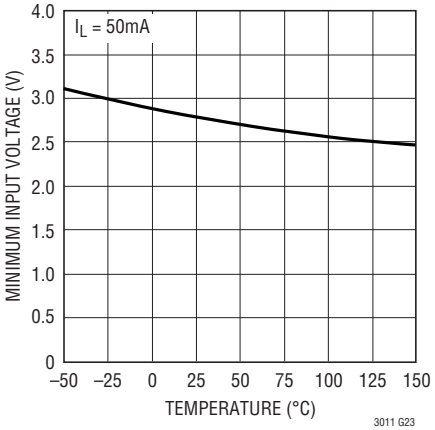
Input Ripple Rejection



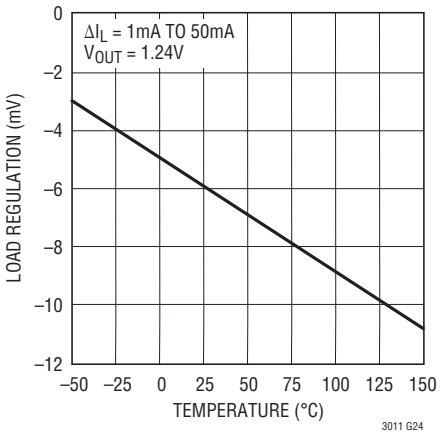
Input Ripple Rejection



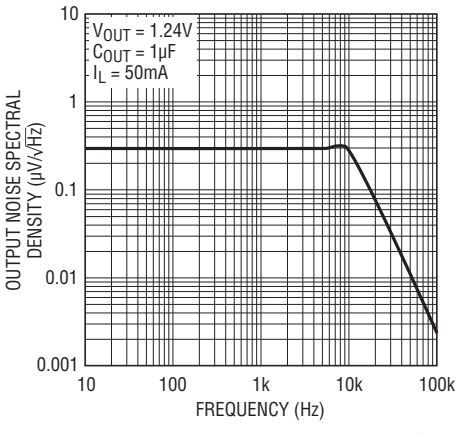
Minimum Input Voltage



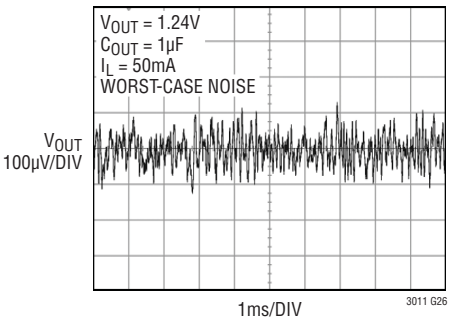
Load Regulation



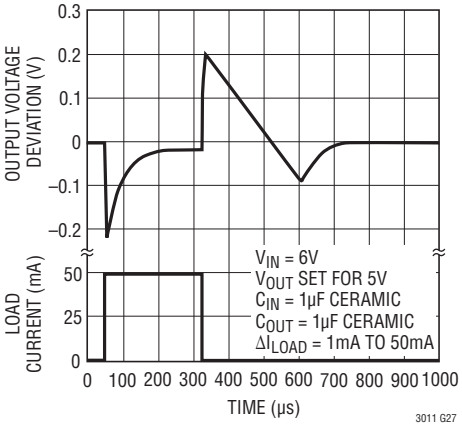
Output Noise Spectral Density



Output Noise (10Hz to 100kHz)



Transient Response



PIN FUNCTIONS (DFN/MSOP)

OUT (Pin 1/Pin 2): Output. The output supplies power to the load. A minimum output capacitor of 1µF is required to prevent oscillations. Larger capacitors will be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

ADJ (Pin 2/Pin 3): Adjust. This is the input to the error amplifier. This pin is internally clamped to ±7V. It has a bias current of 30nA which flows into the pin (see the curve labeled ADJ Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ pin voltage is 1.24V referenced to ground, and the output voltage range is 1.24V to 60V.

GND (Pins 3, 11/Pins 4, 13): Ground. The exposed backside of the package (Pin 11/Pin 13) is an electrical connection for GND. As such, to ensure optimum device operation and thermal performance, the Exposed Pad must be connected directly to Pin 3/Pin 4 on the PC board.

NC (Pins 4, 7, 9/Pins 1, 5, 8, 10, 12): No Connection. These pins have no internal connection. Connecting NC pins to a copper area for heat dissipation provides a small improvement in thermal performance.

PWRGD (Pin 5/Pin 6): Power Good. The PWRGD flag is an open-collector flag to indicate that the output voltage has increased above 90% of the nominal output voltage. There is no internal pull-up on this pin; a pull-up resistor must be used. The PWRGD pin will change state from an open-collector pull-down to high impedance after both the output is above 90% of the nominal voltage and the capacitor on the C_T pin has charged through a 1.67V differential. The maximum pull-down current of the PWRGD pin in the low state is 50µA.

C_T (Pin 6/Pin 7): Timing Capacitor. The C_T pin allows the use of a small capacitor to delay the timing between the point where the output crosses the PWRGD threshold and the PWRGD flag changes to a high impedance state. Current out of this pin during the charging phase is 3µA. The voltage difference between the PWRGD low and PWRGD high states is 1.67V (see the Applications Information section).

$\overline{SHDN}$ (Pin 8/Pin 9): Shutdown. The $\overline{SHDN}$ pin is used to put the LT3011 into a low power shutdown state. The output will be off when the $\overline{SHDN}$ pin is pulled low. The $\overline{SHDN}$ pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is only required to supply the pull-up current of the open-collector gate, normally several microamperes. If unused, the $\overline{SHDN}$ pin must be tied to a logic high or V_{IN}.

IN (Pin 10/Pin 11): Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The LT3011 is designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input voltage, which can occur if a battery is plugged in backwards, the LT3011 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT3011 and no reverse voltage will appear at the load. The device will protect both itself and the load.

Exposed Pad (Pin 11/Pin 13): Ground. The Exposed Pad must be soldered to the PCB.

APPLICATIONS INFORMATION

The LT3011 is a 50mA high voltage/low dropout regulator with micropower quiescent current and shutdown. The device is capable of supplying 50mA at a dropout voltage of 300mV. The low operating quiescent current (46µA) drops to 1µA in shutdown. In addition to low quiescent current, the LT3011 incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT3011 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The LT3011 has an output voltage range of 1.24V to 60V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output to maintain the voltage at the adjust pin at 1.24V referenced to ground. The current in R1 is then equal to 1.24V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in Figure 1. The value of R1 should be less than 250k to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. The adjustable device is tested and specified with the ADJ pin tied to the OUT pin and a 5µA DC load (unless otherwise specified) for an output voltage of 1.24V. Specifications for output voltages greater than 1.24V will be proportional to the ratio of the desired output voltage to 1.24V; (V_{OUT}/1.24V). For example, load regulation for an output current change of 1mA to 50mA is –6mV (typical) at V_{OUT} = 1.24V. At V_{OUT} = 12V, load regulation is:

$$\frac{12V}{1.24V} \bullet -6mV = -58mV$$

Output Capacitance and Transient Response

The LT3011 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 1µF with an ESR of 3Ω or less is recommended to prevent oscillations. The LT3011 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3011, will increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances

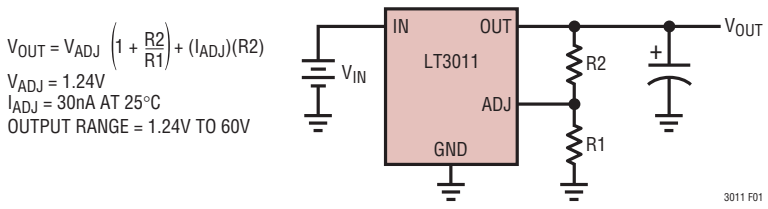


Figure 1. Adjustable Operation

APPLICATIONS INFORMATION

in a small package, but they tend to have strong voltage and temperature coefficients, as shown in Figures 2 and 3. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

PWRGD Flag and Timing Capacitor Delay

The PWRGD flag is used to indicate that the ADJ pin voltage is within 10% of the regulated voltage. The PWRGD pin is an open-collector output, capable of sinking 50µA of current when the ADJ pin voltage is low. There is no internal pull-up on the PWRGD pin; an external pull-up resistor must be used. When the ADJ pin rises to within 10% of its final reference value, a delay timer is started. At the end of this delay, programmed by the value of the capacitor on the C_T pin, the PWRGD pin switches to a high impedance and is pulled up to a logic level by an external pull-up resistor.

To calculate the capacitor value on the C_T pin, use the following formula:

$$C_{TIME} = \frac{I_{CT} \bullet t_{DELAY}}{V_{CT(HIGH)} - V_{CT(LOW)}}$$

Figure 4 shows a block diagram of the PWRGD circuit. At start-up, the timing capacitor is discharged and the PWRGD pin will be held low. As the output voltage increases and the ADJ pin crosses the 90% threshold, the JK flipflop is reset, and the 3µA current source begins to charge the timing capacitor. Once the voltage on the C_T pin reaches the $V_{CT(HIGH)}$ threshold (approximately 1.7V at 25°C), the capacitor voltage is clamped and the PWRGD pin is set to a high impedance state.

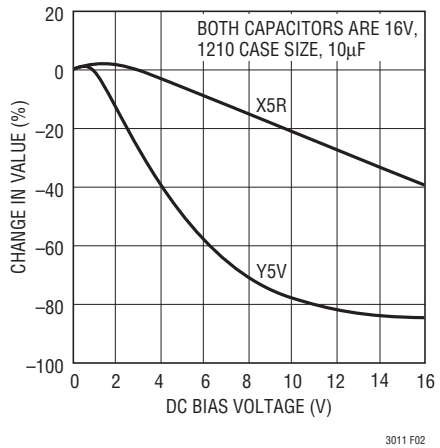


Figure 2. Ceramic Capacitor DC Bias Characteristics

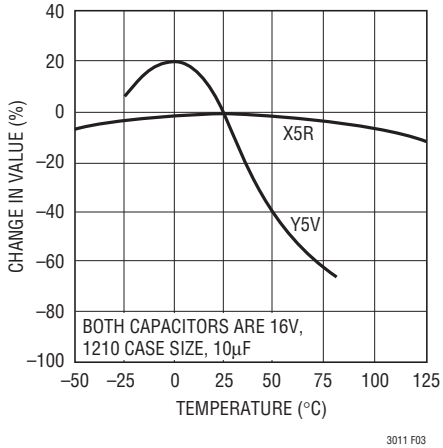


Figure 3. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

During normal operation, an internal glitch filter will ignore short transients (<15µs). Longer transients below the 90% threshold will reset the JK flip-flop. This flip-flop ensures that the capacitor on the C_T pin is quickly discharged all the way to the $V_{CT(LOW)}$ threshold before restarting the time delay. This provides a consistent time delay after the ADJ pin is within 10% of the regulated voltage before the PWRGD pin switches to high impedance.

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C, LT3011E/ LT3011I or 150°C, LT3011H). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \bullet (V_{IN} – V_{OUT})$ and,
2. GND pin current multiplied by the input voltage: $I_{GND} \bullet V_{IN}$

The GND pin current is found by examining the GND pin current curves in the Typical Performance Characteristics section. Power dissipation will be equal to the sum of the two components listed above.

The LT3011 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C (LT3011E/ LT3011I) or 150°C (LT3011H) must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

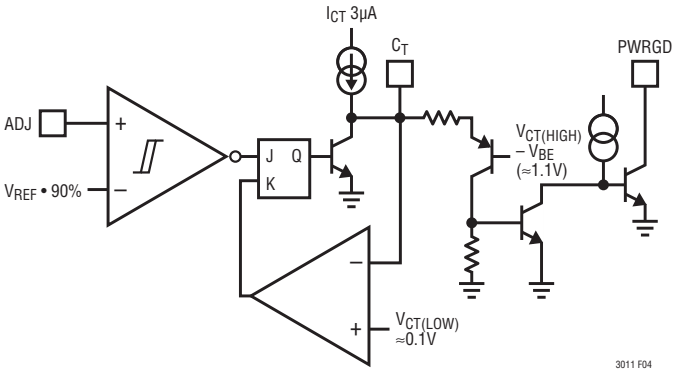


Figure 4. PWRGD Circuit Block Diagram

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. MSOP Measured Thermal Resistance

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE	BACKSIDE		
2500 sq mm	2500 sq mm	2500 sq mm	52°C/W
1000 sq mm	2500 sq mm	2500 sq mm	54°C/W
225 sq mm	2500 sq mm	2500 sq mm	58°C/W
100 sq mm	2500 sq mm	2500 sq mm	64°C/W

Table 2. DFN Measured Thermal Resistance

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE	BACKSIDE		
2500 sq mm	2500 sq mm	2500 sq mm	52°C/W
1000 sq mm	2500 sq mm	2500 sq mm	54°C/W
225 sq mm	2500 sq mm	2500 sq mm	58°C/W
100 sq mm	2500 sq mm	2500 sq mm	64°C/W

The thermal resistance junction-to-case (θ_{JC}), measured at the Exposed Pad on the back of the die, is 16°C/W. Continuous operation at large input/output voltage differentials and maximum load current is not practical due to thermal limitations. Transient operation at high input/ output differentials is possible. The approximate thermal time-constant for a 2500sq mm 3/32" FR-4 board, with maximum topside and backside area for one ounce copper, is three seconds. This time-constant will increase as more thermal mass is added (i.e., vias, larger board and other components).

For an application with transient high power peaks, average power dissipation can be used for junction temperature calculations as long as the pulse period is significantly less than the thermal time constant of the device and board.

APPLICATIONS INFORMATION

Calculating Junction Temperature

Example 1: Given an output voltage of 5V, an input voltage range of 24V to 30V, an output current range of 0mA to 50mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + (I_{GND} \bullet V_{IN(MAX)})$

Where:

$I_{OUT(MAX)} = 50mA$

$V_{IN(MAX)} = 30V$

I_{GND} at ($I_{OUT} = 50mA$, $V_{IN} = 30V$) = 1mA

So:

$P = 50mA \bullet (30V - 5V) + (1mA \bullet 30V) = 1.28W$

The thermal resistance will be in the range of 52°C/W to 64°C/W depending on the copper area. So, the junction temperature rise above ambient will be approximately equal to:

$1.28W \bullet 58°C/W = 74°C$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$T_{JMAX} = 50°C + 74°C = 124°C$

Example 2: Given an output voltage of 5V, an input voltage of 48V that rises to 72V for 5ms (max) out of every 100ms, and a 5mA load that steps to 50mA for 50ms out of every 250ms, what is the junction temperature rise above ambient? Using a 500ms period (well under the time-constant of the board), power dissipation is as follow:

P1 ($48V_{IN}$, 5mA load) = 5mA • (48V – 5V) + (200µA • 48V) = 0.23W

P2 ($48V_{IN}$, 50mA load) = 50mA • (48V – 5V) + (1mA • 48V) = 2.20W

P3 ($72V_{IN}$, 5mA load) = 5mA (72V – 5V) + (200µA • 72V) = 0.35W

P1 ($72V_{IN}$, 50mA load) = 50mA (72V – 5V) + (1mA • 72V) = 3.42W

Operation at the different power levels is as follows:

76% operation at P1, 19% for P2, 4% for P3, and 1% for P4.

P_{EFF} = 76%(0.23W) + 19%(2.20W) + 4%(0.35W) + 1%(3.42W) = 0.64W

With a thermal resistance in the range of 52°C/W to 64°C/W, this translates to a junction temperature rise above ambient of 33°C to 41°C.

High Temperature Operation

Care must be taken when designing LT3011 applications to operate at high ambient temperatures. The LT3011 works at elevated temperatures but erratic operation can occur due to unforeseen variations in external components. Some tantalum capacitors are available for high temperature operation, but ESR is often several ohms; capacitor ESR above 3Ω is unsuitable for use with the LT3011. Ceramic capacitor manufacturers (Murata, AVX, TDK and Vishay Vitramon at this writing) now offer ceramic capacitors that are rated to 150°C using an X8R dielectric. Device instability will occur if the output capacitor value and ESR are outside design limits at elevated temperature and operating DC voltage bias (see information on capacitor characteristics under Output Capacitance and Transient Response). Check each passive component for absolute value and voltage ratings over the operating temperature range.

Leakage in capacitors, or from solder flux left after insufficient board cleaning, adversely affects the low quiescent current operation. Consider junction temperature increase due to power dissipation in both the junction and nearby components to ensure maximum specifications are not violated for the LT3011E/LT3011H/LT3011I or external components.

Protection Features

The LT3011 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse-input voltages, and reverse voltages from output-to-input.

APPLICATIONS INFORMATION

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C (LT3011E/LT3011I) or 150°C (LT3011H).

The input of the device will withstand reverse voltages of 80V. Current flow into the device will be limited to less than 6mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries which can be plugged in backwards.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open-circuit or grounded, the ADJ pin will act like an open-circuit when pulled below ground, and like a large resistor (typically 100k) in series with a diode when pulled above ground. If the input is powered by a voltage source, pulling the ADJ pin below the reference voltage will cause the device to try and force the current limit out of the output. This will cause the output to go to an unregulated high voltage. Pulling the ADJ pin above the reference voltage will turn off all output current.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.24V reference when the output is forced to 60V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 7V. The 53V difference between the OUT and ADJ pin is divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 10.6k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open-circuit. Current flow back into the output will follow the curve shown in Figure 5. The rise in reverse output current above 7V occurs from the breakdown of the 7V clamp on the ADJ pin. With a resistor divider on the regulator output, this current will be reduced depending on the size of the resistor divider.

When the IN pin of the LT3011 is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current will typically drop to less than 2µA. This can happen if the input of the LT3011 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{\text{SHDN}}$ pin will have no effect on the reverse output current when the output is pulled above the input.

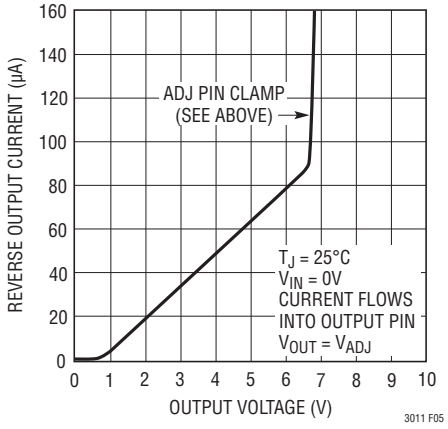
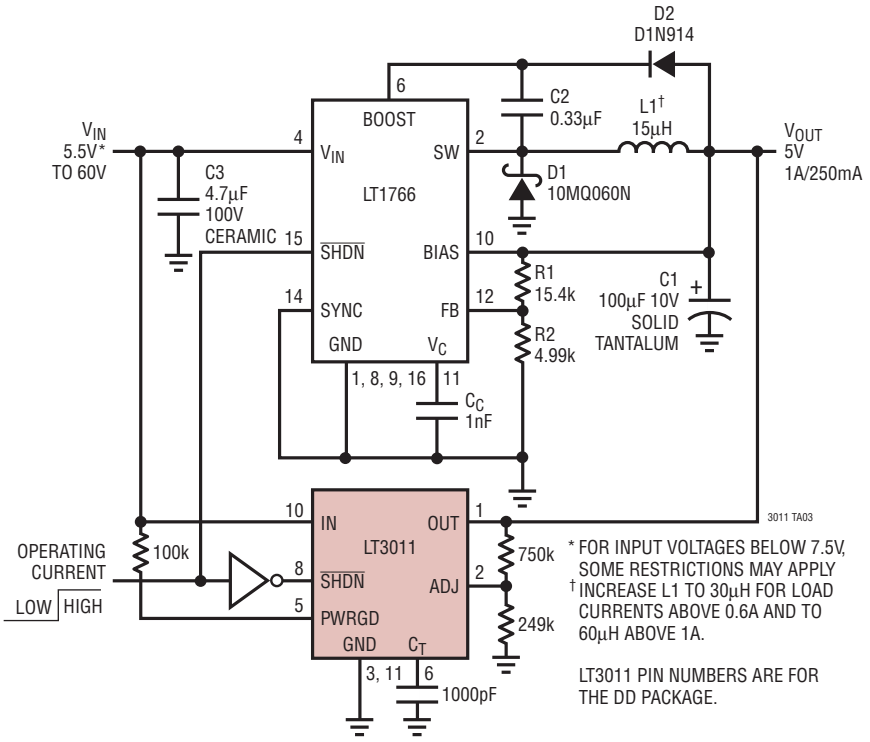


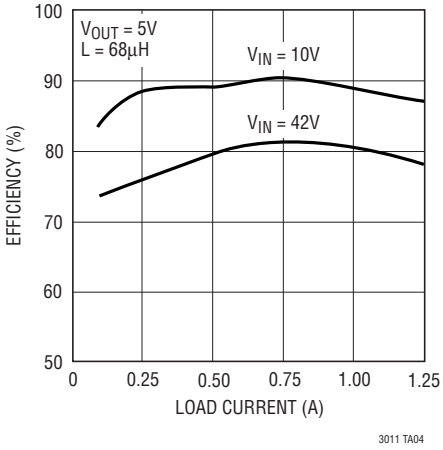
Figure 5. Reverse Output Current

TYPICAL APPLICATIONS

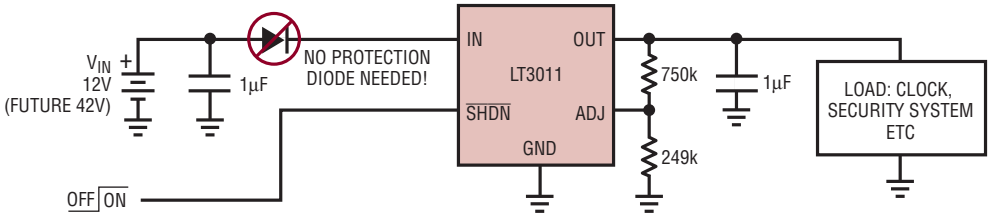
5V Buck Converter with Low Current Keep Alive Backup



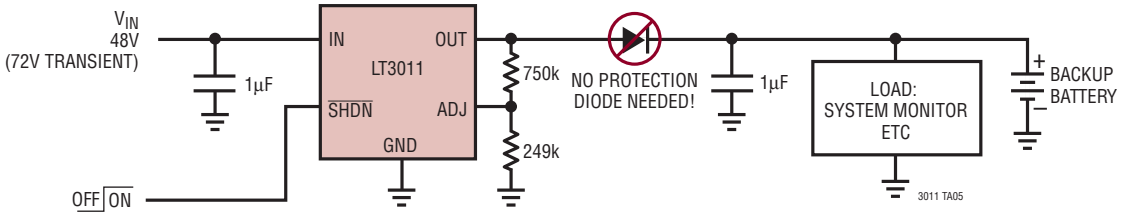
Buck Converter Efficiency vs Load Current



LT3011 Automotive Application

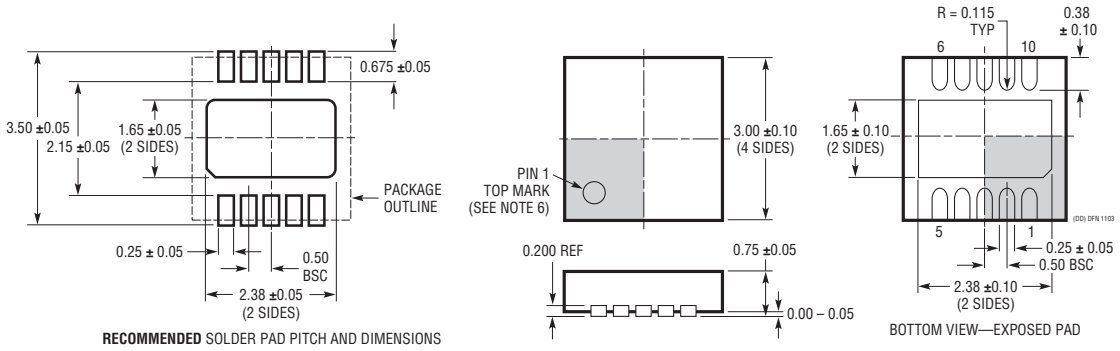


LT3011 Telecom Application



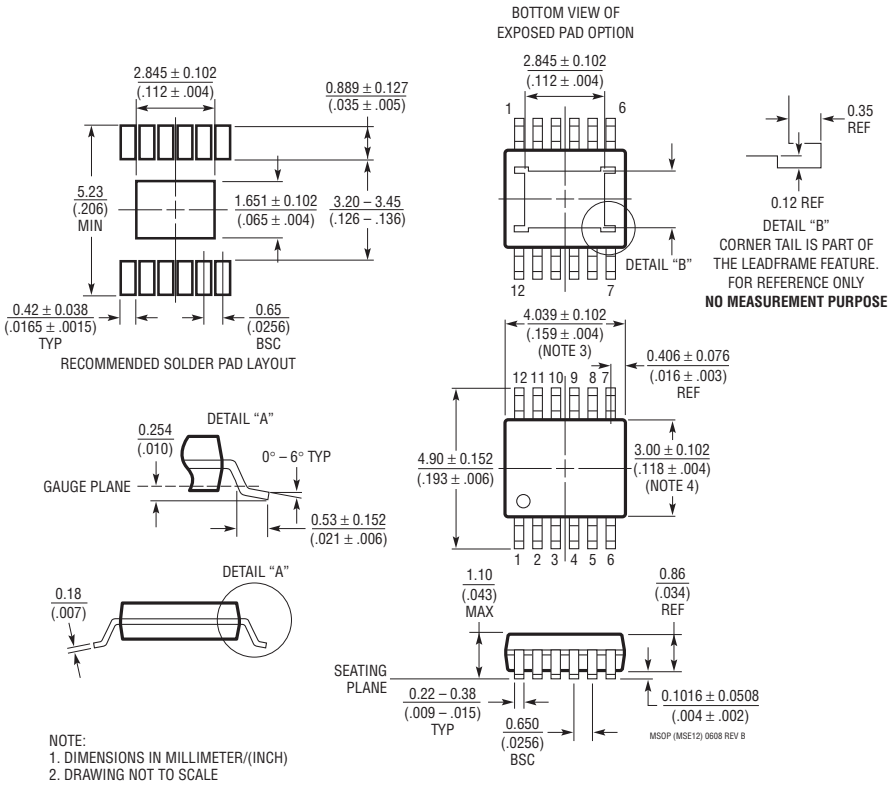
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

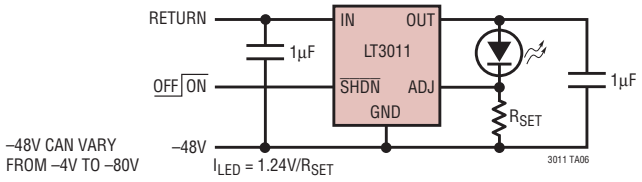
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev B)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Constant Brightness for Indicator LED over Wide Input Voltage Range



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1121/ LT1121HV	150mA, Micropower, LDO	V_{IN}: 4.2V to 30V/36V, $V_{OUT(MIN)}$ = 3.75V, V_{DO} = 0.42V, I_Q = 30µA, I_{SD} = 16µA, Reverse Battery Protection, SOT-223, S8 and Z Packages
LT1676	60V, 440mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 60V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} = 2.5µA, S8 Package
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 20µA, I_{SD} <1µA, Low Noise < 20µV_{RMS}, Stable with 1µF Ceramic Capacitors, ThinSOT™ Package
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 25µA, I_{SD} <1µA, Low Noise < 20µV_{RMS}, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} <1µA, Low Noise < 20µV_{RMS}, S8 Package
LT1764/ LT1764A	3A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} <1µA, Low Noise < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors, DD and TO220-5 Packages
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP-16/E Package
LT1776	40V, 550mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} = 30µA, N8 and S8 Packages
LT1956	60V, 1.2A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP-16/E Package
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.27V, I_Q = 30µA, I_{SD} <1µA, Low Noise < 20µV_{RMS}, MS8 Package
LT1963/ LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} <1µA, Low Noise < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors, DD, TO220-5, SOT-223 and S8 Packages
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	310mV Dropout Voltage, Low Noise = 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DDPak, MSOP and 3mm × 3mm DFN Packages
LT3009	20mA, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q = 3µA, V_{IN}: 1.6V to 20V, ThinSOT and SC-70 Packages
LT3010/ LT3010H	50mA, 3V to 80V, Low Noise Micropower LDO	V_{IN}: 3V to 8V, $V_{OUT(MIN)}$ = 1.275V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} = 1µA, Low Noise < 100µV_{RMS}, MS8E Package, H Grade = +140°C T_{JMAX}
LT3012/ LT3012H	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 40µA, I_{SD} <1µA, TSSOP-16E and 4mm × 3mm DFN-12 Packages, H Grade = +140°C T_{JMAX}
LT3013/ LT3013H	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 65µA, I_{SD} <1µA, TSSOP-16E and 4mm × 3mm DFN-12 Packages, H Grade = +140°C T_{JMAX}, PWRGD Flag
LT3014/HV	20mA, 3V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 3V to 80V (100V for 2ms, HV Version), V_{OUT}: 1.22V to 60V, V_{DO} = 0.35V, I_Q = 7µA, I_{SD} <1µA, ThinSOT and 3mm × 3mm DFN-8 Packages
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise = 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with One Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, TO-220, SOT-223, MSOP and 3mm × 3mm DFN Packages; LT3080-1 Features an Integrated Ballast Resistor

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