# THE DATASHEET OF

# SN75C3222EDWR

www.win-source.net 0086-755-83957316

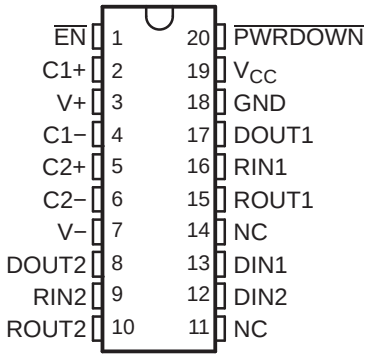
# SN65C3222E, SN75C3222E
# 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVERS/RECEIVERS WITH ±15-kV ESD PROTECTION

SLLS725A – JUNE 2006 – REVISED JULY 2006

## FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2, Contact Discharge**
  - **±15-kV IEC 61000-4-2, Air-Gap Discharge**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operate With 3-V to 5.5-V $V_{CC}$ Supply**
- **Operate up to 1000 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Standby Current . . . 1 μA Typ**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accepts 5-V Logic Input With 3.3-V Supply**

**DB, DW, OR PW PACKAGE**
**(TOP VIEW)**

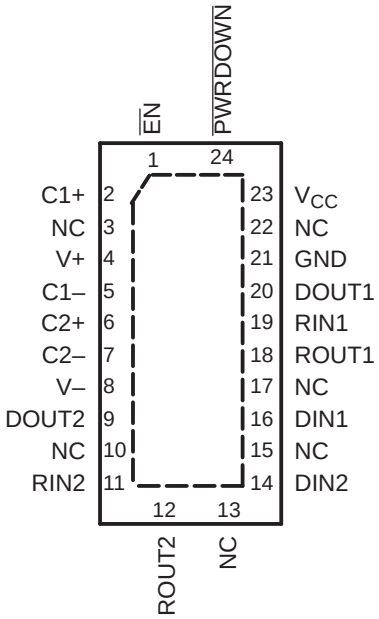



NC − No internal connection

## APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

**RHL PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## DESCRIPTION/ ORDERING INFORMATION

The SN65C3222E and SN75C3222E consist of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND).

The devices meet the requirements of TIA/EIA-232-F and provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at typical data signaling rates up to 1000 kbit/s and are improved drop-in replacements for industry-popular '3222 two-driver, two-receiver functions.

The SN65C3222E and SN75C3222E can be placed in the power-down mode by setting the power-down ($\overline{PWRDOWN}$) input low, which draws only 1 μA from the power supply. When the devices are powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V+ is lowered to $V_{CC}$, and V– is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ($\overline{EN}$) high.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | SOIC – DW | Tube of 25 | SN75C3222EDW | 75C3222E |
| | | Reel of 2000 | SN75C3222EDWR | |
| | SSOP – DB | Tube of 70 | SN75C3222EDB | MY222E |
| | | Reel of 2000 | SN75C3222EDBR | |
| | TSSOP – PW | Tube of 70 | SN75C3222EPW | MY222E |
| | | Reel of 2000 | SN75C3222EPWR | |
| –40°C to 85°C | SOIC – DW | Tube of 25 | SN65C3222EDW | 65C3222E |
| | | Reel of 2000 | SN65C3222EDWR | |
| | SSOP – DB | Tube of 70 | SN65C3222EDB | MU222E |
| | | Reel of 2000 | SN65C3222EDBR | |
| | TSSOP – PW | Tube of 70 | SN65C3222EPW | MU222E |
| | | Reel of 2000 | SN65C3222EPWR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLES

### Each Driver(1)

| INPUTS | | OUTPUT DOUT |
|---|---|---|
| DIN | $\overline{\text{PWRDOWN}}$ | |
| X | L | Z |
| L | H | H |
| H | H | L |

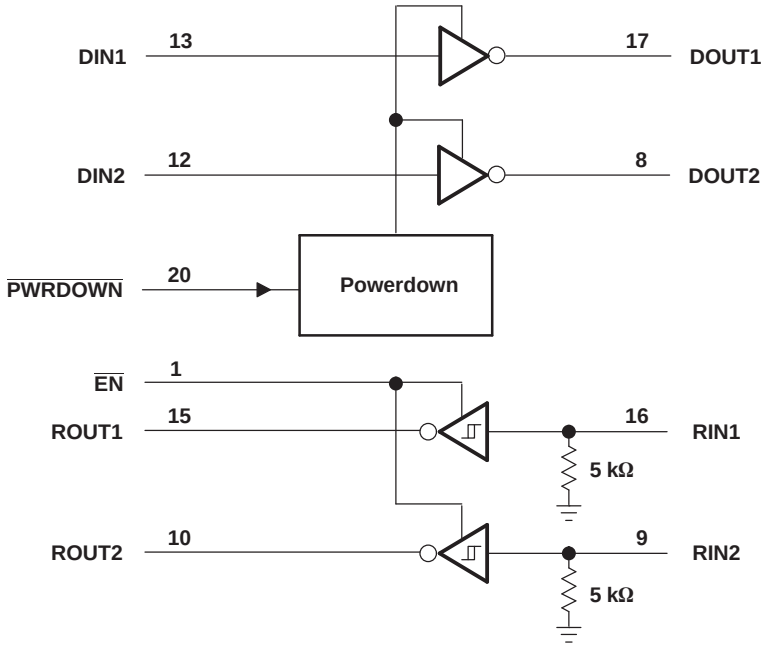
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

### Each Receiver(1)

| INPUTS | | OUTPUT ROUT |
|---|---|---|
| RIN | $\overline{\text{EN}}$ | |
| L | L | H |
| H | L | L |
| X | H | Z |
| Open | L | H |

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

### LOGIC DIAGRAM (POSITIVE LOGIC)




Pin numbers are for the DB, DW, and PW packages.

## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | | –0.3 | 6 | V |
| V+ | Positive-output supply voltage range(2) | | –0.3 | 7 | V |
| V– | Negative-output supply voltage range(2) | | 0.3 | –7 | V |
| V+ – V– | Supply voltage difference(2) | | | 13 | V |
| $V_I$ | Input voltage range | Driver ($\overline{EN}$, $\overline{PWRDOWN}$) | –0.3 | 6 | V |
| | | Receiver | –25 | 25 | |
| $V_O$ | Output voltage range | Driver | –13.2 | 13.2 | V |
| | | Receiver | –0.3 | $V_{CC}$ + 0.3 | |
| $\theta_{JA}$ | Package thermal impedance(3)(4) | DB package | | 70 | °C/W |
| | | DW package | | 58 | |
| | | PW package | | 83 | |
| | | RHL package | | TBD | |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions(1)

See Figure 5

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Supply voltage | | $V_{CC}$ = 3.3 V | 3 | 3.3 | 3.6 | V |
| | | | $V_{CC}$ = 5 V | 4.5 | 5 | 5.5 | |
| $V_{IH}$ | Driver and control high-level input voltage | DIN, $\overline{EN}$, $\overline{PWRDOWN}$ | $V_{CC}$ = 3.3 V | 2 | | | V |
| | | | $V_{CC}$ = 5 V | 2.4 | | | |
| $V_{IL}$ | Driver and control low-level input voltage | DIN, $\overline{EN}$, $\overline{PWRDOWN}$ | | | | 0.8 | V |
| $V_I$ | Driver and control input voltage | DIN, $\overline{EN}$, $\overline{PWRDOWN}$ | | 0 | | 5.5 | V |
| $V_I$ | Receiver input voltage | | | –25 | | 25 | V |
| $T_A$ | Operating free-air temperature | | SN75C3222E | 0 | | 70 | °C |
| | | | SN65C3222E | –40 | | 85 | |

(1) Test conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

## Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_I$ | Input leakage current ($\overline{EN}$, $\overline{PWRDOWN}$) | | | ±0.01 | ±1 | µA |
| $I_{CC}$ | Supply current | No load, $\overline{PWRDOWN}$ at $V_{CC}$ | | 0.3 | 1 | mA |
| | Supply current (powered off) | No load, $\overline{PWRDOWN}$ at GND | | 1 | 10 | µA |

(1) Test conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## DRIVER SECTION

### Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, | DIN = GND | 5 | 5.4 | | V |
| $V_{OL}$ | Low-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, | DIN = $V_{CC}$ | –5 | –5.4 | | V |
| $I_{IH}$ | High-level input current | $V_I$ = $V_{CC}$ | | | ±0.01 | ±1 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ at GND | | | ±0.01 | ±1 | µA |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = 3.6 V | $V_O$ = 0 V | | ±35 | ±60 | mA |
| | | $V_{CC}$ = 5.5 V | | | | | |
| $r_o$ | Output resistance | $V_{CC}$, V+, and V– = 0 V, | $V_O$ = ±2 V | 300 | 10M | | Ω |
| $I_{OZ}$ | Output leakage current | $\overline{\text{PWRDOWN}}$ = GND | $V_{CC}$ = 3 V to 3.6 V, $V_O$ = ±12 V | | | ±25 | µA |
| | | | $V_{CC}$ = 4.5 V to 5.5 V, $V_O$ = ±10 V | | | ±25 | |

(1) Test conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | Maximum data rate (See Figure 1) | $R_L$ = 3 kΩ, One DOUT switching | $C_L$ = 1000 pF | | 250 | | | kbit/s |
| | | | $C_L$ = 250 pF, | $V_{CC}$ = 3 V to 4.5 V | 1000 | | | |
| | | | $C_L$ = 1000 pF, | $V_{CC}$ = 4.5 V to 5.5 V | 1000 | | | |
| $t_{sk(p)}$ | Pulse skew[3] | $C_L$ = 150 pF to 2500 pF, | $R_L$ = 3 kΩ to 7 kΩ, | See Figure 2 | | 300 | | ns |
| SR(tr) | Slew rate, transition region (see Figure 1) | $R_L$ = 7 kΩ, | $C_L$ = 150 pF to 1000 pF | | 8 | | 90 | V/µs |
| | | $R_L$ = 3 kΩ | $C_L$ = 1000 pF | | 12 | | 60 | |
| | | | $C_L$ = 150 pF to 250 pF | | 24 | | 150 | |

(1) Test conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

## RECEIVER SECTION

### Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.1 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $V_{IT+}$ | Positive-going input threshold voltage | $V_{CC}$ = 3.3 V | | 1.5 | 2.4 | V |
| | | $V_{CC}$ = 5 V | | 1.8 | 2.4 | |
| $V_{IT–}$ | Negative-going input threshold voltage | $V_{CC}$ = 3.3 V | 0.6 | 1.2 | | V |
| | | $V_{CC}$ = 5 V | 0.8 | 1.5 | | |
| $V_{hys}$ | Input hysteresis ($V_{IT+} – V_{IT–}$) | | | 0.3 | | V |
| $I_{OZ}$ | Output leakage current | $\overline{EN}$ = 1 | | ±0.05 | ±10 | µA |
| $r_i$ | Input resistance | $V_I$ = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

(1) Test conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.

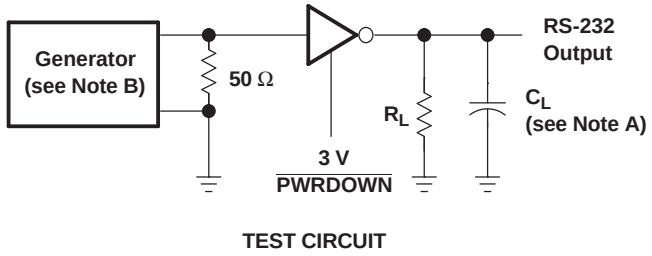
### Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

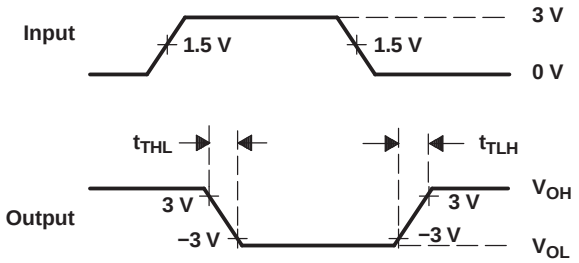
| PARAMETER | | TEST CONDITIONS | TYP(2) | UNIT |
|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 150 pF, See Figure 3 | 300 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | $C_L$ = 150 pF, See Figure 3 | 300 | ns |
| $t_{en}$ | Output enable time | $C_L$ = 150 pF, $R_L$ = 3 kΩ, See Figure 4 | 200 | ns |
| $t_{dis}$ | Output disable time | $C_L$ = 150 pF, $R_L$ = 3 kΩ, See Figure 4 | 200 | ns |
| $t_{sk(p)}$ | Pulse skew(3) | See Figure 3 | 300 | ns |

(1) Test conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT



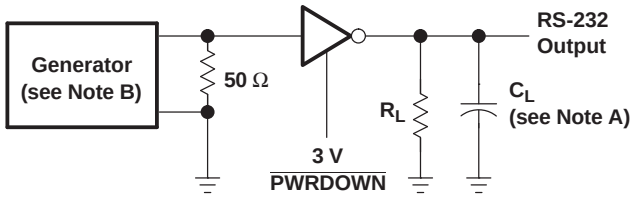

VOLTAGE WAVEFORMS

$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

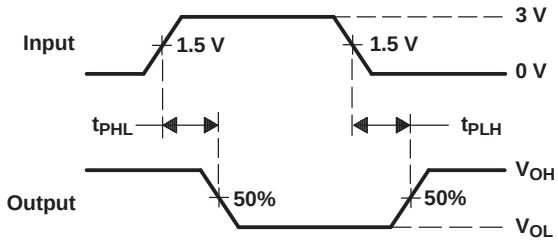
A. $C_L$ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 1. Driver Slew Rate**




TEST CIRCUIT

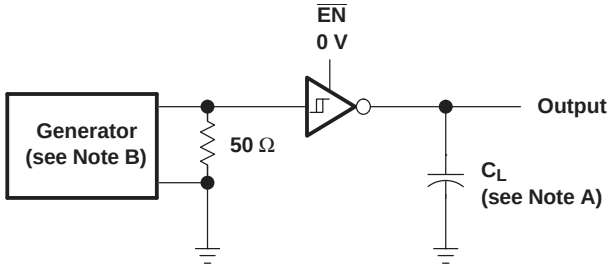



VOLTAGE WAVEFORMS

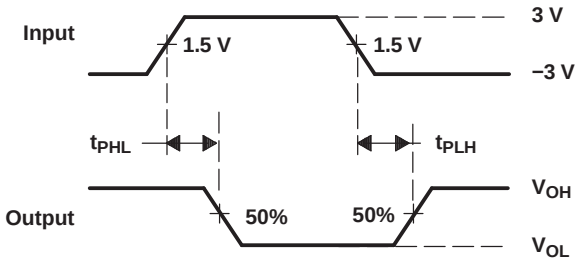
A. $C_L$ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 2. Driver Pulse Skew**




TEST CIRCUIT



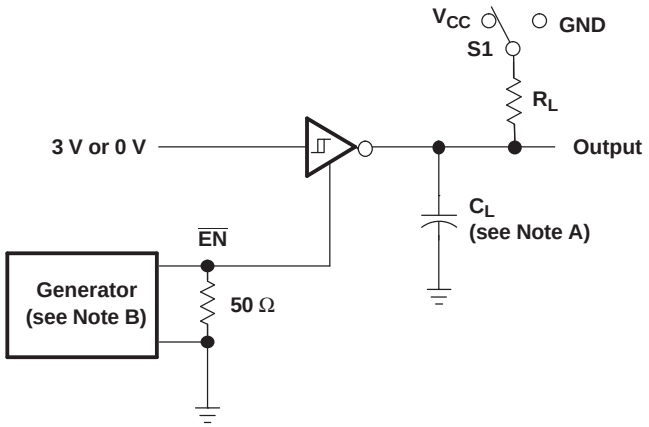

VOLTAGE WAVEFORMS

A. $C_L$ includes probe and jig capacitance.

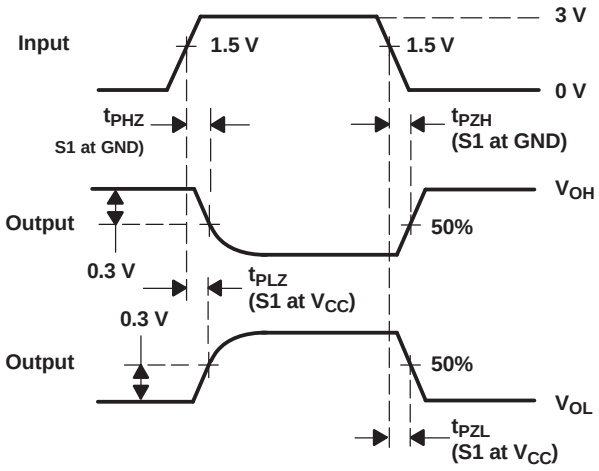
B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 3. Receiver Propagation Delay Times**

## PARAMETER MEASUREMENT INFORMATION (continued)




TEST CIRCUIT



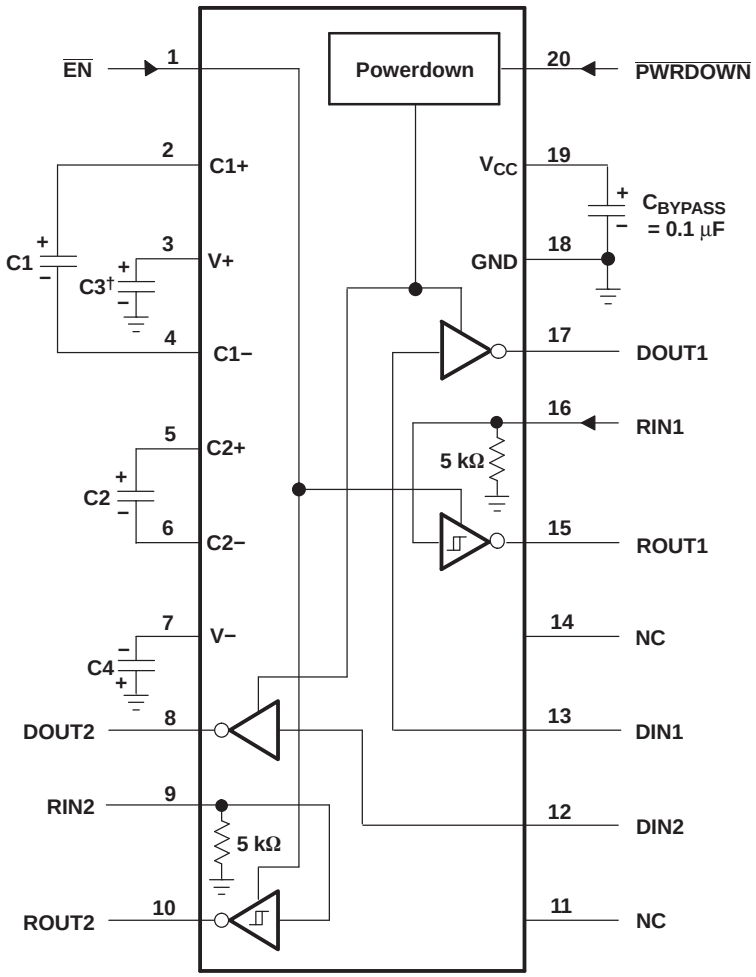

VOLTAGE WAVEFORMS

A. $C_L$ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 4. Receiver Enable and Disable Times**

## APPLICATION INFORMATION




† C3 can be connected to $V_{CC}$ or GND.

NOTES: A. Resistor values shown are nominal.
B. NC − No internal connection
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**$V_{CC}$ vs CAPACITOR VALUES**

| $V_{CC}$ | C1 | C2, C3, and C4 |
|---|---|---|
| 3.3 V ± 0.3 V | 0.1 µF | 0.1 µF |
| 5 V ± 0.5 V | 0.047 µF | 0.33 µF |
| 3 V to 5.5 V | 0.1 µF | 0.47 µF |

**Figure 5. Typical Operating Circuit and Capacitor Values**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65C3222EDB | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN65C3222EDBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN65C3222EDW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C3222E | Samples |
| SN65C3222EDWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C3222E | Samples |
| SN65C3222EPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN65C3222EPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN65C3222EPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN75C3222EPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | MY222E | Samples |
| SN75C3222EPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | MY222E | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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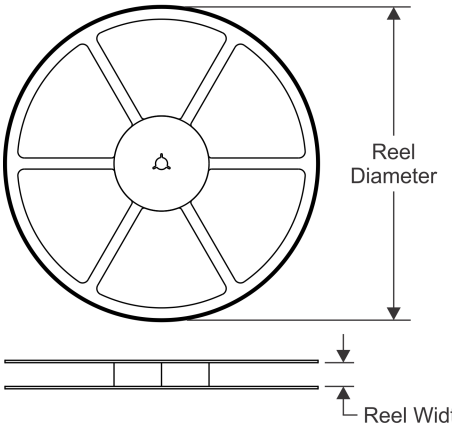
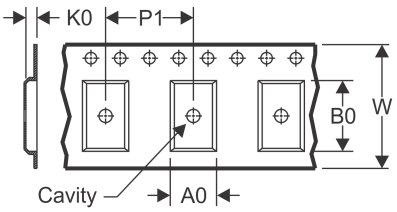
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

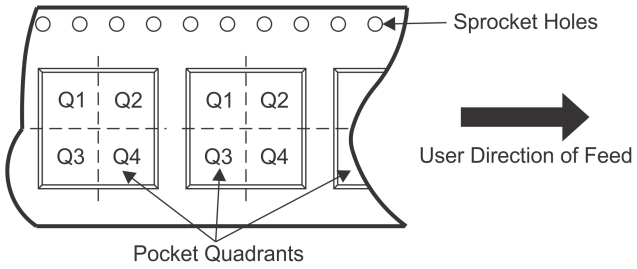



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

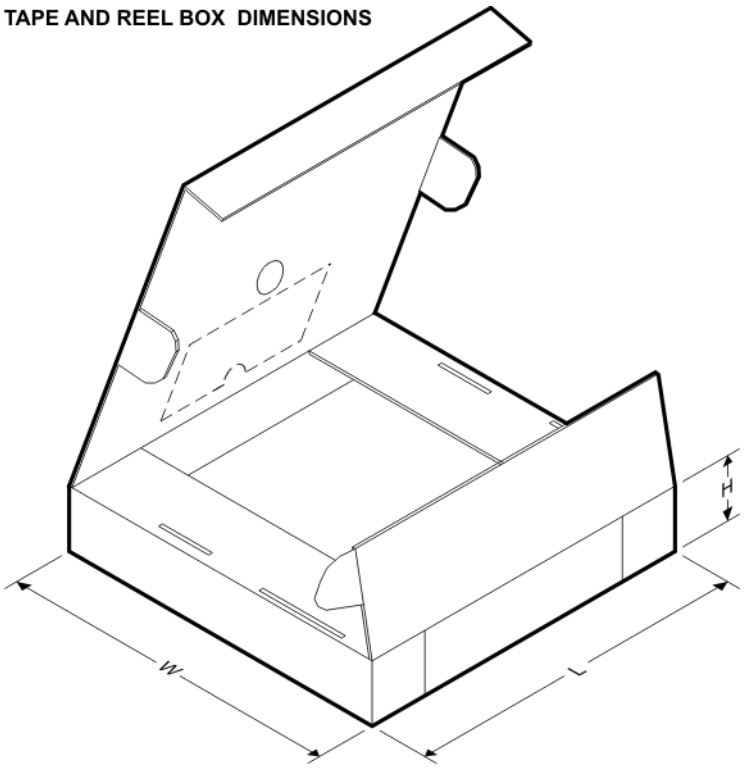
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65C3222EDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C3222EDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

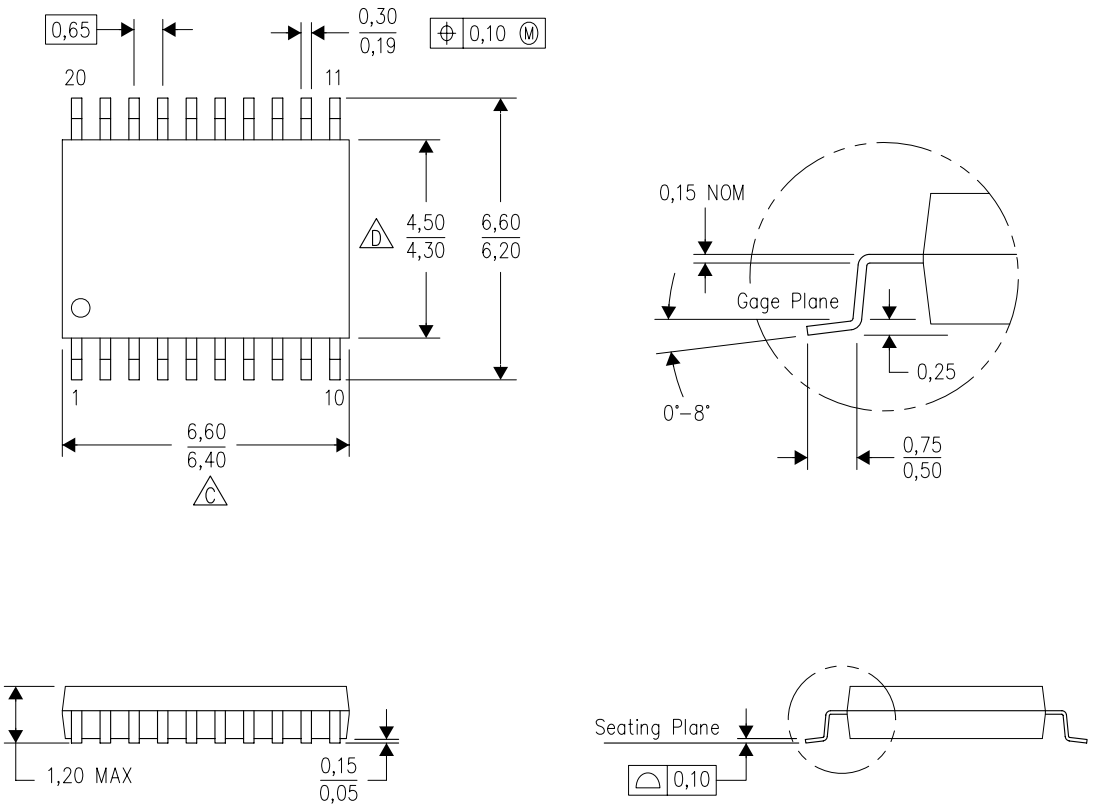
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65C3222EDBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN65C3222EDWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

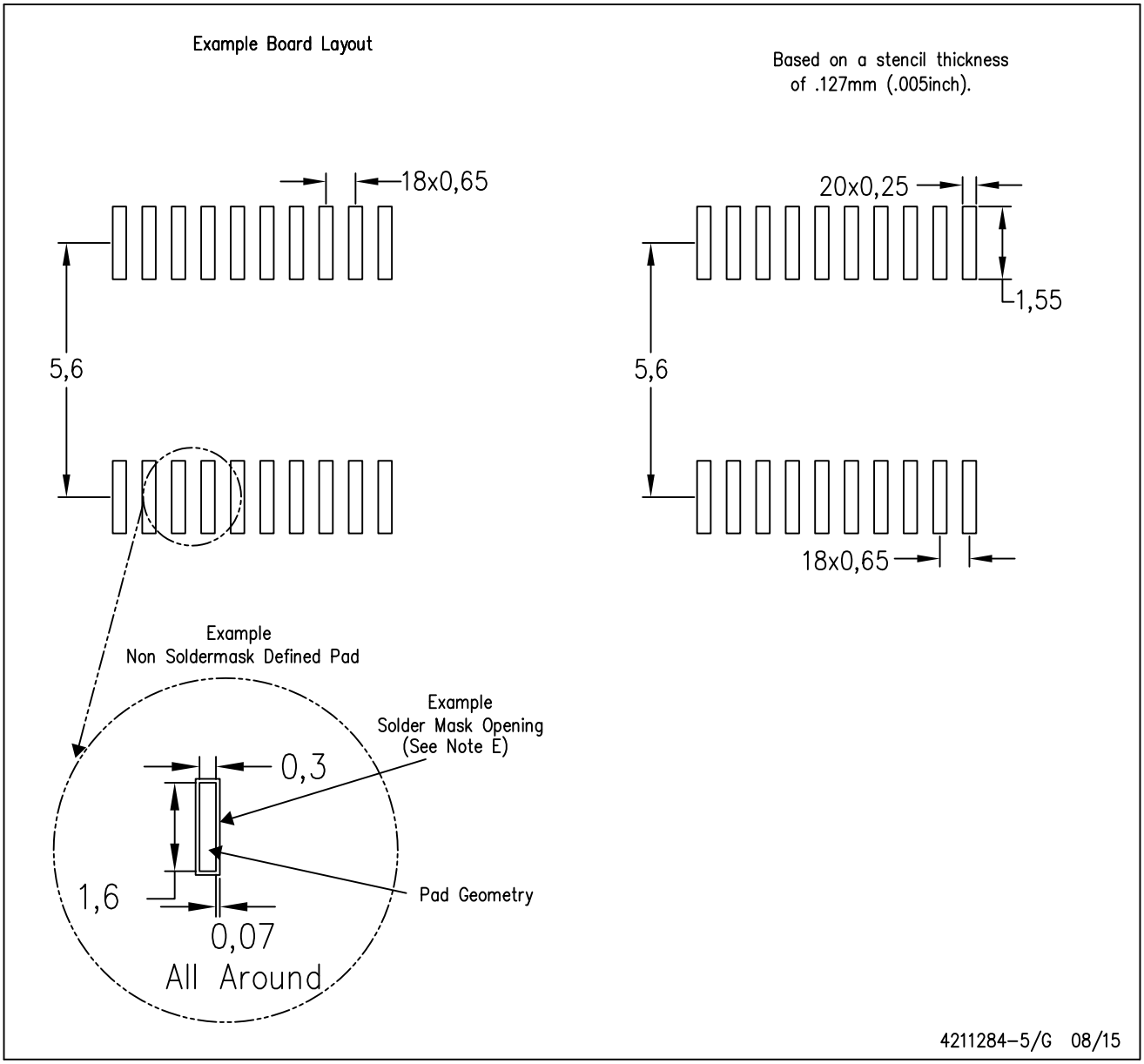
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



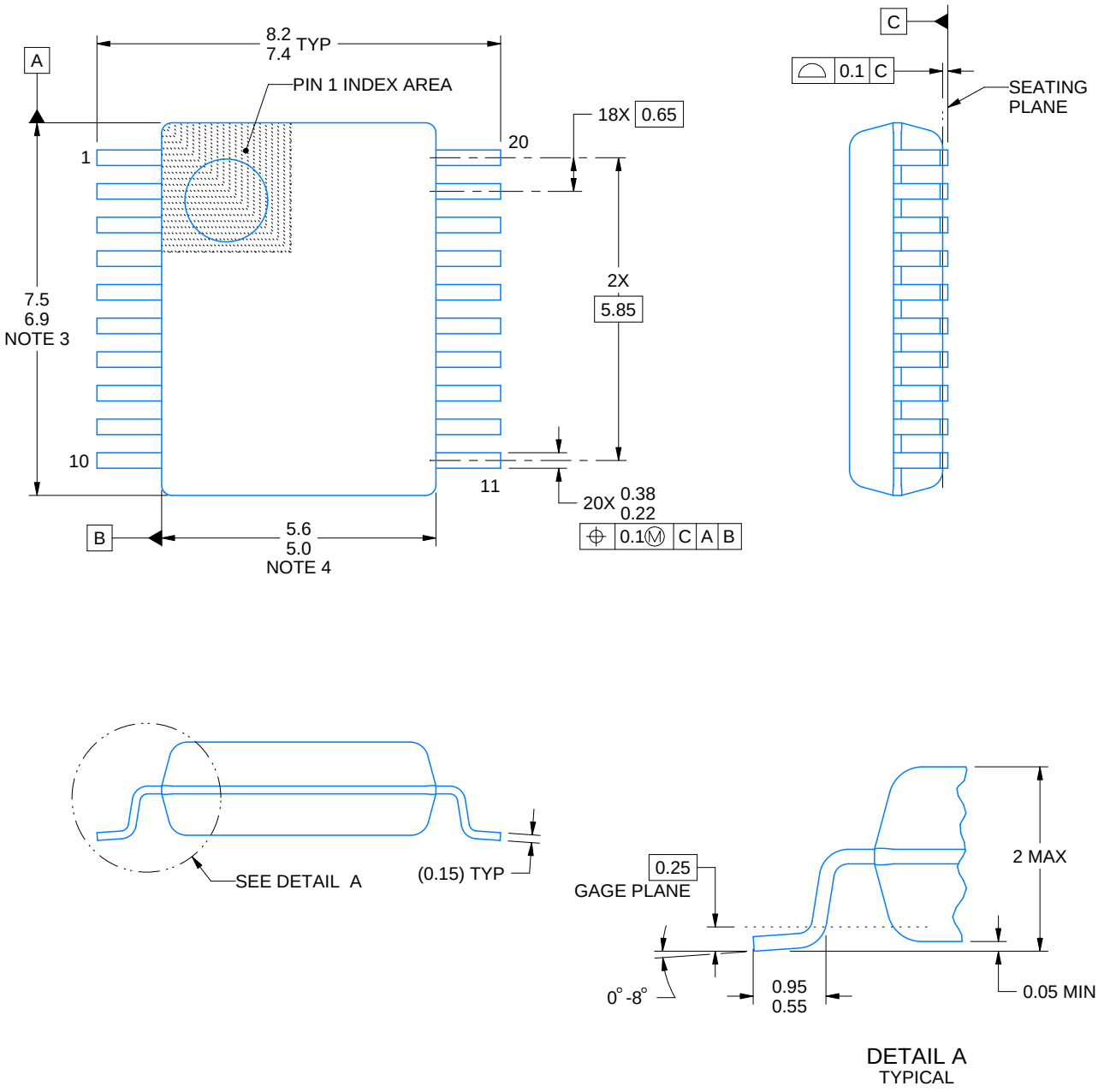

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## DB0020A

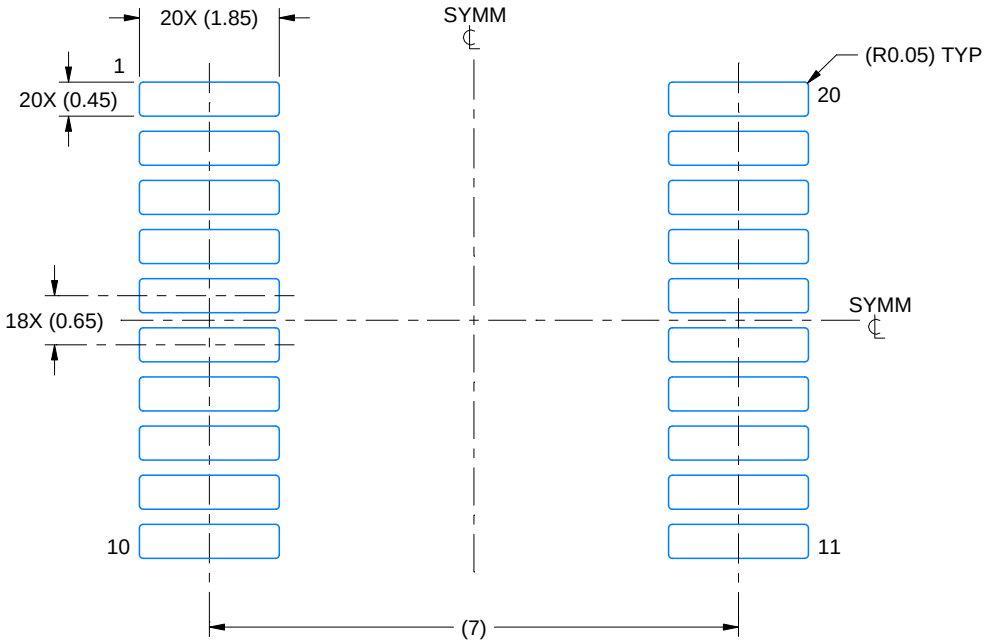
## TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE

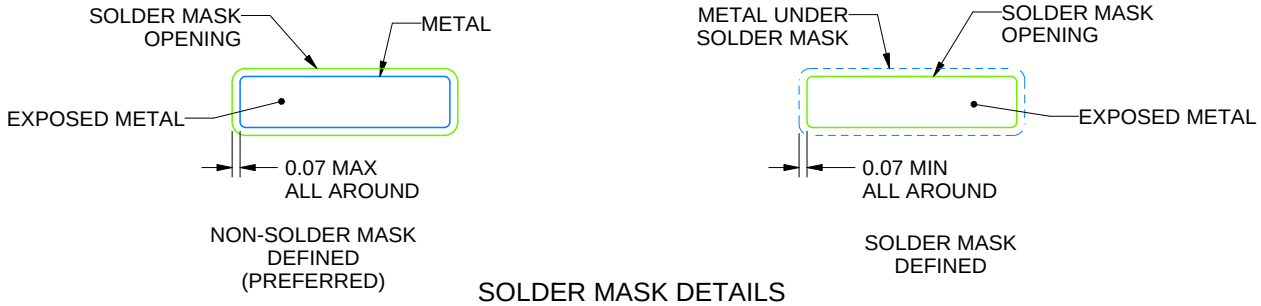



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

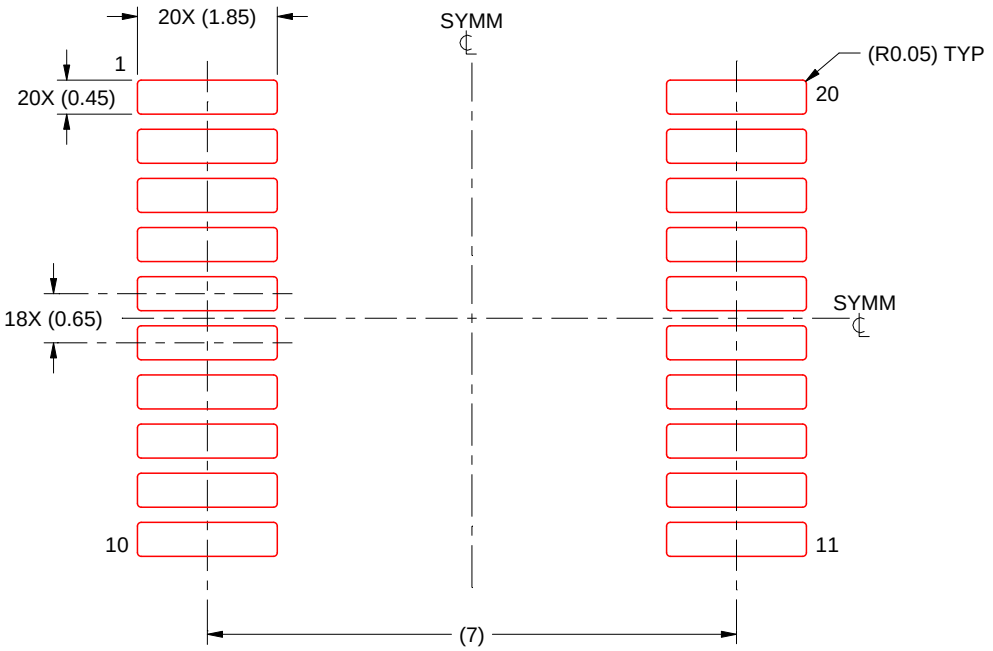



SOLDER MASK DETAILS

4214851/A 12/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

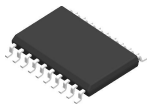



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/A 12/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

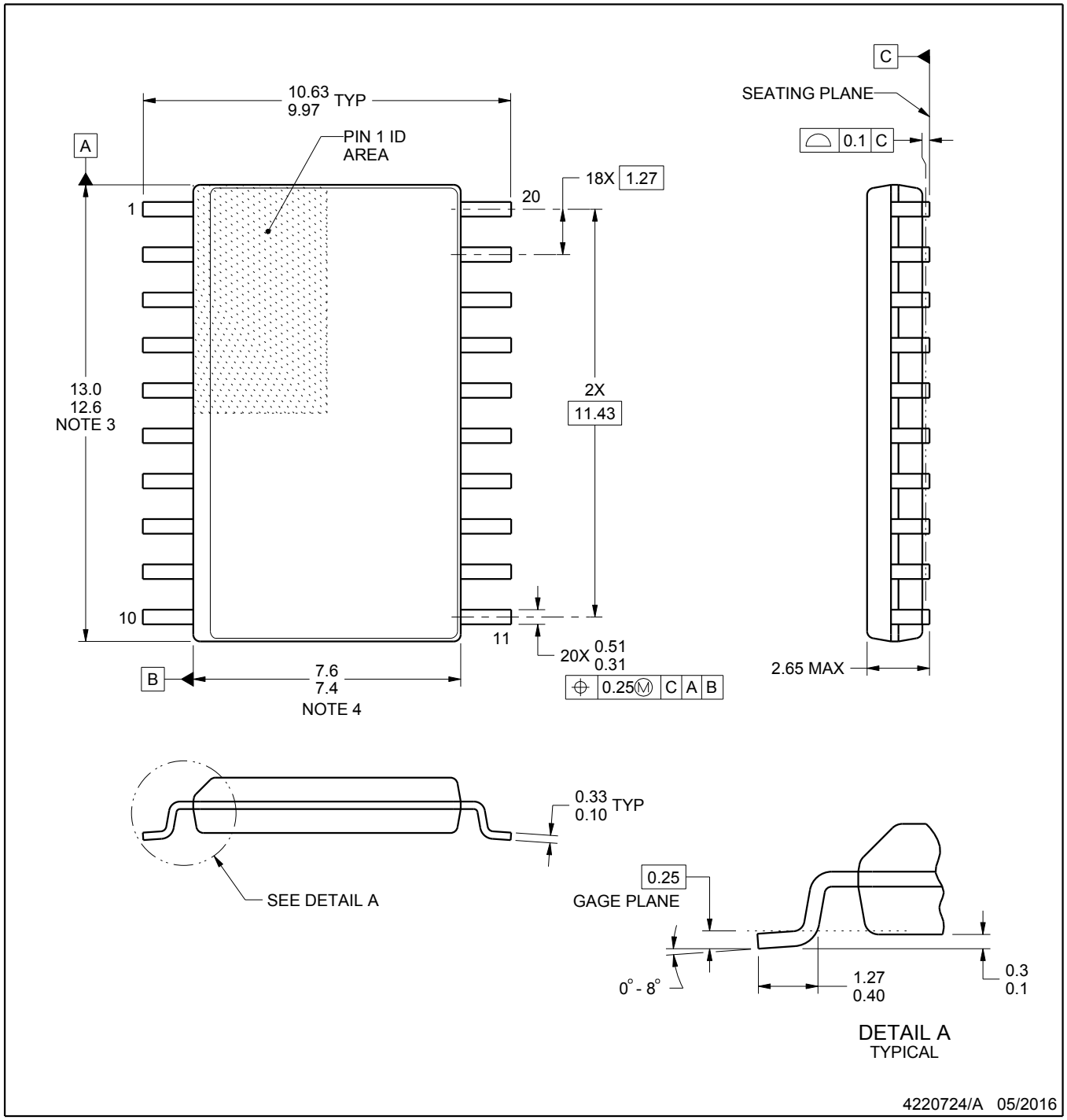


# PACKAGE OUTLINE

## DW0020A

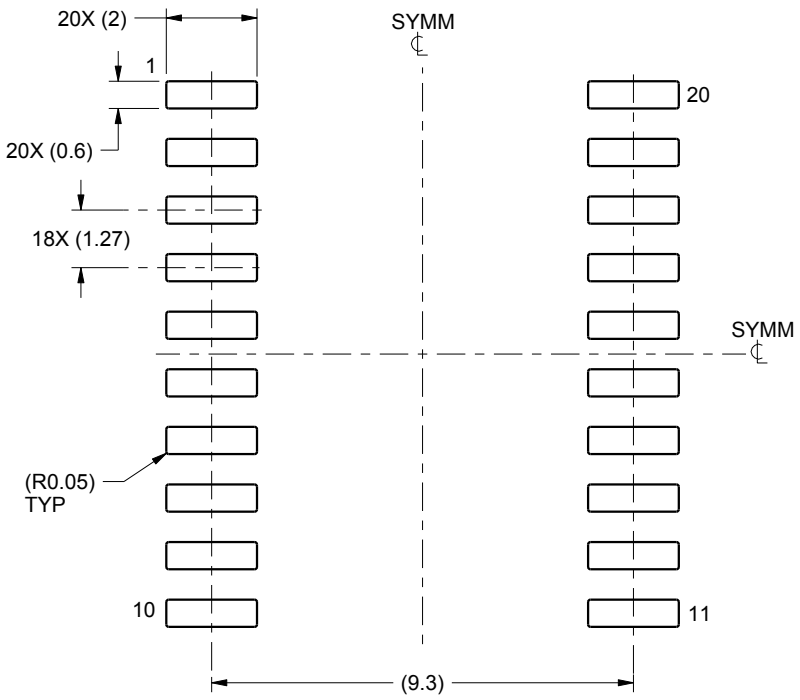
## SOIC - 2.65 mm max height

SOIC

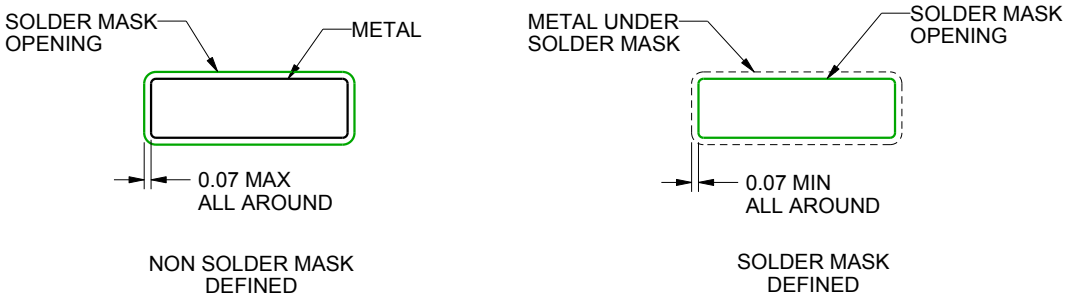



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

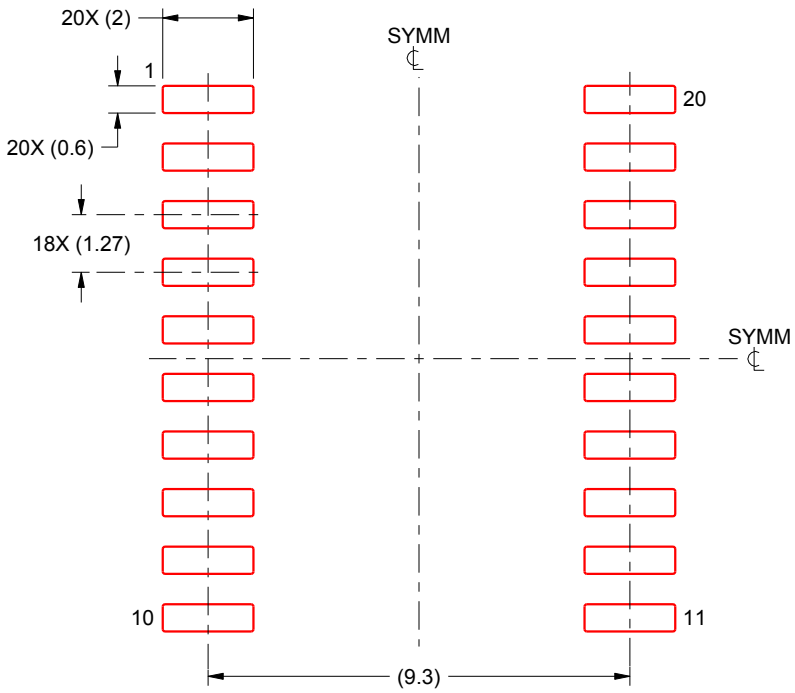



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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