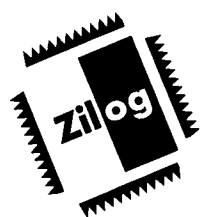




**THE DATASHEET OF
Z86C0412PSCR5335**





Z86C04/C08

CMOS 8-BIT LOW-COST 1K/2K-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C04	1	125	12	Optional	Optional
Z86C08	2	125	12	Optional	Optional

Note: * General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0V to 5.5V Operating Range
- Available Temperature Ranges
 - A = -40°C to +125°C
 - E = -40°C to +105°C
 - S = 0°C to +70°C
- 14 Input / Output Lines
- Six Vectored, Prioritized Interrupts from Six Different Sources
- Two On-Board Comparators
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Clock-Free WDT Reset
- Power-On Reset (POR) Timer
- ROM Mask Options:
 - Low Noise
 - ROM Protect
 - Auto Latch
 - System Clock Driving WDT (Z86C04 only)
 - Permanent Watch-Dog Timer (WDT)
 - RC Oscillator
 - 32 kHz Operation
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonance, LC, or External Clock Drive
- Low-Power Consumption (50 mw)
- Fast Instruction Pointer (1.0 μ s @ 12 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection

GENERAL DESCRIPTION

Zilog's Z86C04/C08 are members of the Z8[®] MCU family and offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86C04/C08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

Note: All signals with a preceding front slash, "/", are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

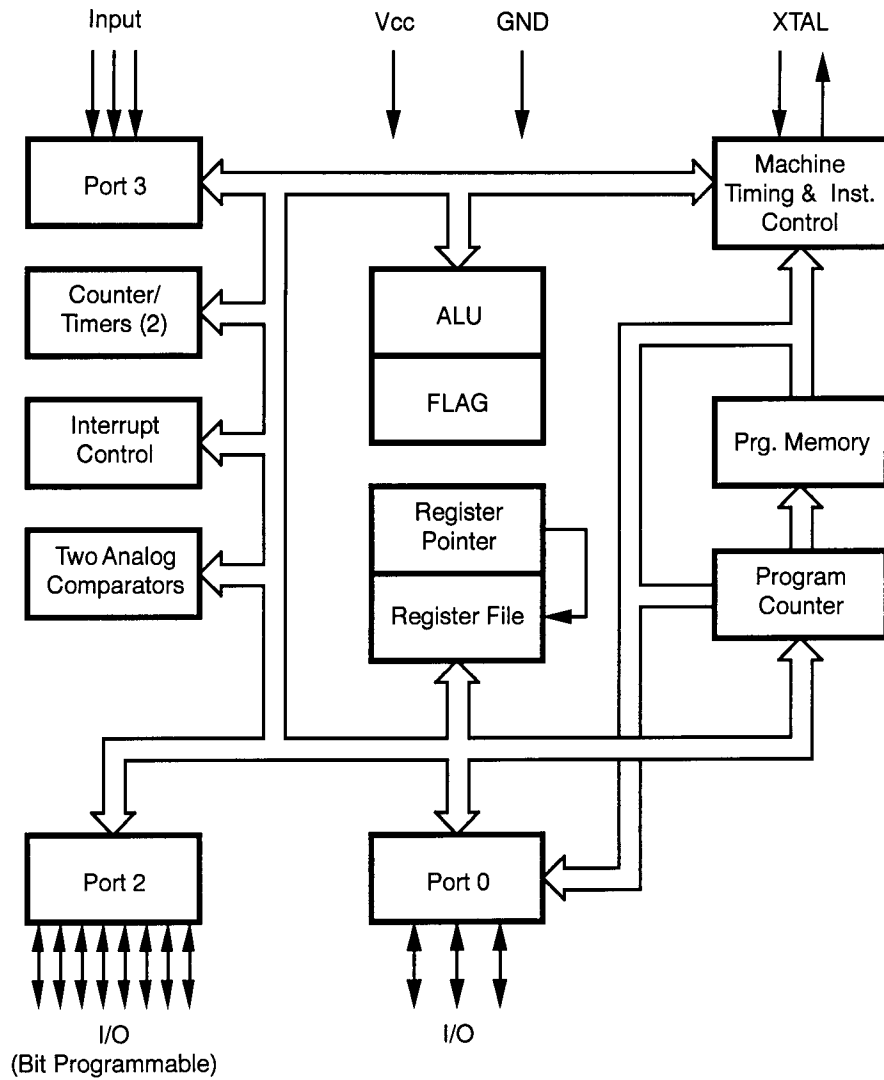


Figure 1. Z86C04/C08 Functional Block Diagram

PIN DESCRIPTIONS

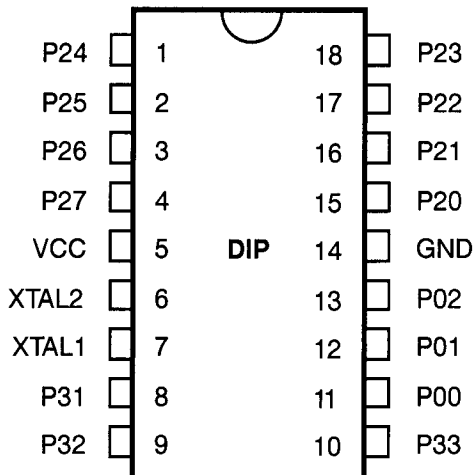


Figure 2. 18-Pin DIP

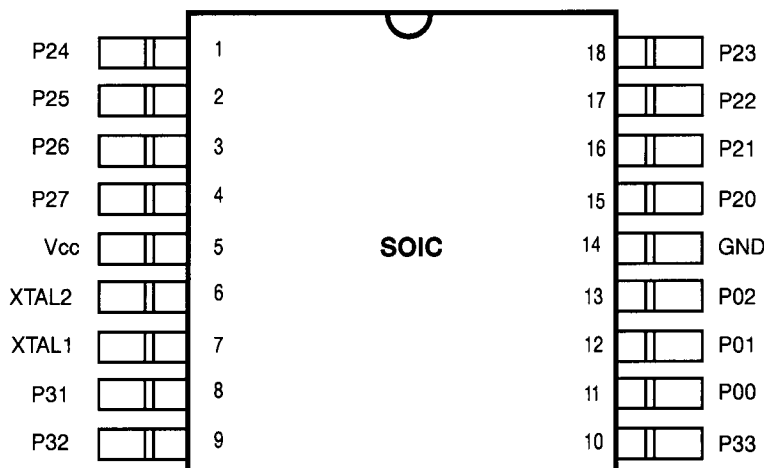


Figure 3. 18-Pin SOIC

Table 1: 18-Pin DIP and SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V _{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	-40	+105	C	
Storage Temperature	-65	+150	C	
Voltage on any Pin with Respect to V_{SS}	-0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V	
Voltage on Pin 7 with Respect to V_{SS}	-0.7	$V_{DD}+1$	V	2
Total Power Dissipation		462	mW	
Maximum Current out of V_{SS}		84	mA	
Maximum Current into V_{DD}		84	mA	
Maximum Current into an Input Pin	-600	+600	μ A	3
Maximum Current into an Open-Drain Pin	-600	+600	μ A	4
Maximum Output Current Sunked by Any I/O Pin		12	mA	
Maximum Output Current Sourced by Any I/O Pin		12	mA	
Total Maximum Output Current Sunked by Port 2		70	mA	
Total Maximum Output Current Sourced by Port 2		70	mA	

Notes:

1. This applies to all pins except where otherwise noted. Maximum current into pin must be $\pm 600\mu$ A.
2. There is no input protection diode from pin to V_{DD} .
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an ex-

tended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Total Power dissipation = $V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

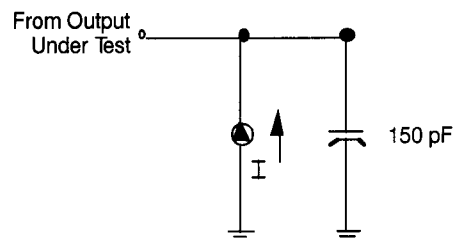


Figure 4. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0 \text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V _{CC} [4]	T _A = -40°C to +125°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V _{CH}	Clock Input High Voltage	3.0V	0.8 V _{CC}	V _{CC} +0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	3.0V	V _{SS} -0.3	0.2 V _{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	3.0V	0.7 V _{CC}	V _{CC} +0.3	1.8	V		1
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		1
V _{IL}	Input Low Voltage	3.0V	V _{SS} -0.3	0.2 V _{CC}	0.8	V		1
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		1
V _{OH}	Output High Voltage	3.0V	V _{CC} -0.4		3.0	V	I _{OH} = -2.0 mA	5
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		3.0V	V _{CC} -0.4		3.0	V	Low Noise @ I _{OH} = -0.5 mA	6
		5.5V	V _{CC} -0.4		4.8	V	Low Noise @ I _{OH} = -0.5 mA	6
V _{OL1}	Output Low Voltage	3.0V		0.8	0.2	V	I _{OL} = +4.0 mA	5
		5.5V		0.6	0.1	V	I _{OL} = +4.0 mA	5
		3.0V		0.6	0.2	V	Low Noise @ I _{OL} = 1.0 mA	6
		5.5V		0.6	0.1	V	Low Noise @ I _{OL} = 1.0 mA	6
V _{OL2}	Output Low Voltage	3.0V		1.2	0.8	V	I _{OL} = +12 mA	5
		5.5V		1.0	0.3	V	I _{OL} = +12 mA	5
V _{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
V _{LV}	V _{CC} Low Voltage Auto Reset		1.6	3.0	2.6	V	Int. CLK Freq @ 2 MHz Max.	5
			1.6	3.0	2.6	V	Int. CLK Freq @ 1 MHz Max.	8
I _{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
		5.5	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	3.0V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
V _{VICR}	Comparator Input Common Mode Voltage Range		0	V _{CC} -1.5		V		
I _{CC}	Supply Current	3.0V		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		3.0V		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		3.0V		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	5,7

DC ELECTRICAL CHARACTERISTICS (Continued)

I_{CC}	Supply Current	5.5V	15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	3.0V	2.5	0.7	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 2$ MHz	5,7
		5.5V	4.0	2.5	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 2$ MHz	5,7
		3.0V	4.0	1.0	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 8$ MHz	5,7
		5.5V	5.0	3.0	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 8$ MHz	5,7
		3.0V	4.5	1.5	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 12$ MHz	5,7
		5.5V	7.0	4.0	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 12$ MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	3.0V	3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V	7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		3.0V	5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V	9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz	7
I_{CC1}	Standby Current (Low Noise Mode)	3.0V	2.5	0.7	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 1$ MHz	7
		5.5V	4.0	2.5	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 1$ MHz	7
		3.0V	3.0	0.9	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 2$ MHz	7
		5.5V	4.5	2.8	mA	HALT Mode $V_{IN} = 0V$, $V_{CC} @ 2$ MHz	7
I_{CC2}	Standby Current	3.0V	20	1.0	μA	STOP Mode $V_{IN} = 0V$, V_{CC} ; WDT is not Running	7
		5.5V	20	1.0	μA	STOP Mode $V_{IN} = 0V$, V_{CC} ; WDT is not Running	7
I_{ALL}	Auto Latch Low Current	3.0V	8.0	3.0	μA	$0V < V_{IN} < V_{CC}$	
		5.5V	36	16	μA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.0V	-5.0	-1.5	μA	$0V < V_{IN} < V_{CC}$	
		5.5V	-22	-8.0	μA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 0, 2, and 3 only
2. $V_{SS} = 0V = GND$
3. The device operates down to V_{LV} . The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. $V_{CC} = 3.0V$ to $5.5V$, typical values measured at $V_{CC} = 3.3V$ and $V_{CC} = 5.0V$.
5. Standard Mode (not Low EMI Mode)
6. Z86C08 only
7. Inputs at power rail and outputs are unloaded.
8. Low EMI Mode

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C		T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max	Min	Max				
V _{CH}	Clock Input High Voltage	3.0V	0.8 V _{CC}	V _{CC} +0.3	0.8 V _{CC}	V _{CC} +0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V _{CC}	V _{CC} +0.3	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	3.0V	V _{SS} -0.3	0.2 V _{CC}	V _{SS} -0.3	0.2 V _{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2 V _{CC}	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	3.0V	0.7 V _{CC}	V _{CC} +0.3	0.7 V _{CC}	V _{CC} +0.3	1.8	V		1
		5.5V	0.7 V _{CC}	V _{CC} +0.3	0.7 V _{CC}	V _{CC} +0.3	2.8	V		1
V _{IL}	Input Low Voltage	3.0V	V _{SS} -0.3	0.2 V _{CC}	V _{SS} -0.3	0.2 V _{CC}	0.8	V		1
		5.5V	V _{SS} -0.3	0.2 V _{CC}	V _{SS} -0.3	0.2 V _{CC}	1.5	V		1
V _{OH}	Output High Voltage	3.0V	V _{CC} -0.4		V _{CC} -0.4		3.0	V	I _{OH} = -2.0 mA	5
		5.5V	V _{CC} -0.4		V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		3.0V	V _{CC} -0.4		V _{CC} -0.4		3.0	V	Low Noise @ I _{OH} = -0.5 mA	6
		5.5V	V _{CC} -0.4		V _{CC} -0.4		4.8	V	Low Noise @ I _{OH} = -0.5 mA	6
V _{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I _{OL} = +4.0 mA	5
		5.5V		0.4		0.4	0.1	V	I _{OL} = +4.0 mA	5
		3.0V		0.4		0.4	0.2	V	Low Noise @ I _{OL} = 1.0 mA	6
		5.5V		0.4		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	6
V _{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I _{OL} = +12 mA	5
		5.5V		0.8		0.8	0.3	V	I _{OL} = +12 mA	5
V _{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V _{LV}	V _{CC} Low Voltage Auto Reset		2.0	2.8			2.6	V	Int. CLK Freq @ 6 MHz Max.	
					1.8	3.0	2.6	V	Int. CLK Freq @ 4 MHz Max.	
I _{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	-1.0	1.0	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	1.0	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	3.0V	-1.0	1.0	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	1.0	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
V _{VICR}	Comparator Input Common Mode Voltage Range		0	V _{CC} -1.0	0	V _{CC} -1.5		V		
I _{CC}	Supply Current	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C		T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max	Min	Max				
I _{CC}	Supply Current	3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I _{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		5.5V		4.0		4.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		3.0V		4.0		4.0	1.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	5,7
		5.5V		5.0		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	5,7
		3.0V		4.5		4.5	1.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz	5,7
		5.5V		7.0		7.0	4.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz	5,7
I _{CC}	Supply Current (Low Noise)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		3.0V		5.8		5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		9.0		9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz	7
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz	7

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C		T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max	Min	Max				
I _{CC1}	Standby Current (Low Noise Mode)	3.0V		2.5		2.5	0.7	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		5.5V		4.0		4.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		3.0V		3.5		5.0	0.9	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz	5,7
		5.5V		5.0		5.0	2.8	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4MHz	5,7
I _{CC2}	Standby Current	3.0V		10		20	1.0	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	7
		5.5V		10		20	1.0	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	7
I _{ALL}	Auto Latch Low Current	3.0V		12		8.0	3.0	μA	0V < V _{IN} < V _{CC}	
		5.5V		30		32	16	μA	0V < V _{IN} < V _{CC}	
I _{ALH}	Auto Latch High Current	3.0V		-8		-5.0	-1.5	μA	0V < V _{IN} < V _{CC}	
		5.5V		-16		-20	-8.0	μA	0V < V _{IN} < V _{CC}	

Notes:

1. Port 0, 2, and 3 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode).
6. Z86C08 only
7. Inputs at power rail and outputs are unloaded.

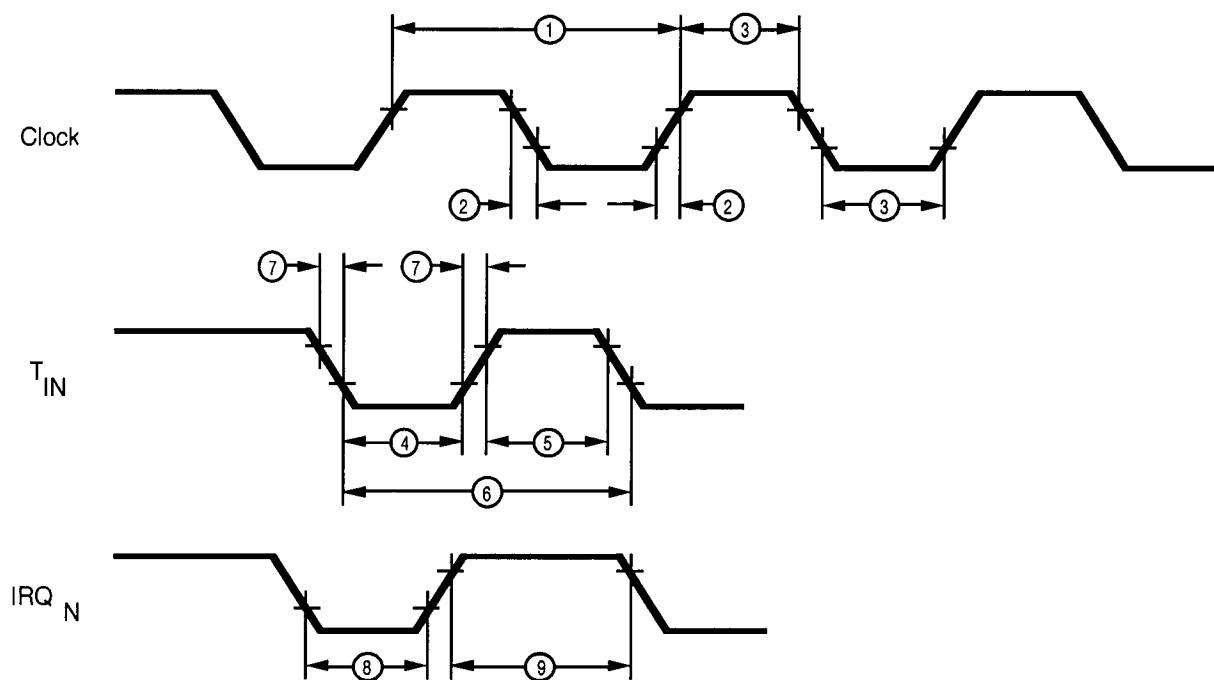


Figure 5. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

$T_A = -40C \text{ to } +125C$									
No	Symbol	Parameter	V_{CC}	8 MHz		12 MHz		Units	Notes
				Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	3.0V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwlL	Int. Request Input Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
9	TwhH	Int. Request Input High Time	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		ms	
			5.5V	8		8		ms	
11	Tpor	Power-On Reset Time	3.0V	50	180	50	180	ms	3
			5.5V	18	100	18	100	ms	3
			3.0V	4	30	4	30	ms	4
			5.5V	2	15	2	15	ms	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Z86C08
4. Z86C04

AC ELECTRICAL CHARACTERISTICS (Continued)

No	Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C				T _A = -40°C to +105°C				Units	Notes
				8 MHz		12 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	1
			5.5V		25		15		25		15	ns	1
3	TwC	Input Clock Width	3.0V	62		41		62		41	ns	1	
			5.5V	62		41		62		41	ns	1	
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100	ns	1	
			5.5V	70		70		70		70	ns	1	
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC		1	
			5.5V	5TpC		5TpC		5TpC		5TpC		1	
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC		1	
			5.5V	8TpC		8TpC		8TpC		8TpC		1	
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100	ns	1,2	
			5.5V	70		70		70		70	ns	1,2	
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC		1	
			5.5V	5TpC		5TpC		5TpC		5TpC		1,2	
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		25		25		ms	
			5.5V	10		10		8		8		ms	3
			5.5V	12		12		12		12		ms	4
11	Tpor	Power-On Reset Time	3.0V	50	160	50	160	50	160	50	160	ms	3
			5.5V	24	80	24	80	18	80	18	80	ms	3
			3.0V	6	30	6	30	4	30	4	30	ms	4
			5.5V	3	15	3	15	2	15	2	15	ms	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31)
3. Z86C08
4. Z86C04

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode (SCLK/TCLK = XTAL)

 $T_A = -40^\circ\text{C to } +125^\circ\text{C}$

1 MHz 2 MHz

No	Symbol	Parameter	V_{CC}	1 MHz		2 MHz		Units	Notes
				Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	1000	DC	500	DC	ns	1
			5.5V	1000	DC	500	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	3.0V	500		250		ns	1
			5.5V	500		250		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwlL	Int. Request Input Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
9	TwlH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		ms	3
			5.5V	8		8		ms	3

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.

AC ELECTRICAL CHARACTERISTICS (Continued)

No	Symbol	Parameter	V _{CC}	T _A = 0°C to 70°C				T _A = -40°C to +105°C				Units	Notes
				1 MHz		4 MHz		1 MHz		4 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	1000	DC	250	DC	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	1000	DC	250	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25		25		25	ns	1
			5.5V		25		25		25		25	ns	1
3	TwC	Input Clock Width	3.0V	500		125		500		125		ns	1
			5.5V	500		125		500		125		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			1
			5.5V	4TpC		4TpC		4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwlL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
9	TwhH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		25		25		ms	3
			5.5V	10		10		8		8		ms	3,5
			5.5V	12		12		12		12		ms	3,4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.
4. Z86C04
5. Z86C08

LOW NOISE VERSION

Low EMI Emission

The Z8[®] MCU can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted

APPLICATION PRECAUTIONS:

1. Emulator does not support the 32 kHz operation.
2. For the Z86C04, the WDT only runs in STOP Mode if the permanent WDT option is selected and if the on-board RC oscillator is selected as the clock source for the WDT.
3. For the Z86C08, the WDT only runs in Stop Mode if the permanent WDT option is selected.
4. The registers %FE (GPR) and %FF (SPL) are reset to 00Hex after Stop Mode recovery or any reset.
5. Emulator does not support the system clock driving the WDT mask option.
6. Must wait two NOPS before analog comparitor outputs are valid after enabling analog mode.
7. Must disable interrupts, enable the analog comparitor, and then clear IRQ3 to IRQ0 when switching from digital to analog mode.

PIN DESCRIPTION

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a RC, parallel-resonant crystal, LC, or an external single-phase clock to the on-chip clock oscillator and buffer.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. After Power-On Reset, this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating

node, reduces excessive supply current flow in the input buffer. To change the Auto Latch state, the auto latches must be over driven with current greater than I_{ALH} (high to low) or I_{ALL} (low to high).

Port 0 (P02-P00). Port 0 is a 3-bit I/O, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be configured under software control to be all inputs or all outputs (Figure 6).

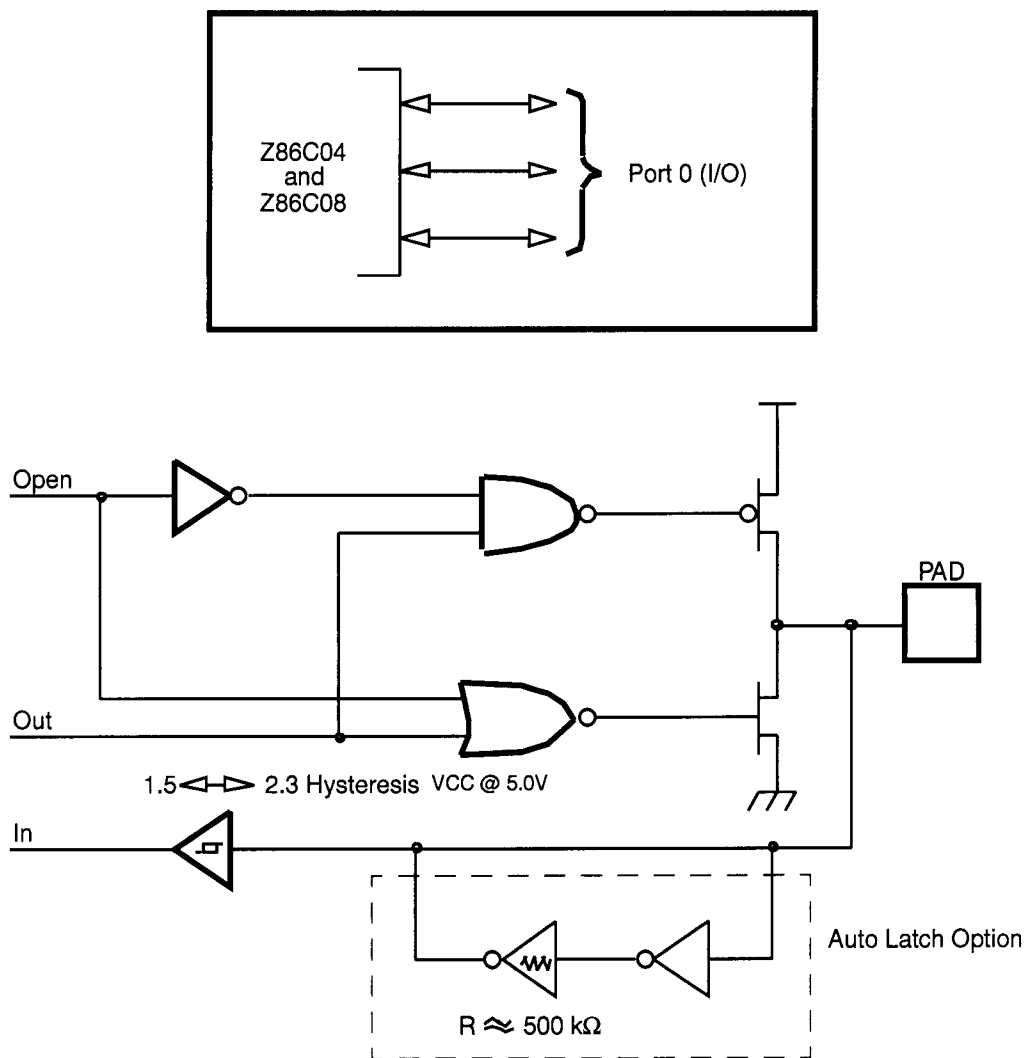


Figure 6. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit-programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under soft-

ware control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 7).

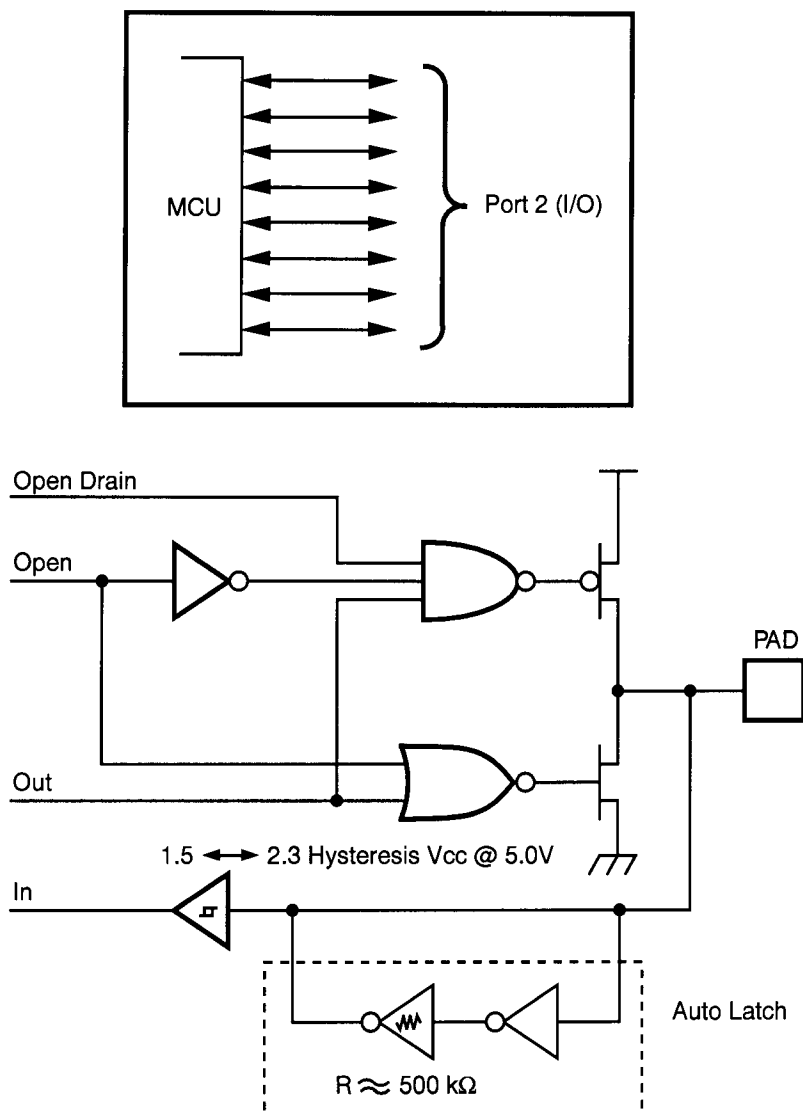


Figure 7. Port 2 Configuration

PIN DESCRIPTION (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, Schmitt-triggered CMOS-compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under soft-

ware control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 8).

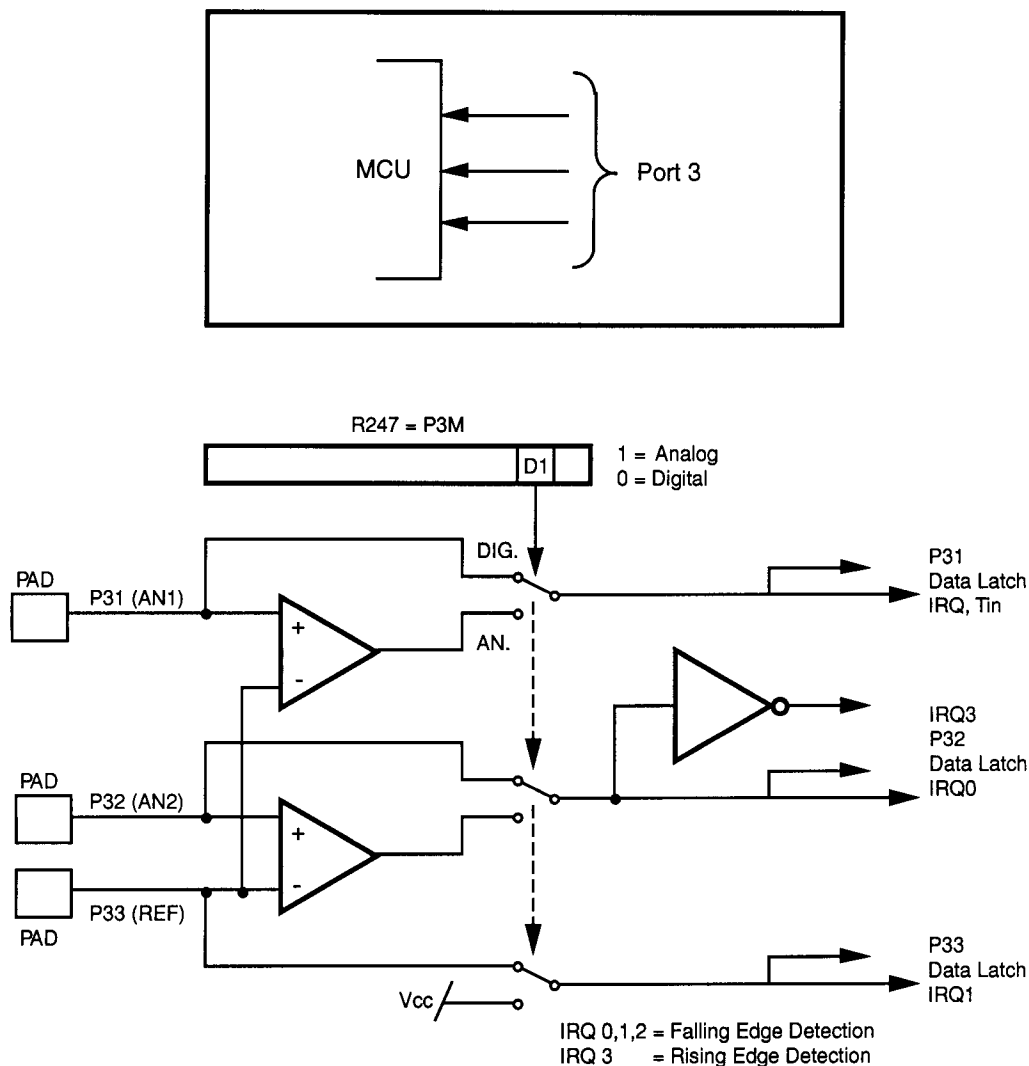


Figure 8. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility. Typical applications for these on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply that discontinues power in STOP Mode. The common voltage range is 0-4V when the V_{CC} is 5.0V. Before the comparator outputs are valid, two NOP delays are required after enabling the analog comparators.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternately, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

RESET. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, and then starts program

execution at address %000C (Hex) (Figure 9). The device control registers' reset value is shown in Table 1.

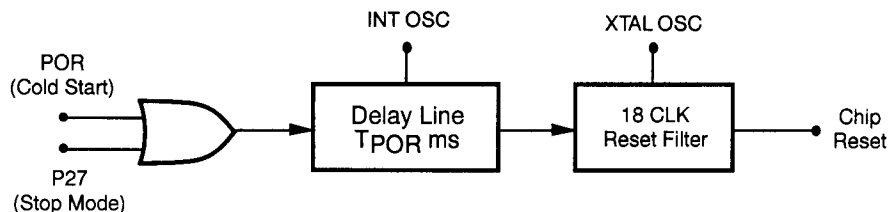


Figure 9. Internal Reset Configuration

Table 1. Z86C04/C08 & C05/C07 Control Registers

Addr.	Reg.	Reset Condition								Comments
		D7	D6	D5	D4	D3	D2	D1	D0	
03H (3)*	Port 3	U	U	U	U	U	U	U	U	
02H (2)*	Port 2	U	U	U	U	U	U	U	U	
00H (0)*	Port 0	U	U	U	U	U	U	U	U	
FFH(255)	SPL	0	0	0	0	0	0	0	0	
FEH (254)	GPR	0	0	0	0	0	0	0	0	
FDH (253)	RP	0	0	0	0	0	0	0	0	
FCH (252)	FLAGS	U	U	U	U	U	U	U	U	
FBH (251)	IMR	0	U	U	U	U	U	U	U	
FAH (250)	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9H (249)	IPR	U	U	U	U	U	U	U	U	
F8H (248)*	P01M	U	U	U	0	U	U	0	1	
F7H (247)*	P3M	U	U	U	U	U	U	0	0	
F6H (246)*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5H (245)	PRE0	U	U	U	U	U	U	U	0	
F4H (244)	T0	U	U	U	U	U	U	U	U	
F3H (243)	PRE1	U	U	U	U	U	U	0	0	
F2H (242)	T1	U	U	U	U	U	U	U	U	
F1H (241)	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be re-configured as shown in Table 1 and the user must avoid bus contention on the port pins or it may affect device reliability.

FUNCTIONAL DESCRIPTION (Continued)

Program Memory. The Z86C04/C08 can address up to 1K/2K bytes of internal program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1023/2047 are on-chip mask-programmed ROM.

Register File. The Register File consists of three I/O port registers, 125 general-purpose registers, and 14 control and status registers (R0, R2-R3, R4-R127, and R241-R255, respectively; see Figure 11). Note that R254 is available for general purpose use.

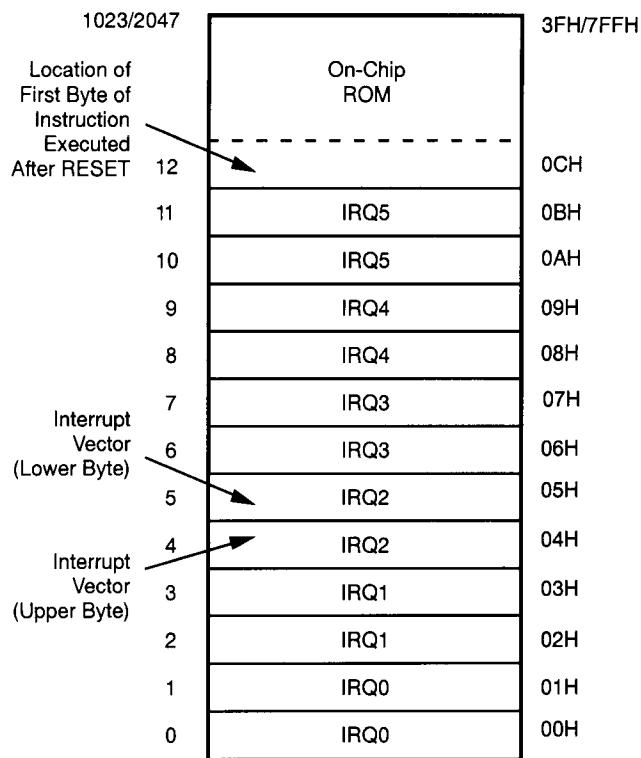


Figure 10. Program Memory Map

Location	Identifiers
255	Stack Pointer (Bits 7-0) SPL
254	Reserved
253	Register Pointer RP
252	Program Control Flags Flags
251	Interrupt Mask Register IMR
250	Interrupt Request Register IRQ
249	Interrupt Priority Register IPR
248	Ports 0-1 Mode P01M
247	Port 3 Mode P3M
246	Port 2 Mode P2M
245	To Prescaler PRE0
244	Timer/Counter0 T0
243	T1 Prescaler PRE1
242	Timer/Counter1 T1
241	Timer Mode TMR
240	Not Implemented
128	
127	General Purpose Registers
4	
3	Port 3 P3
2	Port 2 P2
1	Reserved P1
0	Port 0 P0

Figure 11. Register File

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 12) addresses the starting location of the active working-register group. Upon power-up, the general purpose registers are undefined.

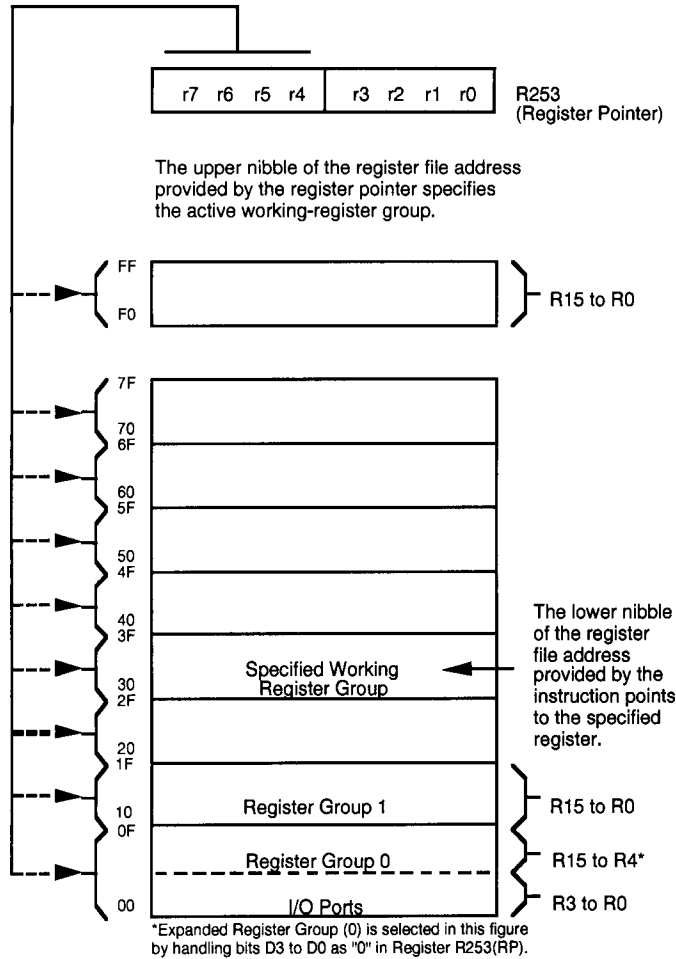


Figure 12. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Register (GPR). The general-purpose register upon device power-up is undefined. The general-purpose register upon a Stop-Mode Recovery and reset stays in its last state. It may not keep its last state from a V_{LV} reset if the V_{CC} drops below 2.6V.

Note: Register R254 has been designated as a general-purpose register and is set to 00H after any reset.

FUNCTIONAL DESCRIPTION (Continued)

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 13).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock.

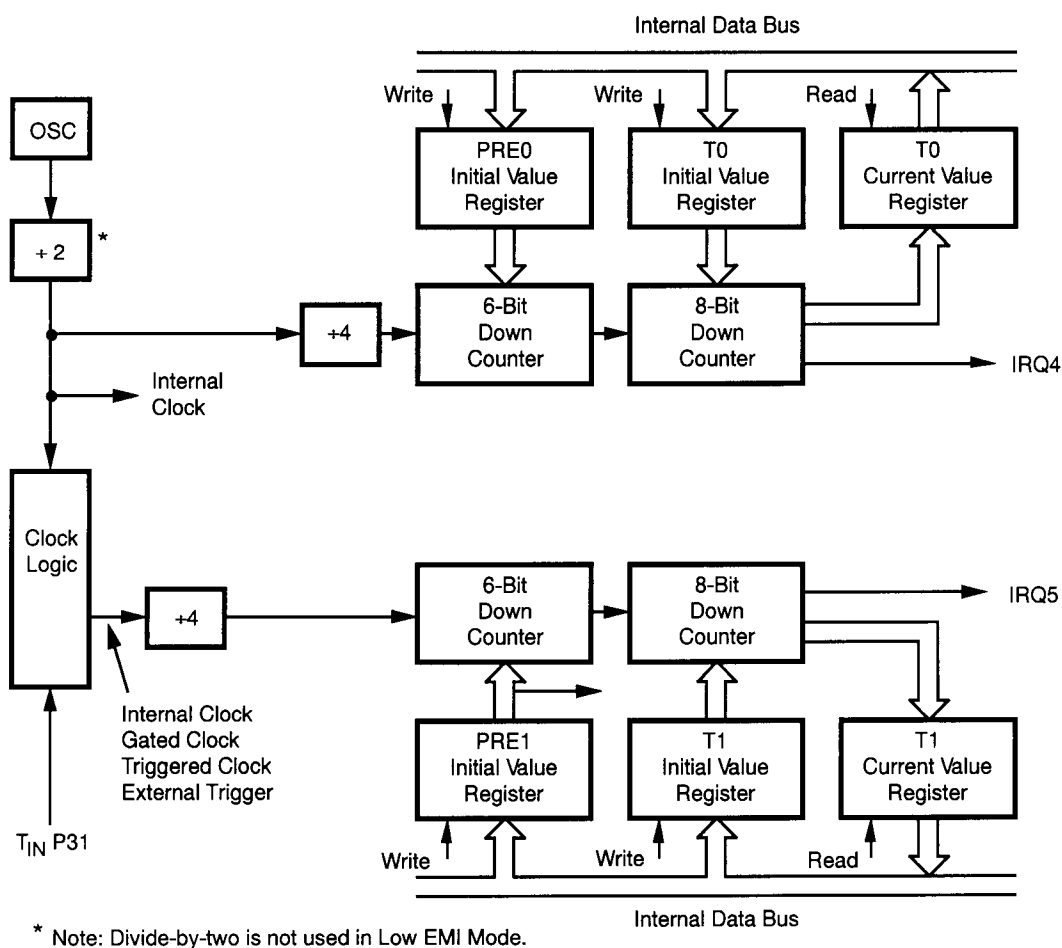


Figure 13. Counter/Timers Block Diagram

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 14). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 2).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86C08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1(P31)	4,5	External (F) Edge
IRQ3	AN2(P32)	6,7	External (R) Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:

F = Falling edge triggered
R = Rising edge triggered

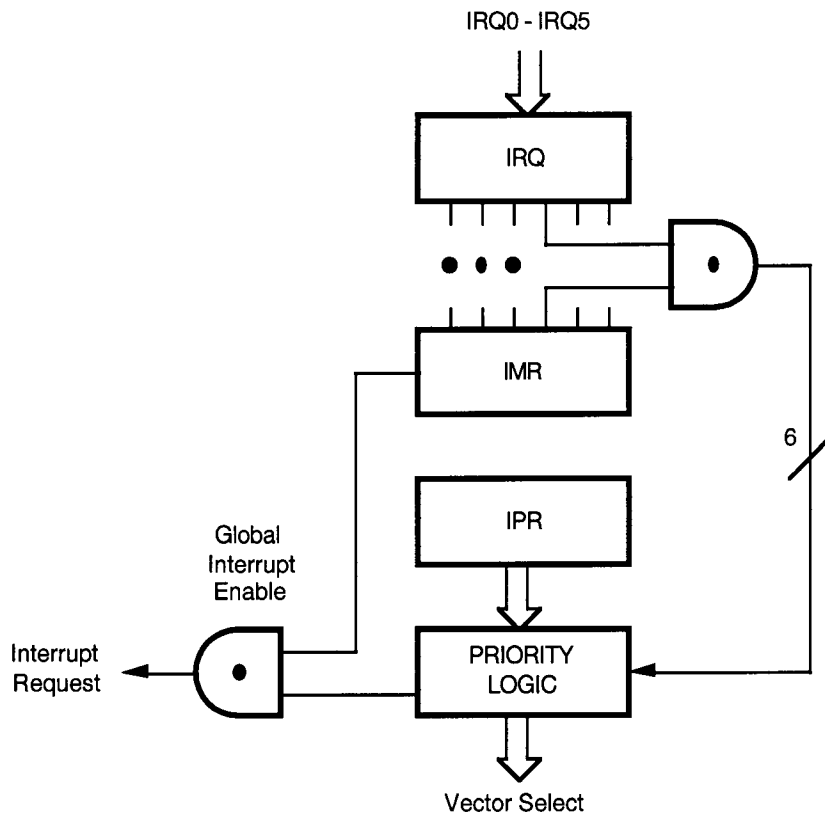


Figure 14. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a RC, crystal, ceramic resonator, LC, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors (which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device Ground pin 14 (Figure 15).

Note that the crystal capacitor loads should be connected to V_{SS} pin 14 to reduce ground noise injection.

To use 32 kHz crystal, the 32 kHz operational mask option must be selected, and an external resistor R must be connected across XTAL1 and XTAL2. To use RC oscillator, the RC oscillator option must be selected.

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC} or dropping the V_{CC} below V_{LV} . The second method is if P27 is at a low level when the device executes the STOP instruction. A low condition on P27 releases the STOP Mode regardless if configured for input or output.

Program execution under both conditions begins at location 000C (Hex). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not re-configured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Note: (X = dependent upon user's application.)
In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, that is, as follows:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
        or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT should be refreshed once the WDT is enabled within every T_{wdt} period; otherwise, the Z8 resets itself. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

WDT = 5F (Hex)

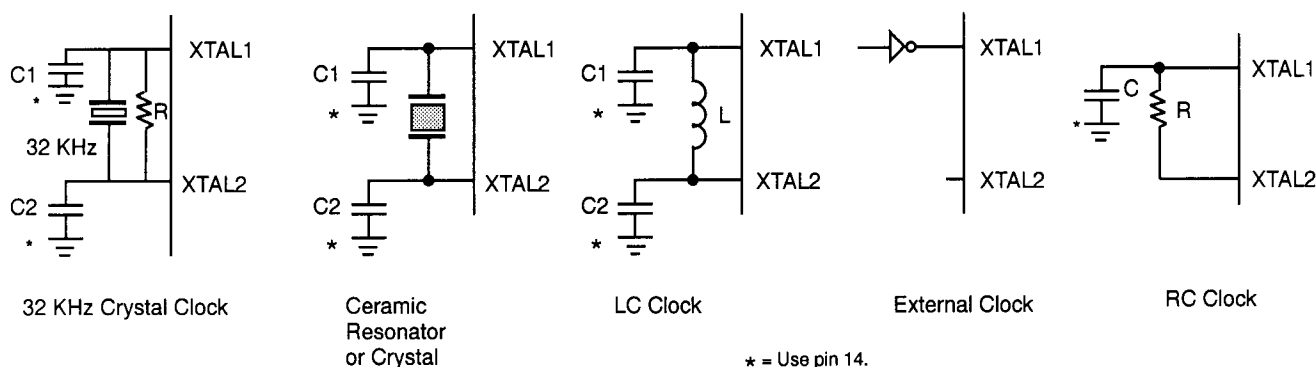


Figure 15. Oscillator Configuration

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done within the maximum T_{WDT} period; otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 XTAL clock cycles. The WDT does not work (run) in STOP Mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

Opcode WDH (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it facilitates running the WDT function during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT Mask Option. Only when the Permanent WDT Mask Option is selected, then the WDT is hardwired to be enabled after reset. The WDT will operate in Run Mode, HALT Mode, and STOP Mode. The Opcode 5FH is used to refresh or clear the WDT counter. The WDT instruction (4FH) has no effect. The WDT will not run in STOP Mode if the system clock driving the WDT is selected (Z86C04 only).

System Clock Driving WDT Mask Option (Z86C04 only)
When this option is selected, the Z8's system clock drives the WDT instead of the on-board RC oscillator driving the

WDT. The WDT time-out will be $SCLK \times 32,512$. The WDT will not run in STOP Mode.

Low-Voltage Protection (V_{LV}). Maximum (V_{LV})
Conditions:

- Case 1: $T_A = -40^\circ\text{C}, +85^\circ\text{C}$, Internal Clock
Frequency equal or less than 6 MHz
- Case 2: $T_A = -40^\circ\text{C}, +105^\circ\text{C}$, Internal Clock
Frequency equal or less than 4 MHz

Note: The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low-Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Cases 1 and 2. The actual low voltage trip point is a function of temperature and process parameters (Figure 16).

1 MHz (Typical)

Temp	-40°C	0°C	$+25^\circ\text{C}$	$+70^\circ\text{C}$	$+105^\circ\text{C}$	$+125^\circ\text{C}$
V_{LV}	3.0	2.75	2.6	2.3	2.1	1.9

ROM Protect. ROM Protect fully protects the Z86C04/C08 ROM code from being read internally. **When ROM Protect is selected, ROM look-up tables can be used in this mode.**

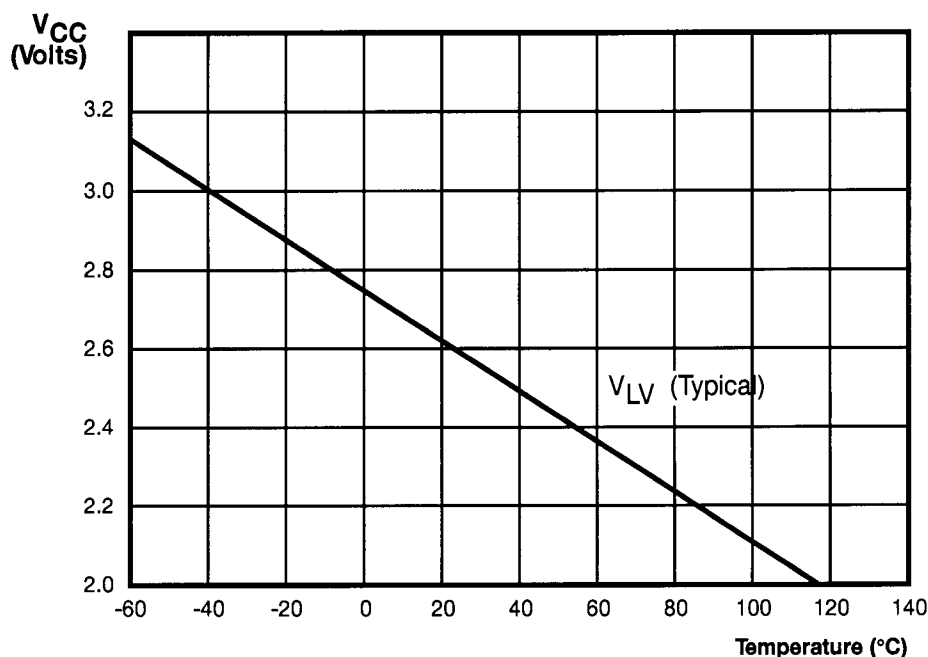


Figure 16. Typical Z86C04/C08 V_{LV} vs. Temperature

Z8 CONTROL REGISTER DIAGRAMS

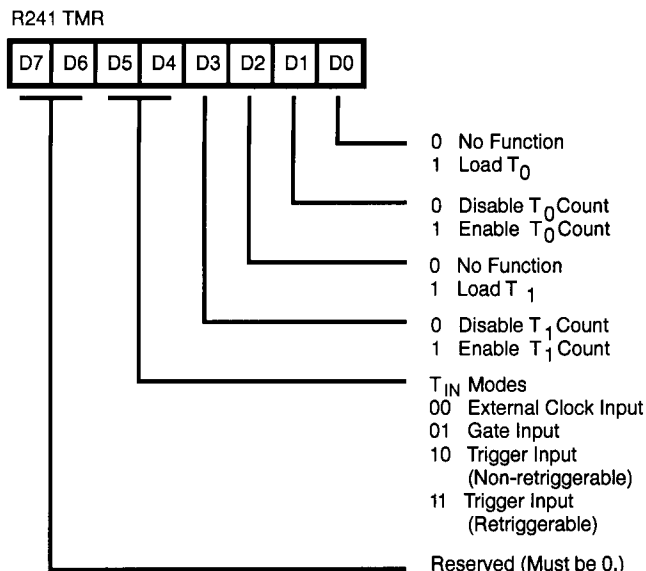


Figure 17. Timer Mode Register (F1_H: Read/Write)

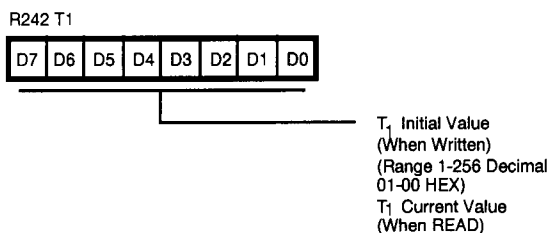


Figure 18. Counter Time 1 Register (F2_H: Read/Write)

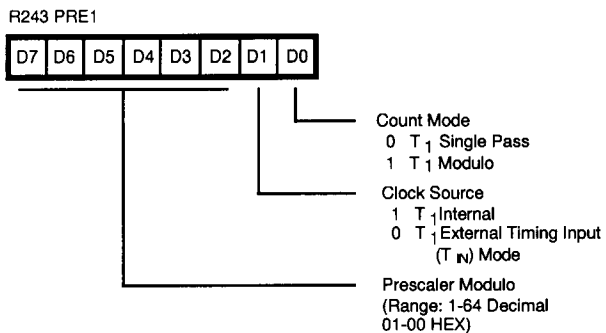


Figure 19. Prescaler 1 Register (F3_H: Write Only)

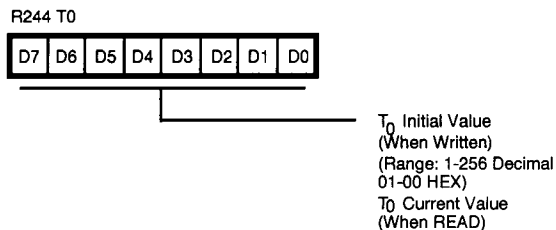


Figure 20. Counter/Timer 0 Register (F4_H: Read/Write)

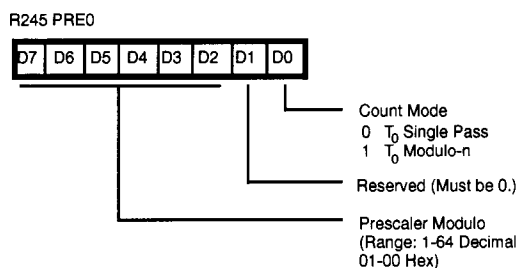


Figure 21. Prescaler 0 Register (F5_H: Write Only)

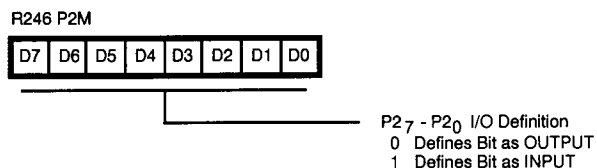


Figure 22. Port 2 Mode Register (F6_H: Write Only)

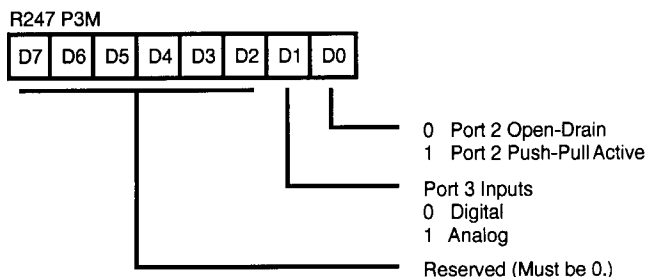


Figure 23. Port 3 Mode Register (F7_H: Write Only)

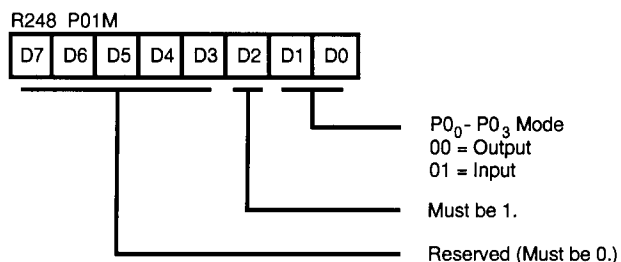


Figure 24. Port 0 and 1 Mode Register (F8_H: Write Only)

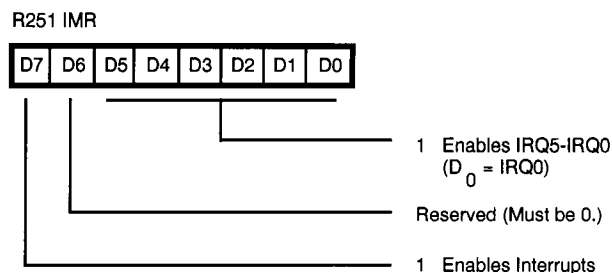


Figure 27. Interrupt Mask Register (FB_H: Read/Write)

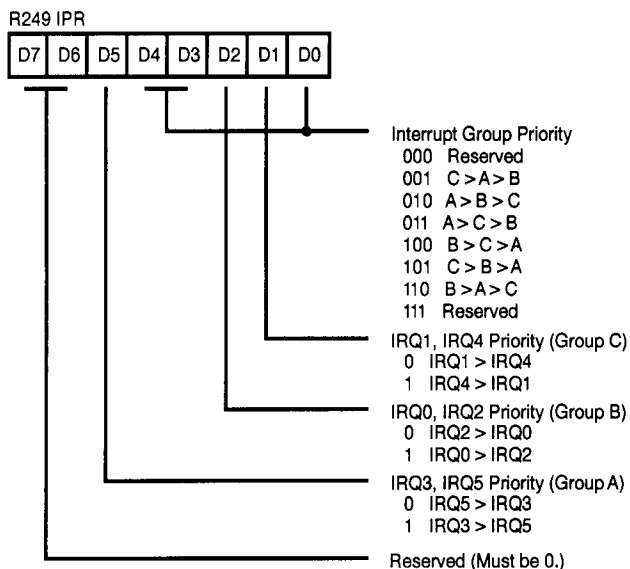


Figure 25. Interrupt Priority Register (F9_H: Write Only)

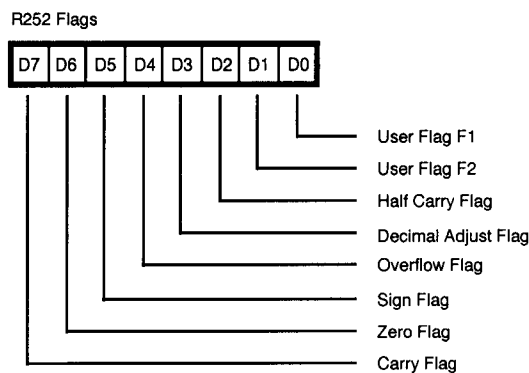


Figure 28. Flag Register (FC_H: Read/Write)

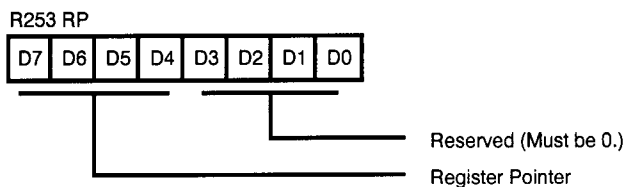


Figure 29. Register Pointer (FD_H: Read/Write)

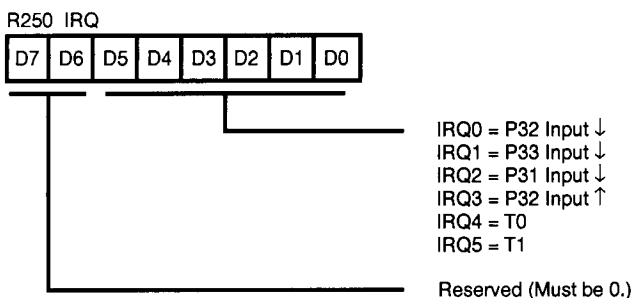


Figure 26. Interrupt Request Register (FA_H: Read/Write)

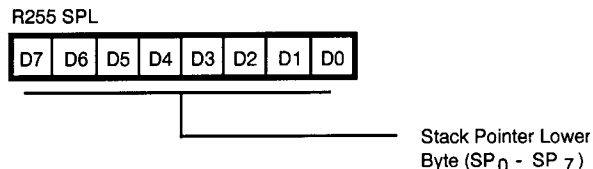


Figure 30. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS

Standard Mode

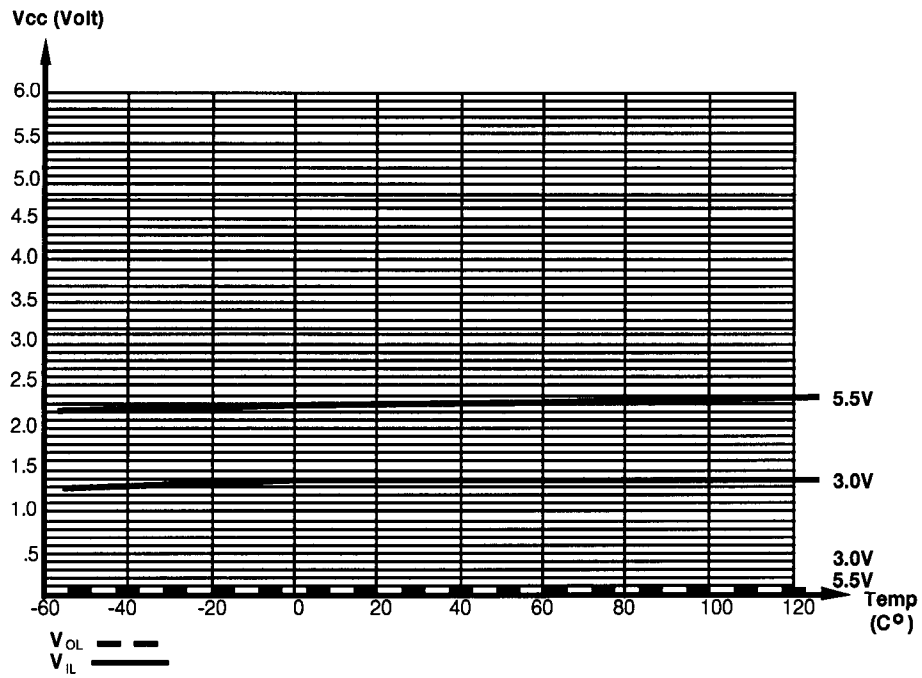


Figure 31. V_{IL} , V_{OL} vs. Temperature

Standard Mode

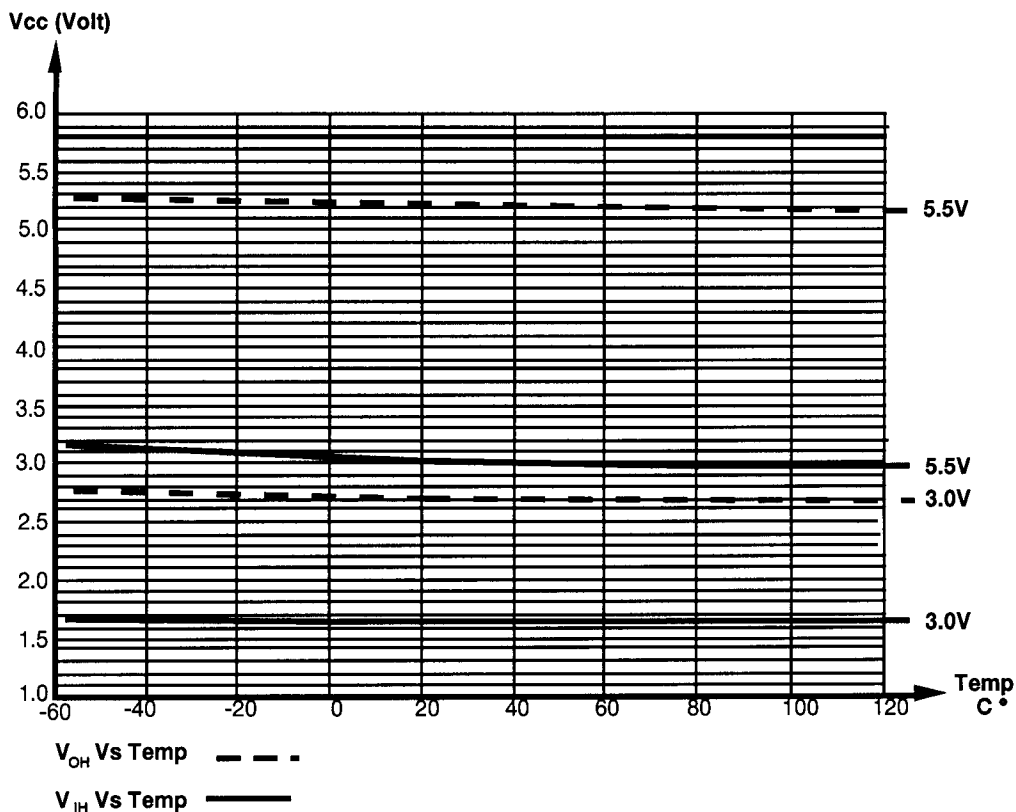


Figure 32. V_{IH} , V_{OH} vs. Temperature

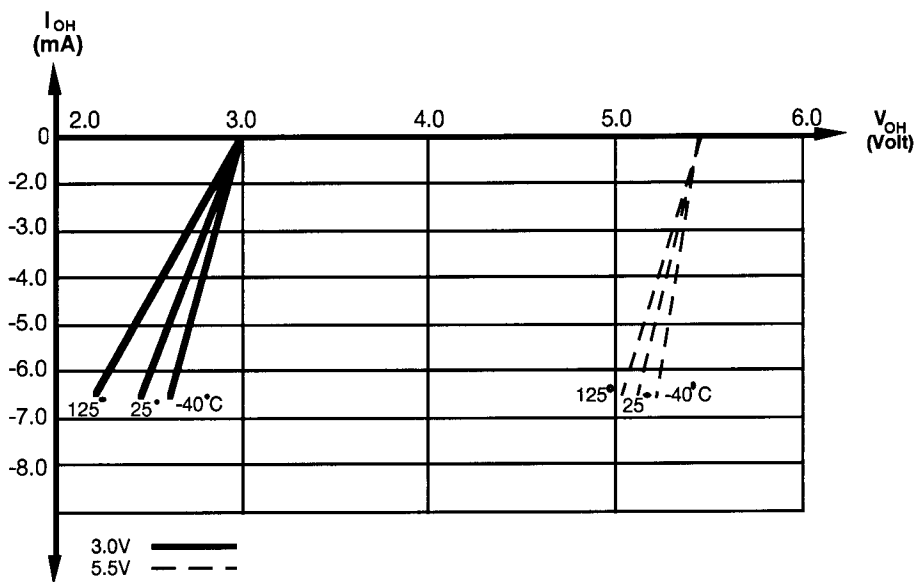


Figure 33. Typical I_{OH} vs. V_{OH}

Z8 CONTROL REGISTER DIAGRAMS (Continued)

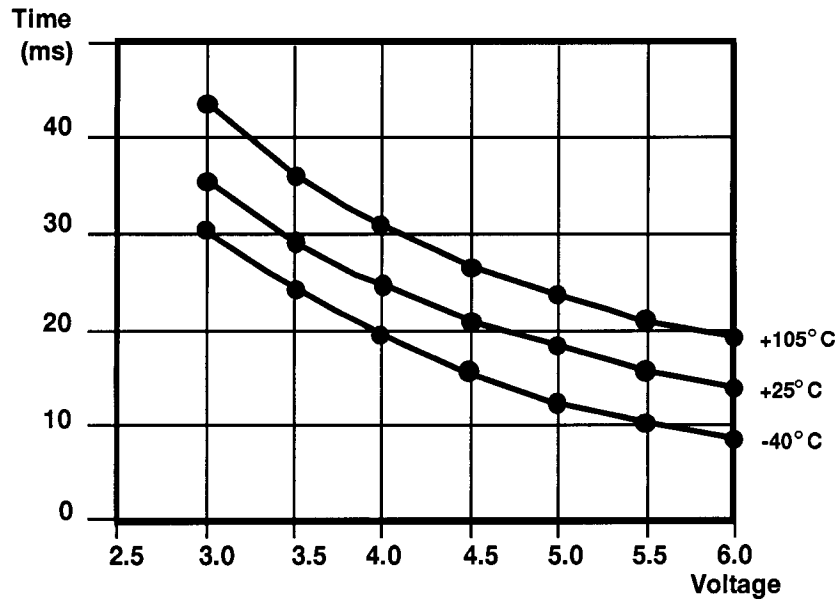
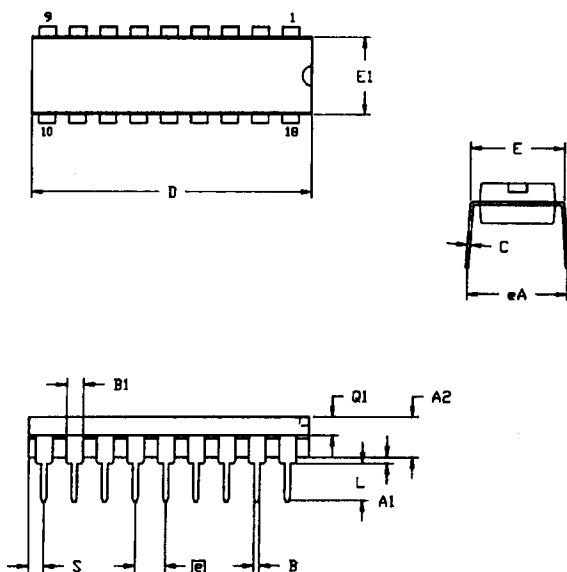


Figure 34. Typical WDT Time Out Period vs. V_{cc} Over Temperature

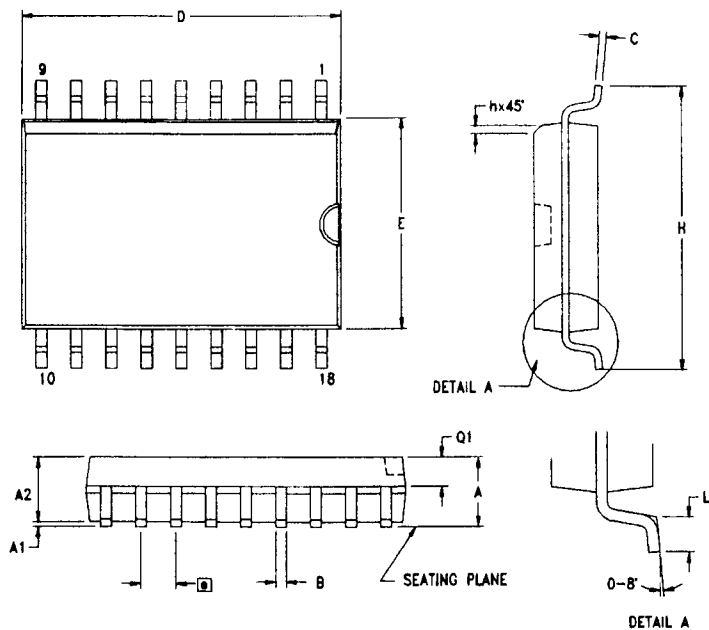
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
□	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 35. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
□	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 36. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C04 (12 MHz)		Z86C08 (12 MHz)	
Standard Temperature		Standard Temperature	
18-Pin DIP Z86C0412PSC	18-Pin SOIC Z86C0412SSC	18-Pin DIP Z86C0812PSC	18-Pin SOIC Z86C0812SSC
Extended Temperature		Extended Temperature	
18-Pin DIP Z86C0412PEC Z86C0412PAC	18-Pin SOIC Z86C0412SEC Z86C0412SAC	18-Pin DIP Z86C0812PEC Z86C0812PAC	18-Pin SOIC Z86C0812SEC Z86C0812SAC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package

P = DIP
S = SOIC

Preferred Temperature

S = 0°C to +70°C

Longer Lead Time

E = -40°C to +105°C
A = -40°C to +125°C

Speeds

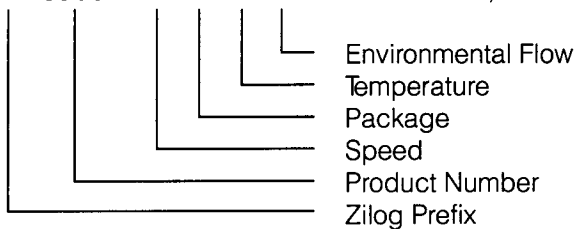
12 = 12 MHz

Environmental

C = Plastic Standard

Example:

Z 86C04 12 P S C is a Z86C04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found,

either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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