

2.5/3.3V 200 MHz High-Speed, Low-Jitter, Low-Skew, Zero-Delay Clock Buffer with 5 Outputs

Features

- Phase-Lock Loop Clock Distribution (Zero Input-to-Output Delay)
- Internal feedback connection
- Distributes one to one bank of five outputs
- High-Performance
 - 30 MHz to 220 MHz operation frequency range
 - <100ps output-to-output skew
 - <100ps cycle-to-cycle jitter
 - Low Power Consumption - 25mA (outputs unloaded)
- Spread-spectrum capable
- Power supply
 - +2.5V ±5%
 - +3.3V ±10%
- Temperature range
 - -40°C to +85°C Industrial temp range
- Packaging (Pb-free & Green):
 - 8-pin TSSOP (L8)
 - 8-pin SOIC (W8)

Description

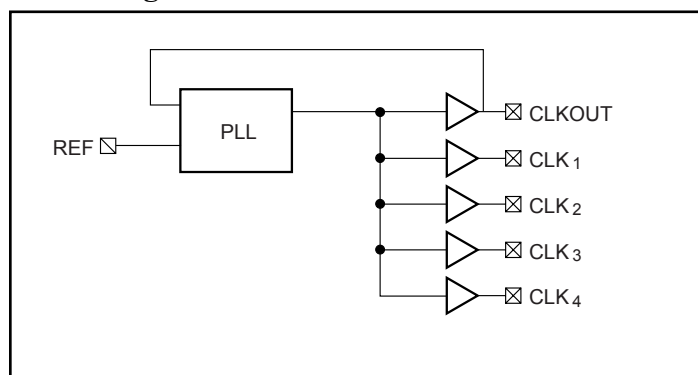
The PI6C22405-1H is a low-jitter, low-skew, high-speed Zero-Delay Buffer with 5 outputs designed to address high-speed clock distribution applications.

The PI6C22405-1H features an internal patented Phase Lock Loop (PLL) with high drive output capability and internal feedback.

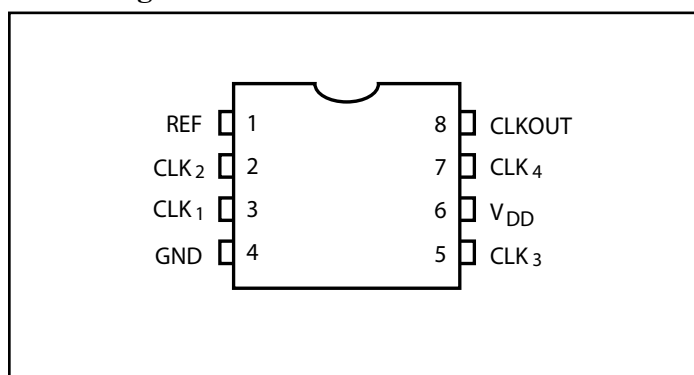
The PI6C22405-1H operates from a 2.5V±5% or 3.3V±10% supply, guaranteed over the full industrial temperature range of -40°C to +85°C. All support documentation can be found on Pericom's web site at: www.pericom.com.

Pericom can customize these devices for specific requirements.

Block Diagram



Pin Configuration



Pin Description

| Pin | Signal | Description |
|---------------|----------------------------|---|
| 1 | REF | Reference clock input with weak pull down. |
| 2, 3, 5, 7 | CLK2, CLK1, CLK3, CLK4, | Clock output. Clock outputs contain a weak pull-down. |
| 8 | CLKOUT | Clock output. Internal feedback on this pin. |
| 4 | GND | Ground |
| 6 | V _{DD} | Power |

Maximum Ratings ⁽¹⁾

| | |
|--|-----------------|
| Supply Voltage | |
| V _{DD} | -0.5V to +4.6V |
| REF..... | -0.5V to +4.6V |
| Input Current | -50mA |
| Output Current | ±50mA |
| Lead Temperature (soldering, 10 sec.)..... | +260°C |
| Storage Temperature (T _s)..... | -65°C to +150°C |
| Junction Temperature..... | +150°C |

Operation Ratings ⁽²⁾

| | |
|---|--------------------|
| Supply Voltage | |
| V _{DD} | +3.0V to +3.6V |
| V _{DD} | +2.375V to +2.625V |
| Operating Temperature (industrial)..... | -40°C to +85°C |
| Package Thermal Resistance ⁽²⁾ | |
| θ _{JA} | |
| Still-Air..... | 157°C/W |
| θ _{JB} | |
| Junction-to-Board..... | 42°C |

Notes:

1. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. θ_{JA} and θ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.

DC Electrical Characteristics

| Parameter | Description | Test Conditions | Min. | Max. | Units | |
|-----------------|---------------------|---|------------------------|------|-------|---|
| V _{IL} | Input LOW Voltage | V _{DD} = 3.3V | | 0.8 | V | |
| | | V _{DD} = 2.5V | | 0.7 | | |
| V _{IH} | Input HIGH Voltage | V _{DD} = 3.3V | 2.0 | | V | |
| | | V _{DD} = 2.5V | 1.7 | | | |
| I _{IL} | Input LOW Current | V _{IN} = 0V | | 10 | μA | |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | | 100 | | |
| V _{OL} | Output LOW Voltage | I _{OL} = 12mA | V _{DD} = 3.3V | | 0.25 | V |
| | | | V _{DD} = 2.5V | | 0.35 | |
| V _{OH} | Output HIGH Voltage | V _{DD} = 2.5V, I _{OH} = -12mA | 1.9 | | V | |
| | | V _{DD} = 3.3V, I _{OH} = -12mA | 2.55 | | | |
| I _{DD} | Supply Current | Unloaded outputs 66 MHz | | 22 | mA | |

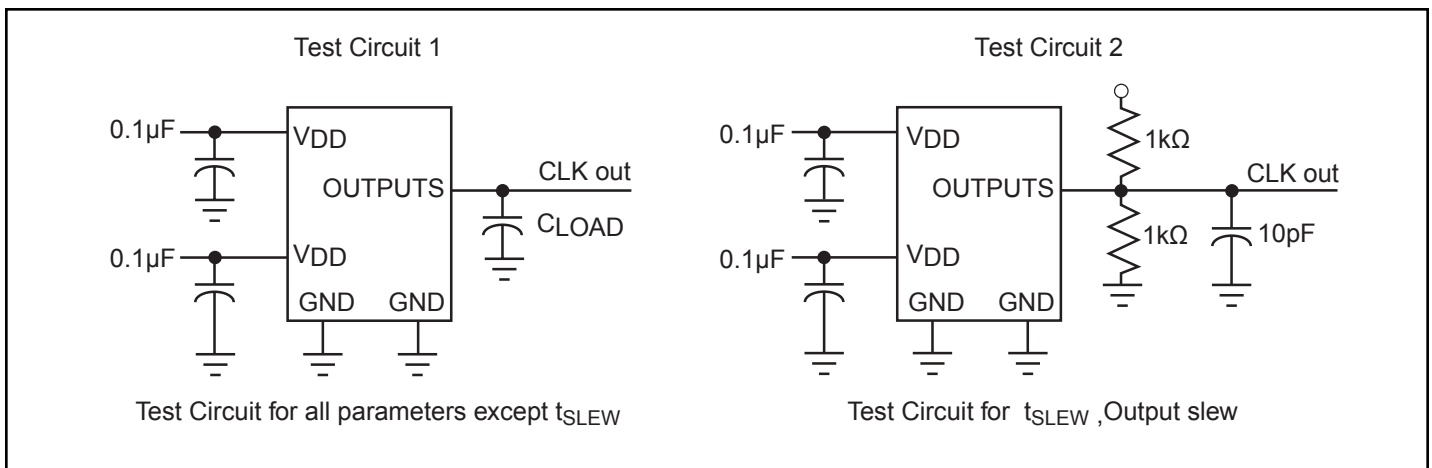
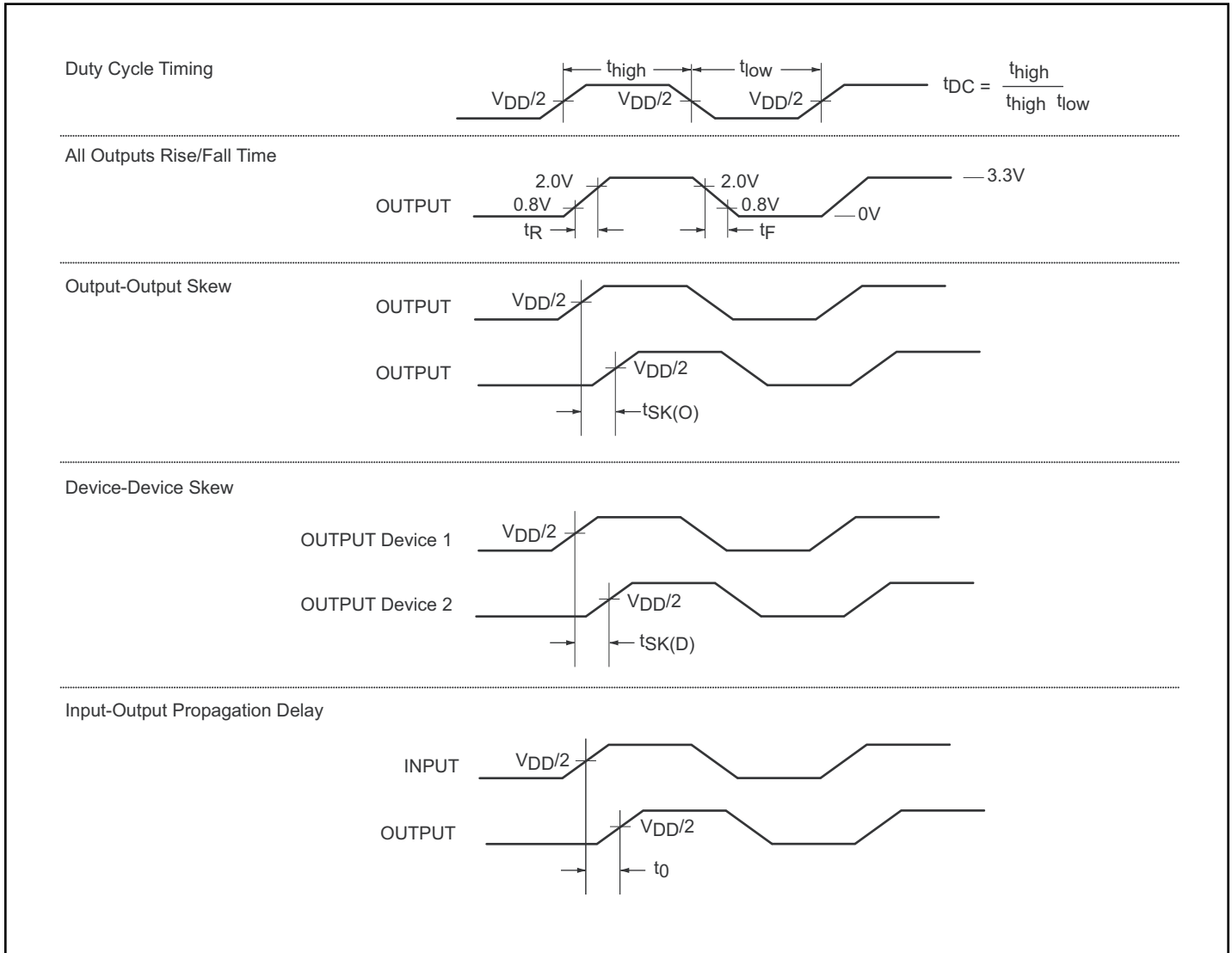
AC Electrical Characteristics

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units | |
|-------------------------------|---|--|------------------------|------|------|-------|----|
| F _O | Output Frequency | V _{DD} = 2.5V, C _L = 15pF | 10 | | 200 | MHz | |
| | | V _{DD} = 3.3V, C _L = 15pF | 10 | | 220 | MHz | |
| BW | Bandwidth for PLL | V _{DD} = 2.5V | | 0.8 | | MHz | |
| | | V _{DD} = 3.3V | | 1.5 | | | |
| t _{DC} | Duty Cycle ⁽¹⁾⁽⁴⁾ | Measured at V _{DD} /2, 10pF load | 45 | 50 | 55 | % | |
| t _R | Rise Time ⁽¹⁾⁽⁴⁾ | For 3.3V: Measured between 0.8V and 2.0V @ 10pF | | | 1 | ns | |
| | | For 2.5V: Measured between 0.6V and 1.8V @ 10pF | | | 1.8 | | |
| t _F | Fall Time ⁽¹⁾⁽⁴⁾ | For 3.3V: Measured between 0.8V and 2.0V @ 10pF | | | 1 | ns | |
| | | For 2.5V: Measured between 0.6V and 1.8V @ 10pF | | | 1.8 | | |
| t _{sk(o)} | Output to Output Skew ⁽²⁾ | All outputs equally loaded | V _{DD} = 3.3V | | 90 | ps | |
| | | | V _{DD} = 2.5V | | 90 | | |
| t ₀ | Delay, REF Rising Edge to CLKOUT Rising Edge ⁽²⁾ | Measured at V _{DD} /2 @ 66MHz | V _{DD} = 3.3V | -100 | 100 | ps | |
| | | | V _{DD} = 2.5V | -200 | 200 | | |
| t _{SK(D)} | Device-to-device Skew ⁽³⁾ | Measured at V _{DD} /2 on CLKx pins of device | -300 | | +300 | | |
| t _{JIT} | Cycle-to-Cycle Jitter | 15pF load, >66MHz, standard drive | V _{DD} = 3.3V | | 47 | 110 | ps |
| | | | V _{DD} = 2.5V | | 42 | 90 | |
| | | 15pF load, >66MHz, high drive | V _{DD} = 3.3V | | 45 | 100 | |
| | | | V _{DD} = 2.5V | | 40 | 80 | |
| | | 30pF load, >66MHz, standard drive | V _{DD} = 3.3V | | 63 | 120 | |
| | | | V _{DD} = 2.5V | | 83 | 130 | |
| 30pF load, >66MHz, high drive | V _{DD} = 3.3V | | 51 | 115 | | | |
| | V _{DD} = 2.5V | | 66 | 115 | | | |
| t _{PJ} | Period Jitter (Peak) | 15pF load, >66MHz, standard drive | V _{DD} = 3.3V | | 39 | 90 | ps |
| | | | V _{DD} = 2.5V | | 28 | 60 | |
| | | 15pF load, >66MHz, high drive | V _{DD} = 3.3V | | 39 | 85 | |
| | | | V _{DD} = 2.5V | | 27 | 55 | |
| | | 30pF load, >66MHz, standard drive | V _{DD} = 3.3V | | 48 | 85 | |
| | | | V _{DD} = 2.5V | | 75 | 90 | |
| | | 30pF load, >66MHz, high drive | V _{DD} = 3.3V | | 43 | 75 | |
| | | | V _{DD} = 2.5V | | 60 | 80 | |
| t _{LOCK} | PLL Lock Time ⁽¹⁾ | Stable power supply, valid clocks presented on REF pin | | | 1.0 | ms | |

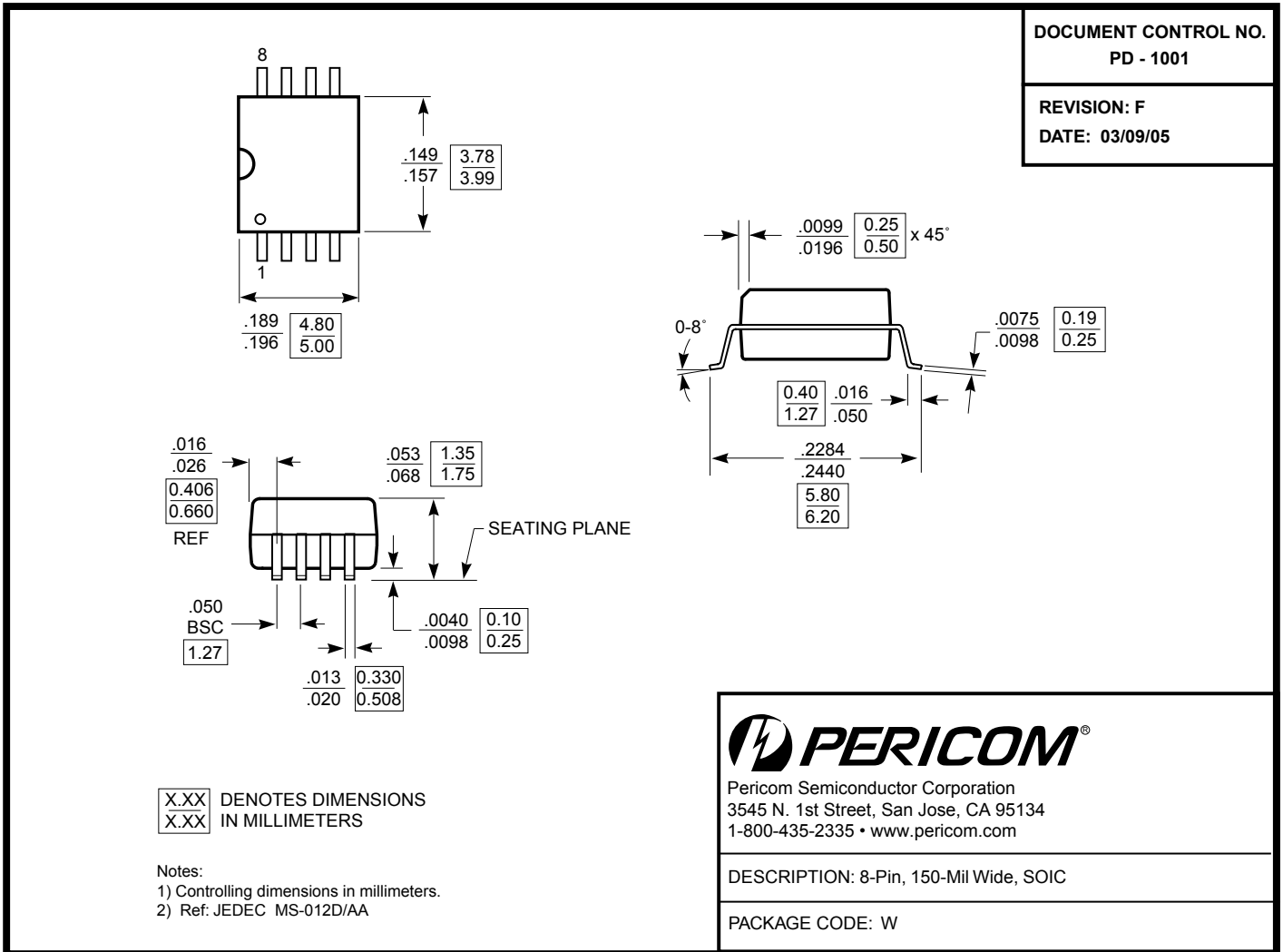
Note:

- See Switching Waveforms
- All clock output should have the same loading to achieve zero delay between the input and outputs and zero output-to-output skew. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-to-output delay. If input-to-output delay adjustments are needed, the CLKOUT load may be changed to vary the delay between the REF input to the clock outputs. Output-to-output skew includes CLK 1-4.
- Specifications are guaranteed by design and not production tested.
- Measured at 100MHz.

Switching Waveforms



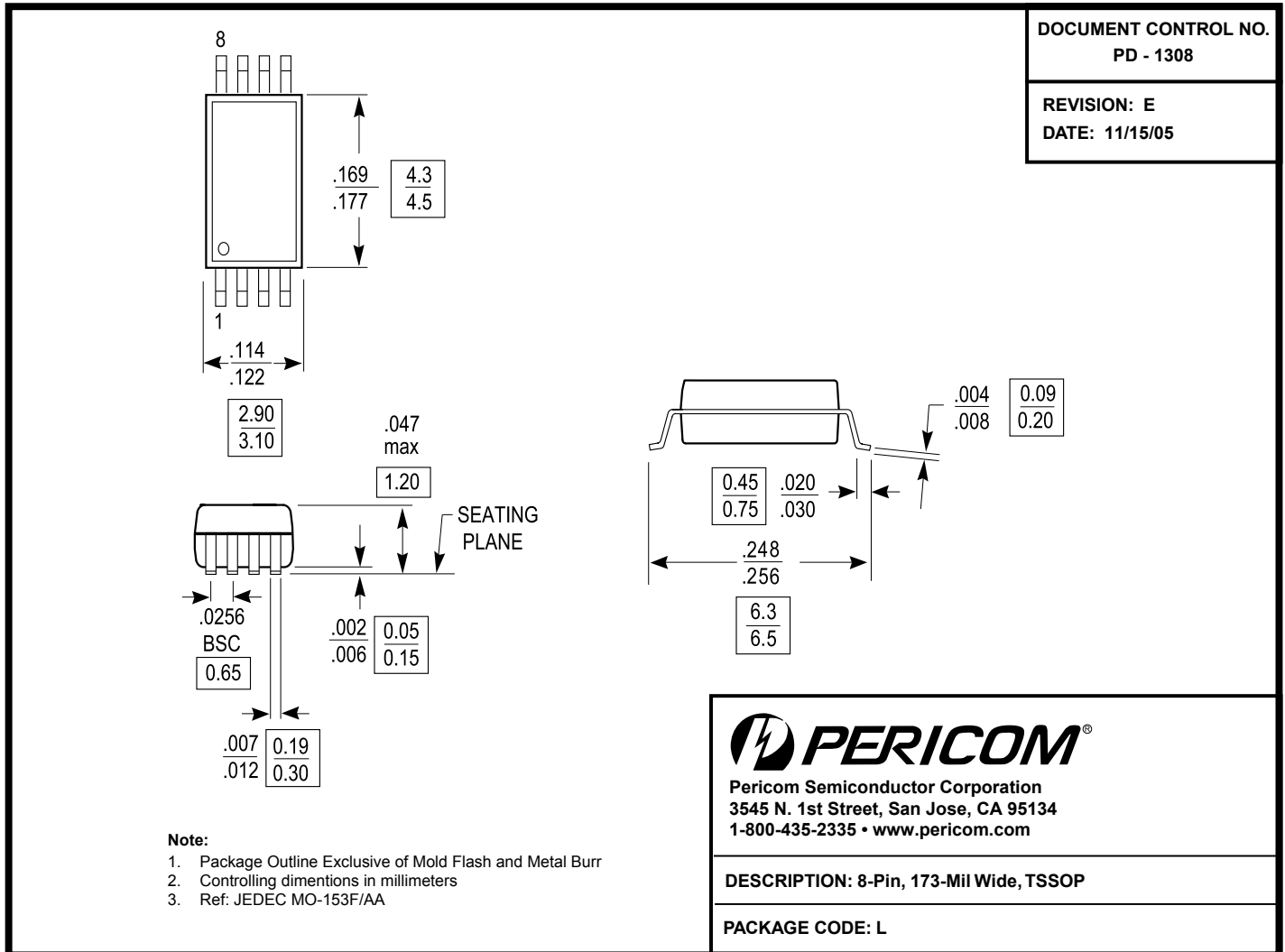
Packaging Mechanical: 8-pin SOIC (W)



Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Packaging Mechanical: 8-pin TSSOP (L)



Note:

• For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information(1,2,3)



| Ordering Code | Package Code | Package Description |
|-----------------|--------------|---|
| PI6C22405-1HWE | W | Pb-free & Green, 8-pin SOIC |
| PI6C22405-1HWIE | W | Pb-free & Green, 8-pin SOIC, Industrial temp range |
| PI6C22405-1HLE | L | Pb-free & Green, 8-pin TSSOP |
| PI6C22405-1HLIE | L | Pb-free & Green, 8-pin TSSOP, Industrial temp range |

Notes:

1. Latest Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. Adding an X suffix = Tape/Reel

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

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-  [Diodes Incorporated Information](#)

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
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