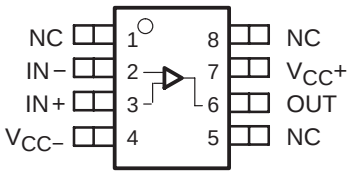
# THE DATASHEET OF

# THS4082CDRG4

www.win-source.net 0086-755-83957316

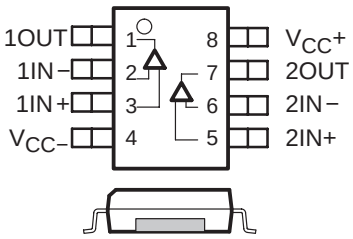
- **Ultralow 3.4 mA Per Channel Quiescent Current**
- **High Speed**
  - **175 MHz Bandwidth (−3 dB, G = 1)**
  - **230 V/μs Slew Rate**
  - **43 ns Settling Time (0.1%)**
- **High Output Drive, $I_O$ = 85 mA (typ)**
- **Excellent Video Performance**
  - **35 MHz Bandwidth (0.1 dB, G = 1)**
  - **0.01% Differential Gain**
  - **0.05° Differential Phase**
- **Very Low Distortion**
  - **THD = −64 dBc (f = 1 MHz, $R_L$ = 150 Ω)**
  - **THD = −79 dBc (f = 1 MHz, $R_L$ = 1 kΩ)**
- **Wide Range of Power Supplies**
  - **$V_{CC}$ = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

**THS4081**
**D OR DGN PACKAGE**
**(TOP VIEW)**




NC − No internal connection

**THS4082**
**D OR DGN PACKAGE**
**(TOP VIEW)**

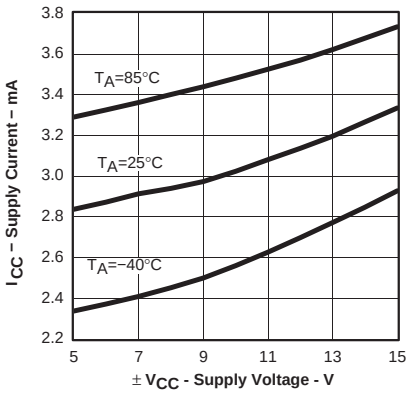



Cross Section View Showing PowerPAD™ Option (DGN)

## description

The THS4081 and THS4082 are ultralow-power, high-speed voltage feedback amplifiers that are ideal for communication and video applications. These amplifiers operate off of a very low 3.4-mA quiescent current per channel and have a high output drive capability of 85 mA. The signal-amplifier THS4081 and the dual-amplifier THS4082 offer very good ac performance with 175-MHz bandwidth, 230-V/μs slew rate, and 43-ns settling time (0.1%). With total harmonic distortion (THD) of −64 dBc at f = 1 MHz, the THS4081 and THS4082 are ideally suited for applications requiring low distortion.

**SUPPLY CURRENT**
**vs**
**SUPPLY VOLTAGE**




| RELATED DEVICES | |
|---|---|
| **DEVICE** | **DESCRIPTION** |
| THS4011/2 | 290-MHz Low Distortion High-Speed Amplifiers |
| THS4031/2 | 100-MHz Low Noise High Speed-Amplifiers |
| THS4051/2 | 70-MHz High-Speed Amplifiers |

CAUTION: The THS4081 and THS4082 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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**AVAILABLE OPTIONS**

| $T_A$ | NUMBER OF CHANNELS | PACKAGED DEVICES | | MSOP SYMBOL | EVALUATION MODULE |
|---|---|---|---|---|---|
| | | PLASTIC SMALL OUTLINE† (D) | PLASTIC MSOP† (DGN) | | |
| 0°C to 70°C | 1 | THS4081CD | THS4081CDGN | AEO | THS4081EVM |
| | 2 | THS4082CD | THS4082CDGN | AER | THS4082EVM |
| −40°C to 85°C | 1 | THS4081ID | THS4081IDGN | AEQ | — |
| | 2 | THS4082ID | THS4082IDGN | AEP | — |

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4081CDGN).

## functional block diagram

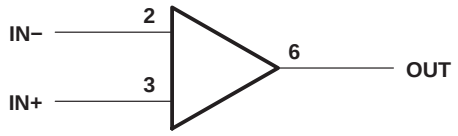



**Figure 1. THS4081 − Single Channel**

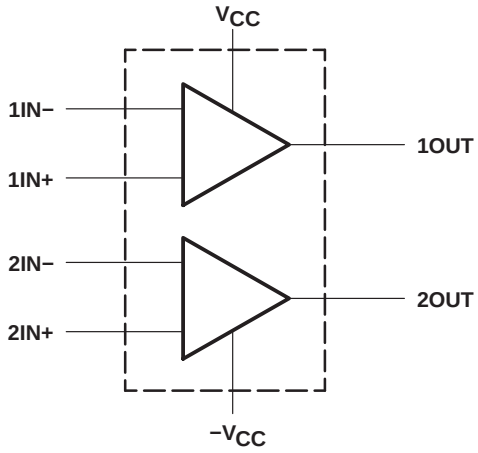



**Figure 2. THS4082 − Dual Channel**

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . ±16.5 V
Input voltage, $V_I$ . . . . . $\pm V_{CC}$
Output current, $I_O$ . . . . . 150 mA
Differential input voltage, $V_{IO}$ . . . . . ±4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Maximum junction temperature, $T_J$ . . . . . 150°C
Operating free-air temperature, $T_A$: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . −40°C to 85°C
Storage temperature, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

| PACKAGE | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) | $T_A$ = 25°C POWER RATING |
|---|---|---|---|
| D | 167‡ | 38.3 | 740 mW |
| DGN§ | 58.4 | 4.7 | 2.14 W |

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the $\theta_{JA}$ is 95°C/W with a power rating at $T_A$ = 25°C of 1.32 W.
§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC+}$ and $V_{CC-}$ | Dual supply | ±5 | | ±15 | V |
| | Single supply | 10 | | 30 | |
| Operating free-air temperature, $T_A$ | C-suffix | 0 | | 70 | °C |
| | I-suffix | −40 | | 85 | |

## electrical characteristics at $T_A$ = 25°C, $V_{CC}$ = ±15 V, $R_L$ = 150 Ω (unless otherwise noted)

### dynamic performance

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| BW | Small-signal bandwidth (−3 dB) | $V_{CC}$ = ±15 V | | Gain = 1 | | 175 | | MHz |
| | | $V_{CC}$ = ±5 V | | | | 160 | | |
| | | $V_{CC}$ = ±15 V | | Gain = −1 | | 70 | | MHz |
| | | $V_{CC}$ = ±5 V | | | | 65 | | |
| | Bandwidth for 0.1 dB flatness | $V_{CC}$ = ±15 V | | Gain = 1 | | 35 | | MHz |
| | | $V_{CC}$ = ±5 V | | | | 35 | | |
| | Full power bandwidth† | $V_{O(pp)}$ = 20 V, | $V_{CC}$ = ±15 V | | | 2.7 | | MHz |
| | | $V_{O(pp)}$ = 5 V, | $V_{CC}$ = ±5 V | | | 7.1 | | |
| SR | Slew rate‡ | $V_{CC}$ = ±15 V, | 20-V step, | Gain = 5 | | 230 | | V/µs |
| | | $V_{CC}$ = ±5 V, | 5-V step | Gain = 1 | | 170 | | |
| $t_s$ | Settling time to 0.1% | $V_{CC}$ = ±15 V, | 5-V step | Gain = −1 | | 43 | | ns |
| | | $V_{CC}$ = ±5 V, | 2-V step | | | 30 | | |
| | Settling time to 0.01% | $V_{CC}$ = ±15 V, | 5-V step | Gain = −1 | | 233 | | ns |
| | | $V_{CC}$ = ±5 V, | 2-V step | | | 280 | | |

† Slew rate is measured from an output level range of 25% to 75%.
‡ Full power bandwidth = slew rate/2π $V_{O(Peak)}$.

### noise/distortion performance

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | $V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2 | $V_{CC}$ = ±15 V | $R_L$ = 150 Ω | | −64 | | dBc |
| | | | | $R_L$ = 1 kΩ | | −79 | | |
| | | | $V_{CC}$ = ±5 V | $R_L$ = 150 Ω | | −64 | | |
| | | | | $R_L$ = 1 kΩ | | −77 | | |
| $V_n$ | Input voltage noise | $V_{CC}$ = ±5 V or ±15 V, | f = 10 kHz | | | 10 | | nV/√Hz |
| $I_n$ | Input current noise | $V_{CC}$ = ±5 V or ±15 V, | f = 10 kHz | | | 0.7 | | pA/√Hz |
| | Differential gain error | Gain = 2, 40 IRE modulation, | NTSC, ±100 IRE ramp | $V_{CC}$ = ±15 V | | 0.01% | | |
| | | | | $V_{CC}$ = ±5 V | | 0.01% | | |
| | Differential phase error | Gain = 2, 40 IRE modulation, | NTSC, ±100 IRE ramp | $V_{CC}$ = ±15 V | | 0.05° | | |
| | | | | $V_{CC}$ = ±5 V | | 0.05° | | |
| $X_T$ | Channel-to-channel crosstalk (THS4082 only) | $V_{CC}$ = ±5 V or ±15 V, | f = 1 MHz | | | −75 | | dB |

## electrical characteristics at $T_A$ = 25°C, $V_{CC}$ = ±15 V, $R_L$ = 150 Ω (unless otherwise noted) (continued)

### dc performance

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Open loop gain | $V_{CC}$ = ±15 V, $V_O$ = ±10 V, $R_L$ = 1 kΩ | $T_A$ = 25°C | 10 | 19 | | V/mV |
| | | | $T_A$ = full range† | 9 | | | |
| | | $V_{CC}$ = ±5 V, $V_O$ = ±2.5 V, $R_L$ = 250 Ω | $T_A$ = 25°C | 8 | 16 | | V/mV |
| | | | $T_A$ = full range† | 7 | | | |
| $V_{OS}$ | Input offset voltage | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 1 | 7 | mV |
| | | | $T_A$ = full range† | | | 8 | |
| | Offset voltage drift | | $T_A$ = full range† | | 15 | | µV/°C |
| $I_{IB}$ | Input bias current | | $T_A$ = 25°C | | 1.2 | 6 | µA |
| | | | $T_A$ = full range† | | | 8 | |
| $I_{OS}$ | Input offset current | | $T_A$ = 25°C | | 20 | 250 | nA |
| | | | $T_A$ = full range† | | | 400 | |
| | Offset current drift | $T_A$ = full range† | | | 0.3 | | nA/°C |

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

### input characteristics

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{ICR}$ | Common mode input voltage range | $V_{CC}$ = ±15 V | | ±13.8 | ±14.1 | | V |
| | | $V_{CC}$ = ±5 V | | ±3.8 | ±3.9 | | |
| CMRR | Common mode rejection ratio | $V_{CC}$ = ±15 V, $V_{ICR}$ = ±12 V, | $T_A$ = full range† | 78 | 90 | | dB |
| | | $V_{CC}$ = ±5 V, $V_{ICR}$ = ±2 V, | $T_A$ = full range† | 84 | 93 | | dB |
| $R_I$ | Input resistance | | | | 1 | | MΩ |
| $C_I$ | Input capacitance | | | | 1.5 | | pF |

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

### output characteristics

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output voltage swing | $V_{CC}$ = ±15 V, | $R_L$ = 250 Ω | ±12 | ±13.6 | | V |
| | | $V_{CC}$ = ±5 V, | $R_L$ = 150 Ω | ±3.4 | ±3.8 | | |
| | | $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ | ±13.5 | ±13.8 | | V |
| | | $V_{CC}$ = ±5 V | | ±3.5 | ±3.9 | | |
| $I_O$ | Output current | $V_{CC}$ = ±15 V | $R_L$ = 20 Ω | 65 | 85 | | mA |
| | | $V_{CC}$ = ±5 V | | 50 | 70 | | |
| $I_{SC}$ | Short-circuit current‡ | $V_{CC}$ = ±15 V | | | 100 | | mA |
| $R_O$ | Output resistance | Open loop | | | 13 | | Ω |

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

## electrical characteristics at $T_A$ = 25°C, $V_{CC}$ = ±15 V, $R_L$ = 150 Ω (unless otherwise noted) (continued)

### power supply

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage operating range | Dual supply | | ±4.5 | | ±16.5 | V |
| | | Single supply | | 9 | | 33 | |
| $I_{CC}$ | Supply current (per amplifier) | $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 3.4 | 4.2 | mA |
| | | | $T_A$ = full range† | | | 5 | |
| | | $V_{CC}$ = ±5 V | $T_A$ = 25°C | | 2.9 | 3.7 | |
| | | | $T_A$ = full range† | | | 4.5 | |
| PSRR | Power supply rejection ratio | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = full range† | 79 | 90 | | dB |

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

## TYPICAL CHARACTERISTICS

**OPEN LOOP GAIN & PHASE RESPONSE vs FREQUENCY**

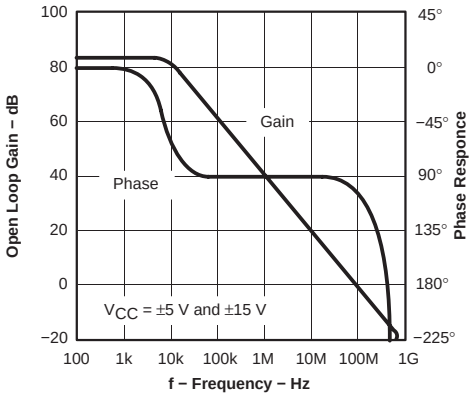



Figure 3

**CROSSTALK vs FREQUENCY**

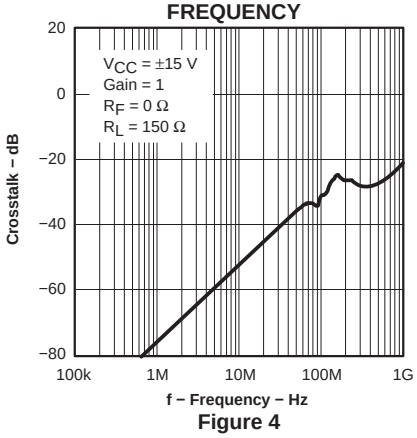



Figure 4

**TOTAL HARMONIC DISTORTION vs FREQUENCY**

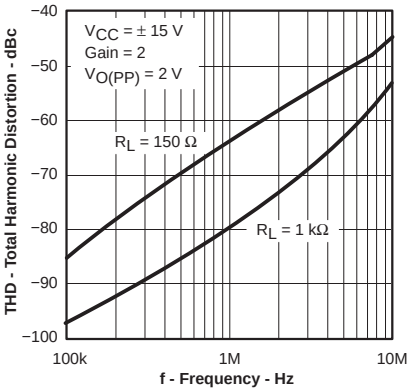



Figure 5

**TOTAL HARMONIC DISTORTION vs FREQUENCY**

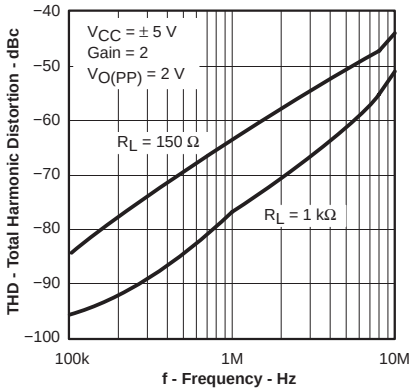



Figure 6

**SETTLING vs OUTPUT STEP**

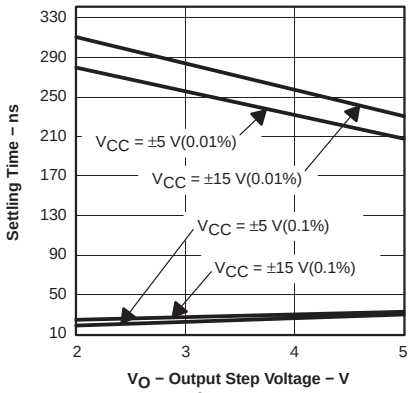



Figure 7

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

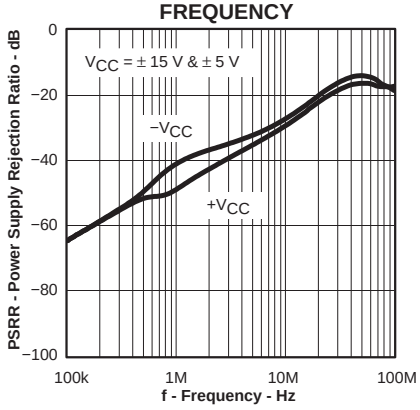



Figure 8

**DISTORTION vs OUTPUT VOLTAGE**

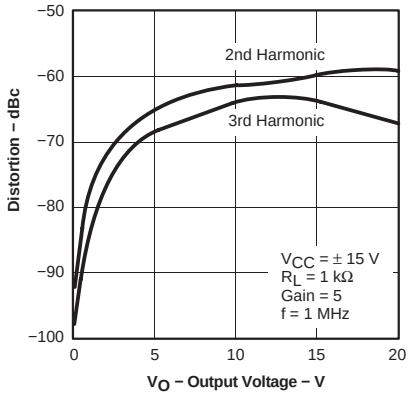



Figure 9

**DISTORTION vs OUTPUT VOLTAGE**

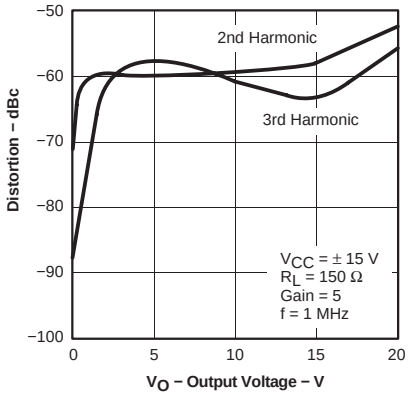



Figure 10

## TYPICAL CHARACTERISTICS

**DISTORTION vs FREQUENCY**

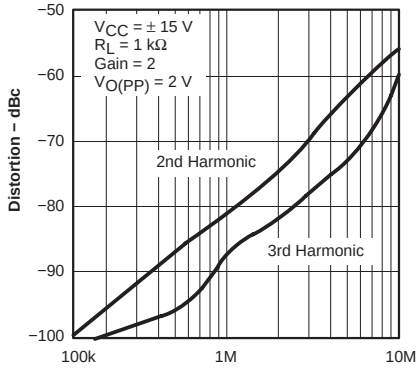



**Figure 11**

**DISTORTION vs FREQUENCY**

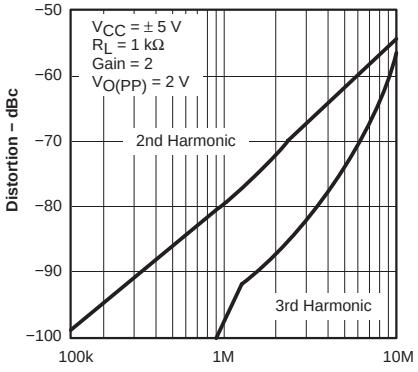



**Figure 12**

**DISTORTION vs FREQUENCY**

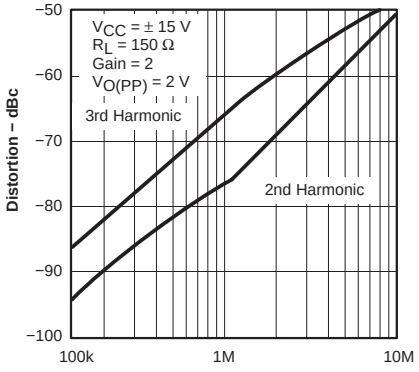



**Figure 13**

**DISTORTION vs FREQUENCY**

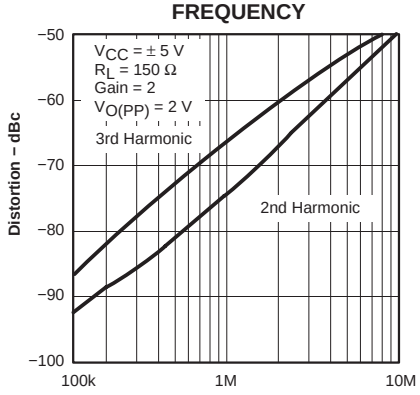



**Figure 14**

**OUTPUT AMPLITUDE vs FREQUENCY**

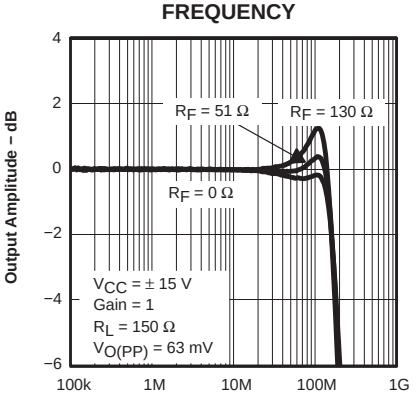



**Figure 15**

**OUTPUT AMPLITUDE vs FREQUENCY**

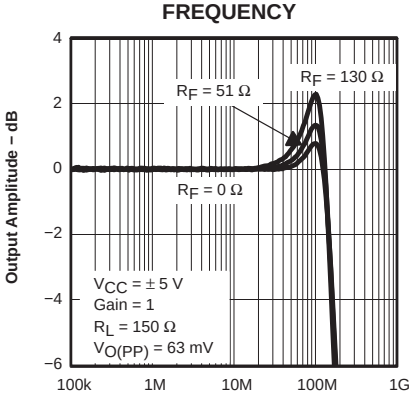



**Figure 16**

**OUTPUT AMPLITUDE vs FREQUENCY**

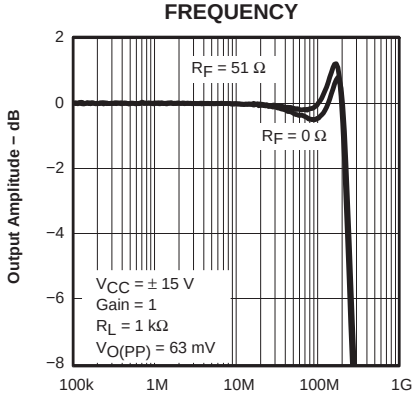



**Figure 17**

**OUTPUT AMPLITUDE vs FREQUENCY**

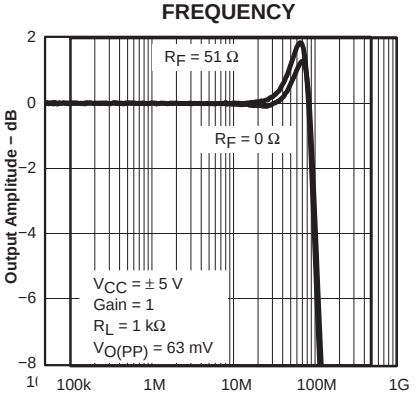



**Figure 18**

**OUTPUT AMPLITUDE vs FREQUENCY**

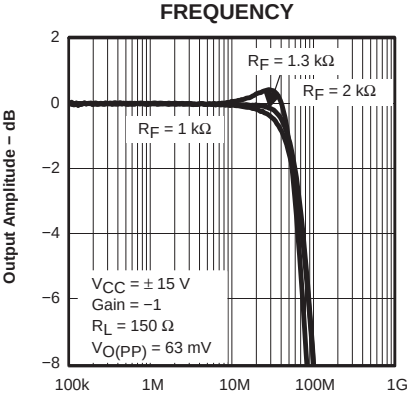



**Figure 19**

## TYPICAL CHARACTERISTICS

**OUTPUT AMPLITUDE vs FREQUENCY**

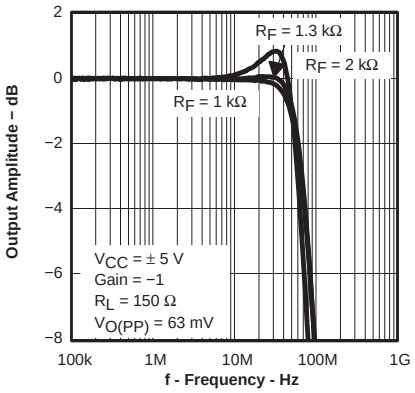



Figure 20

**OUTPUT AMPLITUDE vs FREQUENCY**

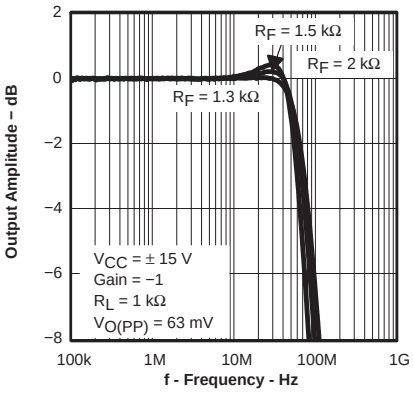



Figure 21

**OUTPUT AMPLITUDE vs FREQUENCY**

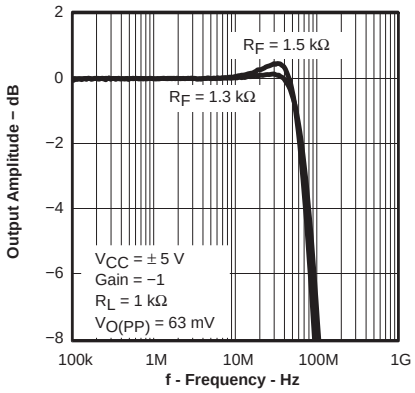



Figure 22

**OUTPUT AMPLITUDE vs FREQUENCY**

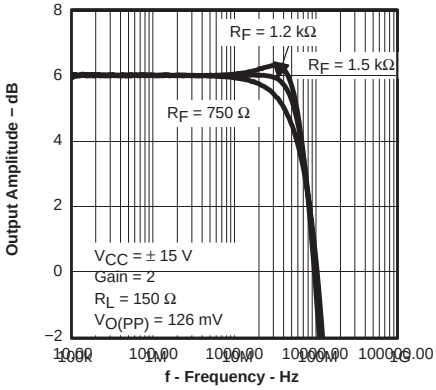



Figure 23

**OUTPUT AMPLITUDE vs FREQUENCY**

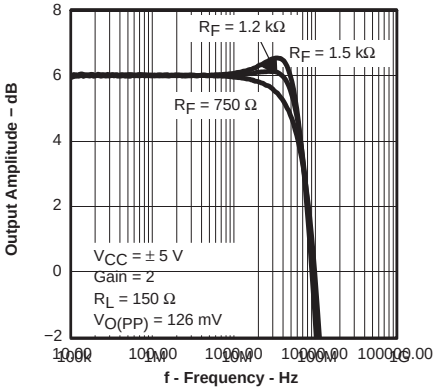



Figure 24

**OUTPUT AMPLITUDE vs FREQUENCY**

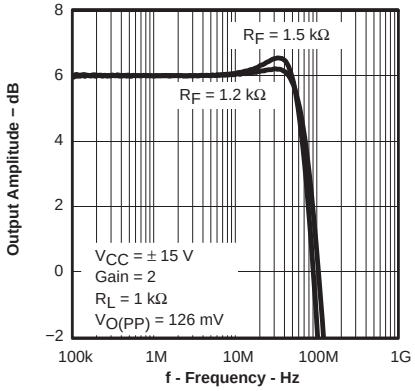



Figure 25

**OUTPUT AMPLITUDE vs FREQUENCY**

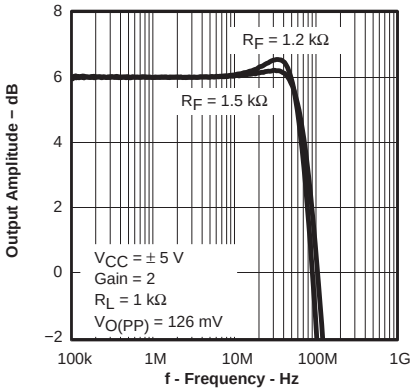



Figure 26

**2-V STEP RESPONSE**

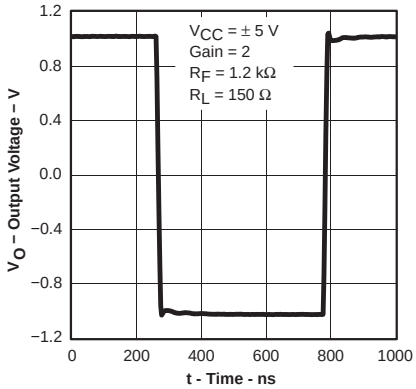



Figure 27

**5-V STEP RESPONSE**

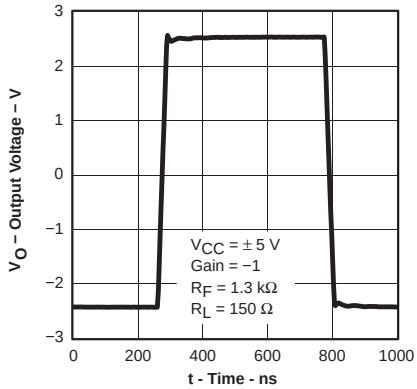



Figure 28

## TYPICAL CHARACTERISTICS

**2-V STEP RESPONSE**

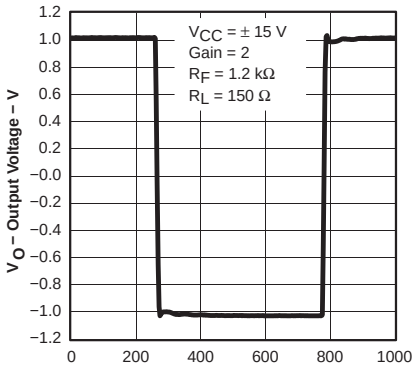



Figure 29

**20-V STEP RESPONSE**

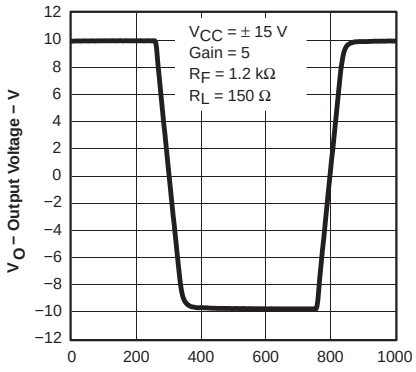



Figure 30

**INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE**

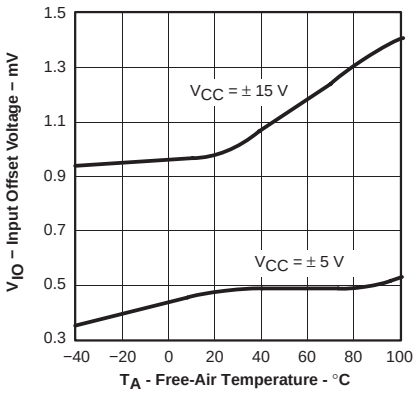



Figure 31

**INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE**

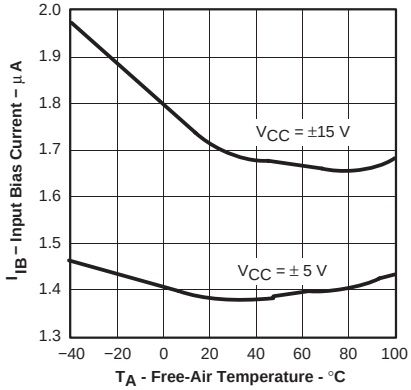



Figure 32

**OUTPUT VOLTAGE vs SUPPLY VOLTAGE**

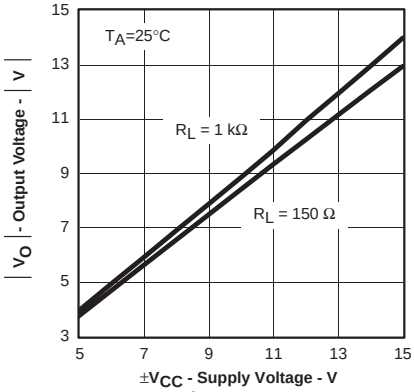



Figure 33

**COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE**

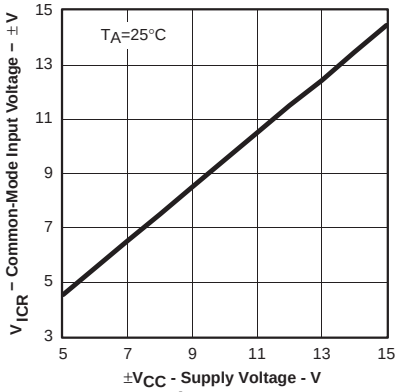



Figure 34

**OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

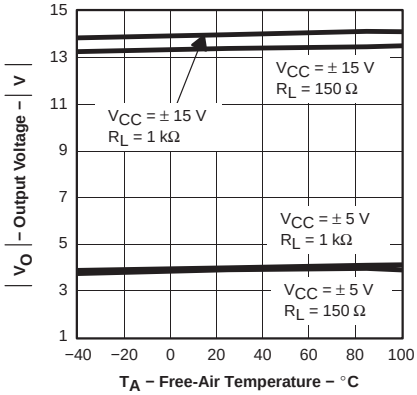



Figure 35

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

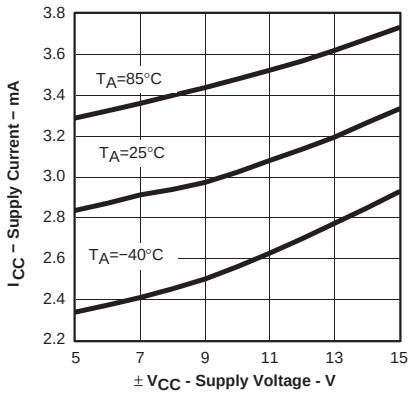



Figure 36

**VOLTAGE & CURRENT NOISE vs FREQUENCY**

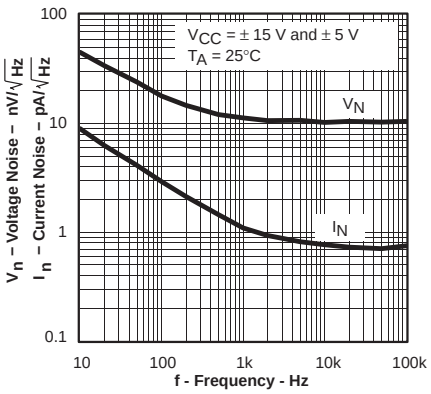



Figure 37

## APPLICATION INFORMATION

### theory of operation

The THS408x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing $f_T$s of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 38.

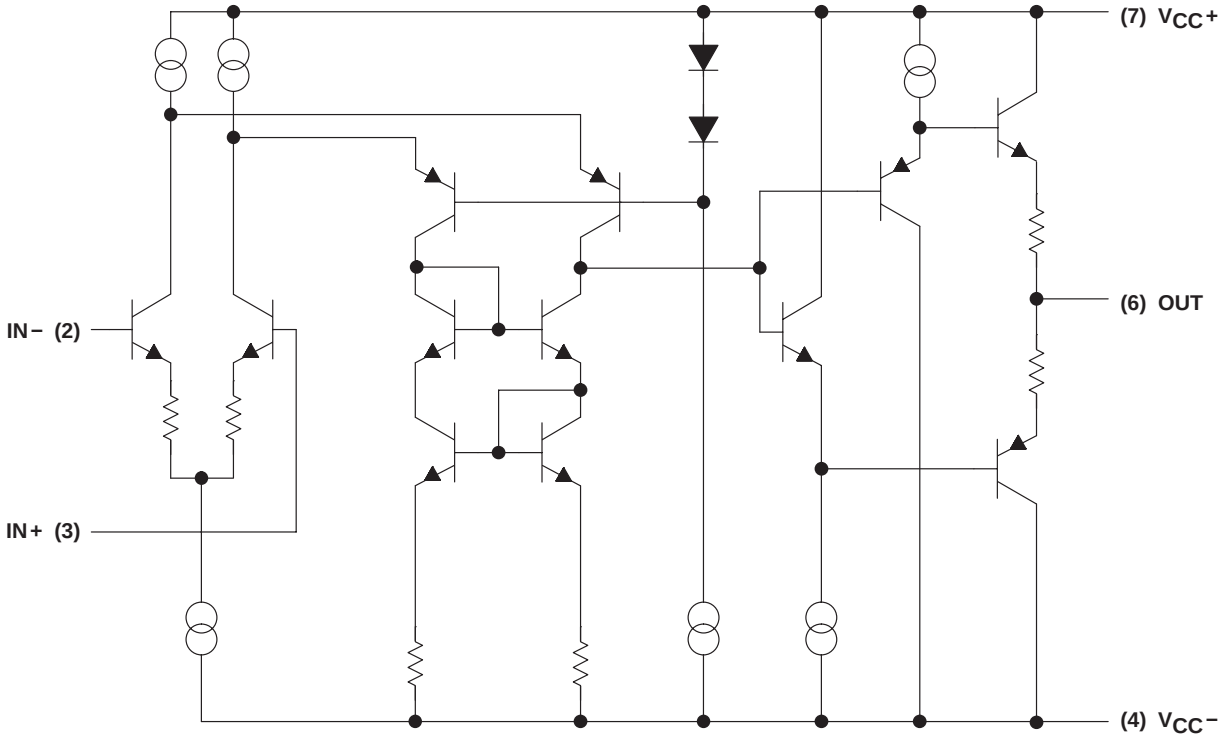



**Figure 38. THS4081 Simplified Schematic**

### noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is very important. The noise model for the THS408x is shown in Figure 39. This model includes all of the noise sources as follows:

- $e_n$ = Amplifier internal voltage noise (nV/$\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise (pA/$\sqrt{\text{Hz}}$)
- IN− = Inverting current noise (pA/$\sqrt{\text{Hz}}$)
- $e_{Rx}$ = Thermal voltage noise associated with each resistor ($e_{Rx}$ = 4 kT$R_x$)

## APPLICATION INFORMATION

### noise calculations and noise figure (continued)

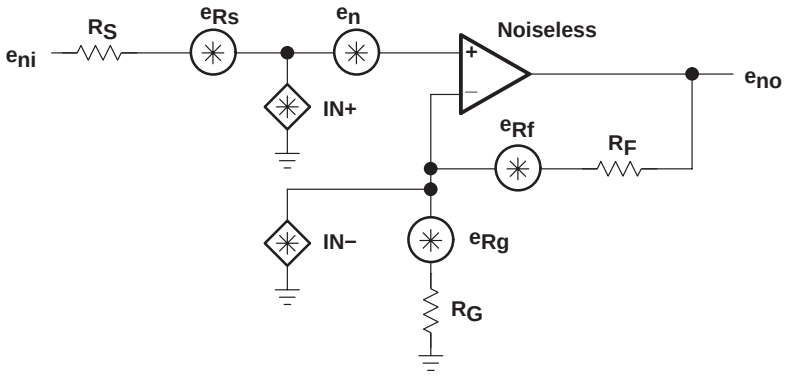



**Figure 39. Noise Model**

The total equivalent input noise density ($e_{ni}$) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = $1.380658 \times 10^{-23}$
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of $R_F$ and $R_G$

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density ($e_{ni}$) by the overall amplifier gain ($A_V$).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing $R_G$), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor ($R_S$) and the internal amplifier noise voltage ($e_n$). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

## APPLICATION INFORMATION

### noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{2}}{\left(e_{Rs}\right)^{2}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_{n}\right)^{2} + \left(IN + \times R_{S}\right)^{2}\right]}{4\,kTR_{S}}\right]$$

Figure 40 shows the noise figure graph for the THS408x.

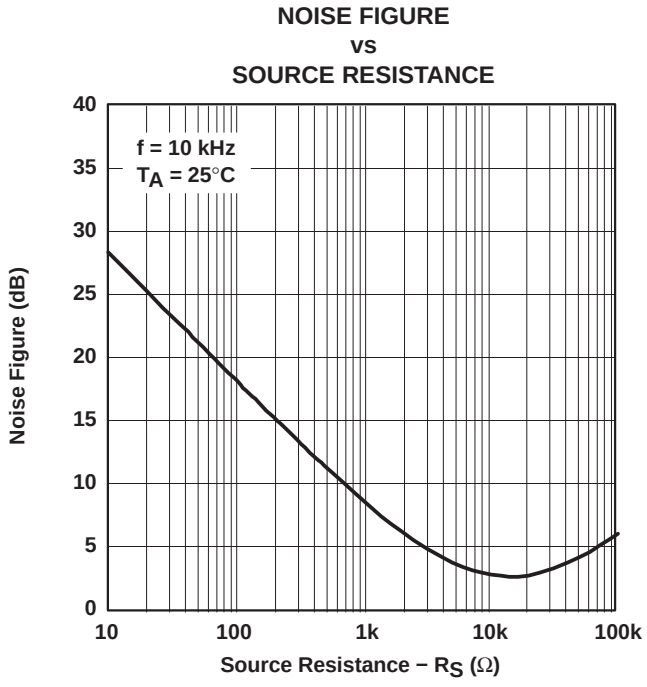



**Figure 40. Noise Figure vs Source Resistance**

## APPLICATION INFORMATION

### driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS408x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 41. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

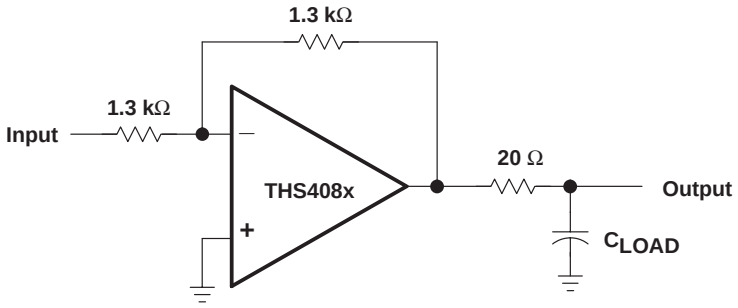
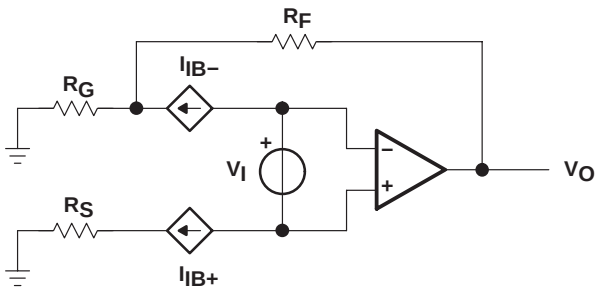



**Figure 41. Driving a Capacitive Load**

### offset voltage

The output offset voltage, ($V_{OO}$) is the sum of the input offset voltage ($V_{IO}$) and both input bias currents ($I_{IB}$) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:




$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

**Figure 42. Output Offset Voltage Model**

## APPLICATION INFORMATION

### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 43).

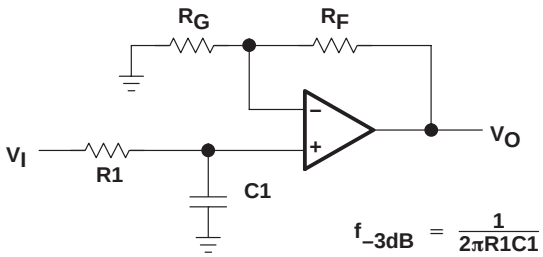



**Figure 43. Single-Pole Low-Pass Filter**

### circuit layout considerations

To achieve the levels of high frequency performance of the THS408x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS408x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

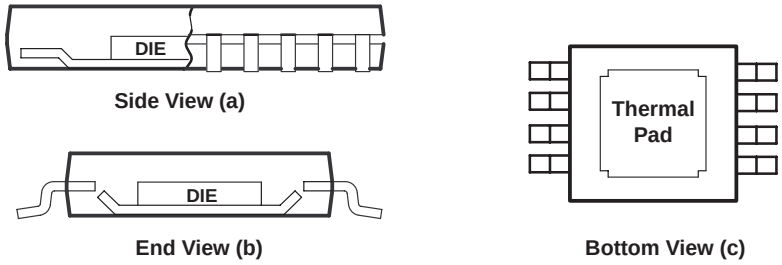
## APPLICATION INFORMATION

### general PowerPAD™ design considerations

The THS408x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD™ family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 44(a) and Figure 44(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 44(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD™ package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.




NOTE A: The thermal pad is electrically isolated from all terminals in the package.

**Figure 44. Views of Thermally Enhanced DGN Package**

## APPLICATION INFORMATION

### general PowerPAD™ design considerations (continued)

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

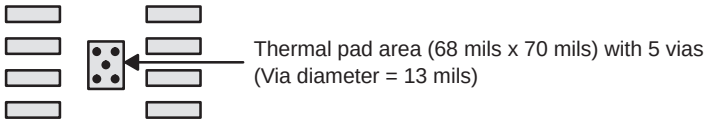



**Figure 45. PowerPAD PCB Etch and Via Pattern**

1. Prepare the PCB with a top side etch pattern as shown in Figure 45. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS408xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS408xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS408xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

## APPLICATION INFORMATION

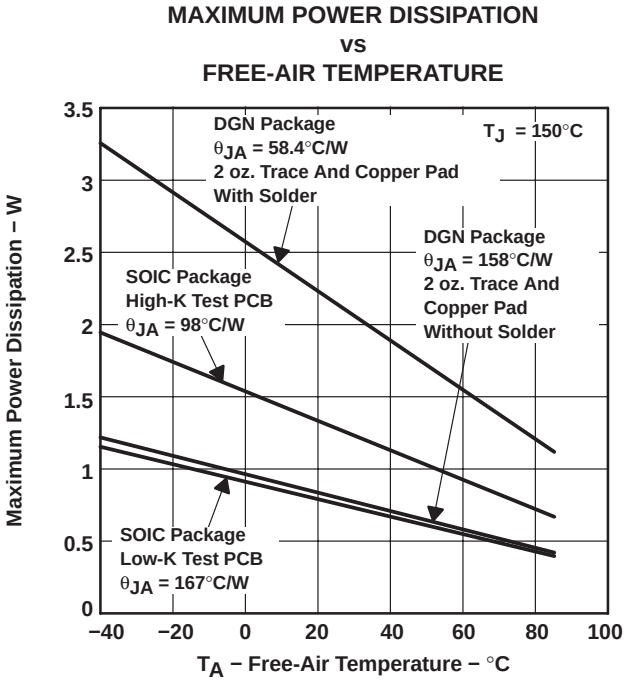
### general PowerPAD™ design considerations (continued)

The actual thermal performance achieved with the THS408xDGN in its PowerPAD™ package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, $\theta_{JA}$, is about 58.4°C/W. For comparison, the non-PowerPAD™ version of the THS408x IC (SOIC) is shown. For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 46 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

$P_D$ = Maximum power dissipation of THS408x IC (watts)
$T_{MAX}$ = Absolute maximum junction temperature (150°C)
$T_A$ = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
$\theta_{JC}$ = Thermal coefficient from junction to case
$\theta_{CA}$ = Thermal coefficient from case to ambient air (°C/W)




NOTE A: Results are with no air flow and PCB size = 3”× 3”

**Figure 46. Maximum Power Dissipation vs Free-Air Temperature**

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

## APPLICATION INFORMATION

### general PowerPAD™ design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 47 to Figure 50 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using $V_{CC}$ = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using $V_{CC}$ = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD™ devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD™. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, $\theta_{JA}$ decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4082), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier's outputs are identical.

**THS4081**
**MAXIMUM RMS OUTPUT CURRENT**
**vs**
**RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS**

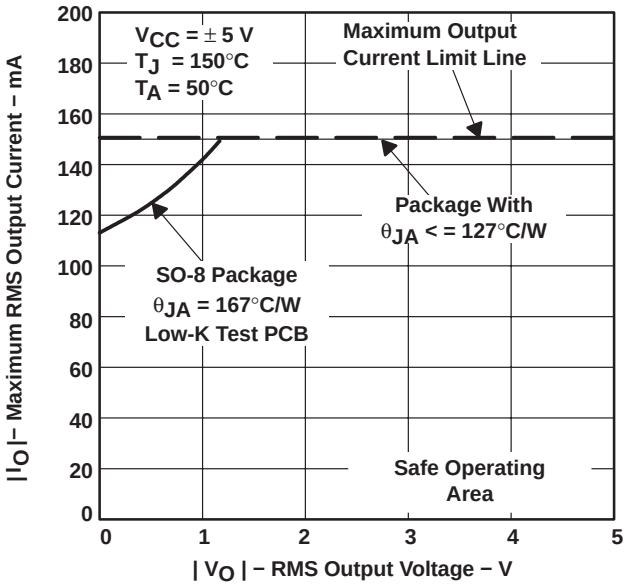



**Figure 47**

**THS4081**
**MAXIMUM RMS OUTPUT CURRENT**
**vs**
**RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS**

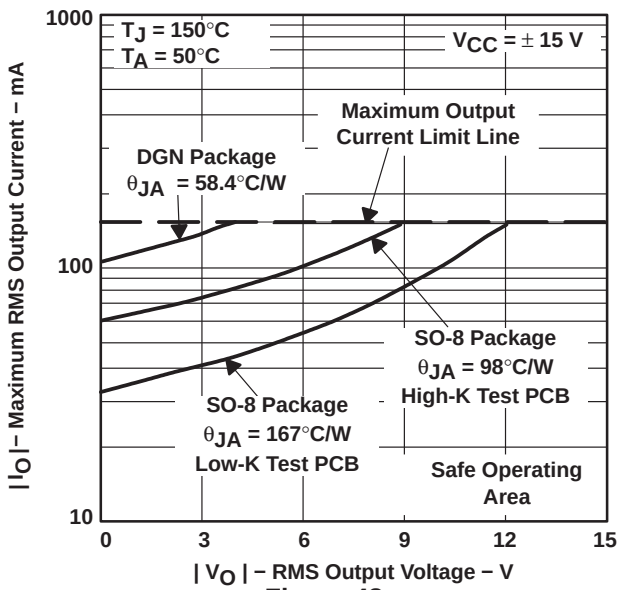



**Figure 48**

## APPLICATION INFORMATION

### general PowerPAD™ design considerations (continued)

THS4082
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

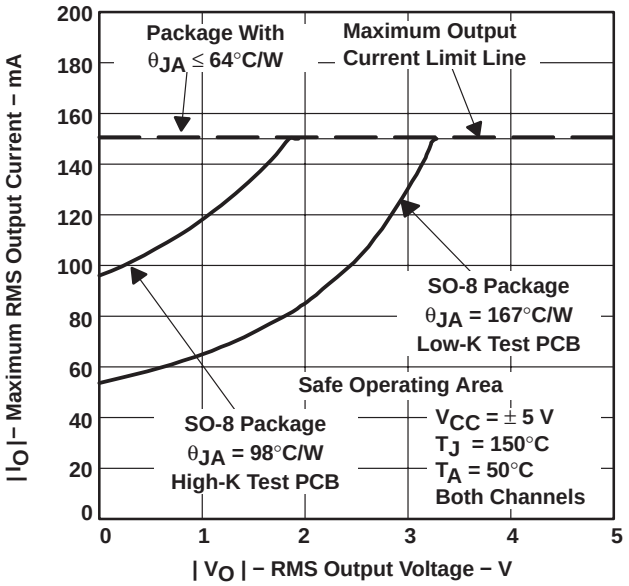



Figure 49

THS4082
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

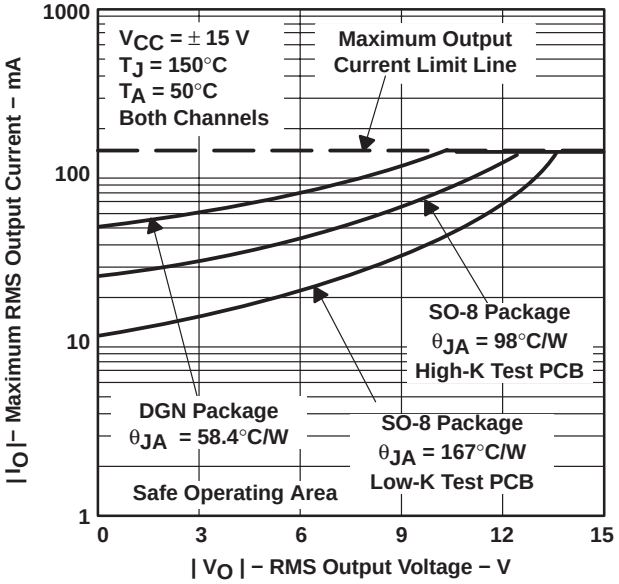



Figure 50

## APPLICATION INFORMATION

### evaluation board

An evaluation board is available for the THS4081 (literature number SLOP242) and THS4082 (literature number SLOP239). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 51. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4081 EVM User's Guide* or the *THS4082 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

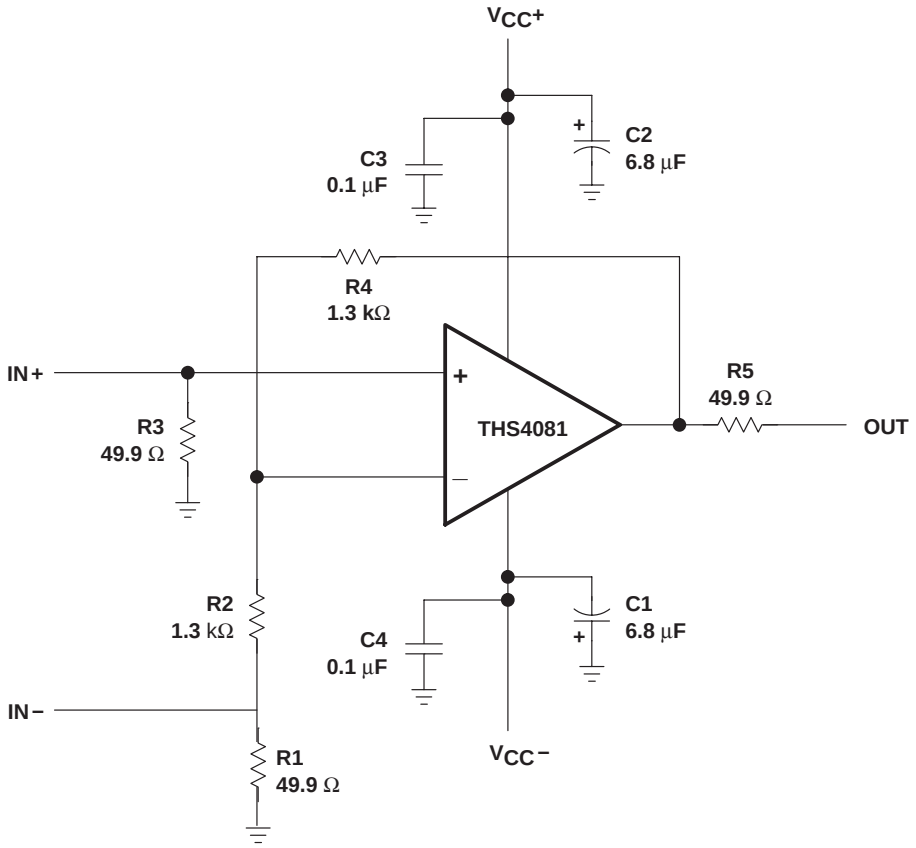



**Figure 51. THS4081 Evaluation Board**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| THS4081CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 4081C | Samples |
| THS4081CDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AEO | Samples |
| THS4081CDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AEO | Samples |
| THS4081CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 4081C | Samples |
| THS4081ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 4081I | Samples |
| THS4081IDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AEQ | Samples |
| THS4081IDGNG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AEQ | Samples |
| THS4081IDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AEQ | Samples |
| THS4082CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 4082C | Samples |
| THS4082CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 4082C | Samples |
| THS4082CDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AER | Samples |
| THS4082CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 4082C | Samples |
| THS4082ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 4082I | Samples |
| THS4082IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 4082I | Samples |
| THS4082IDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU \| Call TI | Level-1-260C-UNLIM | -40 to 85 | AEP | Samples |
| THS4082IDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| Call TI | Level-1-260C-UNLIM | -40 to 85 | AEP | Samples |
| THS4082IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 4082I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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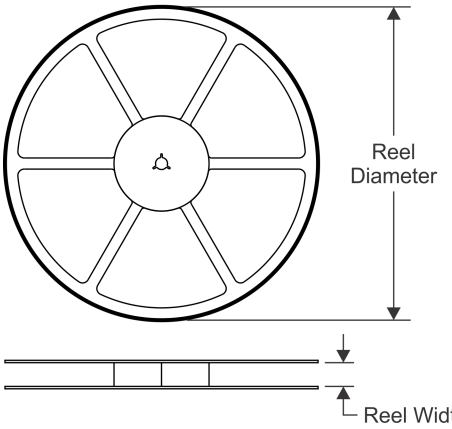
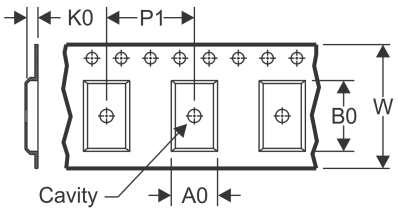
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

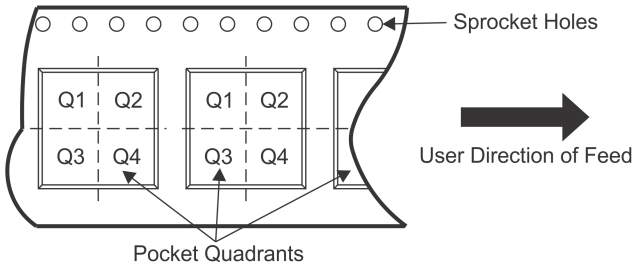



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

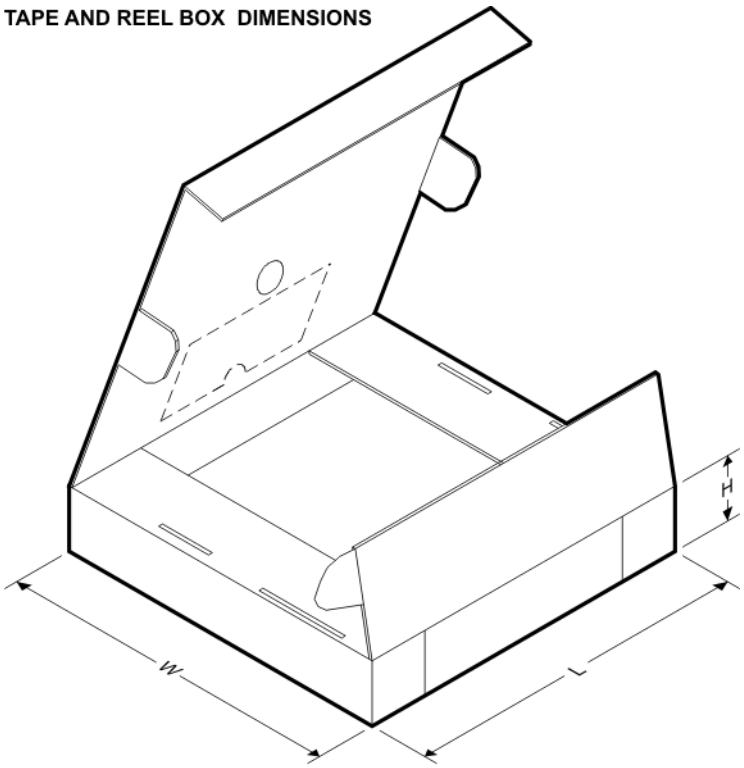
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

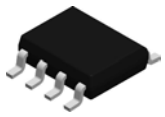
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THS4081CDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| THS4081CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS4081IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| THS4082CDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| THS4082CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS4082IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| THS4082IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THS4081CDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| THS4081CDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| THS4081IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| THS4082CDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| THS4082CDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| THS4082IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| THS4082IDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |

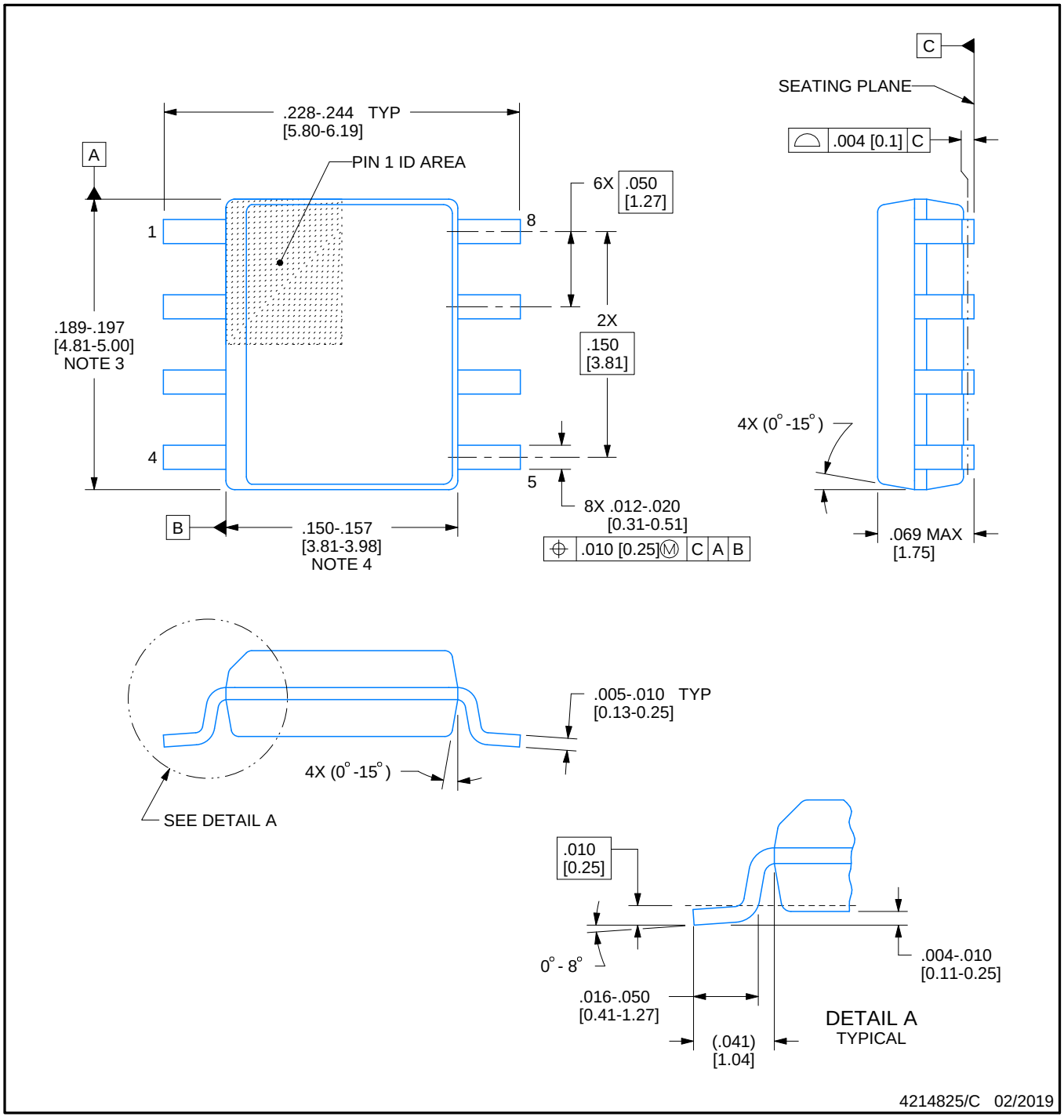


# PACKAGE OUTLINE

## D0008A

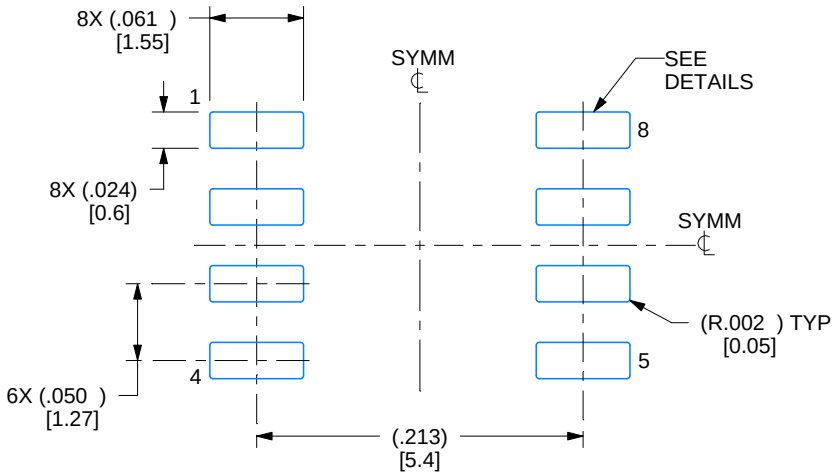
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

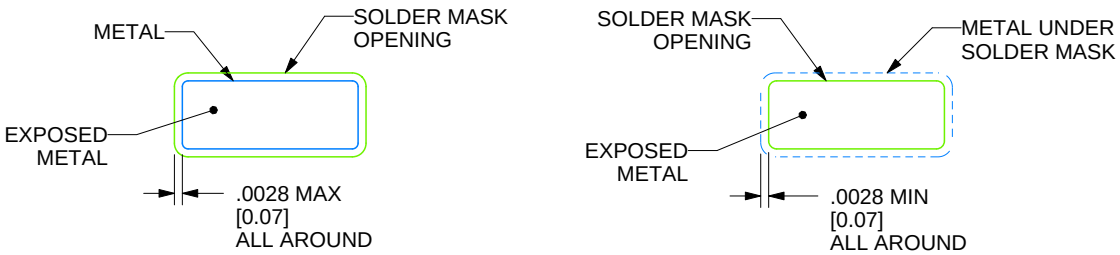



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

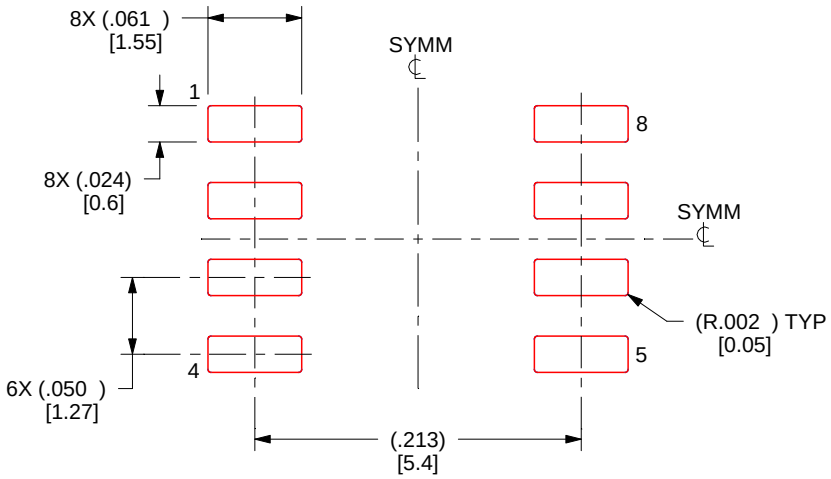
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



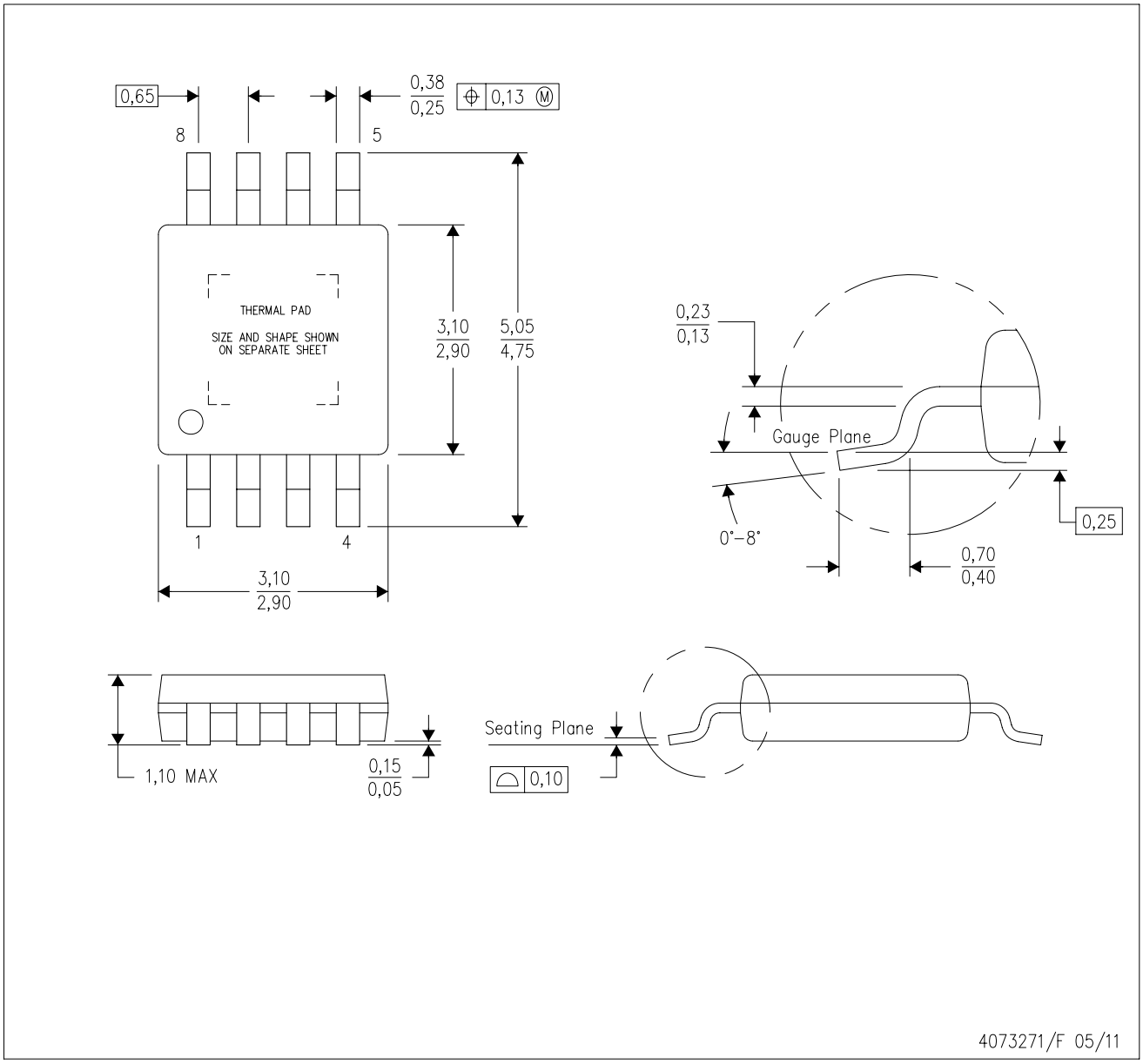

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

**PowerPAD is a trademark of Texas Instruments.**

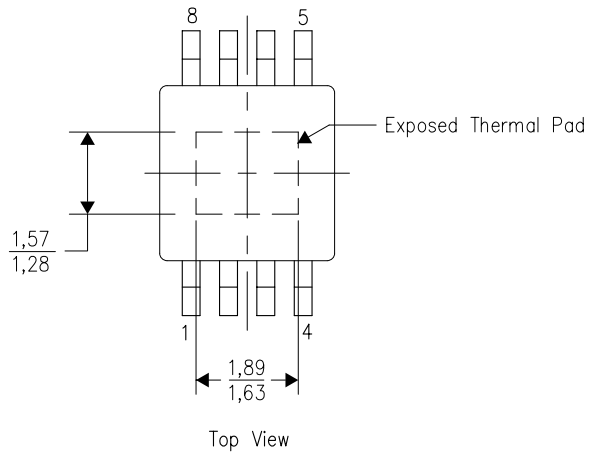
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

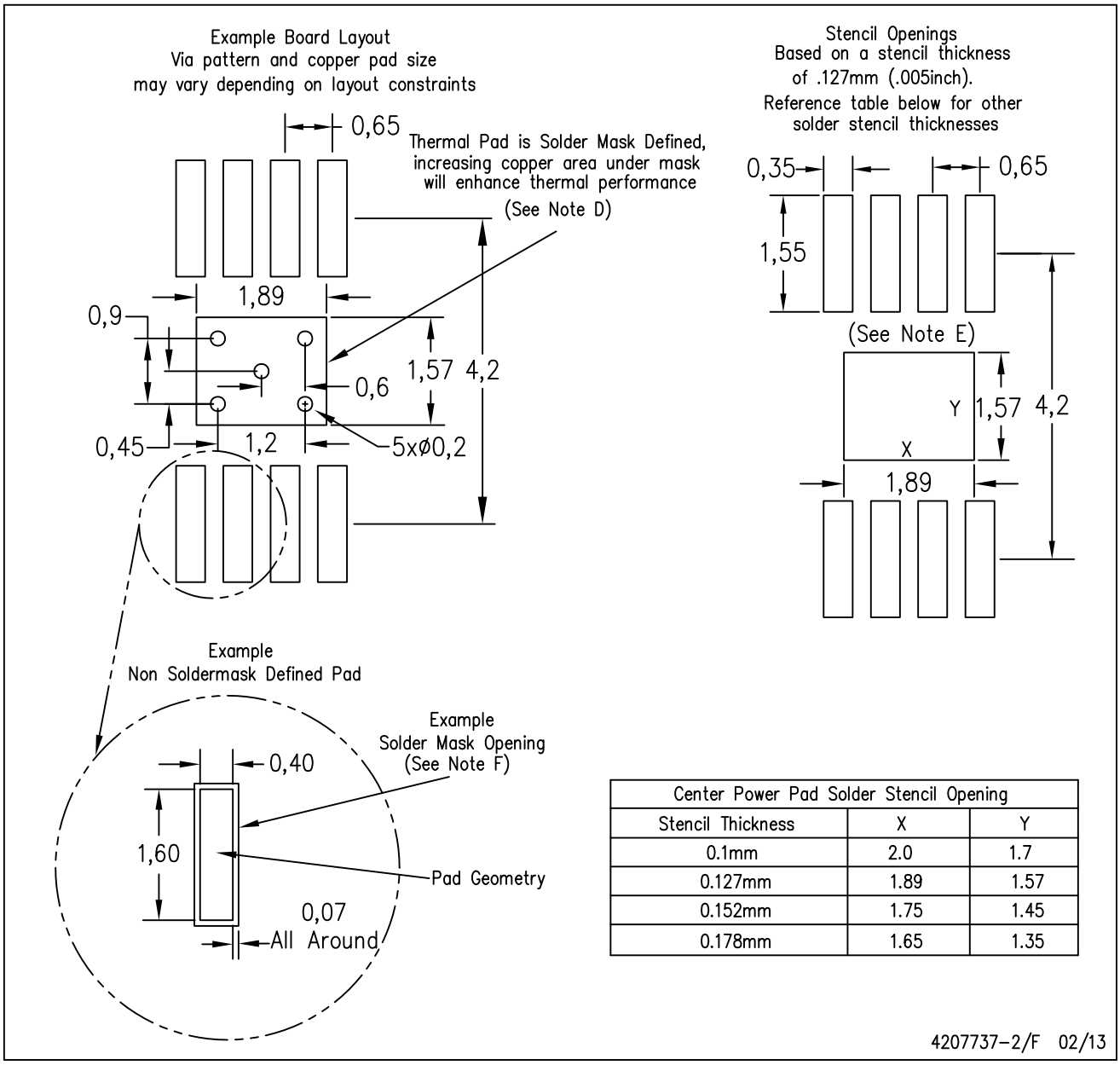
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.89 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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