MCP1700

Low Quiescent Current LDO

Features

- AEC-Q100 Qualified and PPAP Capable
- 1.6 µA Typical Quiescent Current
- Input Operating Voltage Range: 2.3V to 6.0V
- Output Voltage Range: 1.2V to 5.0V
- 250 mA Output Current for Output Voltages ≥ 2.5V
- 200 mA Output Current for Output Voltages < 2.5V
- Low Dropout (LDO) Voltage
  - 178 mV Typical @ 250 mA for V_{OUT} = 2.8V
- 0.4% Typical Output Voltage Tolerance
- Standard Output Voltage Options:
  - 1.2V, 1.8V, 2.5V, 2.8V, 2.9V, 3.0V, 3.3V, 5.0V
- Stable with 1.0 µF Ceramic Output Capacitor
- Short Circuit Protection
- Overtemperature Protection

Applications

- Battery-Powered Devices
- Battery-Powered Alarm Circuits
- Smoke Detectors
- CO_2 Detectors
- Pagers and Cellular Phones
- Smart Battery Packs
- Low Quiescent Current Voltage Reference
- PDAs
- Digital Cameras
- Microcontroller Power

Related Literature

- AN765, *"Using Microchip's Micropower LDOs"* (DS00765), Microchip Technology Inc., 2002
- AN766, *"Pin-Compatible CMOS Upgrades to BiPolar LDOs"* (DS00766), Microchip Technology Inc., 2002
- AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), Microchip Technology Inc., 2001

General Description

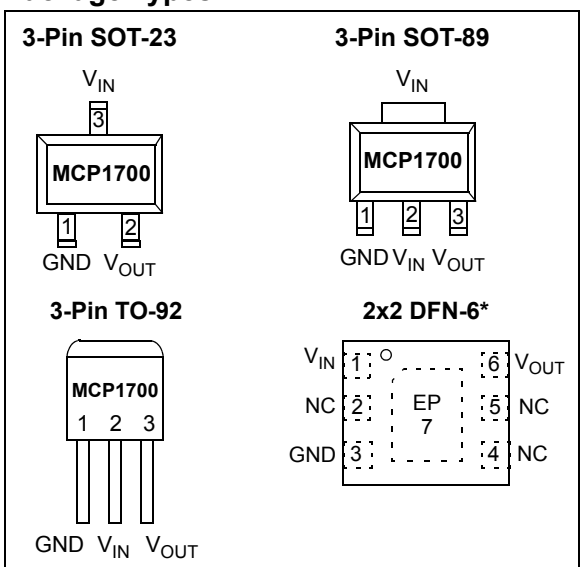
The MCP1700 is a family of CMOS low dropout (LDO) voltage regulators that can deliver up to 250 mA of current while consuming only 1.6 µA of quiescent current (typical). The input operating range is specified from 2.3V to 6.0V, making it an ideal choice for two and three primary cell battery-powered applications, as well as single cell Li-Ion-powered applications.

The MCP1700 is capable of delivering 250 mA with only 178 mV of input to output voltage differential (V_{OUT} = 2.8V). The output voltage tolerance of the MCP1700 is typically ±0.4% at +25°C and ±3% maximum over the operating junction temperature range of -40°C to +125°C.

Output voltages available for the MCP1700 range from 1.2V to 5.0V. The LDO output is stable when using only 1 µF output capacitance. Ceramic, tantalum or aluminum electrolytic capacitors can all be used for input and output. Overcurrent limit and overtemperature shutdown provide a robust solution for any application.

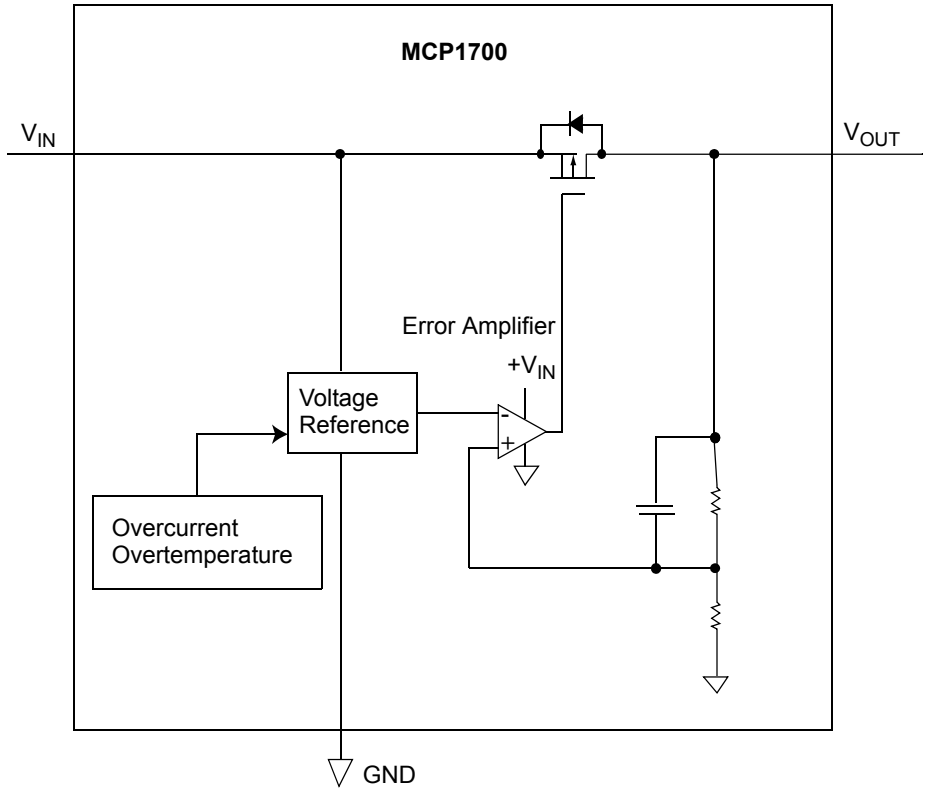
Package options include SOT-23, SOT-89, TO-92 and 2x2 DFN-6.

Package Types

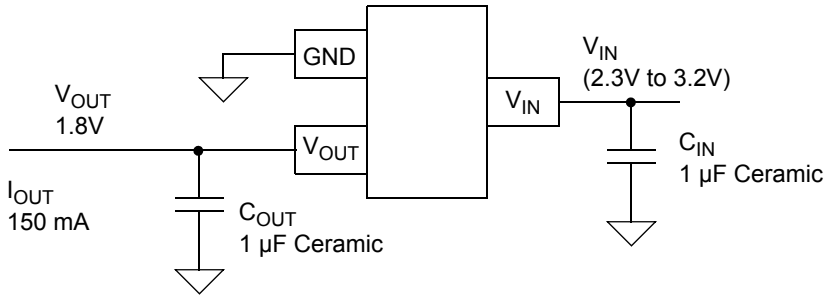


* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagrams



Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} ..... +6.5V
All inputs and outputs w.r.t. ..... (V_{SS} - 0.3V) to (V_{IN} + 0.3V)
Peak Output Current ..... Internally Limited
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... 150°C
Operating Junction Temperature ..... -40°C to +125°C
ESD protection on all pins (HBM;MM) ..... ≥ 4 kV; ≥ 400V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, $I_{LOAD} = 100\ \mu A$, $C_{OUT} = 1\ \mu F$ (X7R), $C_{IN} = 1\ \mu F$ (X7R), $T_A = +25°C$.
Boldface type applies for junction temperatures, T_J (**Note 6**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input/Output Characteristics						
Input Operating Voltage	V_{IN}	**2.3**	—	**6.0**	V	**Note 1**
Input Quiescent Current	I_q	—	1.6	**4**	µA	I_L = 0 mA, $V_{IN} = V_R + 1V$
Maximum Output Current	I_{OUT_mA}	**250** **200**	— —	— —	mA	For $V_R \geq 2.5V$ For $V_R < 2.5V$
Output Short Circuit Current	I_{OUT_SC}	—	408	—	mA	$V_{IN} = V_R + 1V$, V_{OUT} = GND Current (peak current) measured 10 ms after short is applied.
Output Voltage Regulation	V_{OUT}	V_R - 2.0% **V_R - 3.0%**	V_R ± 0.4%	V_R + 2.0% **V_R + 3.0%**	V	**Note 2**
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	50	—	ppm/°C	**Note 3**
Line Regulation	$\Delta V_{OUT}/(V_{OUT} X \Delta V_{IN})$	**-1.0**	±0.75	**+1.0**	%/V	$(V_R + 1)V \leq V_{IN} \leq 6V$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-1.5**	±1.0	**+1.5**	%	I_L = 0.1 mA to 250 mA for $V_R \geq 2.5V$ I_L = 0.1 mA to 200 mA for $V_R < 2.5V$ **Note 4**
Dropout Voltage $V_R > 2.5V$	$V_{IN} - V_{OUT}$	—	178	**350**	mV	I_L = 250 mA, (**Note 1**, **Note 5**)
Dropout Voltage $V_R < 2.5V$	$V_{IN} - V_{OUT}$	—	150	**350**	mV	I_L = 200 mA, (**Note 1**, **Note 5**)
Output Rise Time	T_R	—	500	—	µs	10% V_R to 90% V_R V_{IN} = 0V to 6V, R_L = 50Ω resistive

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq (V_R + 3.0\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 2.9V, 3.0V, 3.3V, 4.0V, 5.0V. The input voltage $V_{IN} = V_R + 1.0V$; I_{OUT} = 100 µA.

3: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT\text{-}HIGH}$ = highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with a V_R + 1V differential applied.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

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DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, $I_{LOAD} = 100\ \mu A$, $C_{OUT} = 1\ \mu F$ (X7R), $C_{IN} = 1\ \mu F$ (X7R), $T_A = +25°C$.
Boldface type applies for junction temperatures, T_J (**Note 6**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Noise	e_N	—	3	—	$\mu V/(Hz)^{1/2}$	$I_L = 100$ mA, f = 1 kHz, $C_{OUT} = 1\ \mu F$
Power Supply Ripple Rejection Ratio	PSRR	—	44	—	dB	f = 100 Hz, $C_{OUT} = 1\ \mu F$, $I_L = 50$ mA, $V_{INAC} = 100$ mV pk-pk, $C_{IN} = 0\ \mu F$, $V_R = 1.2V$
Thermal Shutdown Protection	T_{SD}	—	140	—	°C	$V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq (V_R + 3.0\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage. For example: $V_R = 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 2.9V, 3.0V, 3.3V, 4.0V, 5.0V$. The input voltage $V_{IN} = V_R + 1.0V$; $I_{OUT} = 100\ \mu A$.

3: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT\text{-}HIGH}$ = highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with a $V_R + 1V$ differential applied.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, $I_{LOAD} = 100\ \mu A$, $C_{OUT} = 1\ \mu F$ (X7R), $C_{IN} = 1\ \mu F$ (X7R), $T_A = +25°C$.
Boldface type applies for junction temperatures, T_J (**Note 1**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40		+125	°C	
Operating Temperature Range	T_J	-40		+125	°C	
Storage Temperature Range	T_A	-65		+150	°C	
Thermal Package Resistance						
Thermal Resistance, 2x2 DFN	θ_{JA}	—	91	—	°C/W	EIA/JEDEC® JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	286	—	°C/W	
	$\theta_{JC(Bottom)}$	—	28.57	—	°C/W	
	Ψ_{JT}	—	8.95	—	°C/W	
Thermal Resistance, SOT-23	θ_{JA}	—	212	—	°C/W	EIA/JEDEC JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	139	—	°C/W	
	$\theta_{JC(Bottom)}$	—	11.95	—	°C/W	
	Ψ_{JT}	—	6.15	—	°C/W	
Thermal Resistance, SOT-89	θ_{JA}	—	104	—	°C/W	EIA/JEDEC JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	74	—	°C/W	
	Ψ_{JT}	—	30	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

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TEMPERATURE SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, $I_{LOAD} = 100\ \mu A$, $C_{OUT} = 1\ \mu F$ (X7R), $C_{IN} = 1\ \mu F$ (X7R), $T_A = +25°C$.
Boldface type applies for junction temperatures, T_J (**Note 1**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Thermal Resistance, TO-92	θ_{JA}	—	92	—	°C/W	EIA/JEDEC JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	74	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: V_R = 1.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1V.

Note: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

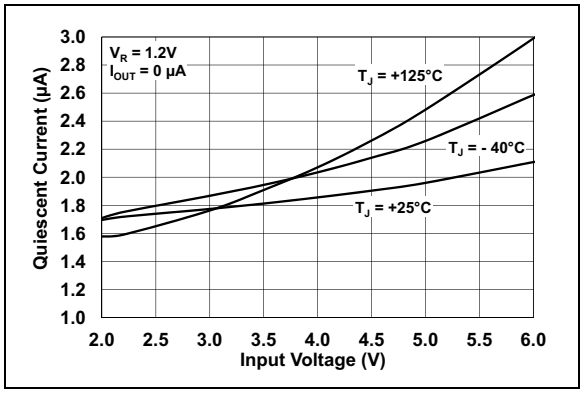

FIGURE 2-1: *Input Quiescent Current vs. Input Voltage.*

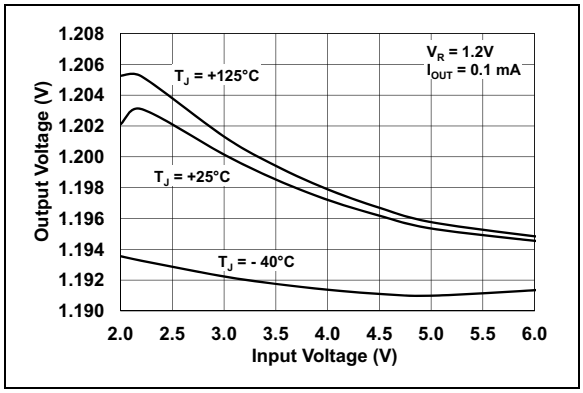

FIGURE 2-4: *Output Voltage vs. Input Voltage (V_R = 1.2V).*

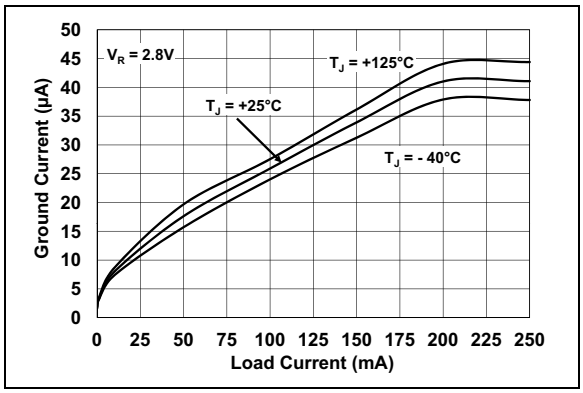

FIGURE 2-2: *Ground Current vs. Load Current.*

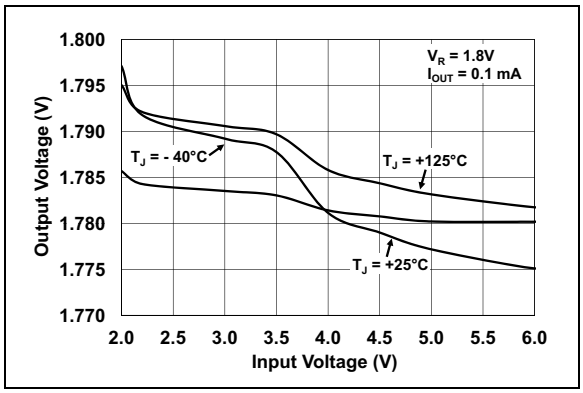

FIGURE 2-5: *Output Voltage vs. Input Voltage (V_R = 1.8V).*

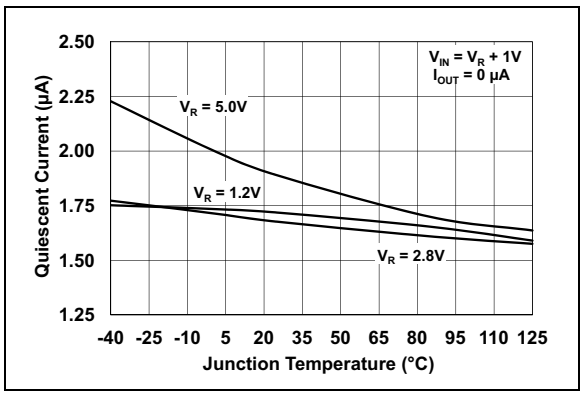

FIGURE 2-3: *Quiescent Current vs. Junction Temperature.*

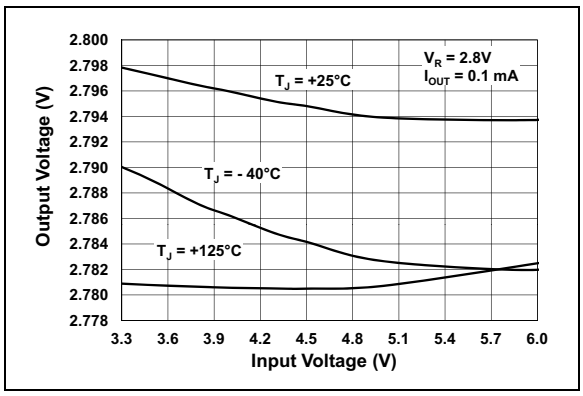

FIGURE 2-6: *Output Voltage vs. Input Voltage (V_R = 2.8V).*

Note: Unless otherwise indicated: V_R = 1.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1V.

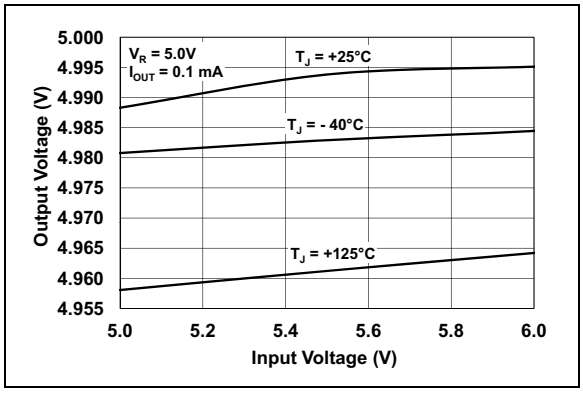

FIGURE 2-7: *Output Voltage vs. Input Voltage (V_R = 5.0V).*

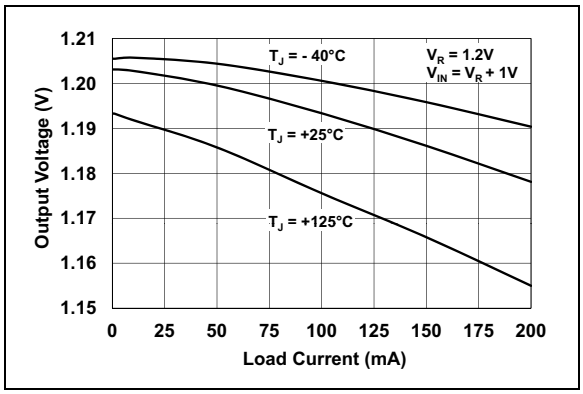

FIGURE 2-8: *Output Voltage vs. Load Current (V_R = 1.2V).*

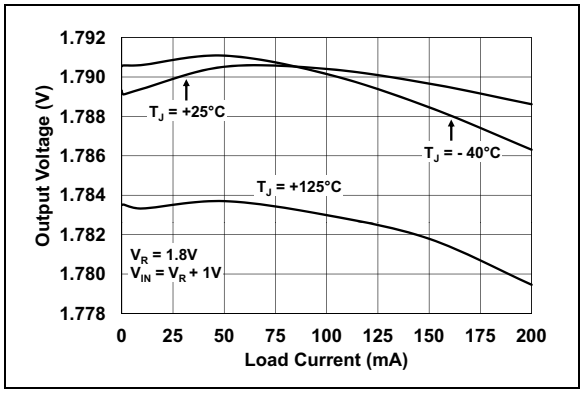

FIGURE 2-9: *Output Voltage vs. Load Current (V_R = 1.8V).*

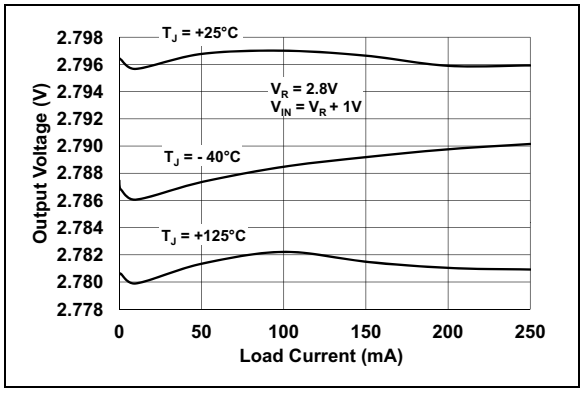

FIGURE 2-10: *Output Voltage vs. Load Current (V_R = 2.8V).*

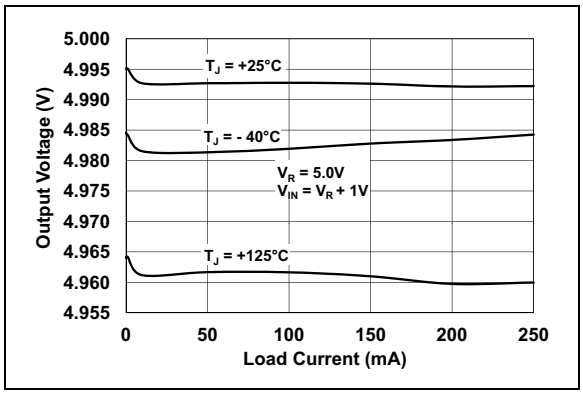

FIGURE 2-11: *Output Voltage vs. Load Current (V_R = 5.0V).*

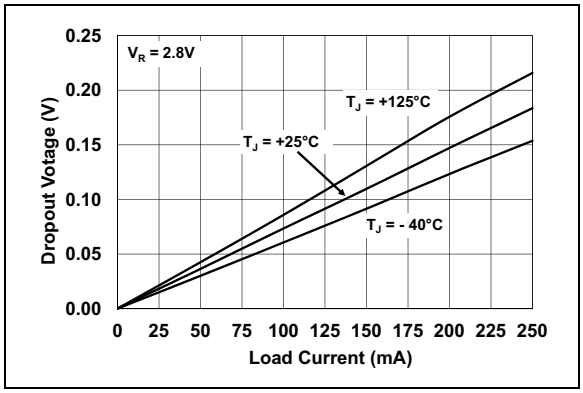

FIGURE 2-12: *Dropout Voltage vs. Load Current (V_R = 2.8V).*

Note: Unless otherwise indicated: V_R = 1.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1V.

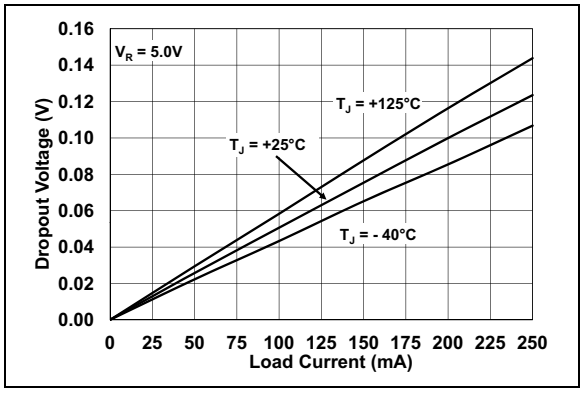

FIGURE 2-13: *Dropout Voltage vs. Load Current (V_R = 5.0V).*

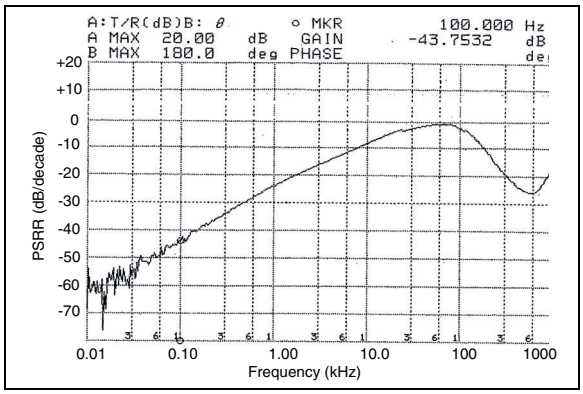

FIGURE 2-14: *Power Supply Ripple Rejection vs. Frequency (V_R = 1.2V).*

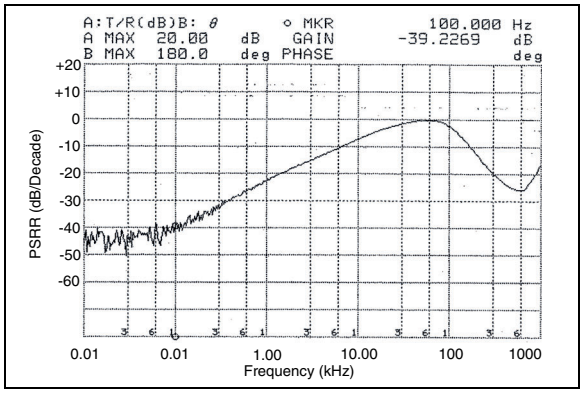

FIGURE 2-15: *Power Supply Ripple Rejection vs. Frequency (V_R = 2.8V).*

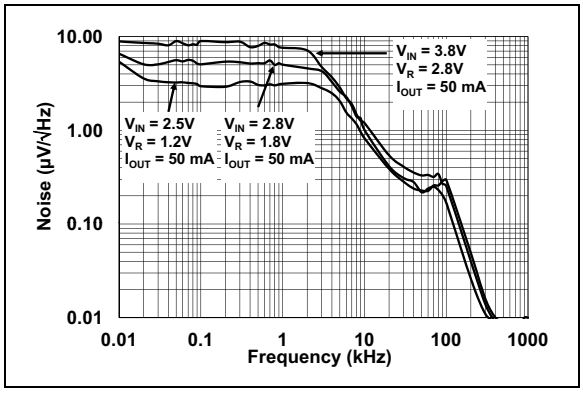

FIGURE 2-16: *Noise vs. Frequency.*

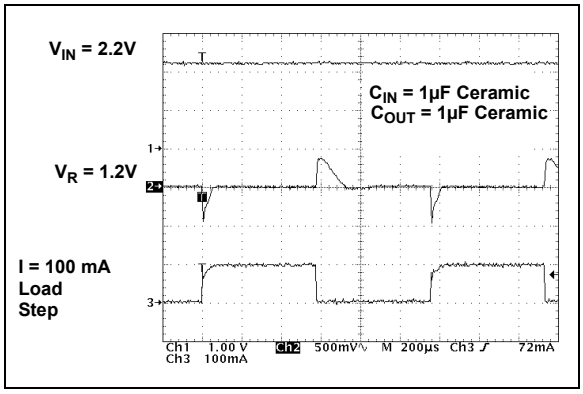

FIGURE 2-17: *Dynamic Load Step (V_R = 1.2V).*

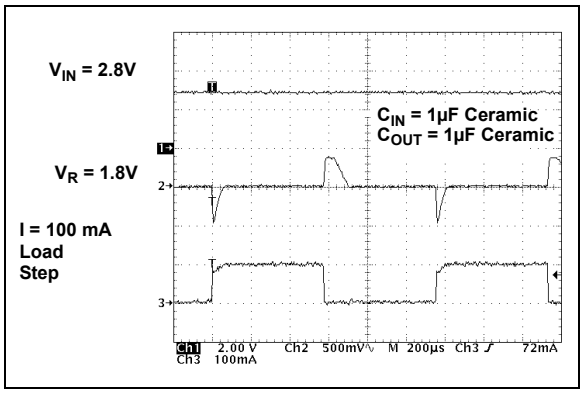

FIGURE 2-18: *Dynamic Load Step (V_R = 1.8V).*

Note: Unless otherwise indicated: V_R = 1.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1V.

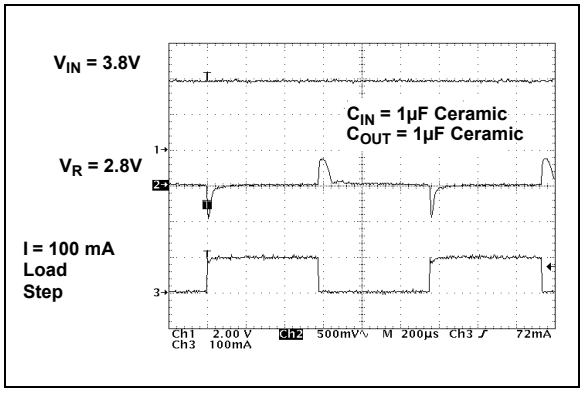

FIGURE 2-19: *Dynamic Load Step (V_R = 2.8V).*

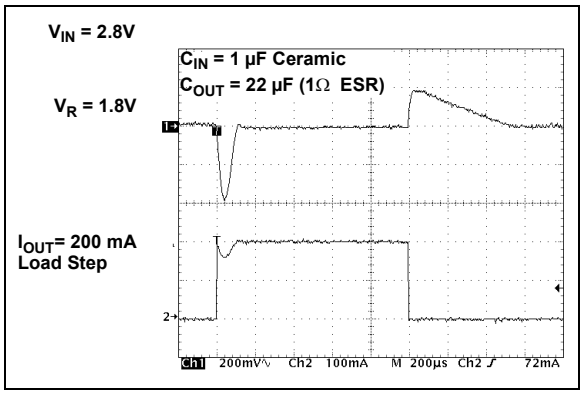

FIGURE 2-20: *Dynamic Load Step (V_R = 1.8V).*

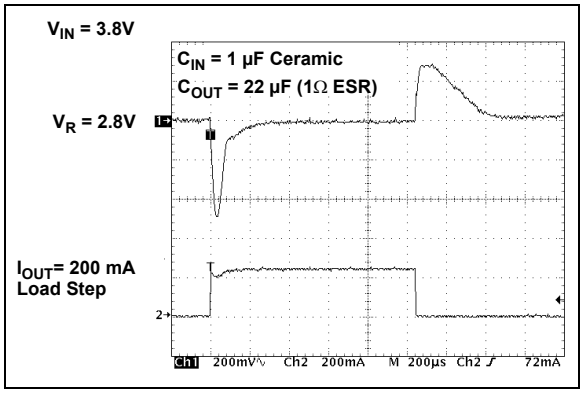

FIGURE 2-21: *Dynamic Load Step (V_R = 2.8V).*

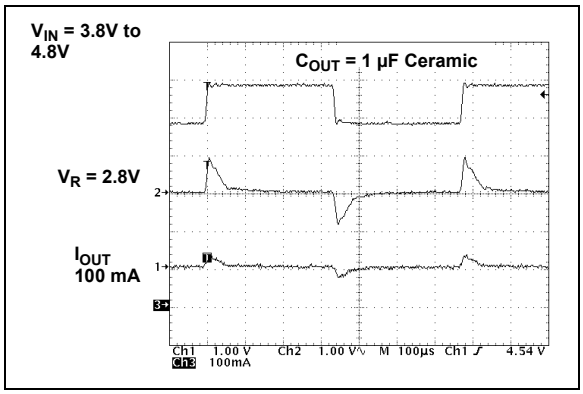

FIGURE 2-22: *Dynamic Load Step (V_R = 5.0V).*

FIGURE 2-23: *Dynamic Line Step (V_R = 2.8V).*

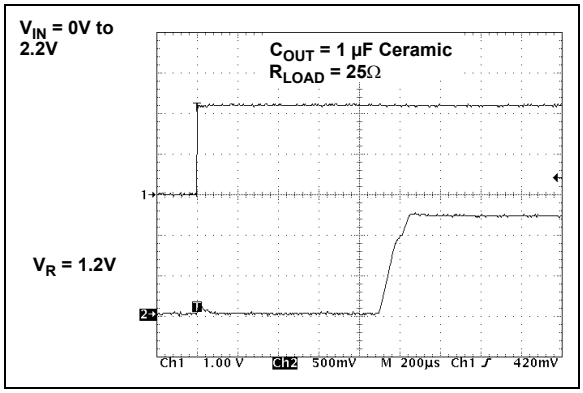

FIGURE 2-24: *Start-up from V_{IN} (V_R = 1.2V).*

Note: Unless otherwise indicated: V_R = 1.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1V.

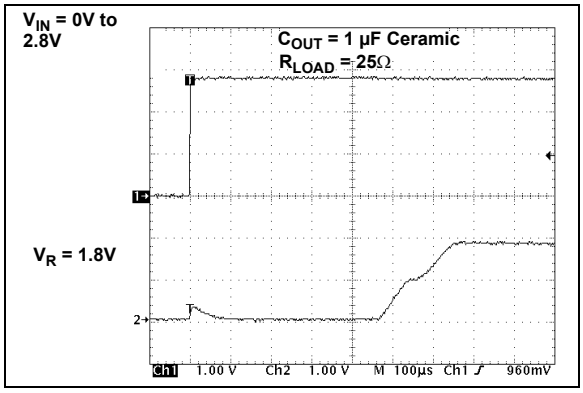

FIGURE 2-25: *Start-up from V_{IN} (V_R = 1.8V).*

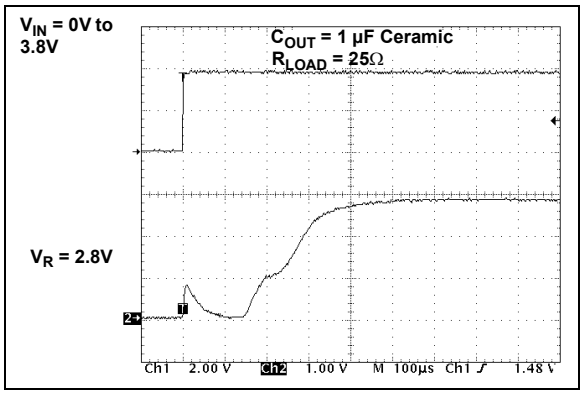

FIGURE 2-26: *Start-up from V_{IN} (V_R = 2.8V).*

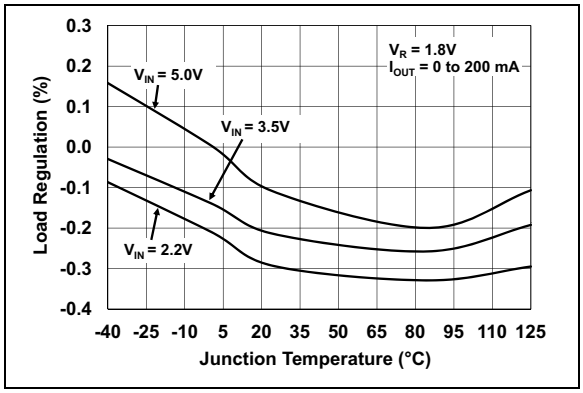

FIGURE 2-27: *Load Regulation vs. Junction Temperature (V_R = 1.8V).*

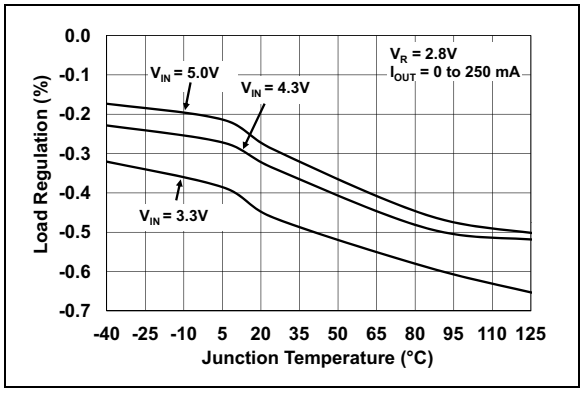

FIGURE 2-28: *Load Regulation vs. Junction Temperature (V_R = 2.8V).*

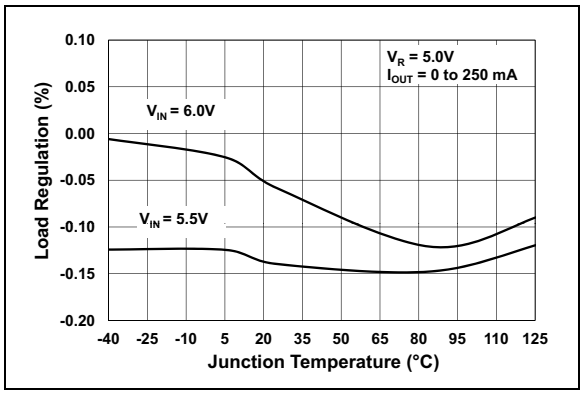

FIGURE 2-29: *Load Regulation vs. Junction Temperature (V_R = 5.0V).*

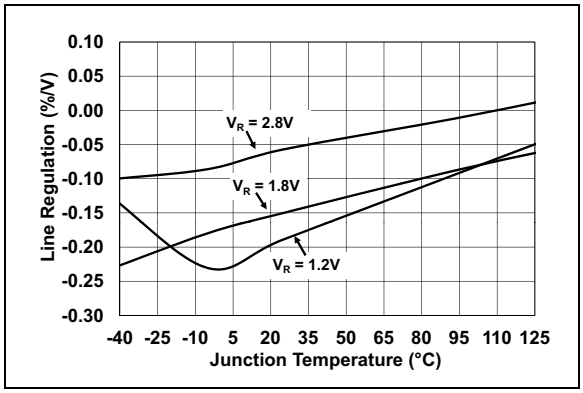

FIGURE 2-30: *Line Regulation vs. Temperature (V_R = 1.2V, 1.8V, 2.8V).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. SOT-23	Pin No. SOT-89	Pin No. TO-92	Pin No. 2x2 DFN-6	Name	Function
1	1	1	3	GND	Ground Terminal
2	3	3	6	V_{OUT}	Regulated Voltage Output
3	2	2	1	V_{IN}	Unregulated Supply Voltage
—	—	—	2, 4, 5	NC	No Connect
—	—	—	7	EP	Exposed Thermal Pad

3.1 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (1.6 µA typical) flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.2 Regulated Output Voltage (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO V_{OUT} pin as is practical. The current flowing out of this pin is equal to the DC load current.

3.3 Unregulated Input Voltage Pin (V_{IN})

Connect V_{IN} to the input unregulated source voltage. As with all low dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 1 µF of capacitance will ensure stable operation of the LDO circuit. For applications that have load currents below 100 mA, the input capacitance requirement can be lowered. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.4 No Connect (NC)

No internal connection. The pins marked NC are true “No Connect” pins.

3.5 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the GND pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

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4.0 DETAILED DESCRIPTION

4.1 Output Regulation

A portion of the LDO output voltage is fed back to the internal error amplifier and compared with the precision internal bandgap reference. The error amplifier output will adjust the amount of current that flows through the P-Channel pass transistor, thus regulating the output voltage to the desired value. Any changes in input voltage or output current will cause the error amplifier to respond and adjust the output voltage to the target voltage (refer to Figure 4-1).

4.2 Overcurrent

The MCP1700 internal circuitry monitors the amount of current flowing through the P-Channel pass transistor. In the event of a short circuit or excessive output current, the MCP1700 will turn off the P-Channel device for a short period, after which the LDO will attempt to restart. If the excessive current remains, the cycle will repeat itself.

4.3 Overtemperature

The internal power dissipation within the LDO is a function of input-to-output voltage differential and load current. If the power dissipation within the LDO is excessive, the internal junction temperature will rise above the typical shutdown threshold of 140°C. At that point, the LDO will shut down and begin to cool to the typical turn-on junction temperature of 130°C. If the power dissipation is low enough, the device will continue to cool and operate normally. If the power dissipation remains high, the thermal shutdown protection circuitry will again turn off the LDO, protecting it from catastrophic failure.

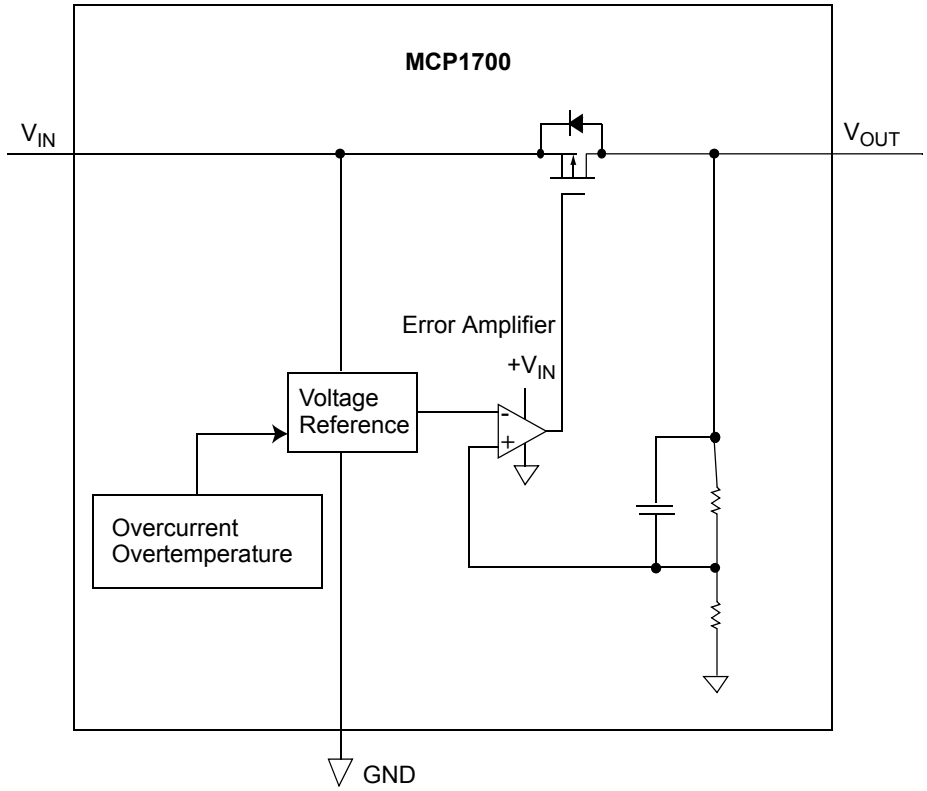

FIGURE 4-1: *Block Diagram.*

5.0 FUNCTIONAL DESCRIPTION

The MCP1700 CMOS low dropout linear regulator is intended for applications that need the lowest current consumption while maintaining output voltage regulation. The operating continuous load of the MCP1700 ranges from 0 mA to 250 mA ($V_R \geq 2.5V$). The input operating voltage ranges from 2.3V to 6.0V, making it capable of operating from two, three or four alkaline cells or a single Li-Ion cell battery input.

5.1 Input

The input of the MCP1700 is connected to the source of the P-Channel PMOS pass transistor. As with all LDO circuits, a relatively low source impedance (10Ω) is needed to prevent the input impedance from causing the LDO to become unstable. The size and type of the required capacitor depend heavily on the input source type (battery, power supply) and the output current range of the application. For most applications (up to 100 mA), a 1 µF ceramic capacitor will be sufficient to ensure circuit stability. Larger values can be used to improve circuit AC performance.

5.2 Output

The maximum rated continuous output current for the MCP1700 is 250 mA ($V_R \geq 2.5V$). For applications where $V_R < 2.5V$, the maximum output current is 200 mA.

A minimum output capacitance of 1.0 µF is required for small signal stability in applications that have up to 250 mA output current capability. The capacitor type can be ceramic, tantalum or aluminum electrolytic. The ESR range on the output capacitor can range from 0Ω to 2.0Ω.

5.3 Output Rise time

When powering up the internal reference output, the typical output rise time of 500 µs is controlled to prevent overshoot of the output voltage.

6.0 APPLICATION CIRCUITS AND ISSUES

6.1 Typical Application

The MCP1700 is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage make it ideal for many battery-powered applications.

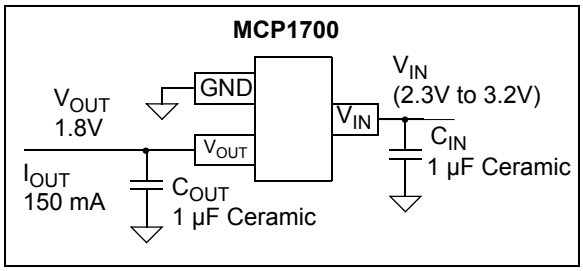

FIGURE 6-1: *Typical Application Circuit.*

6.1.1 APPLICATION INPUT CONDITIONS

Package Type = SOT-23
Input Voltage Range = 2.3V to 3.2V
V_{IN} maximum = 3.2V
V_{OUT} typical = 1.8V
I_{OUT} = 150 mA maximum

6.2 Power Calculations

6.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1700 is a function of input voltage, output voltage and output current. The power dissipation resulting from the quiescent current draw is so low it is insignificant (1.6 µA x V_{IN}). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

P_{LDO} = Internal power dissipation of the LDO Pass device
$V_{IN(MAX)}$ = Maximum input voltage
$V_{OUT(MIN)}$ = Minimum output voltage of the LDO

The maximum continuous operating junction temperature specified for the MCP1700 is +125°C. To estimate the internal junction temperature of the MCP1700, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT-23 pin package is estimated at 230°C/W.

EQUATION 6-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{A(MAX)}$$

$T_{J(MAX)}$ = Maximum continuous junction temperature
P_{TOTAL} = Total power dissipation of the device
$R\theta_{JA}$ = Thermal resistance from junction to ambient
$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the maximum internal power dissipation of the package.

EQUATION 6-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum power dissipation of the device
$T_{J(MAX)}$ = Maximum continuous junction temperature
$T_{A(MAX)}$ = Maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION 6-4:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in the device's junction temperature over the ambient temperature
P_{TOTAL} = Maximum power dissipation of the device
$R\theta_{JA}$ = Thermal resistance from junction to ambient

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EQUATION 6-5:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction Temperature

$T_{J(RISE)}$ = Rise in the device's junction temperature over the ambient temperature

T_A = Ambient temperature

6.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation resulting from ground current is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = SOT-23

Input Voltage

V_{IN} = 2.3V to 3.2V

LDO Output Voltages and Currents

V_{OUT} = 1.8V

I_{OUT} = 150 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$P_{LDO(MAX)}$ = ($V_{IN(MAX)}$ - $V_{OUT(MIN)}$) x $I_{OUT(MAX)}$

P_{LDO} = (3.2V - (0.97 x 1.8V)) x 150 mA

P_{LDO} = 218.1 milliwatts

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC® standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, *"High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages"*. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, *"A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

$T_{J(RISE)}$ = P_{TOTAL} x $R\theta_{JA}$

$T_{J(RISE)}$ = 218.1 milliwatts x 212.0°C/Watt

$T_{J(RISE)}$ = 46.2°C

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

T_J = $T_{J(RISE)}$ + $T_{A(MAX)}$

T_J = 86.2°C

Maximum Package Power Dissipation at +40°C Ambient Temperature

2x2 DFN-6 (91°C/Watt = θ_{JA})

$P_{D(MAX)}$ = (125°C - 40°C) / 91°C/W

$P_{D(MAX)}$ = 934 milliwatts

SOT-23 (212.0°C/Watt = θ_{JA})

$P_{D(MAX)}$ = (125°C - 40°C) / 212°C/W

$P_{D(MAX)}$ = 401 milliwatts

SOT-89 (104°C/Watt = θ_{JA})

$P_{D(MAX)}$ = (125°C - 40°C) / 104°C/W

$P_{D(MAX)}$ = 817 milliwatts

TO-92 (92°C/Watt = θ_{JA})

$P_{D(MAX)}$ = (125°C - 40°C) / 92°C/W

$P_{D(MAX)}$ = 924 milliwatts

6.4 Voltage Reference

The MCP1700 can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1700 LDO. The low cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1700 as a voltage reference.

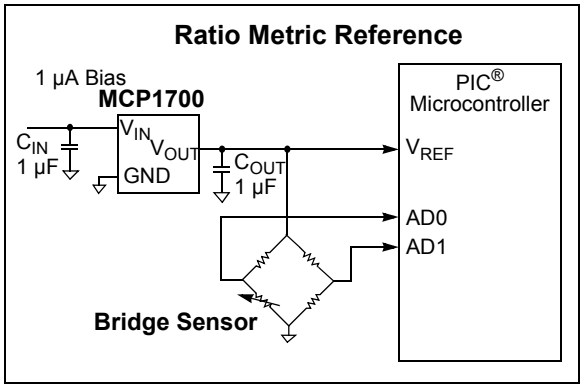


FIGURE 6-2: *Using the MCP1700 as a voltage reference.*

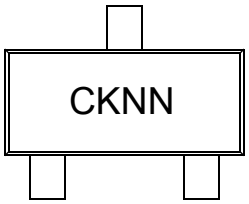
6.5 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 250 mA maximum specification of the MCP1700. The internal current limit of the MCP1700 will prevent high peak load demands from causing non-recoverable damage. The 250 mA rating is a maximum average continuous rating. As long as the average current does not exceed 250 mA, pulsed higher load currents can be applied to the MCP1700. The typical current limit for the MCP1700 is 550 mA (T_A + 25°C).

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

3-Pin SOT-23

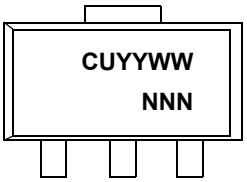


Standard	
Extended Temp	
Symbol	**Voltage ***
CK	1.2
CM	1.8
CP	2.5
CQ	2.8
GC	2.9
CR	3.0
CS	3.3
CU	5.0

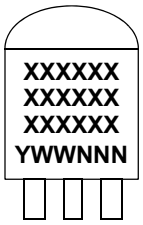
* Custom output voltages available upon request.

Contact your local Microchip sales office for more information.

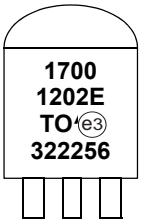
3-Pin SOT-89



3-Pin TO-92



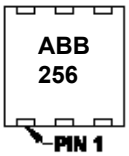
Example



6-Lead DFN (2x2x0.9 mm)

Part Number	Code
MCP1700T-1202E/MAY	ABB
MCP1700T-1802E/MAY	ABC
MCP1700T-2502E/MAY	ABD
MCP1700T-2802E/MAY	ABF
MCP1700T-3002E/MAY	ABE
MCP1700T-3302E/MAY	AAZ
MCP1700T-5002E/MAY	ABA

Example

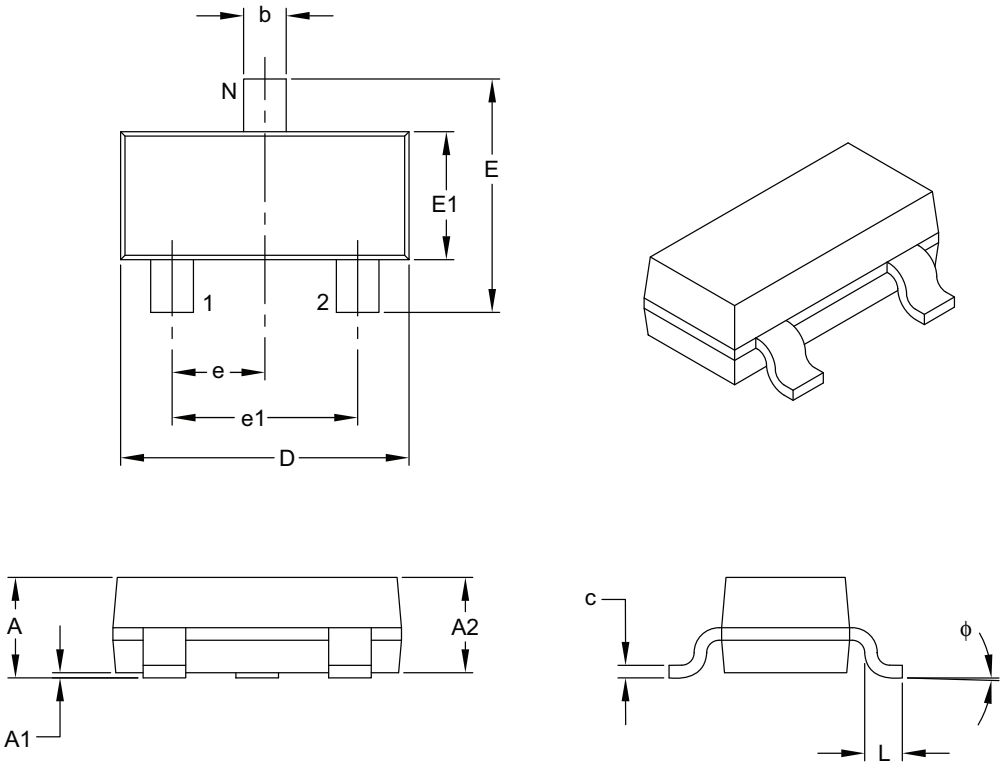


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	3		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.89	–	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.30	–	0.54

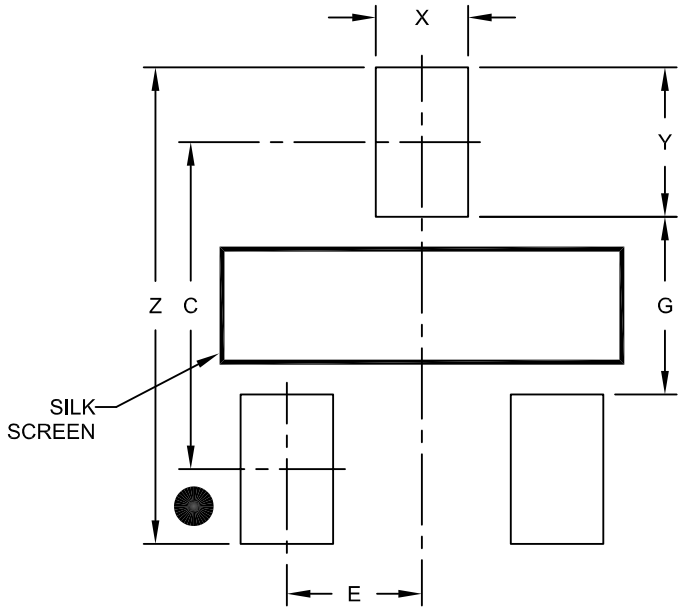
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-104B

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X			0.65
Contact Pad Length (X3)	Y			1.05
Distance Between Pads	G	1.25		
Overall Width	Z			3.35

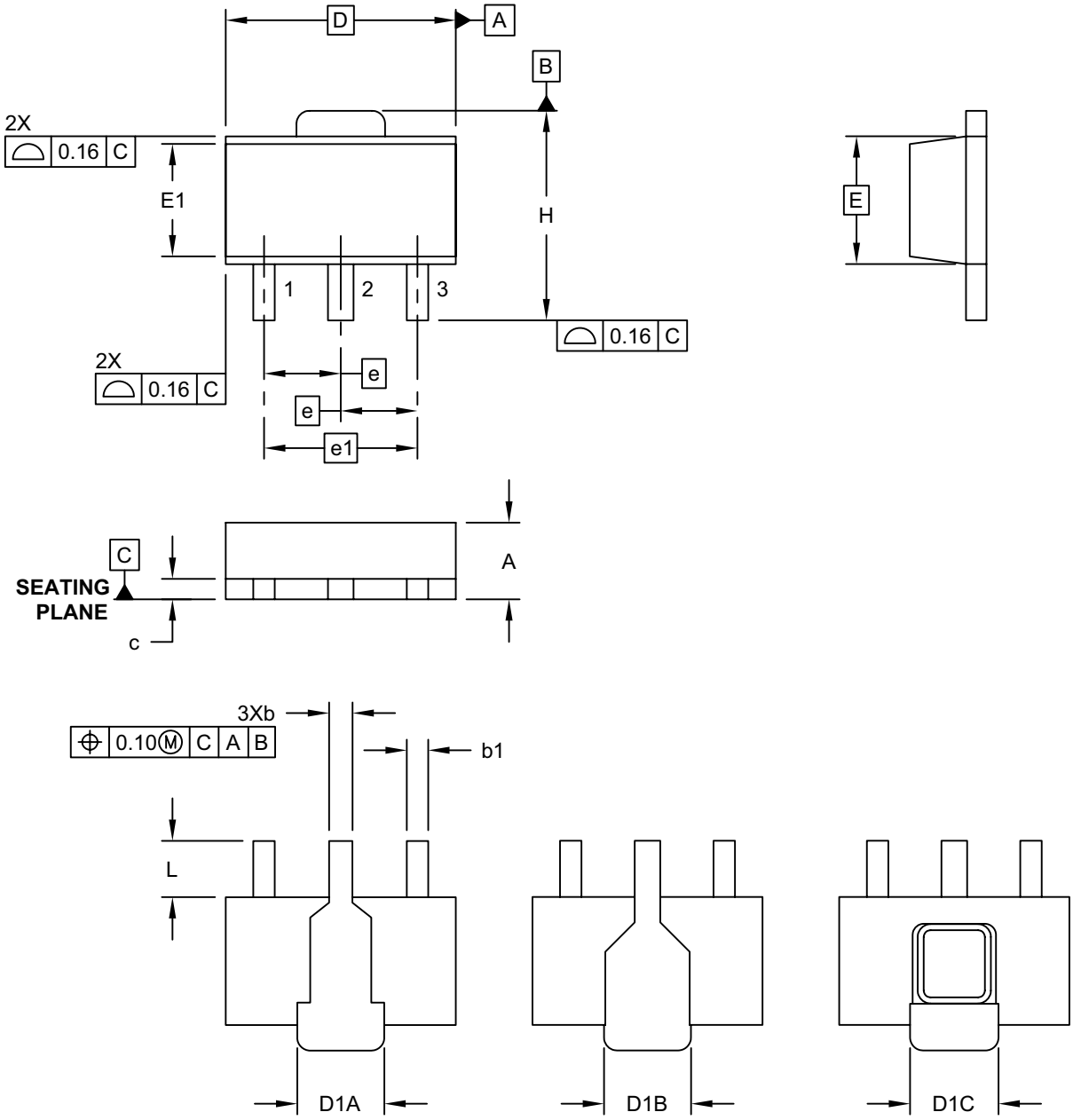
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2104A

3-Lead Plastic Small Outline Transistor (MB) - [SOT-89]

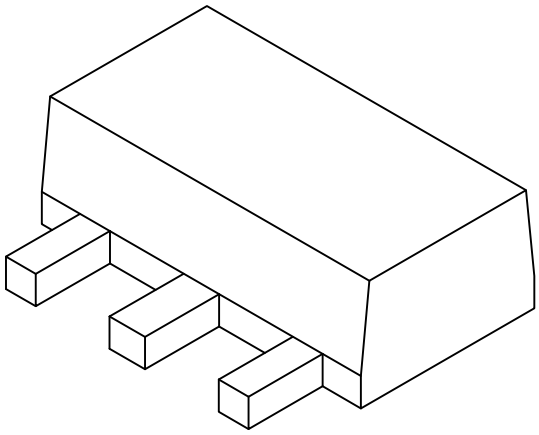
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-029C Sheet 1 of 2

3-Lead Plastic Small Outline Transistor (MB) - [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	3		
Pitch	e	1.50 BSC		
Outside Lead Pitch	e1	3.00 BSC		
Overall Height	A	1.40	1.50	1.60
Overall Width	H	3.94	4.10	4.25
Molded Package Width at Base	E	2.50 BSC		
Molded Package Width at Top	E1	2.13	2.20	2.29
Overall Length	D	4.50 BSC		
Tab Length (Option A)	D1A	1.63	1.73	1.83
Tab Length (Option B)	D1B	1.40	1.60	1.75
Tab Length (Option C)	D1C	1.62	1.73	1.83
Foot Length	L	0.79	1.10	1.20
Lead Thickness	c	0.35	0.40	0.44
Lead 2 Width	b	0.41	0.50	0.56
Leads 1 & 3 Width	b1	0.36	0.42	0.48

Notes:

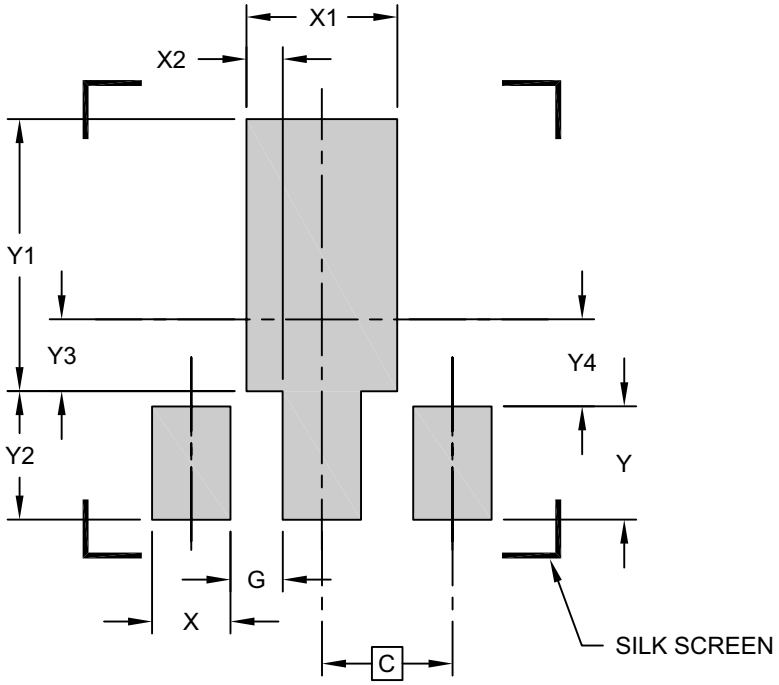
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029C Sheet 2 of 2

3-Lead Plastic Small Outline Transistor (MB) - [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units	MILLIMETERS		
Dimension Limits	MIN	NOM	MAX
C		1.50 (BSC)	
X (3 PLACES)		0.900	
X1		1.733	
X2 (2 PLACES)		0.416	
G (2 PLACES)		0.600	
Y (2 PLACES)		1.300	
Y1		3.125	
Y2		1.475	
Y3		0.825	
Y4		1.000	

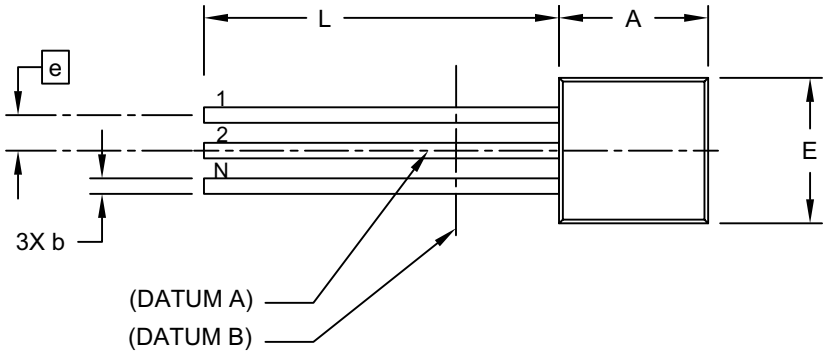
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

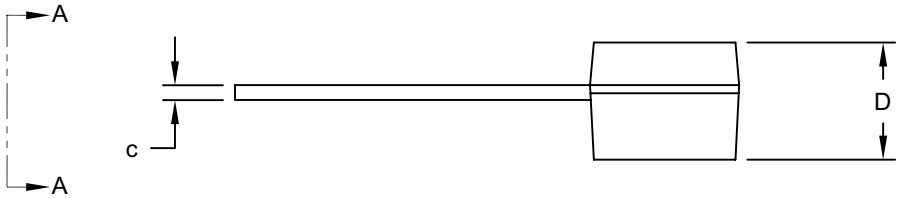
Microchip Technology Drawing C04-2029C

3-Lead Plastic Transistor Outline (TO) [TO-92]

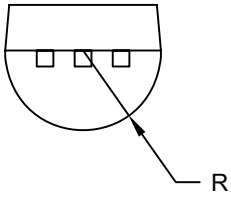
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

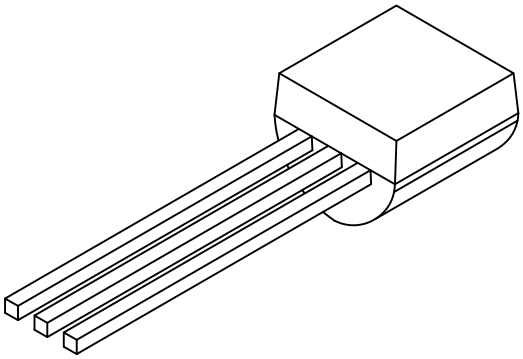


VIEW A-A

Microchip Technology Drawing C04-101 Rev C Sheet 1 of 2

3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	3		
Pitch	e	.050 BSC		
Bottom to Package Flat	D	.125	-	.165
Overall Width	E	.175	-	.205
Overall Length	A	.170	-	.210
Molded Package Radius	R	.080	-	.105
Tip to Seating Plane	L	.500	-	-
Lead Thickness	c	.014	-	.021
Lead Width	b	.014	-	.022

Notes:

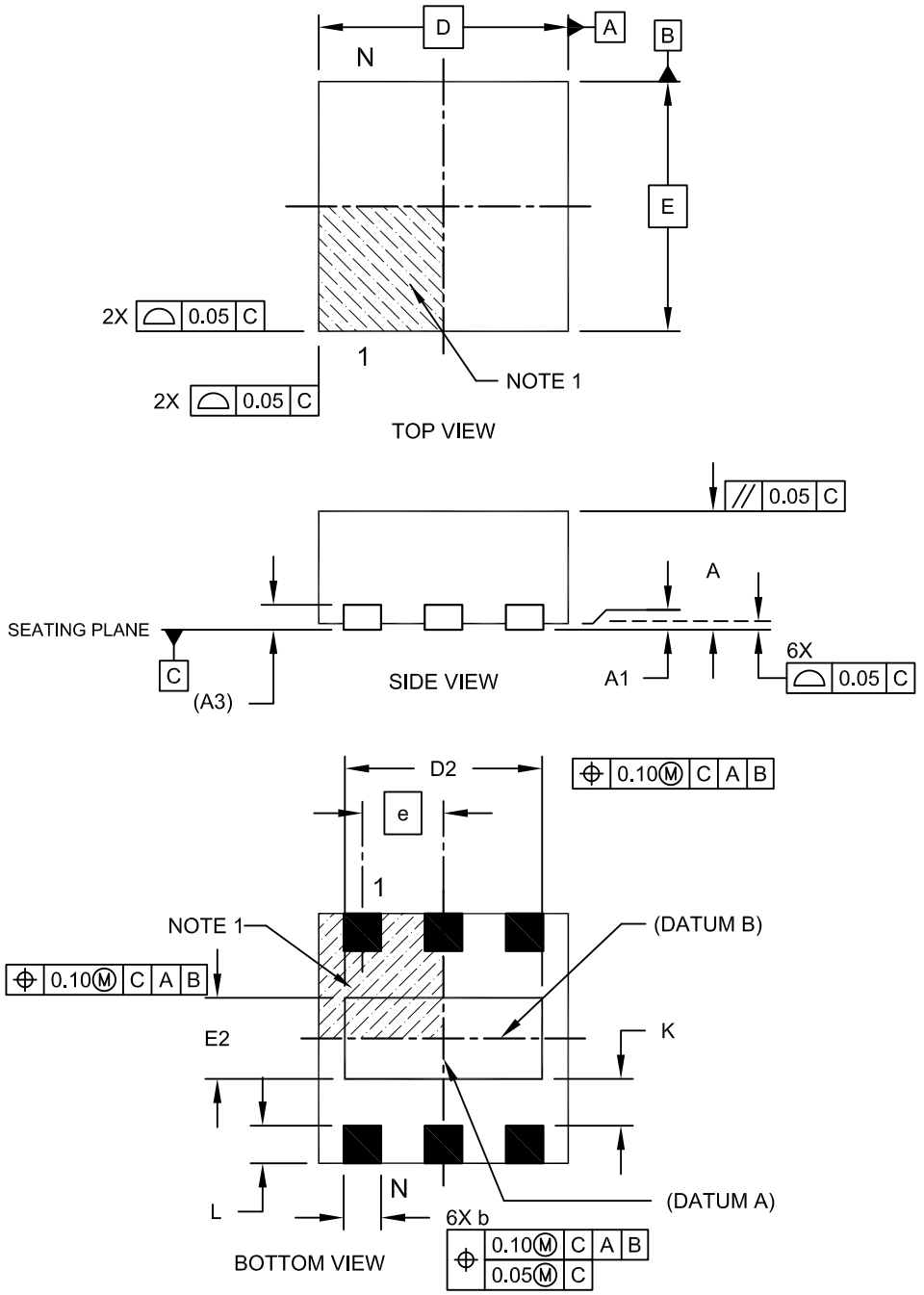
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101 Rev C Sheet 2 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

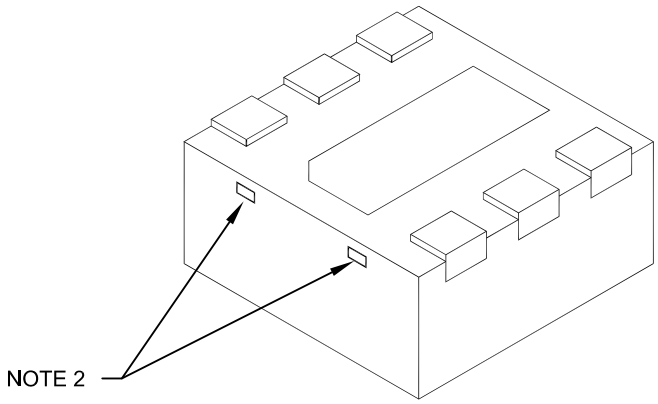
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-120C Sheet 1 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	2.00 BSC		
Exposed Pad Length	D2	1.50	1.60	1.70
Exposed Pad Width	E2	0.90	1.00	1.10
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120C Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision E (November 2018)

The following is the list of modifications:

- Added information related to the 2.9V option throughout the document
- Updated Features.
- Updated DC Characteristics.
- Updated Temperature Specifications.
- Updated Power Dissipation example in **Section 6.3 "Voltage Regulator"**.
- Updated Package Marking Information in **Section 7.0 "Packaging Information"**.
- Updated Product Identification System.

Revision D (September 2016)

The following is the list of modifications:

- Updated DC Characteristics.
- Updated Product Identification System.
- Minor typographical changes.

Revision C (October 2013)

The following is the list of modifications:

- Added new package to the family (2x2 DFN-6) and related information throughout the document.
- Updated thermal package resistance information in Temperature Specifications.
- Updated **Section 3.0 "Pin Descriptions"**.
- Added package markings and drawings for the 2x2 DFN-6 package.
- Added information related to the 2.8V option throughout the document.
- Updated Product Identification System.
- Minor typographical changes.

Revision B (February 2007)

- Updated Packaging Information.
- Corrected Product Identification System.
- Changed X5R to X7R in Notes to DC Characteristics, Temperature Specifications, and **Section 2.0 "Typical Performance Curves"**.

Revision A (November 2005)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	XXX	X	X	/XX
MCP1700	Tape & Reel	Voltage Output	Tolerance	Temp. Range	Package

Device:	MCP1700: Low Quiescent Current LDO	
Tape and Reel:	T:	Tape and Reel only applies to SOT-23 and SOT-89 devices
Standard Output Voltage: *	120 = 1.2V 180 = 1.8V 250 = 2.5V 280 = 2.8V 290 = 2.9V 300 = 3.0V 330 = 3.3V 500 = 5.0V * Custom output voltages available upon request. Contact your local Microchip sales office for more information	
Tolerance:	2 = 2% (Standard)	
Temperature Range:	E = -40°C to +125°C (Extended)	
Package:	MAY = Plastic Small Outline Transistor (DFN), 6-lead MB = Plastic Small Outline Transistor (SOT-89), 3-lead TO = Plastic Small Outline Transistor (TO-92), 3-lead TT = Plastic Small Outline Transistor (SOT-23), 3-lead	

Examples:

2x2 DFN-6 Package:

a) MCP1700T-1202E/MAY: 1.2V V_{OUT}
b) MCP1700T-1802E/MAY: 1.8V V_{OUT}
c) MCP1700T-2502E/MAY: 2.5V V_{OUT}
d) MCP1700T-2802E/MAY: 2.8V V_{OUT}
e) MCP1700T-3002E/MAY: 3.0V V_{OUT}
f) MCP1700T-3302E/MAY: 3.3V V_{OUT}
g) MCP1700T-5002E/MAY: 5.0V V_{OUT}

SOT-89 Package:

a) MCP1700T-1202E/MB: 1.2V V_{OUT}
b) MCP1700T-1802E/MB: 1.8V V_{OUT}
c) MCP1700T-2502E/MB: 2.5V V_{OUT}
d) MCP1700T-2802E/MB: 2.8V V_{OUT}
e) MCP1700T-3002E/MB: 3.0V V_{OUT}
f) MCP1700T-3302E/MB: 3.3V V_{OUT}
g) MCP1700T-5002E/MB: 5.0V V_{OUT}

TO-92 Package:

a) MCP1700-1202E/TO: 1.2V V_{OUT}
b) MCP1700-1802E/TO: 1.8V V_{OUT}
c) MCP1700-2502E/TO: 2.5V V_{OUT}
d) MCP1700-2802E/TO: 2.8V V_{OUT}
e) MCP1700-3002E/TO: 3.0V V_{OUT}
f) MCP1700-3302E/TO: 3.3V V_{OUT}
g) MCP1700-5002E/TO: 5.0V V_{OUT}

SOT-23 Package:

a) MCP1700T-1202E/TT: 1.2V V_{OUT}
b) MCP1700T-1802E/TT: 1.8V V_{OUT}
c) MCP1700T-2502E/TT: 2.5V V_{OUT}
d) MCP1700T-2802E/TT: 2.8V V_{OUT}
e) MCP1700T-2902E/TT: 2.9V V_{OUT}
f) MCP1700T-3002E/TT: 3.0V V_{OUT}
g) MCP1700T-3302E/TT: 3.3V V_{OUT}
h) MCP1700T-5002E/TT: 5.0V V_{OUT}

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