



**THE DATASHEET OF
STL100N6LF6**



N-channel 60 V, 3.3 mΩ typ., 25 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet – production data

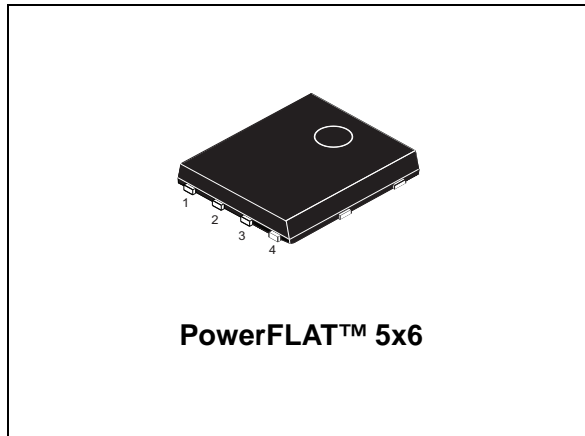
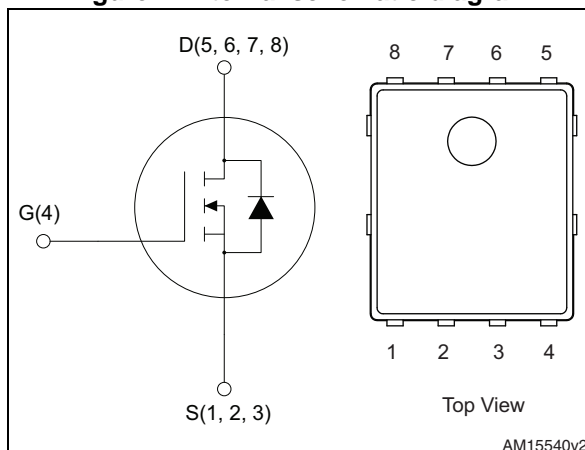


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL100N6LF6	60 V	4.4 mΩ	25 A

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL100N6LF6	100N6LF6	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	130	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	25	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	18	A
$I_{DM}^{(3)}$	Drain current (pulsed)	100	A
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. The value is rated according to R_{thj-c}
2. The value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^\circ\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case max	1.13	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 52\text{ V}$)	1370	mJ

2 Electrical characteristics

($T_J = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 60\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}$, $T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$		3.3	4.4	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 11\text{ A}$		4.3	5.5	m Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	6600	-	pF
C_{oss}	Output capacitance		-	670	-	pF
C_{rss}	Reverse transfer capacitance		-	315	-	pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 20\text{ A}$	-	121	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$	-	17	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14)	-	22	-	nC
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias=0 test signal level=20 mV $I_D = 0$	-	1.2	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	20	-	ns
t_r	Rise time		-	13	-	ns
$t_{d(off)}$	Turn-off delay time		-	108	-	ns
t_f	Fall time		-	22	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22 \text{ A}, V_{GS} = 0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 20 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 48\text{V}, T_J = 150 \text{ }^\circ\text{C}$ (see Figure 15)	-	34		ns
Q_{rr}	Reverse recovery charge		-	44		nC
I_{RRM}	Reverse recovery current		-	2.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

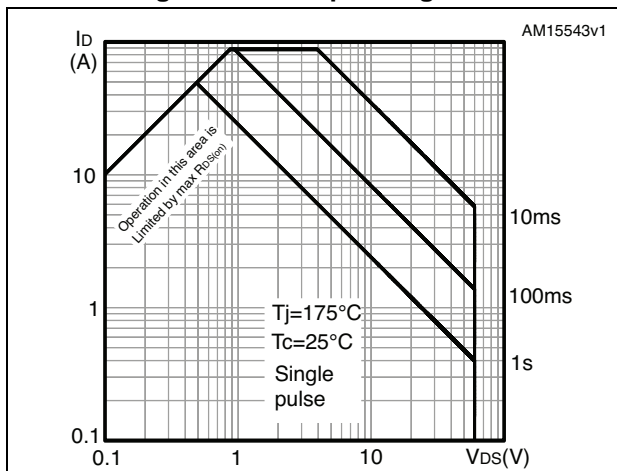


Figure 3. Thermal impedance

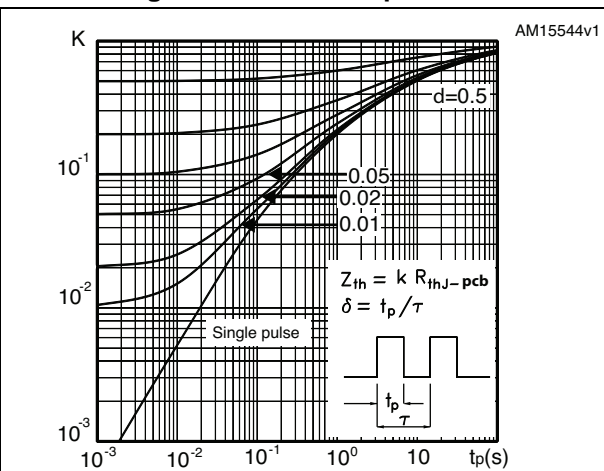


Figure 4. Output characteristics

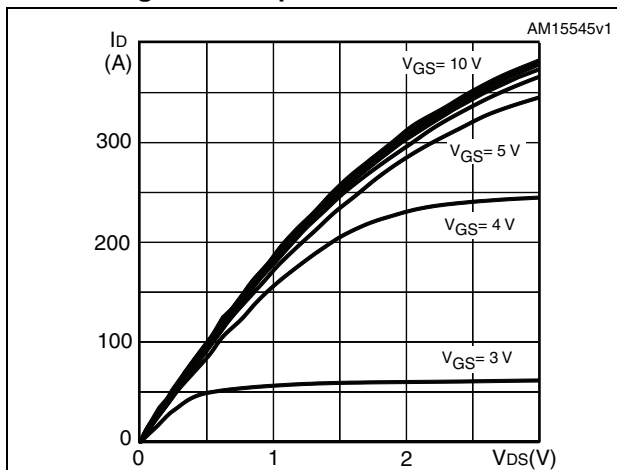


Figure 5. Transfer characteristics

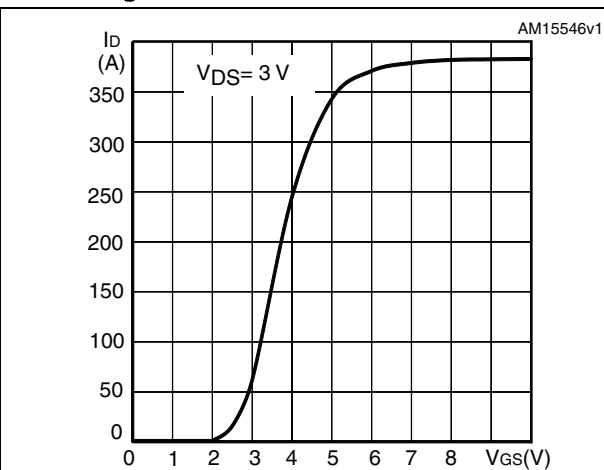


Figure 6. Gate charge vs gate-source voltage

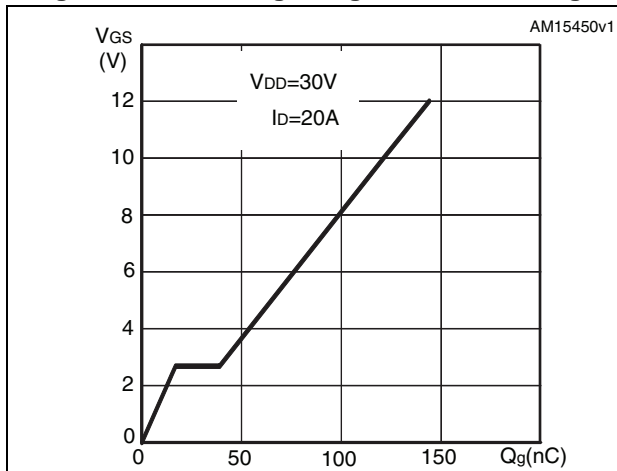


Figure 7. Static drain-source on-resistance

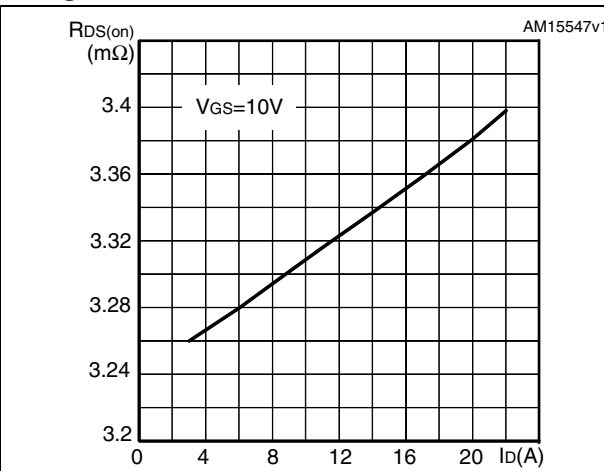


Figure 8. Capacitance variations

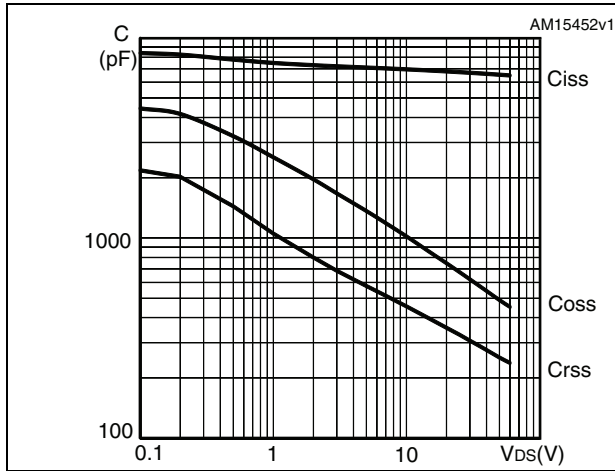


Figure 9. Source-drain diode forward characteristics

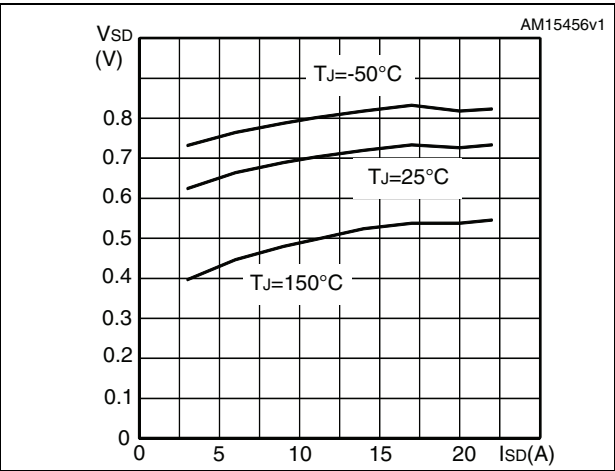


Figure 10. Normalized gate threshold voltage vs temperature

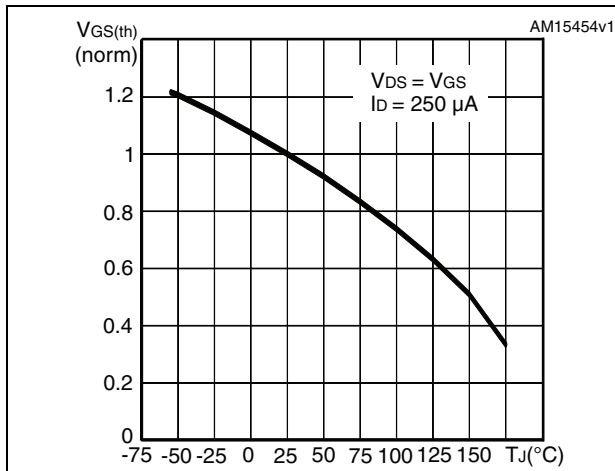


Figure 11. Normalized on-resistance vs temperature

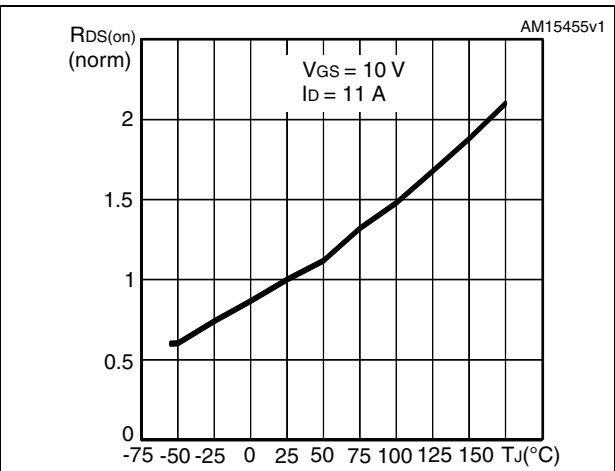
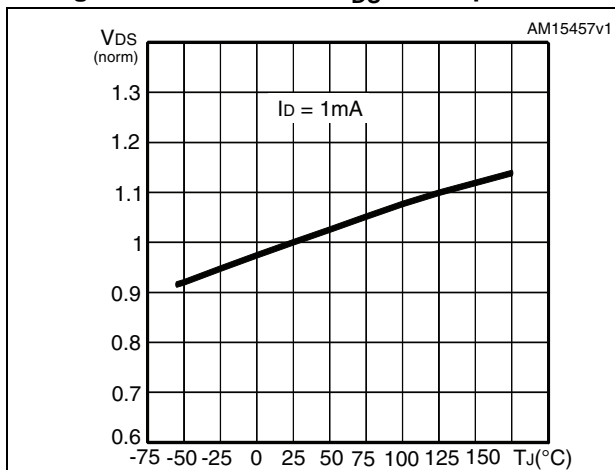


Figure 12. Normalized V_{DS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

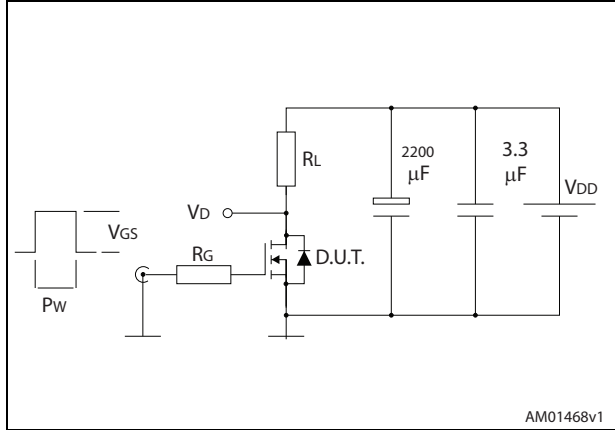


Figure 14. Gate charge test circuit

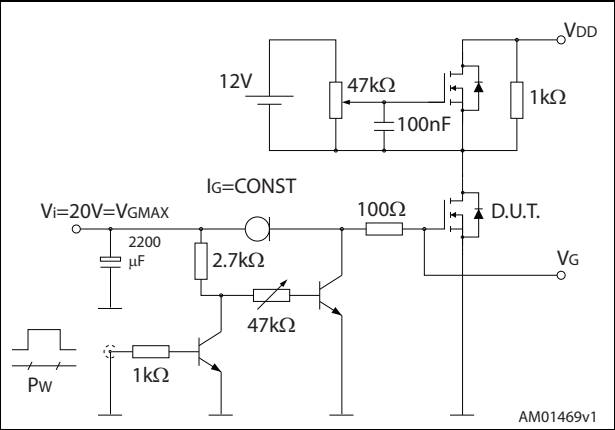


Figure 15. Test circuit for inductive load switching and diode recovery times

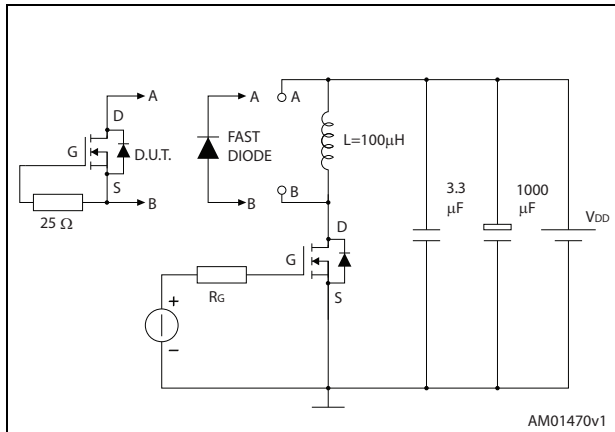


Figure 16. Unclamped inductive load test circuit

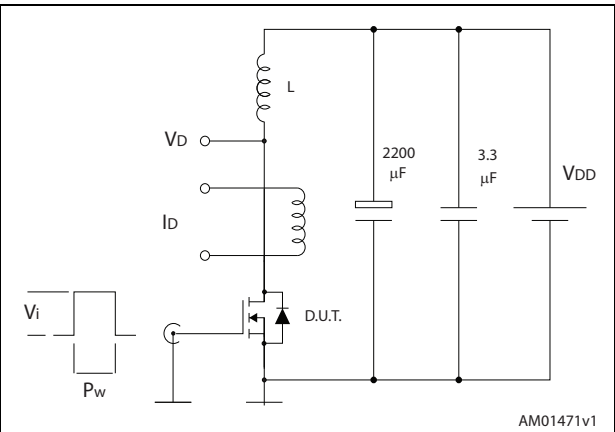


Figure 17. Unclamped inductive waveform

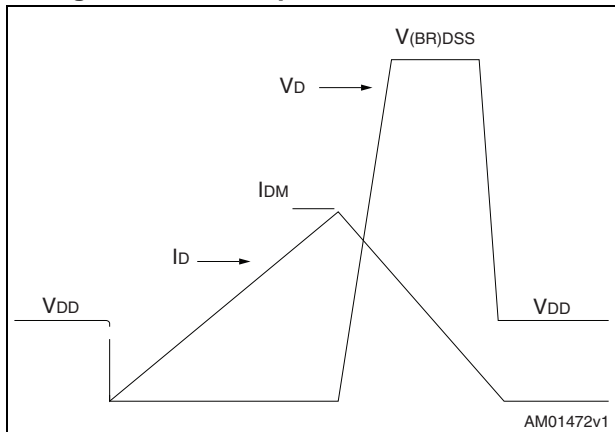
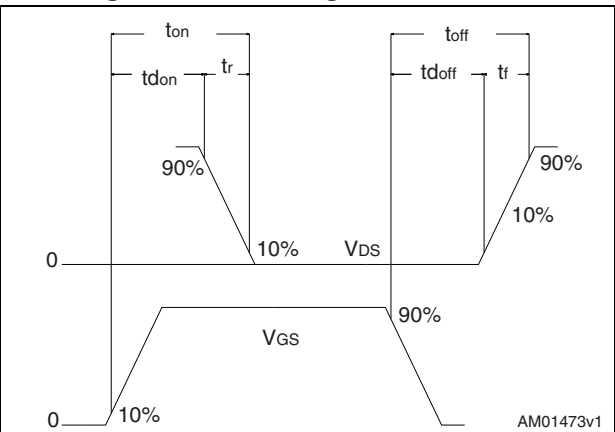


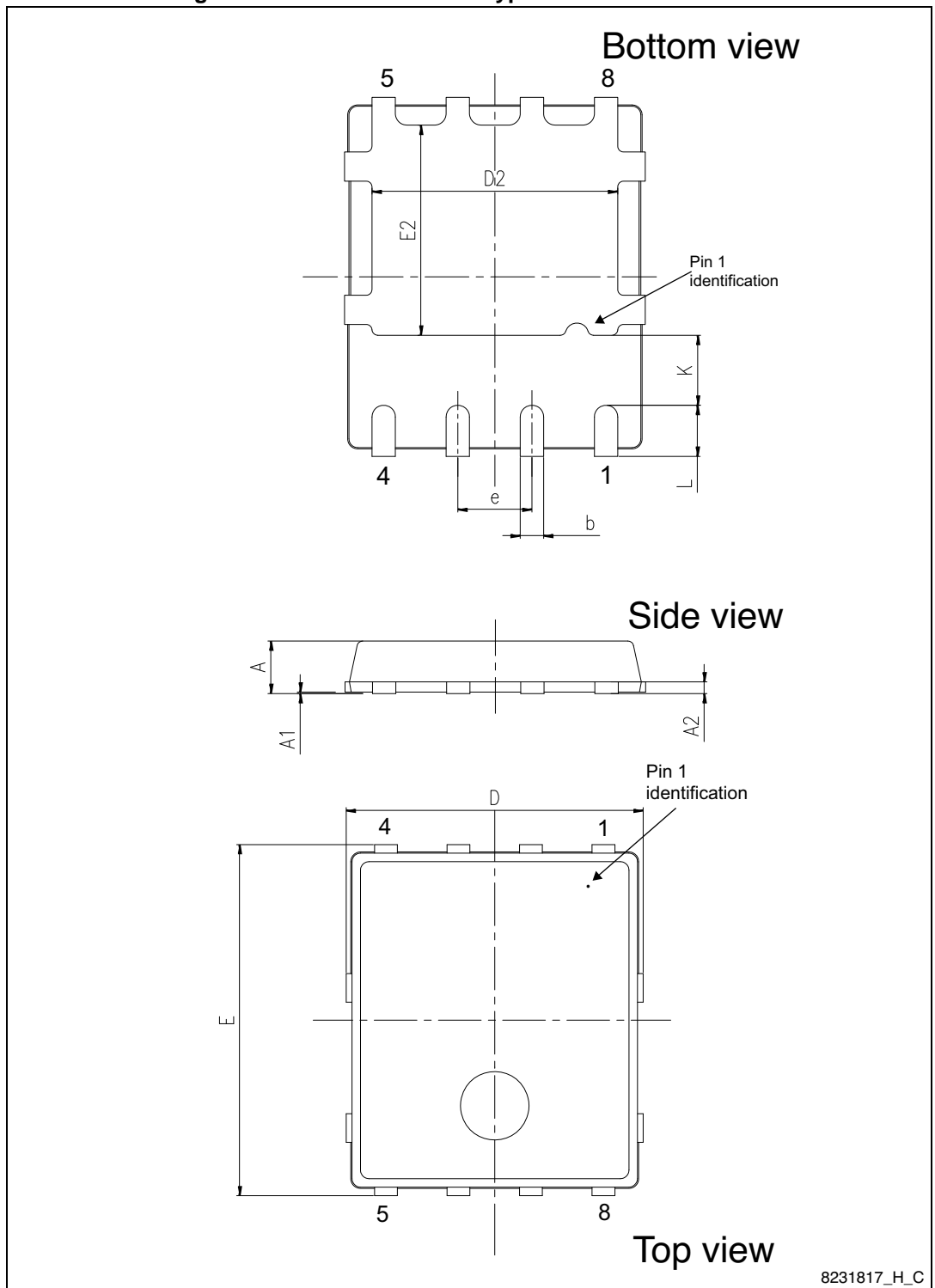
Figure 18. Switching time waveform



4 Package mechanical data

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Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

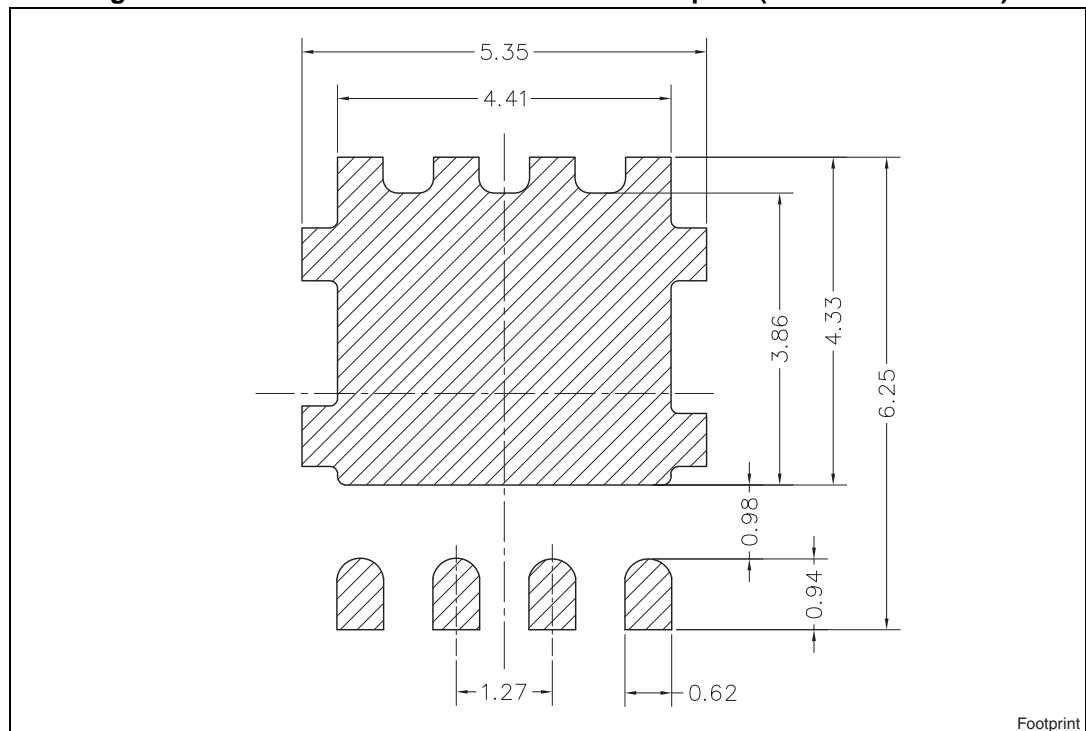


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Table 9. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(a)

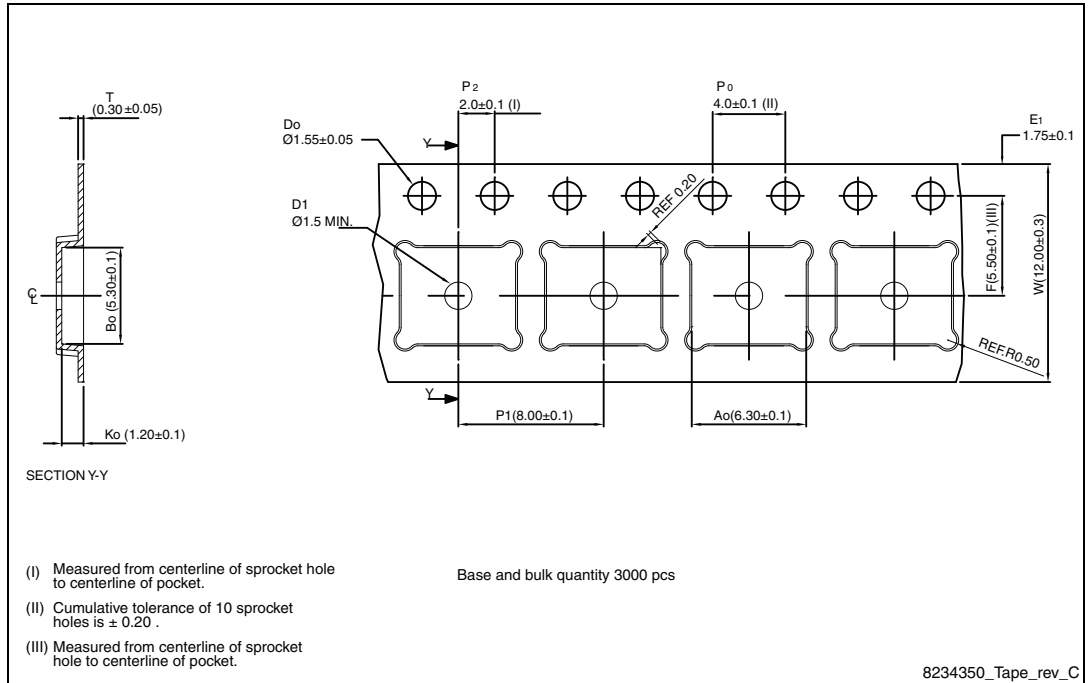
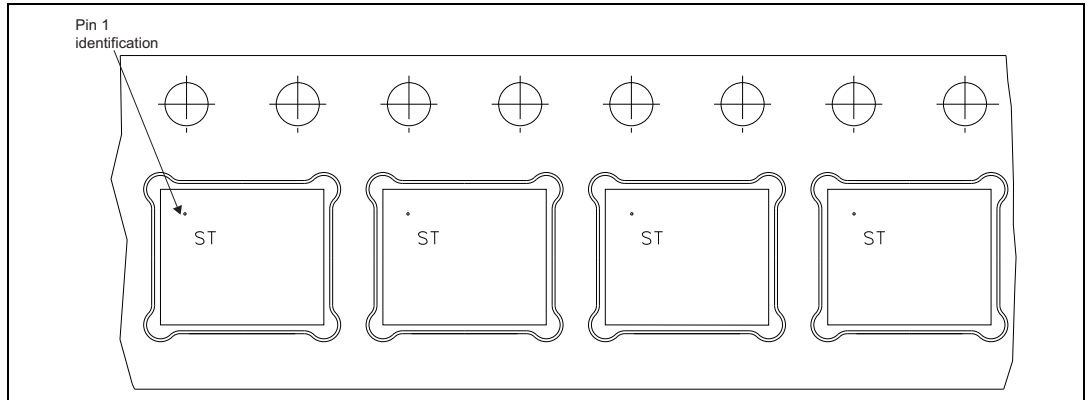
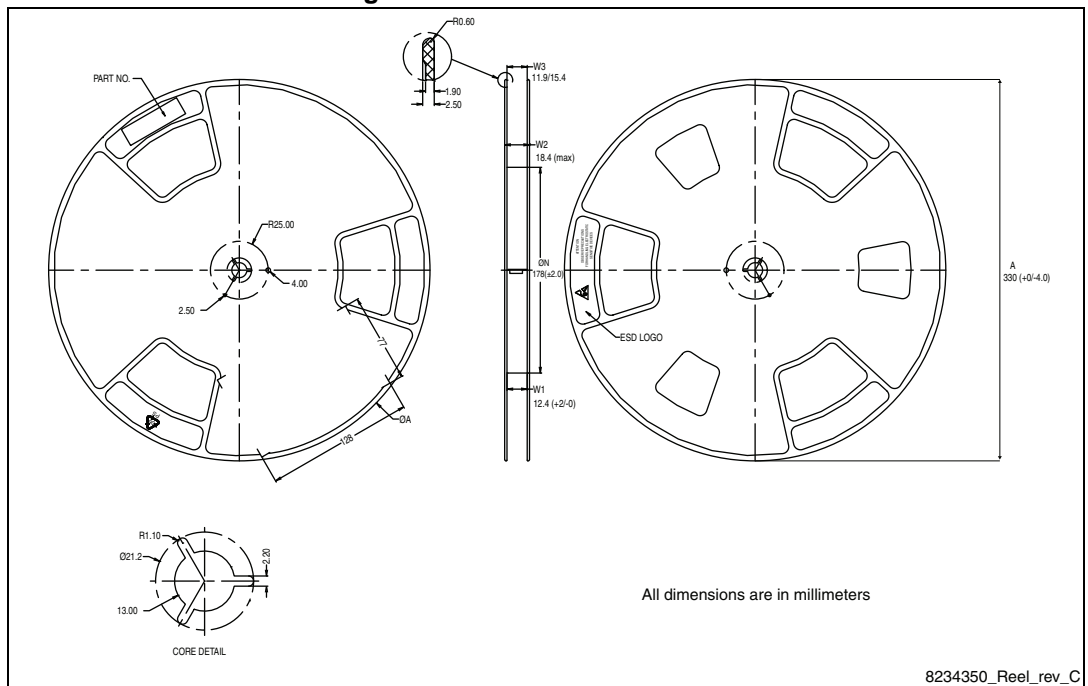


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Feb-2011	1	First release
10-Nov-2011	2	Section 4: Package mechanical data has been updated. Minor text changes.
10-Mar-2014	3	<ul style="list-style-type: none"> – Updated: title on the cover page. – Modified: $R_{DS(on)}$ and I_D values on cover page – Modified: drain current (continuous) at $T_C = 25\text{ °C}$, drain current (continuous) at $T_{pcb} = 25\text{ °C}$, drain current (continuous) at $T_{pcb}=100\text{ °C}$, I_{DM}, total dissipation at $T_{pcb} = 25\text{ °C}$, T_{stg} and T_j values on table 2, $R_{thj-case}$ value on Table 3, max values on Table 4, $R_{DS(on)}$ typ and max. values, typical values on Table 6, 7 and 8 – Inserted: Section 2.1: Electrical characteristics (curves) – Updated: Section 4: Package mechanical data – Added: Section 5: Packaging mechanical data – Minor text changes

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