THE DATASHEET OF

CDCL6010RGZT

1.8V, 11 Output Clock Multiplier, Distributor, Jitter Cleaner, and Buffer

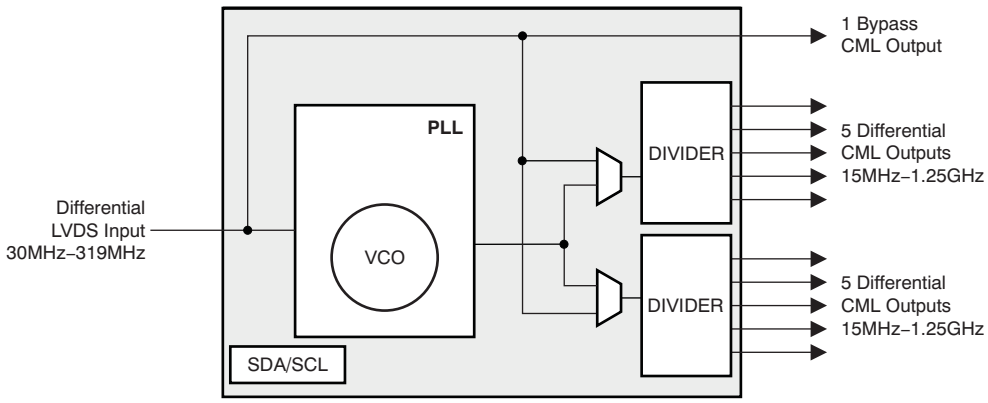
Check for Samples: CDCL6010

FEATURES

- **Single 1.8V Supply**
- **High-Performance Clock Multiplier, Distributor, Jitter Cleaner, and Buffer With 11 Outputs**
- **Low Output Jitter: 400fs RMS**
- **Output Group Phase Adjustment**
- **Low-Voltage Differential Signaling (LVDS) Input, 100Ω Differential On-Chip Termination, 30MHz to 319MHz Frequency Range**
- **Differential Current Mode Logic (CML) Outputs, 50Ω Single-Ended On-Chip Termination, 15MHz to 1.25GHz Frequency Range**
- **One Dedicated Differential CML Output, Straight PLL and Frequency Divider Bypass**
- **Two Groups of Five Outputs Each with Independent Frequency Division Ratios; Optional PLL Bypass**
- **Fully Integrated Voltage Controlled Oscillator (VCO); Supports Wide Output Frequency Range**
- **Output Frequency Derived From VCO Frequency with Divide Ratios of 1, 2, 4, 5, 8, 10, 16, 20, 32, 40, and 80**
- **Meets OBSAI RP1 v1.0 Standard and CPRI v2.0 Requirements**
- **Meets ANSI TIA/EIA-644-A-2001 LVDS Standard Requirements**
- **Integrated LC Oscillator Allows External Bandwidth Adjustment**
- **PLL Lock Indication**
- **Power Consumption: 640mW Typical**
- **Output Enable Control for Each Output**
- **SDA/SCL Device Management Interface**
- **48-pin QFN (RGZ) Package**
- **Industrial Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Low Jitter Clocking for High-Speed SERDES**
- **Jitter Cleaning of SERDES Reference Clocks for 1G/10G Ethernet, 1X/2X/4X/10X Fibre Channel, PCI Express, Serial ATA, SONET, CPRI, OBSAI, etc.**
- **Up to 1-to-11 Clock Buffering and Fan-out**



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CDCL6010 is a high-performance, low phase noise clock multiplier, distributor, jitter cleaner, and low skew buffer. It effectively cleans a noisy system clock with a fully-integrated low noise Voltage Controlled Oscillator (VCO) that operates in the 1.2GHz–1.275GHz range. (Note that the LC oscillator oscillates in the 2.4GHz–2.55GHz range. The frequency is predivided by 2 before the post-dividers P0 and P1.)

The output frequency (F_{OUT}) is synchronized to the frequency of the input clock (F_{IN}). The programmable pre-dividers, M and N, and the post-dividers, P0 and P1, give a high flexibility to the ratio of the output frequency to the input frequency:

$$F_{OUT} = F_{IN} \times N/(M \times P)$$

Where:

P (P0, P1) = 1, 2, 4, 5, 8, 10, 16, 20, 32, 40, 80

M = 1, 2, 4, 8

N = 32, 40

provided that:

$30MHz < (F_{IN} /M) < 40MHz$

$1200MHz < (F_{OUT} \times P) < 1275MHz$

The PLL loop bandwidth is user-selectable by external filter components or by using the internal loop filter. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements.

The CDCL6010 supports one differential LVDS clock input and a total of 11 differential CML outputs. One output is a straight bypass with no support for jitter cleaning or clock multiplication. The remaining 10 outputs are available in two groups of five outputs each with independent frequency division ratios. Those 10 outputs can be optionally setup to bypass the PLL when no jitter cleaning is needed. The CML outputs are compatible with LVDS receivers if ac-coupled.

With careful observation of the input voltage swing and common-mode voltage limits, the CDCL6010 can support a single-ended clock input as outlined in the Pin Description Table

The CDCL6010 can operate as a multi-output clock buffer in a PLL bypass mode.

All device settings are programmable through the SDA/SCL, serial two-wire interface.

The serial interface is 1.8V tolerant only.

The phase of one output group relative to the other can be adjusted through the SDA/SCL interface. For post-divide ratios (P0, P1) that are multiples of 5, the total number of phase adjustment steps (*n*) equals the divide-ratio divided by 5. For post-divide ratios (P0, P1) that are not multiples of 5, the total number of steps (*n*) is the same as the post-divide ratio. The phase adjustment step (ΔΦ) in time units is given as:

$$\Delta\Phi = 1/(n \times F_{OUT})$$

where F_{OUT} is the respective output frequency.

The device operates in a 1.8V supply environment and is characterized for operation from –40°C to +85°C.

The CDCL6010 is available in a 48-pin QFN (RGZ) package.

Table 1. AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES	FEATURES
–40°C to +85°C	CDCL6010RGZT	48-pin QFN (RGZ) Package, small tape and reel
–40°C to +85°C	CDCL6010RGZR	48-pin QFN (RGZ) Package, tape and reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted).(1)

		VALUE	UNIT
V_{DD}, AV_{DD}	Supply voltage(2)	–0.3 to 2.5	V
V_{LVDS}	Voltage range at LVDS input pins(2)	–0.3 to V_{DD} + 0.6	V
V_I	Voltage range at all non-LVDS input pins(2)	–0.3 to V_{DD} + 0.6	V
ESD	Electrostatic discharge (HBM)	2	kV
T_J	Junction temperature	+125	°C
T_{STG}	Storage temperature range	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating condition* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Digital supply voltage	1.7	1.8	1.9	V
AV_{DD}	Analog supply voltage	1.7	1.8	1.9	V
T_A	Ambient temperature (no airflow, no heatsink)	–40		+85	°C
T_J	Junction temperature			+105	°C

THERMAL INFORMATION

THERMAL METRIC(1)			RGZ (48 Pins)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2):	airflow = 0 lfm	28.3	°C/W
		airflow = 50 lfm	22.4	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		20.5	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (Bottom) thermal resistance		5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) No heatsink; power uniformly distributed; 36 ground vias (6 x 6 array) tied to the thermal exposed pad; 4-layer high-K board.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Total current from digital 1.8V supply	All outputs enabled; $V_{DD} = V_{DD,typ}$ 30.72MHz input; 61.44MHz output		270		mA
I_{AVDD}	Total current from analog 1.8V supply	All outputs enabled; $AV_{DD} = V_{DD,typ}$ 30.72MHz input; 61.44MHz output		85		mA
$V_{IL,CMOS}$	Low level CMOS input voltage	V_{DD} = 1.8V	–0.2		0.6	V
$V_{IH,CMOS}$	High level CMOS input voltage	V_{DD} = 1.8V	V_{DD} – 0.6		V_{DD}	V
$I_{IL,CMOS}$	Low level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IL} = 0.0V			–120	µA
$I_{IH,CMOS}$	High level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IH} = 1.9V			65	µA
$V_{OL,SDA}$	Low level CMOS output voltage for the SDA pin	Sink current = 3mA	0		$0.2V_{DD}$	V
$I_{OL,CMOS}$	Low level CMOS output current				8	mA

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{D,IN}$	Differential input impedance for the LVDS input terminals		90		132	Ω
$V_{CM,IN}$	Common-mode voltage, LVDS input		1125	1200	1375	mV
$V_{S,IN}$	Single-ended LVDS input voltage swing		100		600	mV_{PP}
$V_{D,IN}$	Differential LVDS input voltage swing		200		1200	mV_{PP}
$t_{R,OUT}$, $t_{F,OUT}$	Output signal rise/fall time	20%–80%		100		ps
$V_{CM,OUT}$	Common-mode voltage, CML outputs		V_{DD} –0.31	V_{DD} –0.23	V_{DD} –0.19	V
$V_{S,OUT}$	Single-ended CML output voltage swing	ac-coupled	180	230	280	mV_{PP}
$V_{D,OUT}$	Differential CML output voltage swing	Measured in a 50Ω scope; The CML output incorporates 50Ω resistors to V_{DD}	360	460	560	mV_{PP}
F_{IN}	Clock input frequency		30		319	MHz
F_{OUT}	Clock output frequency		15		1250	MHz
L_{OUT}	Residual clock output phase noise	F_{IN} = 30.72MHz , F_{OUT} = 61.44MHz 400kHz PLL bandwidth				
		at 10Hz offset		–103		dBc/Hz
		at 100Hz offset		–114		dBc/Hz
		at 1kHz offset		–123		dBc/Hz
		at 10kHz offset		–121		dBc/Hz
		at 100kHz offset		–119		dBc/Hz
		at 1MHz offset		–138		dBc/Hz
		at 10MHz offset		–152		dBc/Hz
		at 20MHz offset		–152		dBc/Hz
J_{OUT}	Residual clock output jitter	F_{IN} = 30.72MHz, F_{OUT} = 61.44MHz 400kHz PLL bandwidth				
		10Hz–1MHz offset		2.01		ps RMS
		1MHz–20MHz offset		0.45		ps RMS
		12kHz–20MHz offset		2.11		ps RMS
T_P	Input-to-output delay	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz YP[9:0] outputs, PLL bypass mode		3		ns
		F_{IN} = 30.72MHz, F_{OUT} = 61.44MHz YP[9:0] outputs, PLL mode		150		ps
TS_{OUT}	Clock output skew	F_{IN} = 30.72MHz, F_{OUT} = 61.44MHz YP[9:0] outputs relative to YP[0]	–64		64	ps
		F_{IN} = 122.88MHz, F_{OUT} (Y0 to Y4) = 61.44MHz, F_{OUT} (Y5 to Y9) = 122.88MHz (Y0 to Y4) lag (Y5 to Y9)	1.46		2.52	ns
$DCycle_{OUT}$	Clock output duty cycle(1)		45%		55%	

(1) Output duty cycle of the bypass output and for post-divide ratio = 1 is just as good as the input duty cycle.

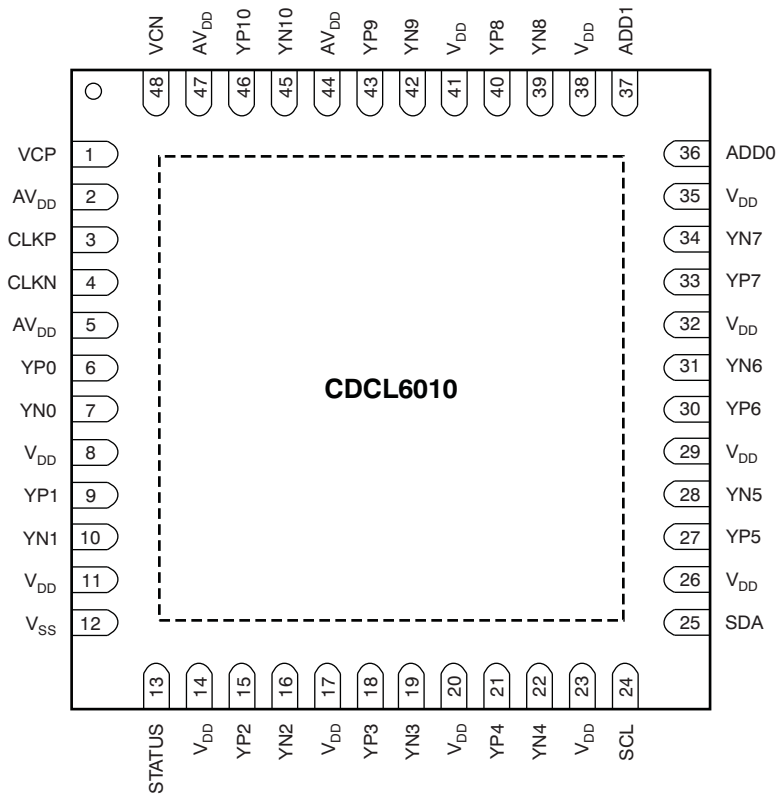
AC ELECTRICAL CHARACTERISTICS FOR THE SDA/SCL INTERFACE(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCL}	SCL frequency			400	kHz
$t_{h(START)}$	START hold time	0.6			µs
$t_{w(SCLL)}$	SCL low-pulse duration	1.3			µs
$t_{w(SCLH)}$	SCL high-pulse duration	0.6			µs
$t_{su(START)}$	START setup time	0.6			µs
$t_{h(SDATA)}$	SDA hold time	0			µs
$t_{su(DATA)}$	SDA setup time	0.6			µs
$t_{r(SDATA)}$	SCL / SDA input rise time			0.3	µs
$t_{f(SDATA)}$	SCL / SDA input fall time			0.3	µs
$t_{su(STOP)}$	STOP setup time	0.6			µs
t_{BUS}	Bus free time	1.3			µs

(1) See Figure 4 for the timing behavior.

DEVICE INFORMATION

48-PIN QFN (RGZ)
(TOP VIEW)



NOTE: Exposed thermal pad must be soldered to V_{SS}.

The CDCL6010 is available in a 48-pin QFN (RGZ) package with a pin pitch of 0,5mm. The exposed thermal pad serves both thermal and electrical grounding purposes.

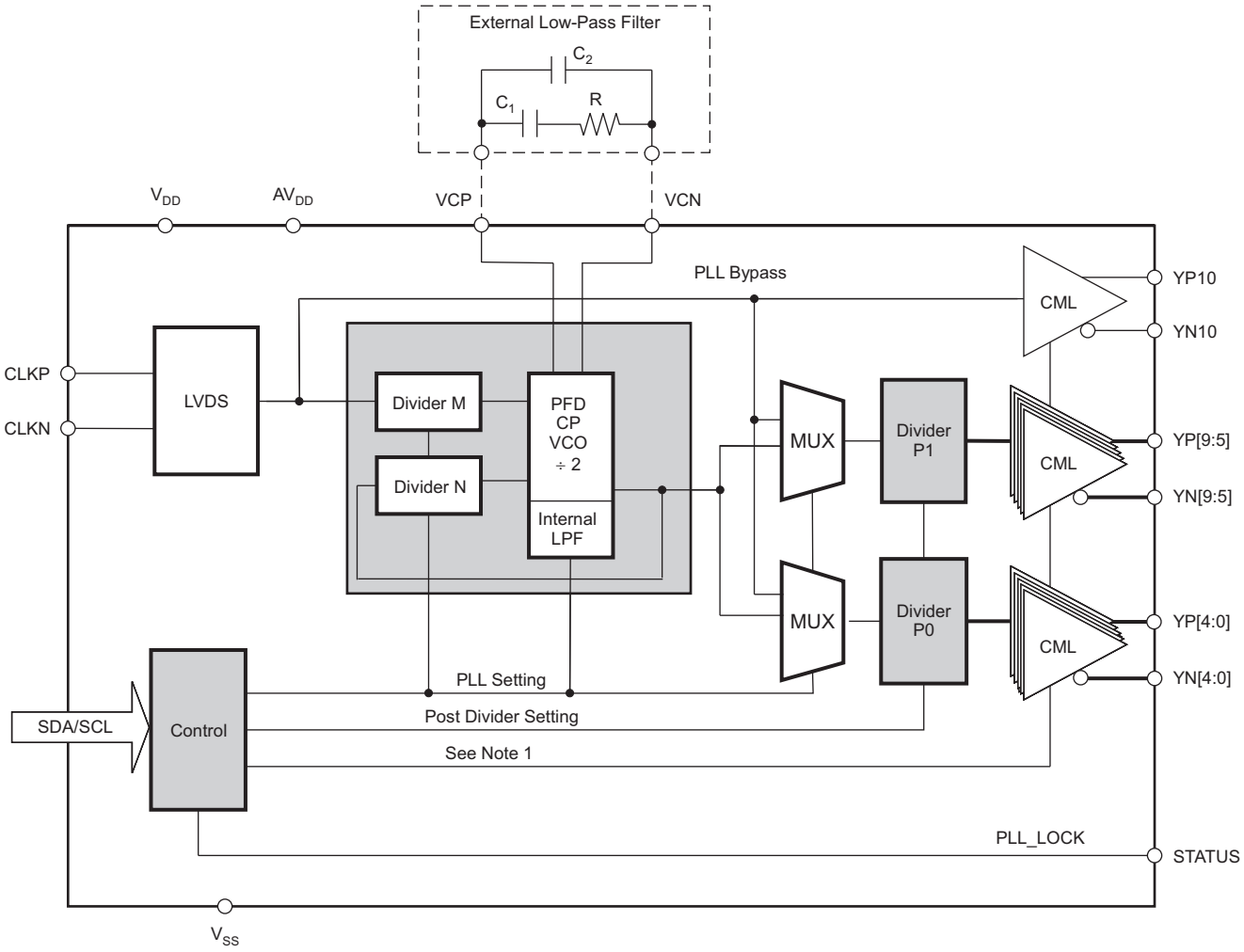
NOTE

The device must be soldered to ground (V_{SS}) using as many ground vias as possible. The device performance will be severely impacted if the exposed thermal pad is not grounded appropriately.

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	PIN NO.		
V_{DD}	8, 11, 14,17, 20, 23, 26, 29, 32, 35, 38, 41	Power	1.8V digital power supply.
AV_{DD}	2, 5, 44, 47	Power	1.8V analog power supply.
V_{SS}	Exposed thermal pad and pin 12	Power	Ground reference.
VCP, VCN	1, 48	I	External loop filter terminals.
CLKP, CLKN	3, 4	I	Differential LVDS input. Single-ended 1.8V input can be dc-coupled to pin 3 with pin 4 either tied to pin 3 (recommended) or left open.
YP0, YN0 YP1, YN1 YP2, YN2 YP3, YN3 YP4, YN4 YP5, YN5 YP6, YN6 YP7, YN7 YP8, YN8 YP9, YN9	6, 7 9, 10 15, 16 18, 19 21, 22 27, 28 30, 31 33, 34 40, 39 43, 42	O	10 differential CML outputs with support for jitter cleaning and clock multiplication. Support optional PLL bypass mode when jitter cleaning is not needed.
YP10, YN10	46, 45	O	Differential CML output. Straight bypass with no jitter cleaning and no clock multiplication.
SCL	24	I	SCL serial clock pin. Open drain. Always connect to a pull-up resistor. SCL tolerated 1.8V on the input only.
SDA	25	I/O	SDA bidirectional serial data pin. Open drain. Always connect to a pull-up resistor. SDA tolerates 1.8V on the input only
STATUS	13	O	LVCMOS status signaling. High status indicates PLL lock.
ADD1, ADD0	37, 36	I	Configurable least significant bits (ADD[1:0]) of the SDA/SCL device address. The fixed most significant bits (ADD[6:2]) of the 7-bit device address are 11010.

FUNCTIONAL BLOCK DIAGRAM



(1) Outputs can be disabled to floating. When outputs are left floating, internal 50Ω termination to V_{DD} pulls both YN and YP to V_{DD}.

TYPICAL CHARACTERISTICS

Typical operating conditions are at V_{DD} = 1.8V and T_A = +25°C, $V_{D,IN}$ = 200mV_{PP} (unless otherwise noted).

TRANSIENT PERFORMANCE: F_{IN} = 30.72MHz, F_{OUT} = 61.44MHz

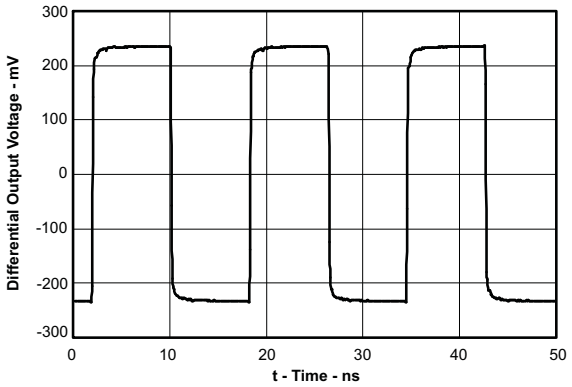


Figure 1.

TRANSIENT PERFORMANCE: F_{IN} = 250MHz, F_{OUT} = 1.25GHz

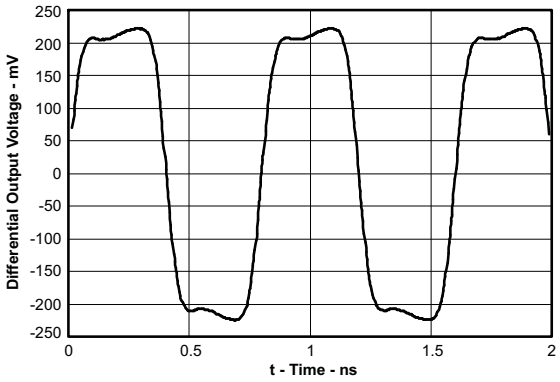


Figure 2.

PHASE NOISE: F_{IN} = 30.72MHz, F_{OUT} = 61.44MHz

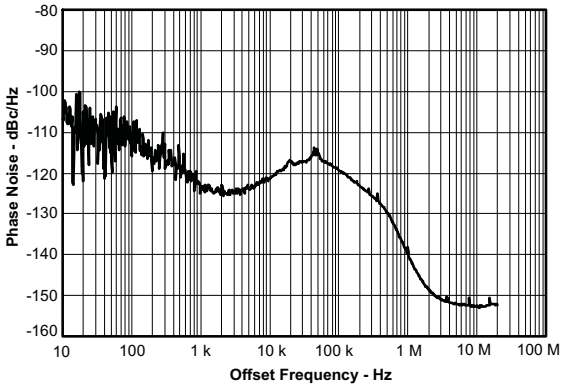


Figure 3.

SDA/SCL INTERFACE

This section describes the SDA/SCL interface of the CDCL6010 device. The CDCL6010 operates as a slave device of the industry standard 2-pin SDA/SCL bus. It operates in the fast-mode at a bit-rate of up to 400kbit/s and supports 7-bit addressing compatible with the popular two-pin serial interface standard.

SDA/SCL Bus Slave Device Address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	ADD1	ADD0	0/1

The device address is made up of the fixed internal address, 11010 (A6:A2), and configurable external pins ADD1 (A1) and ADD0 (A0). Four different devices with addresses 1101000, 1101001, 1101010 and 1101011, can be addressed via the same SDA/SCL bus interface. The least significant bit of the address byte designates a write or read operation.

R/W Bit:

0 = Write to CDCL6010 device

1 = Read from CDCL6010 device

Command Code Definition

BIT	DESCRIPTION
C7	1 = *Byte Write* / *Read* or *Word Write* / *Read* operation
(C6:C0)	Byte Offset for *Byte Write* / *Read* and Word Write / Read operation.

Command Code for *Byte Write* / *Read* Operation	Hex Code	C7	C6	C5	C4	C3	C2	C1	C0
Byte 0	80h	1	0	0	0	0	0	0	0
Byte 1	81h	1	0	0	0	0	0	0	1
Byte 2	82h	1	0	0	0	0	0	1	0
Byte 3	83h	1	0	0	0	0	0	1	1
Byte 4	84h	1	0	0	0	0	1	0	0
Byte 5	85h	1	0	0	0	0	1	0	1
Byte 6	86h	1	0	0	0	0	1	1	0
Byte 7	87h	1	0	0	0	0	1	1	1

Command Code for *Word Write* / *Read* Operation	Hex Code	C7	C6	C5	C4	C3	C2	C1	C0
Word 0: Byte 0 and byte 1	80h	1	0	0	0	0	0	0	0
Word 1: Byte 1 and byte 2	81h	1	0	0	0	0	0	0	1
Word 2: Byte 2 and byte 3	82h	1	0	0	0	0	0	1	0
Word 3: Byte 3 and byte 4	83h	1	0	0	0	0	0	1	1
Word 4: Byte 4 and byte 5	84h	1	0	0	0	0	1	0	0
Word 5: Byte 5 and byte 6	85h	1	0	0	0	0	1	0	1
Word 6: Byte 6 and byte 7	86h	1	0	0	0	0	1	1	0
Word 7: Byte 7	87h	1	0	0	0	0	1	1	1

SDA/SCL Timing Characteristics

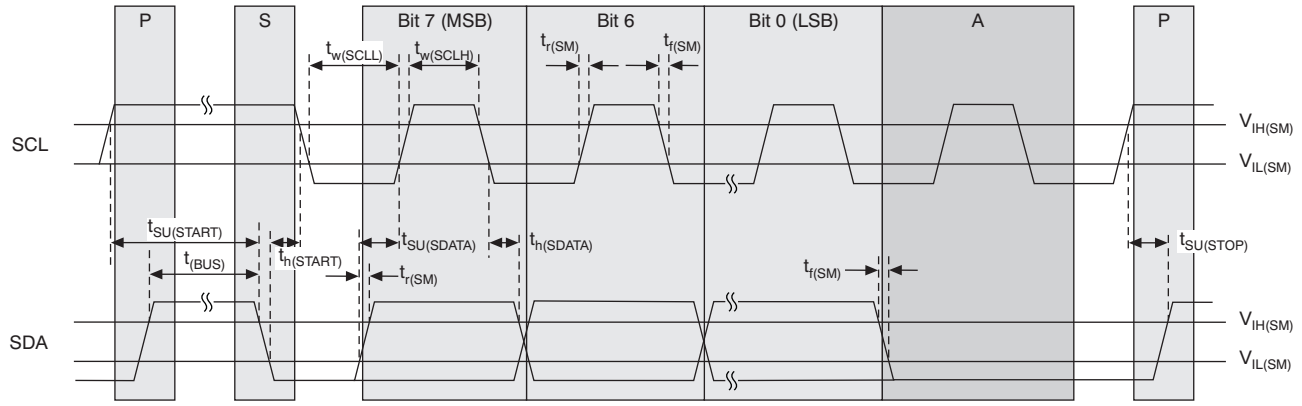


Figure 4. Timing Diagram for the SDA/SCL Serial Control Interface

SDA/SCL Programming Sequence

LEGEND FOR PROGRAMMING SEQUENCE

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	P

S	Start condition
Sr	Repeated start condition
Rd	Read (bit value = 1)
Wr	Write (bit value = 0)
A	Acknowledge (bit value = 0)
N	Not acknowledge (bit value = 1)
P	Stop condition
	Master to Slave transmission
	Slave to Master transmission

Byte Write Programming Sequence:

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

Byte Read Programming Sequence:

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	N	P

***Word Write* Programming Sequence:**

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

***Word Read* Programming Sequence:**

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	Data Byte	N	P

SDA/SCL Connections Recommendations

The serial interface inputs don't have glitch suppression circuit. So, any noises or glitches at serial input lines may cause programming error. The serial interface lines should be routed in such a way that the lines would have minimum noise impact from the surroundings.

Figure 5 is recommended to improve the interconnections.

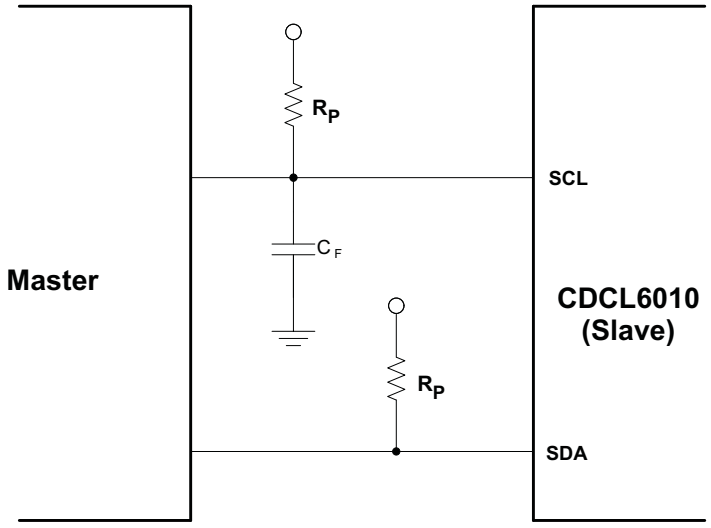


Figure 5. Serial Interface Connections

Lower R_P resistor value (around 1 kΩ) should be chosen so that signals will have faster rise time. A capacitor can be connected to SCL line to ground which will act as a filter.

An I^2C level translator will help to overcome the noises issue.

SDA/SCL Bus Configuration Command Bitmap

Byte 0:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	PLL-LOCK	1 if PLL has achieved lock, otherwise 0	R	0	
6	MANF[6]	Manufacturer reserved	R		
5	MANF[5]	Manufacturer reserved	R		
4	MANF[4]	Manufacturer reserved	R		
3	MANF[3]	Manufacturer reserved	R		
2	MANF[2]	Manufacturer reserved	R		
1	MANF[1]	Manufacturer reserved	R		
0	MANF[0]	Manufacturer reserved	R		

Byte 1:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENPH	Phase select enable	R/W	1	
4	PH1[4]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 5, Table 6
3	PH1[3]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 5, Table 6
2	PH1[2]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 5, Table 6
1	PH1[1]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 5, Table 6
0	PH1[0]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 5, Table 6

Byte 2:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENP1	Post-divider P1 enable; if 0 output YP[9:5] and YN[9:5] are disabled	R/W	1	
4	ENBP1	Bypass PLL for post-divider P1: If 1 input is CLKP/CLKN, if 0 input is PLL clock	R/W	0	
3	SELP1[3]	Divide ratio select for post-divider P1	R/W	0	Table 2
2	SELP1[2]	Divide ratio select for post-divider P1	R/W	1	Table 2
1	SELP1[1]	Divide ratio select for post-divider P1	R/W	1	Table 2
0	SELP1[0]	Divide ratio select for post-divider P1	R/W	1	Table 2

Byte 3:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	PLLLOCK OW	PLL Lock Overwrite: If 1 output not gated by PLL Lock status.	R/W	0	
4	PH0[4]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 5, Table 6
3	PH0[3]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 5, Table 6
2	PH0[2]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 5, Table 6
1	PH0[1]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 5, Table 6
0	PH0[0]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 5, Table 6

Byte 4:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENP0	Post-divider P0 enable. If 0, output YP[4:0] and YN[4:0] are disabled	R/W	1	
4	ENBP0	Bypass PLL for post-divider P0. If 1, input is CLKP/CLKN; if 0 input is PLL clock	R/W	0	
3	SELP0[3]	Divide ratio select for post-divider P0	R/W	0	Table 2
2	SELP0[2]	Divide ratio select for post-divider P0	R/W	1	Table 2
1	SELP0[1]	Divide ratio select for post-divider P0	R/W	1	Table 2
0	SELP0[0]	Divide ratio select for post-divider P0	R/W	1	Table 2

Byte 5:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	EN	Chip enable; if 0 chip is in Iddq mode	R/W	1	
6	ENDRV10	YP10, YN10 enable; if 0 output is disabled	R/W	1	
5	ENDRV9	YP[9], YN[9] enable; if 0 output is disabled	R/W	1	
4	ENDRV8	YP[8], YN[8] enable; if 0 output is disabled	R/W	1	
3	ENDRV7	YP[7], YN[7] enable; if 0 output is disabled	R/W	1	
2	ENDRV6	YP[6], YN[6] enable; if 0 output is disabled	R/W	1	
1	ENDRV5	YP[5], YN[5] enable; if 0 output is disabled	R/W	1	
0	ENDRV4	YP[4], YN[4] enable; if 0 output is disabled	R/W	1	

Byte 6:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	ENDRV3	YP[3], YN[3] enable; if 0 output is disabled	R/W	1	
6	ENDRV2	YP[2], YN[2] enable; if 0 output is disabled	R/W	1	
5	ENDRV1	YP[1], YN[1] enable; if 0 output is disabled	R/W	1	
4	ENDRV0	YP[0], YN[0] enable; if 0 output is disabled	R/W	1	
3	SELBW[3]	PLL BW select; if 1 external loop filter is expected	R/W	0	Table 7
2	SELBW[2]	PLL BW select; if 1 external loop filter is expected	R/W	0	Table 7
1	SELBW[1]	PLL BW select; if 1 external loop filter is expected	R/W	0	Table 7
0	SELBW[0]	PLL BW select; if 1 external loop filter is expected	R/W	0	Table 7

Byte 7:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	ENPLL	PLL enable; if 0 PLL is switched off	R/W	1	
6	RES	Reserved	R/W	0	
5	SELM[1]	Divide ratio select for input clock CLKP and CLKN	R/W	0	Table 4
4	SELM[0]	Divide ratio select for input clock CLKP and CLKN	R/W	0	Table 4
3	SELN[3]	Divide ratio select for pre-divider N (PLL clock)	R/W	1	Table 3
2	SELN[2]	Divide ratio select for pre-divider N (PLL clock)	R/W	0	Table 3
1	SELN[1]	Divide ratio select for pre-divider N (PLL clock)	R/W	0	Table 3
0	SELN[0]	Divide ratio select for pre-divider N (PLL clock)	R/W	1	Table 3

Table 2. Divide Ratio Settings for Post-Divider P0 or P1

Divide Ratio	SELP1[3] or SELP0[3]	SELP1[2] or SELP0[2]	SELP1[1] or SELP0[1]	SELP1[0] or SELP0[0]	Notes
1	0	0	0	0	
2	0	0	0	1	
4	0	0	1	0	
5	0	0	1	1	
8	0	1	0	0	
10	0	1	0	1	
16	0	1	1	0	
20	0	1	1	1	Default
32	1	0	0	0	
40	1	0	0	1	
80	1	0	1	0	

Table 3. Divide Ratio Settings for Divider N

Divide Ratio	SELN[3]	SELN[2]	SELN[1]	SELN[0]	Notes
32	1	0	0	0	
40	1	0	0	1	Default

Table 4. Divide Ratio Settings for Divider M

Divide Ratio	SELM[1]	SELM[0]	Notes
1	0	0	Default
2	0	1	
4	1	0	
8	1	1	

Table 5. Phase Settings for Divide Ratio = 5, 10, 20, 40, 80

Divide Ratio	With PH0[4:0] = 00000					Phase Lead (radian)	Notes
	PH1						
	[4]	[3]	[2]	[1]	[0]		
5	X	X	X	X	X	0	Phase setting not available
10	X	X	X	0	X	0	
	X	X	X	1	X	(2π/2)	
20	X	X	0	0	X	0	00000:Default
	X	X	0	1	X	(2π/4)	
	X	X	1	0	X	2(2π/4)	
	X	X	1	1	X	3(2π/4)	
40	X	0	0	0	X	0	
	X	0	0	1	X	(2π/8)	
	X	0	1	0	X	2(2π/8)	
	X	0	1	1	X	3(2π/8)	
	X	1	0	0	X	4(2π/8)	
	X	1	0	1	X	5(2π/8)	
	X	1	1	0	X	6(2π/8)	
	X	1	1	1	X	7(2π/8)	
80	0	0	0	0	X	0	
	0	0	0	1	X	(2π/16)	
	0	0	1	0	X	2(2π/16)	
	0	0	1	1	X	3(2π/16)	
	0	1	0	0	X	4(2π/16)	
	0	1	0	1	X	5(2π/16)	
	0	1	1	0	X	6(2π/16)	
	0	1	1	1	X	7(2π/16)	
	1	0	0	0	X	8(2π/16)	
	1	0	0	1	X	9(2π/16)	
	1	0	1	0	X	10(2π/16)	
	1	0	1	1	X	11(2π/16)	
	1	1	0	0	X	12(2π/16)	
	1	1	0	1	X	13(2π/16)	
	1	1	1	0	X	14(2π/16)	
	1	1	1	1	X	15(2π/16)	

Table 6. Phase Settings for Divide Ratio = 1, 2, 4, 8, 16, 32

Divide Ratio	With PH0[4:0] = 00000					Phase Lead (radian)	Notes
	PH1						
	[4]	[3]	[2]	[1]	[0]		
1	X	X	X	X	X	0	Phase setting not available
2	X	X	X	X	0	0	
	X	X	X	X	1	(2π/2)	
4	X	X	X	0	0	0	
	X	X	X	0	1	(2π/4)	
	X	X	X	1	0	2(2π/4)	
	X	X	X	1	1	3(2π/4)	
8	X	X	0	0	0	0	
	X	X	0	0	1	(2π/8)	
	X	X	0	1	0	2(2π/8)	
	X	X	0	1	1	3(2π/8)	
	X	X	1	0	0	4(2π/8)	
	X	X	1	0	1	5(2π/8)	
	X	X	1	1	0	6(2π/8)	
	X	X	1	1	1	7(2π/8)	
16	X	0	0	0	0	0	
	X	0	0	0	1	(2π/16)	
	X	0	0	1	0	2(2π/16)	
	X	0	0	1	1	3(2π/16)	
	X	0	1	0	0	4(2π/16)	
	X	0	1	0	1	5(2π/16)	
	X	0	1	1	0	6(2π/16)	
	X	0	1	1	1	7(2π/16)	
	X	1	0	0	0	8(2π/16)	
	X	1	0	0	1	9(2π/16)	
	X	1	0	1	0	10(2π/16)	
	X	1	0	1	1	11(2π/16)	
	X	1	1	0	0	12(2π/16)	
	X	1	1	0	1	13(2π/16)	
	X	1	1	1	0	14(2π/16)	
	X	1	1	1	1	15(2π/16)	

Table 6. Phase Settings for Divide Ratio = 1, 2, 4, 8, 16, 32 (continued)

Divide Ratio	With PH0[4:0] = 00000					Phase Lead (radian)	Notes
	PH1						
	[4]	[3]	[2]	[1]	[0]		
32	0	0	0	0	0	0	
	0	0	0	0	1	(2π/32)	
	0	0	0	1	0	2(2π/32)	
	0	0	0	1	1	3(2π/32)	
	0	0	1	0	0	4(2π/32)	
	0	0	1	0	1	5(2π/32)	
	0	0	1	1	0	6(2π/32)	
	0	0	1	1	1	7(2π/32)	
	0	1	0	0	0	8(2π/32)	
	0	1	0	0	1	9(2π/32)	
	0	1	0	1	0	10(2π/32)	
	0	1	0	1	1	11(2π/32)	
	0	1	1	0	0	12(2π/32)	
	0	1	1	0	1	13(2π/32)	
	0	1	1	1	0	14(2π/32)	
	0	1	1	1	1	15(2π/32)	
	1	0	0	0	0	16(2π/32)	
	1	0	0	0	1	17(2π/32)	
	1	0	0	1	0	18(2π/32)	
	1	0	0	1	1	19(2π/32)	
	1	0	1	0	0	20(2π/32)	
	1	0	1	0	1	21(2π/32)	
	1	0	1	1	0	22(2π/32)	
	1	0	1	1	1	23(2π/32)	
	1	1	0	0	0	24(2π/32)	
	1	1	0	0	1	25(2π/32)	
	1	1	0	1	0	26(2π/32)	
	1	1	0	1	1	27(2π/32)	
	1	1	1	0	0	28(2π/32)	
	1	1	1	0	1	29(2π/32)	
	1	1	1	1	0	30(2π/32)	
	1	1	1	1	1	31(2π/32)	

Table 7. PLL Bandwidth Setting

PLL Bandwidth(1) (kHz)	SELBW				C_1 (nF)	R (Ω)	C_2 (nF)	On-Chip Loop Filter ON/OFF	Notes
	[3]	[2]	[1]	[0]					
400	0	0	0	0	N/A	N/A	N/A	ON	Default
350	0	0	1	0	2.2	8660	0	OFF	
300	0	0	1	1	3.3	7500	0	OFF	
250	0	1	0	0	4.7	6200	0	OFF	
200	0	1	1	0	8.2	4990	0	OFF	
175	1	0	0	0	10	4300	0	OFF	
150	1	0	1	0	15	3740	0	OFF	
125	1	1	1	1	22	3090	0	OFF	
100	1	1	1	1	33	2490	0.24	OFF	
75	1	1	1	1	56	1870	0.82	OFF	
50	1	1	1	1	150	1210	2.70	OFF	
20	1	1	1	1	680	470	18	OFF	
10	1	1	1	1	3300	220	68	OFF	

(1) Refer to Functional Block Diagram for the external low pass filter architecture.

FREQUENCY SETTINGS FOR SOME APPLICATIONS

APPLICATION									
PROTOCOL	Output Clock MHz	Output Divider P0, P1	VCO Freq GHz	PLL Divider N (max f)	Ref Clock Divider M (max f)	Ref Clock Max Freq MHz	PLL Divider N (min f)	Ref Clock Divider M (min f)	Ref Clock Min Freq MHz
10G Ethernet	312.5	4	1.250	32	8	312.5	40	1	31.25
(XAUI)	156.25	8	1.250	32	8	312.5	40	1	31.25
	78.125	16	1.250	32	8	312.5	40	1	31.25
	62.5	20	1.250	32	8	312.5	40	1	31.25
1G Ethernet	250	5	1.250	40	8	250	40	1	31.25
Serial ATA	125	10	1.250	40	8	250	40	1	31.25
	62.5	20	1.250	40	8	250	40	1	31.25
10X FIBRE CHANNEL	159.375	8	1.275	32	8	318.75	40	1	31.875
	63.75	20	1.275	32	8	318.75	40	1	31.875
CPRI	245.76	5	1.229	40	8	245.78	40	1	30.72
	122.88	10	1.229	40	8	245.78	40	1	30.72
	61.44	20	1.229	40	8	245.78	40	1	30.72
	30.72	40	1.229	40	8	245.78	40	1	30.72
OBSAI	153.6	8	1.229	32	8	307.2	32	1	38.4
	76.8	16	1.229	32	8	307.2	32	1	38.4
PCI Express	250	5	1.250	40	8	250	40	1	31.25
Serial ATA	150	8	1.200	32	8	300	32	1	37.5
	75	16	1.200	32	8	300	32	1	37.5
SONET	622.08	2	1.244	32	8	311.04	40	1	31.104
	311.04	4	1.244	32	8	311.04	40	1	31.104
	155.52	8	1.244	32	8	311.04	40	1	31.104
	62.208	20	1.244	32	8	311.04	40	1	31.104

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2007) to Revision A **Page**

- Added second specification condition for clock output skew parameter. 4

Changes from Revision A (March 2008) to Revision B **Page**

- Added Sentence to the Description: The serial interface is 1.8V tolerant only. 2
- Changed V_{ILVDS} From: -0.3 to 4.0 To: -0.3 to V_{DD} + 0.6 in the Abs Max table 3
- Changed V_I From: -0.3 to 3.0 To: -0.3 to V_{DD} + 0.6 in the Abs Max table 3
- Added the THERMAL INFORMATION table 3
- Changed the Test Conditions of $V_{D,OUT}$ in the AC Electrical Characteristics table 4
- Changed the description of SCL and SDA in the PIn Functions table 7
- Added Note 1 to the FUNCTIONAL BLOCK DIAGRAM 8
- Added the SDA/SCL Connections Recommendations section 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCL6010RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCL 6010	Samples
CDCL6010RGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCL 6010	Samples
CDCL6010RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCL 6010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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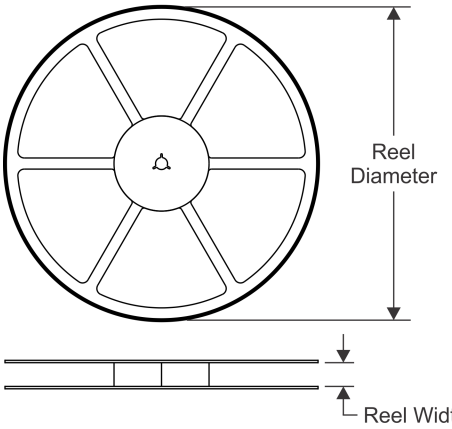
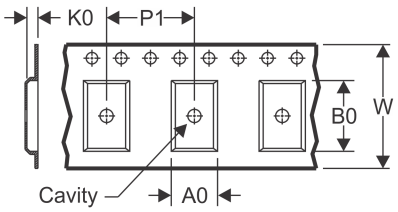
TAPE AND REEL INFORMATION

REEL DIMENSIONS

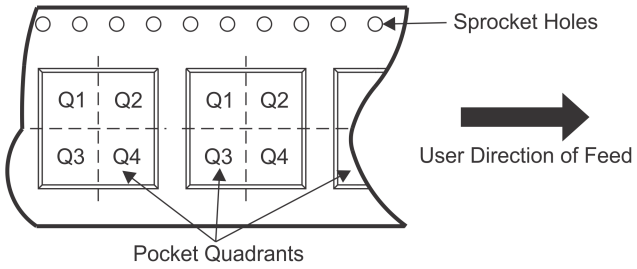


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

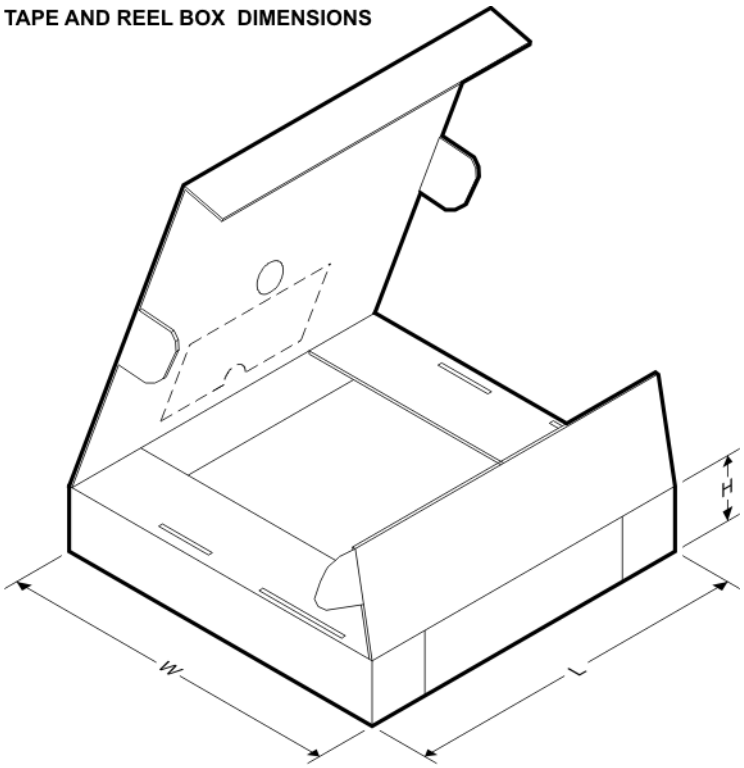
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCL6010RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCL6010RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCL6010RGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
CDCL6010RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

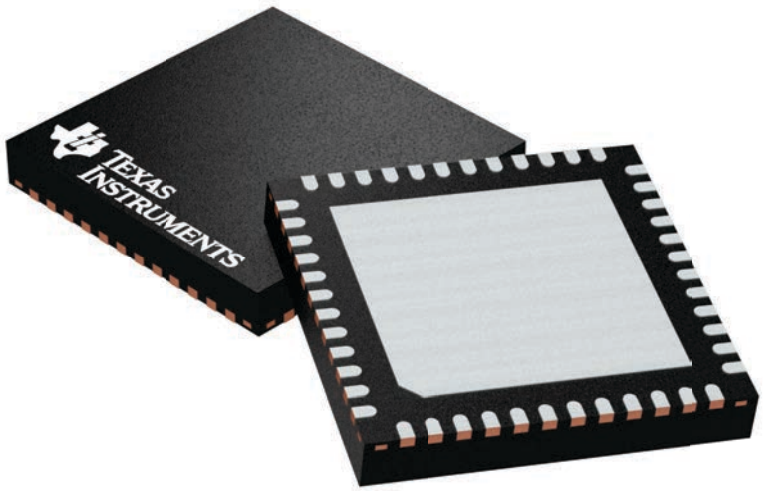
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

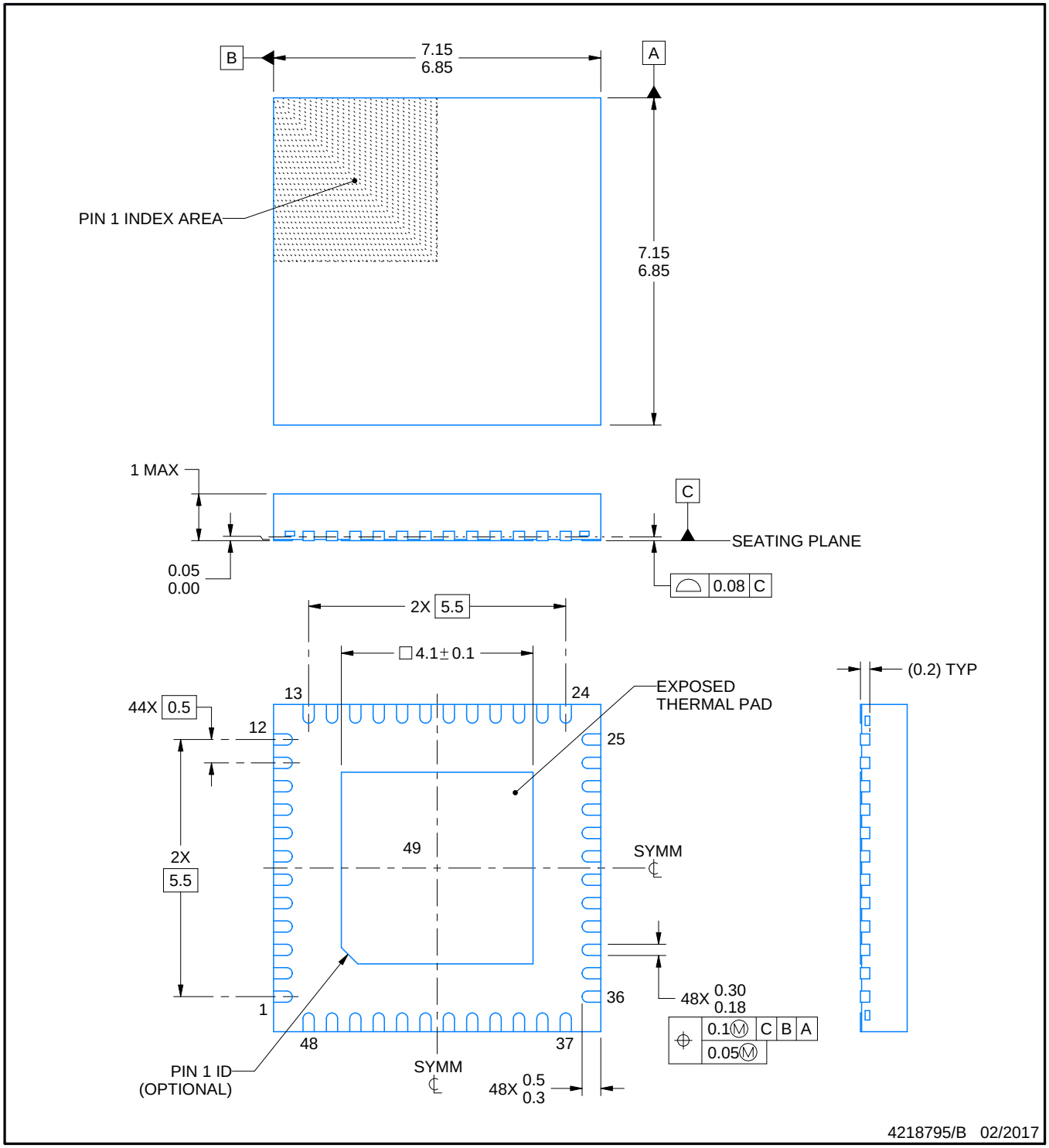
4224671/A

RGZ0048B

PACKAGE OUTLINE

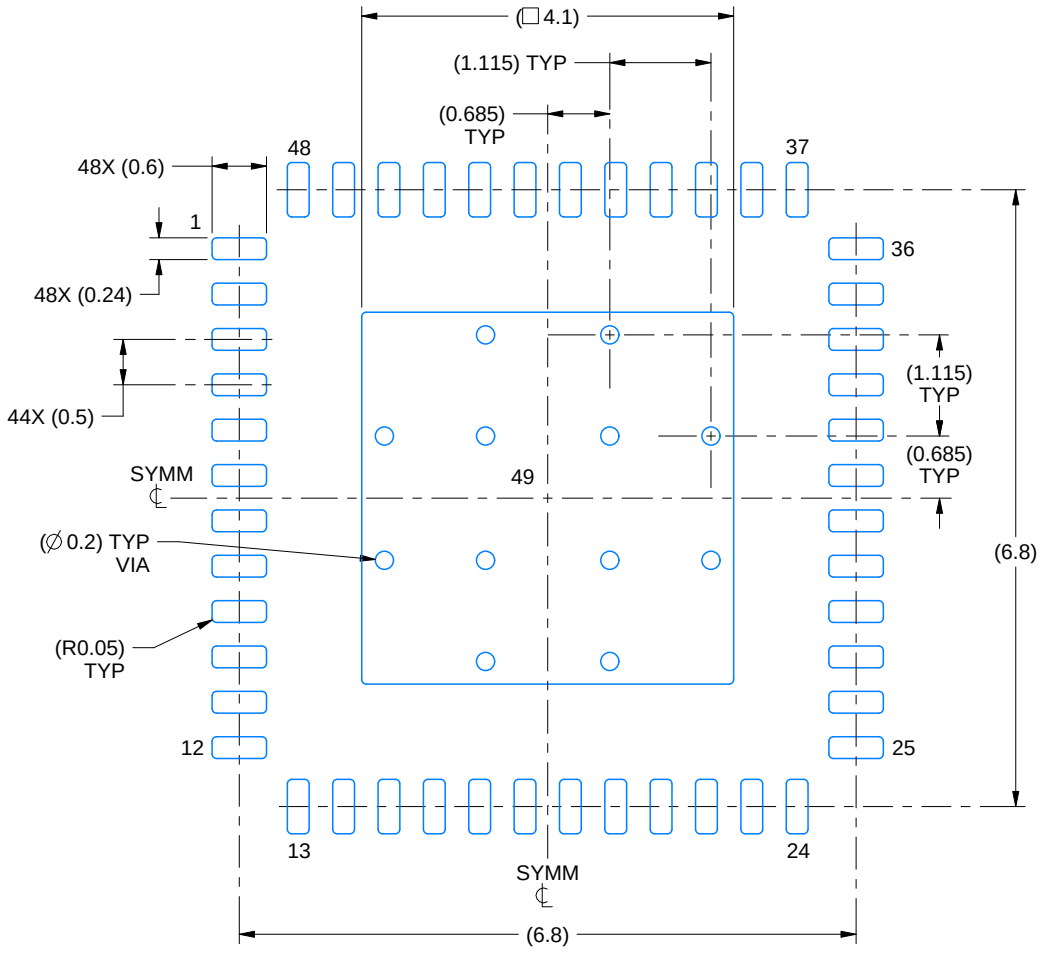
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

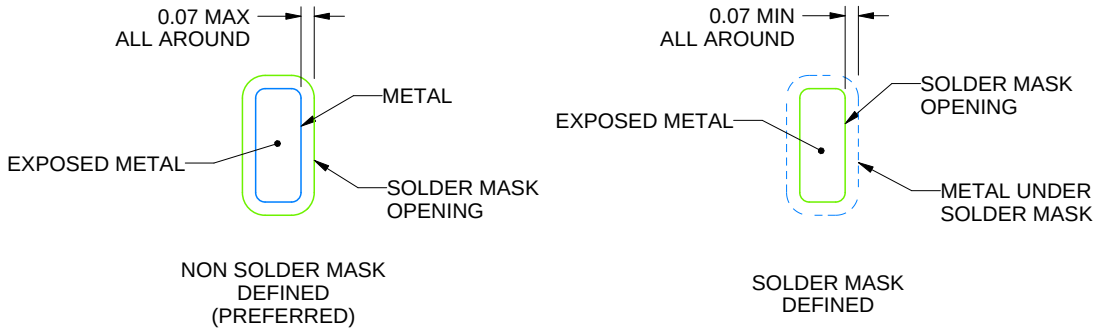


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

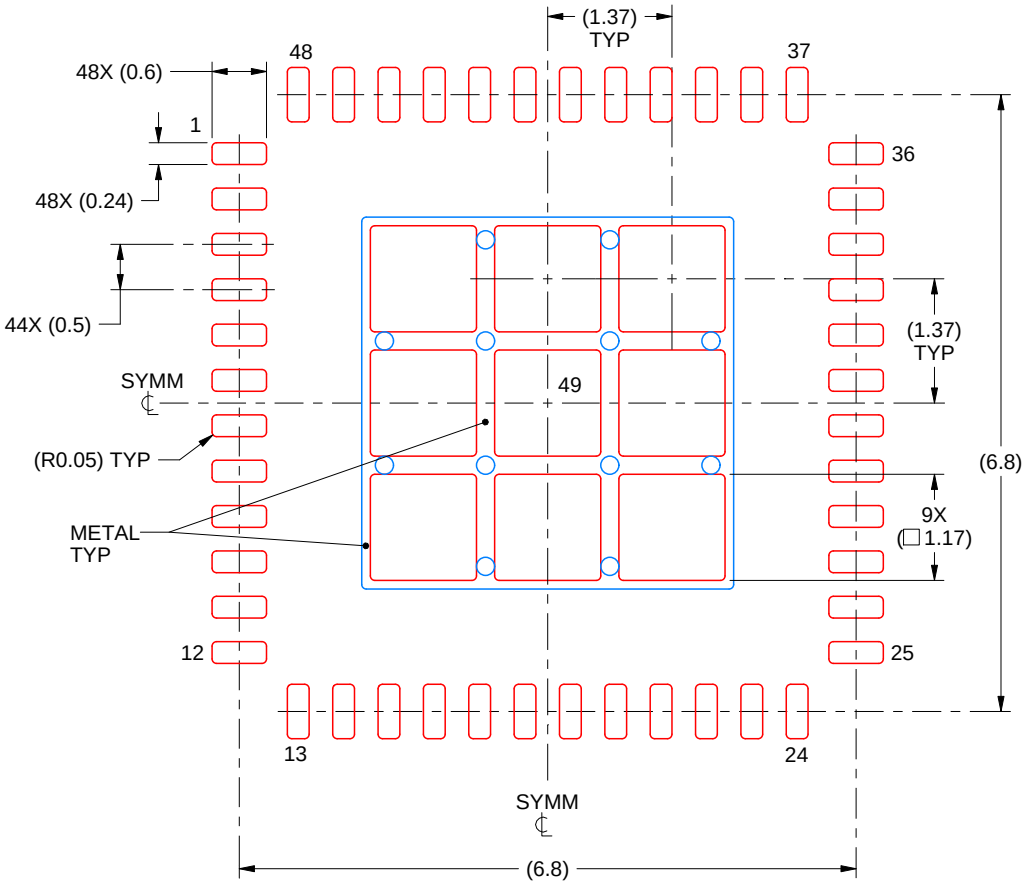


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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