THE DATASHEET OF

SC4215JSETRT

SC4215J

Very Low Input /Very Low Dropout 2 Amp Regulator With Soft-Start

Features

- Input Voltage as Low as 1.4V
- 400mV Dropout @ 2A
- Adjustable Output from 0.5V
- 1ms Internal Soft-Start Minimizes Inrush Current
- Over Current and Over Temperature Protection
- Enable Function Option
- 10µA Quiescent Current in Shutdown
- Reverse Blocking from Output to Input
- Full Industrial Temperature Range
- Fully WEEE and RoHS Compliant

Applications

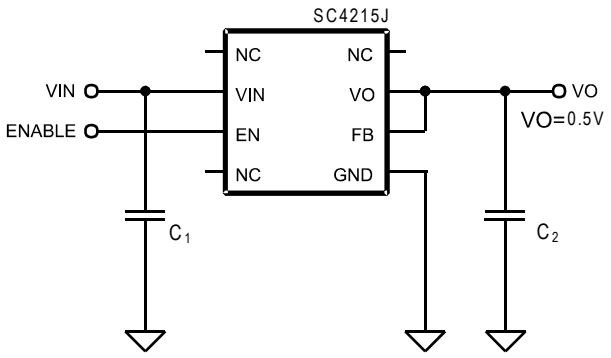
- Telecom and Networking Cards
- Motherboards and Peripheral Cards
- Industrial Applications
- Wireless Infrastructure
- Medical Equipment

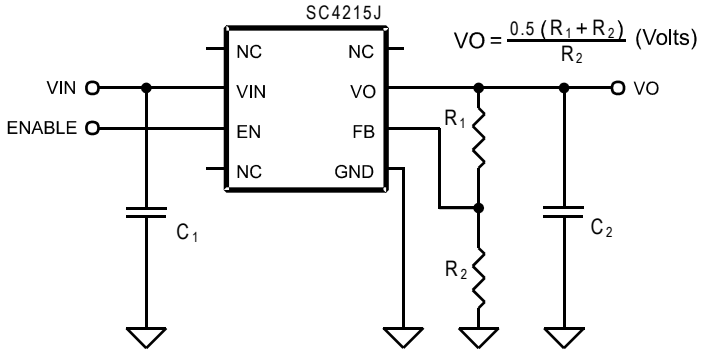
Description

The SC4215J is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 2 amperes. It operates with a Vin as low as 1.4V, with output voltage programmable as low as 0.5V. The SC4215J features ultra low dropout, ideal for applications where Vout is very close to Vin. Additionally, the SC4215J has an enable pin to further reduce power dissipation while shut down. The SC4215J provides excellent regulation over variations in line, load and temperature.

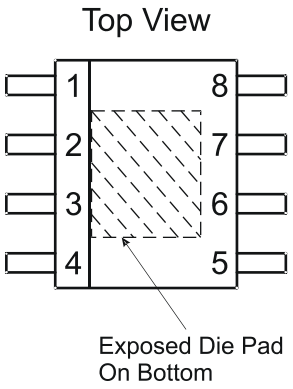
The SC4215J is available in the SOIC-8-EDP (Exposed Die Pad) package. The output voltage can be set via an external divider or to a fixed setting of 0.5V depending upon how the FB pin is configured.

Typical Application Circuit





Pin Configuration

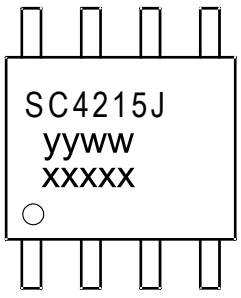


Ordering Information

Device	Package
SC4215JSETRT[1][2]	SOIC-8-EDP
SC4215JEVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 2,500 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant and halogen free.

Marking Information



yyww = Datecode (Example: 0752)
xxxxx = Semtech Lot No. (Example: 00101)

SEMTECH

Absolute Maximum Ratings

VIN, EN, VO, FB to GND (V) ..... -0.3 to +7.0
Power Dissipation ..... Internally Limited
ESD Protection Level[1] (kV) 4

Recommended Operating Conditions

VIN (V) ..... $1.4 \leq V_{IN} \leq 6.0$
Junction Temperature Range (°C) ..... $-40 \leq T_J \leq +125$
Maximum Output Current (A) 2

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 36
Thermal Resistance, Junc to Case[2] (°C/W) 5.5
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: $V_{EN} = V_{IN}$, $V_{FB} = V_O$, V_{IN} = 1.40V to 6.0V, I_O = 10µA to 2A, T_J = 25° C.
Values in bold apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
V_{IN} Operating Range [1]				**1.4**		**6.0**	V
Quiescent Current	I_Q	V_{IN} = 3.3V, I_O = 0A				**3**	mA
		V_{IN} = 6.0V, V_{EN} =0V			10	**50**	µA
Dropout Voltage[2][3]	V_{DO}	I_O =1A	1.4V ≤ V_{IN} < 1.6V		90	**400**	mV
			1.6V ≤ V_{IN} ≤ 6.0V			**200**	
		I_O =1.5A	1.4V ≤ V_{IN} < 1.6V		200	**500**	
			1.6V ≤ V_{IN} ≤ 6.0V			**300**	
		I_O = 2A	1.4V ≤ V_{IN} < 1.6V		300	**600**	
			1.6V ≤ V_{IN} ≤ 6.0V			**400**	
Minimum Load Current[4]	I_O					**10**	µA
Current Limit	I_{CL}			**2.1**	3	**4.4**	A

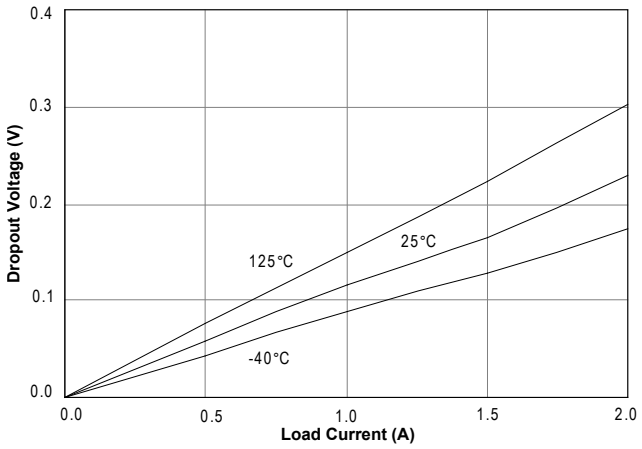
Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Feedback						
Reference Voltage[2]	V_{REF}	V_{IN} = 3.3V, I_O =10mA	0.495	0.500	0.505	V
			0.490		**0.510**	
			0.485		**0.515**	
Line Regulation		I_O = 10mA		0.2		%/V
Load Regulation [5]		I_O = 10mA to 2A		0.3		%
Feedback Pin Current		$V_{FB} = V_{REF}$		80	**200**	nA
EN						
Enable Pin Current	I_{EN}	V_{EN} = 0V, V_{IN} =3.3V		1.5	**10**	µA
Enable Pin Threshold	V_{IH}	V_{IN}=3.3V	**1.6**			V
	V_{IL}				**0.4**	
Over Temperature Protection						
High Trip Level	T_{HI}			160		°C
Hysteresis	T_{HYST}			10		°C
Soft-Start						
Soft-Start Time [6]	t_{SS}		**0.7**	1		ms

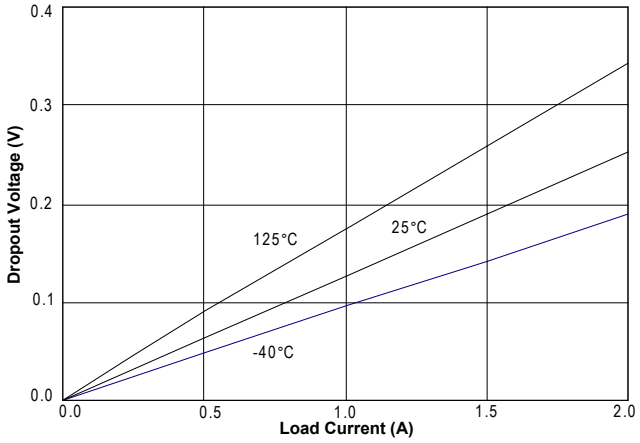
Notes:
(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.4V, whichever is greater.
(2) Low duty cycle pulse testing with Kelvin connections required.
(3) $V_{DO} = V_{IN} - V_O$ when V_O decreases by 1.5% of its nominal output voltage with $V_{IN} = V_O$ +0.8V.
(4) Required to maintain regulation. Voltage set resistors R_1 and R_2 are usually utilized to meet this requirement.
(5) Where the power dissipation does not exceed the maximum rating of the package. Refer to Figure 1 on page 8.
(6) Time taken for the output to rise from 0% to 95% of the programmed output voltage.

Typical Characteristics

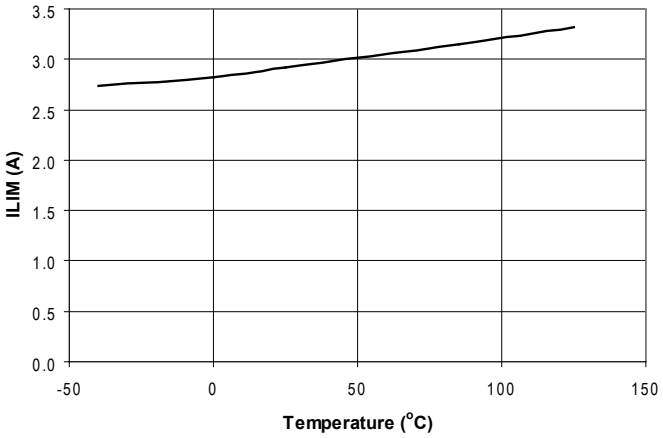
Dropout Voltage at V_O = 3.3V



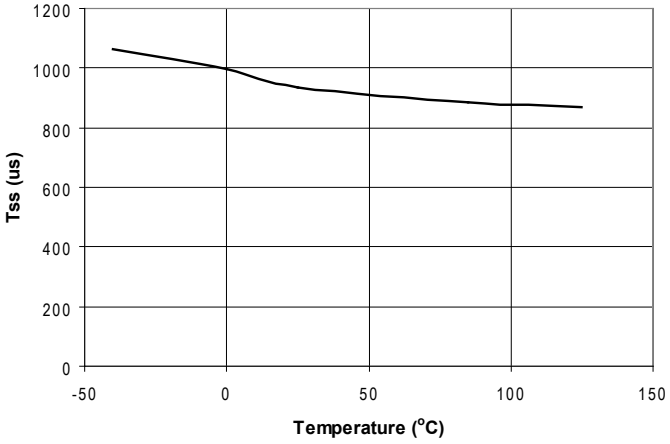
Dropout Voltage at V_O = 1.5V



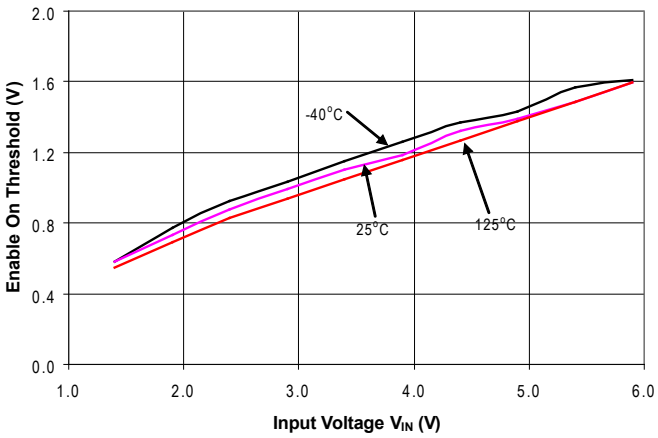
Current Limit vs Temperature



Startup Time vs Temperature

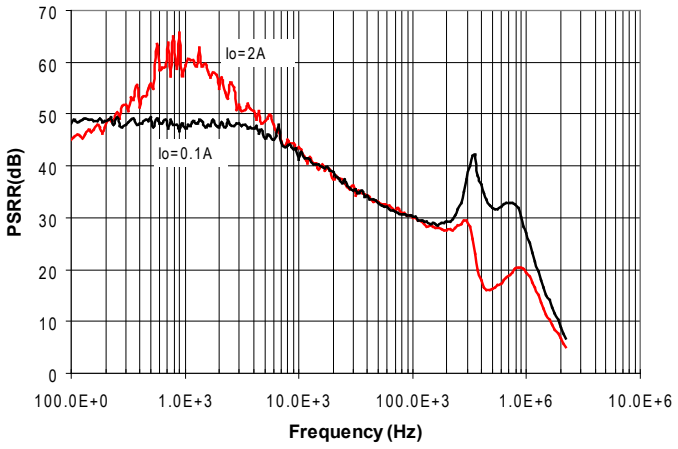


EN Threshold vs V_{IN}



Power-Supply Ripple Rejection vs Frequency

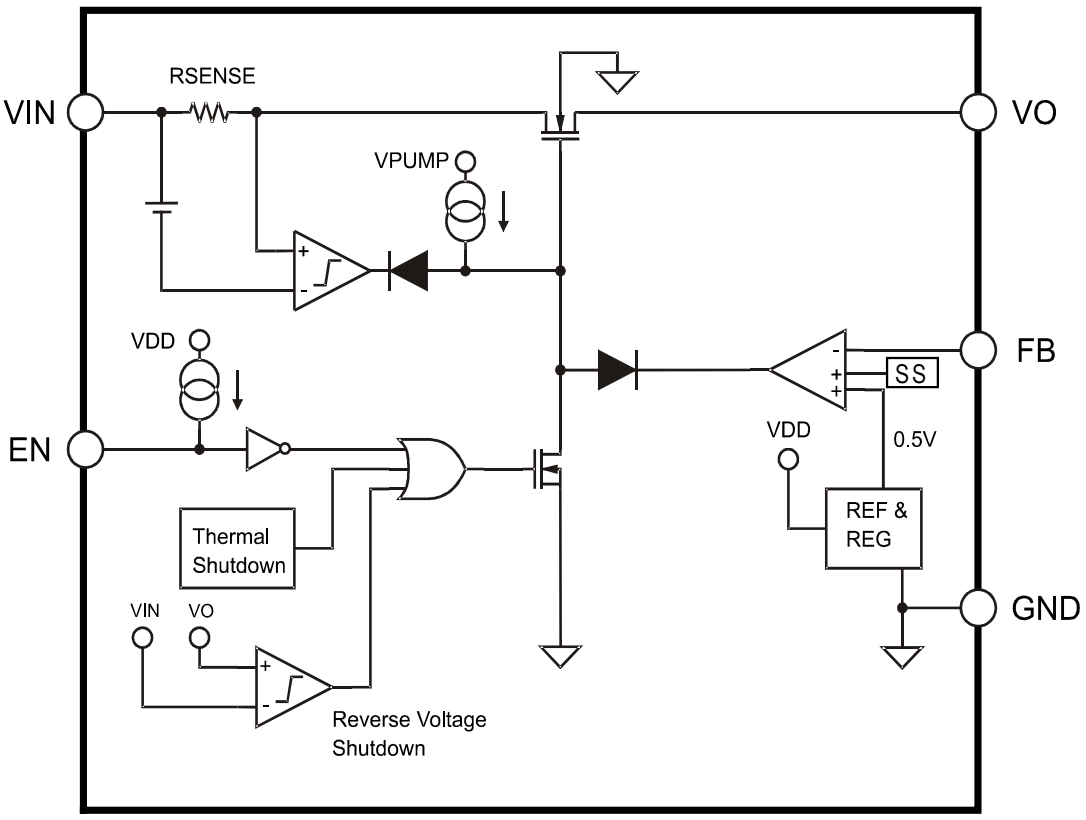
V_{IN} = 5.0V, V_{OUT} = 3.3V



Pin Descriptions

Pin #	Pin Name	Pin Function
2	EN	Enable input. Driving this pin high turns on the regulator. Driving this pin low shuts off the regulator. If not driven from a control circuit, tie this pin to the VIN pin.
3	VIN	Input supply pin. A large bulk capacitance should be placed close to this pin to ensure that the input supply does not sag below the minimum V_{IN}. Also a minimum of 4.7uF ceramic capacitor should be placed directly at this pin.
6	VO	Regulator output pin. Refer to the Applications Information section for output capacitor selection.
7	FB	Inverting input of the error amplifier. This pin is used to set the output voltage (See typical Application Circuits on page 1).
8	GND	Ground pin.
1, 4, 5	NC	No connection.
	THERMAL PAD	The exposed pad enhances thermal performance and is not electrically connected to GND inside the package. It is recommended to connect the exposed pad to the ground plane.

Block Diagram



Applications Information

Introduction

The SC4215J is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little PCB area. Additional features include an enable pin to allow for a very low power consumption in standby mode, and a fully adjustable output.

Noise Immunity

In very electrically noisy environments, it is recommended that 0.1µF ceramic capacitors be placed from VIN to GND and VO to GND as close to the device pins as possible.

V_O Setting: V_O=V_{REF}

By connecting the FB pin directly to the VO pin, the output voltage will be regulated to the 0.5V internal reference.

V_O Setting with External Resistors

The use of 1% resistors, and designing for a current flow ≥ 10µA is recommended to ensure a well regulated output (thus R_2 ≤50kΩ). A suitable value for R_2 can be chosen in the range of 1kΩ to 50kΩ. R_1 can then be calculated from.

$$R_1 = R_2 \cdot \frac{(V_O - V_{REF})}{V_{REF}}$$

Enable

Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Driving this pin high enables the regulator. A pull up resistor up to 400kOhms should be connected from this pin to the VIN pin in applications where the Enable pin is not driven from a control circuit.

Input Capacitor

A large bulk capacitance ≥ 10µF/A (output load) should be placed close to the input supply pin of the SC4215J to ensure that V_{IN} does not drop below the minimum V_{IN}. Also a minimum of 4.7µF ceramic capacitor is recommended to be placed directly next to the VIN pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, the input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.

Output Capacitor

A minimum bulk capacitance of 10µF/A (output load), along with a 0.1µF ceramic decoupling capacitor is recommended. For V_O less than 0.6V, a minimum bulk capacitance of 40µF, along with a 0.1µF ceramic decoupling capacitor is recommended. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC4215J is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Soft-Start

The soft-start is achieved by using a voltage ramp as the voltage reference for the internal error amplifier during startup. This voltage ramp is created by an internal current source charging an internal soft-start capacitor. When the voltage ramp reaches 500mV, the voltage reference for the internal error amplifier switches to the fixed 500mV V_{REF}. Thus, during soft-start, the output tracks the internal voltage ramp, which limits the input inrush current and provides a programmed soft-start profile for a wide range of applications.

Over-Current and Thermal Shutdown

The over-current protection and thermal shutdown functions protect the regulator against damage due to excessive power dissipation. The SC4215J is designed to current limit when the output current reashes 3A (typical). When the load exceeds 3A, the output voltage is reduced to maintain a constant current limit.
The thermal shutdown function limits the junction temperature to a maximum of 160°C (typical). Thermal shutdown turns off the regulator as the junction temperature begins to exceed 160°C. When the junction temperature

Applications Information (Cont.)

drops below 150°C (typical), the regulator is turned on again.

Thermal Considerations

The power dissipation in the SC4215J is given by the following equation:

$$P_D \approx I_O(V_{IN} - V_O)$$

The allowable power dissipation will be dependant upon the thermal impedance achieved in the application. The derating curve below is valid for the thermal impedance specified in the Thermal Information section on page 3.

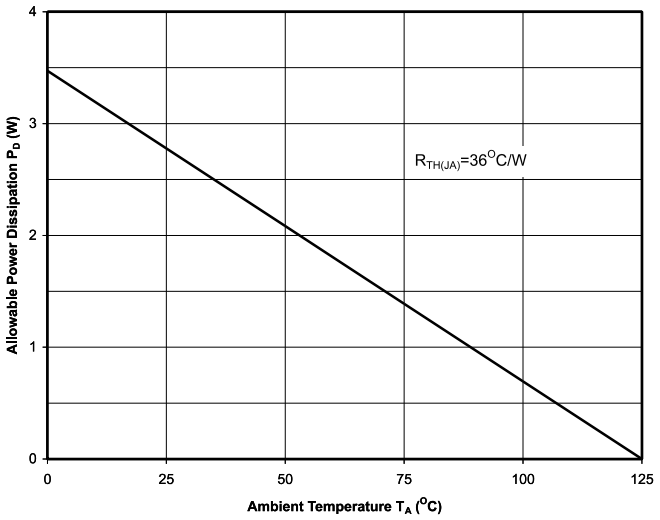
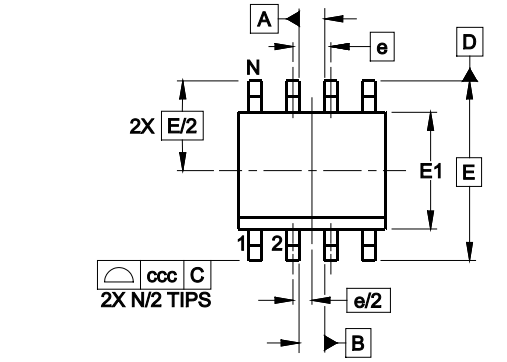
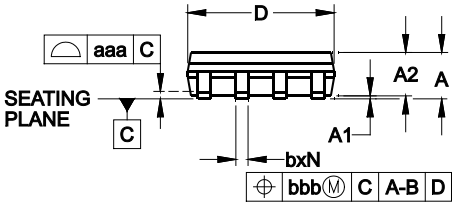


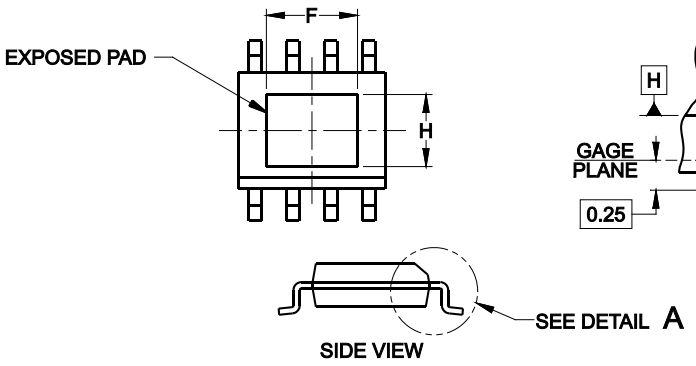
Figure 1. Power Derating Curve

Outline Drawing — SOIC-8-EDP-2





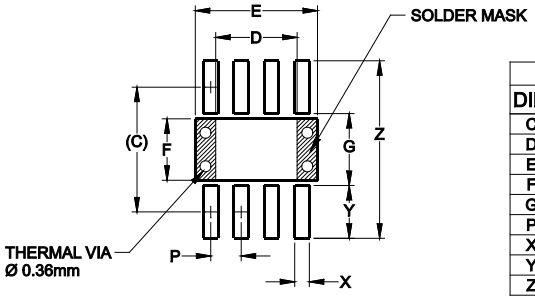
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.116	.120	.130	2.95	3.05	3.30
H	.085	.095	.099	2.15	2.41	2.51
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION BA.

Land Pattern — SOIC-8-EDP-2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

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www.semtech.com

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