THE DATASHEET OF

LP38851MRX-ADJ/NOPB

www.win-source.net 0086-755-83957316

LP38851 800 mA Fast-Response High-Accuracy Adjustable LDO Linear Regulator with Enable and Soft-Start

Check for Samples: LP38851

FEATURES

- **Adjustable V_{OUT} Range of 0.80V to 1.8V**
- **Wide V_{BIAS} Supply Operating Range of 3.0V to 5.5V**
- **Stable with 10µF Ceramic Capacitors**
- **Dropout Voltage of 115 mV (Typical) at 800 mA Load Current**
- **Precision V_{ADJ} across All Line and Load Conditions:**
  - **±1.5% V_{ADJ} for T_J = 25°C**
  - **±2.0% V_{ADJ} for 0°C ≤ T_J ≤ +125°C**
  - **±3.0% V_{ADJ} for -40°C ≤ T_J ≤ +125°C**
- **Over-Temperature and Over-Current Protection**
- **Available in 8-Lead SO PowerPad, 7-Lead SFM and 7-Lead PFM Packages**
- **−40°C to +125°C Operating Junction Temperature Range**

APPLICATIONS

- **ASIC Power Supplies in:**
  - **Desktops, Notebooks, and Graphics Cards, Servers**
  - **Gaming Set Top Boxes, Printers and Copiers**
- **Server Core and I/O Supplies**
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulator**

DESCRIPTION

The LP38851-ADJ is a high current, fast response regulator which can maintain output voltage regulation with extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides voltage to drive the gate of the N-MOS power transistor, while V_{IN} is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The part is available in PSOP 8–pin, SFM 7–pin, and TO-263 7-pin packages.

- **Dropout Voltage:** 115 mV (typical) at 800 mA load current
- **Low Ground Pin Current:** 10 mA (typical) at 800 mA load current
- **Soft-Start:** Programmable Soft-Start time
- **Precision ADJ Voltage:** ±1.5% for T_J = 25°C, and ±2.0% for 0°C ≤ T_J ≤ +125°C, across all line and load conditions

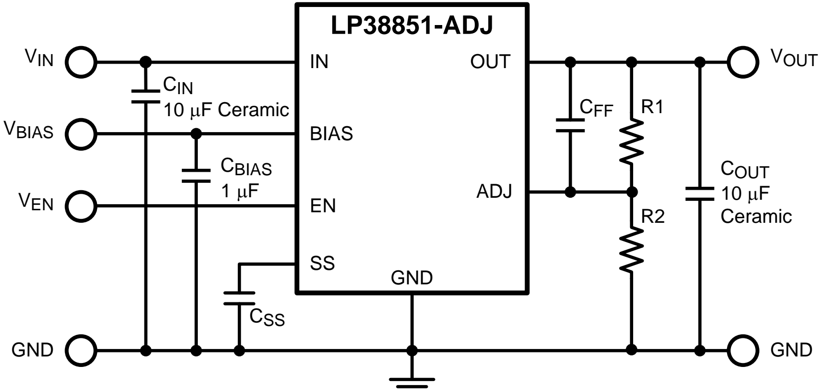
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2007–2013, Texas Instruments Incorporated

TYPICAL APPLICATION CIRCUIT



Connection Diagram

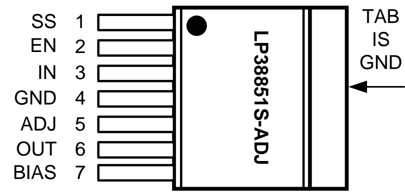


Figure 1. 7-Lead PFM - Top View
See KTW0007B Package

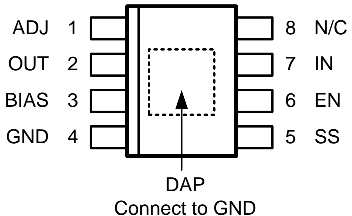


Figure 3. 8-Lead SO PowerPad - Top View
See DDA Package

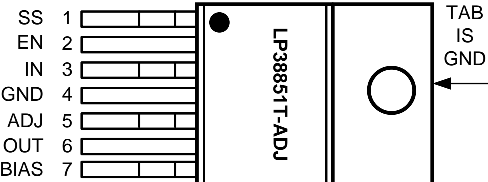


Figure 2. 7-Lead SFM - Top View
See NDZ0007B Package

PIN DESCRIPTIONS

SFM Pin #	PFM Pin #	SO PowerPad Pin #	Pin Symbol	Pin Description
1	1	5	SS	Soft-Start capacitor connection. Used to control the rise time of V_{OUT} at turn-on.
2	2	6	EN	Device Enable, High = On, Low = Off.
3	3	7	IN	The unregulated voltage input
4	4	4	GND	Ground
5	5	1	ADJ	The feedback connection to set the output voltage
6	6	2	OUT	The regulated output voltage
7	7	3	BIAS	The supply for the internal control and reference circuitry.
-	-	8	N/C	No internal connection
TAB	TAB	-	TAB	The SFM and PFM TAB is a thermal and electrical connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See APPLICATION INFORMATION for details.

 Copyright © 2007–2013, Texas Instruments Incorporated

PIN DESCRIPTIONS (continued)

SFM Pin #	PFM Pin #	SO PowerPad Pin #	Pin Symbol	Pin Description
-	-	DAP	DAP	The SO PowerPad DAP is a thermal connection only that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See APPLICATION INFORMATION for details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature Range		−65°C to +150°C
Lead Temperature	Soldering, 5 seconds	260°C
ESD Rating	Human Body Model (2)	±2 kV
Power Dissipation (3)		Internally Limited
V_{IN} Supply Voltage (Survival)		−0.3V to +6.0V
V_{BIAS} Supply Voltage (Survival)		−0.3V to +6.0V
V_{SS} SoftStart Voltage (Survival)		−0.3V to +6.0V
V_{OUT} Voltage (Survival)		−0.3V to +6.0V
I_{OUT} Current (Survival)		Internally Limited
Junction Temperature		−40°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specifications and conditions, see the Electrical Characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114.
(3) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance (θ_{JA}). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See APPLICATION INFORMATION for details.

OPERATING RATINGS (1)

V_{IN} Supply Voltage		(V_{OUT} + V_{DO}) to V_{BIAS}
V_{BIAS} Supply Voltage	$0.8V \leq V_{OUT} \leq 1.2V$	3.0V to 5.5V
	$1.2V < V_{OUT} \leq 1.8V$	4.5V to 5.5V
V_{EN} Voltage		0.0V to V_{BIAS}
I_{OUT}		0 mA to 800 mA
Junction Temperature Range (2)		−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specifications and conditions, see the Electrical Characteristics.
(2) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance (θ_{JA}). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See APPLICATION INFORMATION for details.

Copyright © 2007–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{OUT} = 0.80V, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, V_{EN} = V_{BIAS}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = open. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADJ}	V_{ADJ} Accuracy	$V_{OUT(NOM)}+1V \le V_{IN} \le V_{BIAS} \le 4.5V$ (1) $3.0V \le V_{BIAS} \le 5.5V$, $10 mA \le I_{OUT} \le 800 mA$	492.5 **485.0**	500.	507.5 **515.0**	mV
		$V_{OUT(NOM)}+1V \le V_{IN} \le V_{BIAS} \le 4.5V$ (1) $3.0V \le V_{BIAS} \le 5.5V$, $10 mA \le I_{OUT} \le 800 mA$, $0°C \le T_J \le +125°C$	490.0	500.	510.0	
V_{OUT}	V_{OUT} Range	$3.0V \le V_{BIAS} \le 5.5V$	0.80		1.20	V
		$4.5V \le V_{BIAS} \le 5.5V$	0.80		1.80	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, V_{IN} (2)	$V_{OUT(NOM)}+1V \le V_{IN} \le V_{BIAS}$	-	0.04	-	%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line Regulation, V_{BIAS} (2)	$3.0V \le V_{BIAS} \le 5.5V$	-	0.10	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (3)	$10 mA \le I_{OUT} \le 800 mA$	-	0.2	-	%/A
V_{DO}	Dropout Voltage (4)	I_{OUT} = 800 mA	-	115	150 **200**	mV
$I_{GND(IN)}$	Quiescent Current Drawn from V_{IN} Supply	V_{OUT} = 0.80V V_{BIAS} = 3.0V $10 mA \le I_{OUT} \le 800 mA$	-	7.0	8.5 **9.0**	mA
		$V_{EN} \le 0.5V$		1	100 **300**	µA
$I_{GND(BIAS)}$	Quiescent Current Drawn from V_{BIAS} Supply	$10 mA \le I_{OUT} \le 800 mA$	-	3.0	3.8 **4.5**	mA
		$V_{EN} \le 0.5V$		100	170 **200**	µA
UVLO	Under-Voltage Lock-Out Threshold	V_{BIAS} rising until device is functional	2.20 **2.00**	2.45	2.70 **2.90**	V
$UVLO_{(HYS)}$	Under-Voltage Lock-Out Hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional	60 **50**	150	300 **350**	mV
I_{SC}	Output Short-Circuit Current	V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, V_{OUT} = 0.0V	-	2.3	-	A
Soft-Start						
r_{SS}	Soft-Start internal resistance		11.0	14.0	17.0	kΩ
t_{SS}	Soft-Start time $t_{SS} = C_{SS} \times r_{SS} \times 5$	C_{SS} = 10 nF	-	700	-	µs
Enable						
I_{EN}	ENABLE pin Current	V_{EN} = V_{BIAS}	-	0.01	-	µA
		V_{EN} = 0.0V, V_{BIAS} = 5.5V	-24 **-21**	-35	-43 **-50**	
$V_{EN(ON)}$	Enable Voltage Threshold	V_{EN} rising until Output = ON	1.00 **0.90**	1.25	1.50 **1.55**	V
$V_{EN(HYS)}$	Enable Voltage Hysteresis	V_{EN} falling from $V_{EN(ON)}$ until Output = OFF	50 **30**	100	150 **200**	mV
t_{OFF}	Turn-OFF Delay Time	$R_{LOAD} \times C_{OUT} << t_{OFF}$	-	20	-	µs
t_{ON}	Turn-ON Delay Time	$R_{LOAD} \times C_{OUT} << t_{ON}$	-	15	-	
AC Parameters						

(1) V_{IN} cannot exceed either V_{BIAS} or 4.5V, whichever value is lower.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(4) Dropout voltage is defined as the input to output voltage differential (V_{IN} - V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.

 Copyright © 2007–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified: V_{OUT} = 0.80V, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, V_{EN} = V_{BIAS}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = open. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	V_{IN} = $V_{OUT(NOM)}$ + 1V, f = 120 Hz	-	72	-	dB
		V_{IN} = $V_{OUT(NOM)}$ + 1V, f = 1 kHz	-	61	-	
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	V_{BIAS} = $V_{OUT(NOM)}$ + 3V, f = 120 Hz	-	54	-	
		V_{BIAS} = $V_{OUT(NOM)}$ + 3V, f = 1 kHz	-	53	-	
e_n	Output Noise Density	f = 120 Hz	-	1	-	µV/√Hz
	Output Noise Voltage	BW = 10 Hz − 100 kHz	-	150	-	$µV_{RMS}$
		BW = 300 Hz − 300 kHz	-	90	-	
Thermal Parameters						
T_{SD}	Thermal Shutdown Junction Temperature		-	160	-	°C
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis		-	10	-	
$θ_{J-A}$	Thermal Resistance, Junction to Ambient (5)	SFM	-	60	-	°C/W
		PFM	-	60	-	
		SO PowerPad	-	168	-	
$θ_{J-C}$	Thermal Resistance, Junction to Case (5) (6)	SFM	-	3	-	
		PFM	-	3	-	
		SO PowerPad	-	11	-	

(5) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance ($θ_{JA}$). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See APPLICATION INFORMATION for details.

(6) For SFM and PFM: $θ_{J-C}$ refers to the BOTTOM surface of the package, under the epoxy body, as the 'CASE'. For SO PowerPad: $θ_{J-C}$ refers to the DAP (aka: Exposed Pad) on BOTTOM surface of the package as the 'CASE'.

Copyright © 2007–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS

Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified: T_J = 25°C, R1 = 1.40 kΩ, R2 = 1.00 kΩ, C_{FF}= 180 pF, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = 10 µF Ceramic, C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, , C_{SS} = Open.

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}

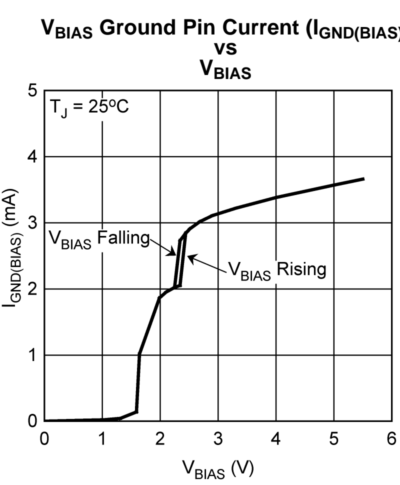


Figure 4.

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature

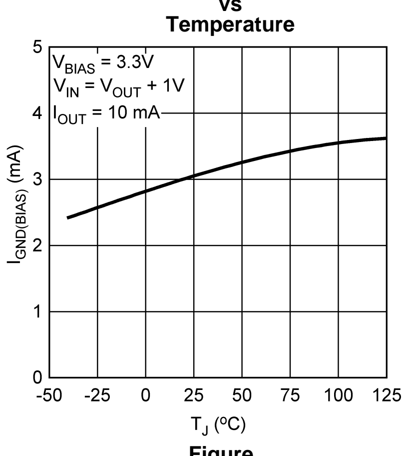


Figure .

V_{IN} Ground Pin Current vs Temperature

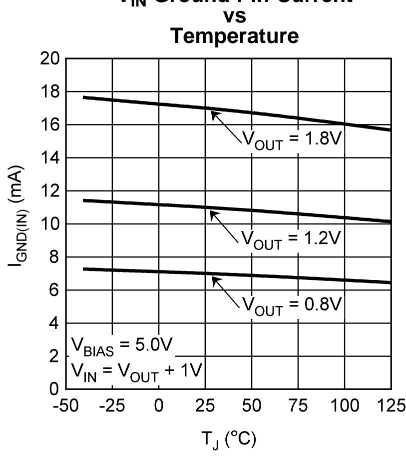


Figure 5.

Load Regulation vs Temperature

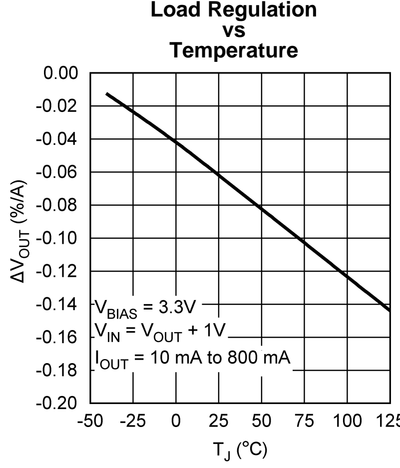


Figure 6.

Dropout Voltage (V_{DO}) vs Temperature

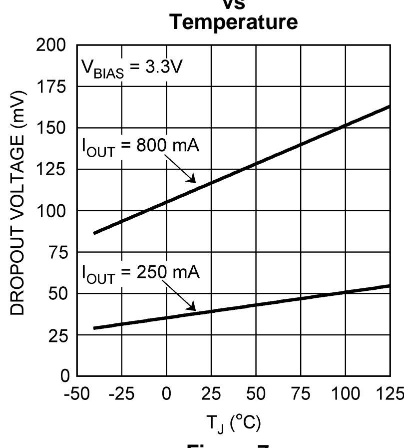


Figure 7.

Output Current Limit (I_{SC}) vs Temperature

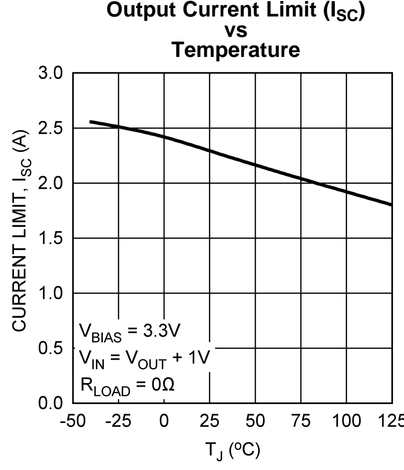


Figure 8.

Copyright © 2007–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified: T_J = 25°C, R1 = 1.40 kΩ, R2 = 1.00 kΩ, C_{FF}= 180 pF, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = 10 µF Ceramic, C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, , C_{SS} = Open.

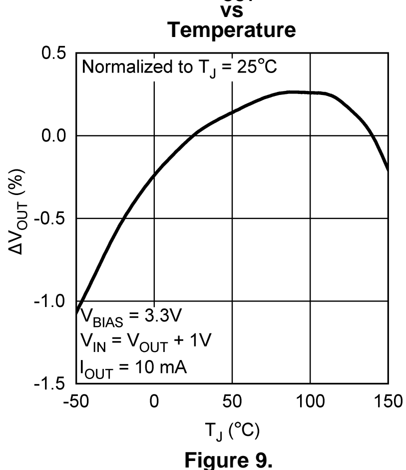


Figure 9.

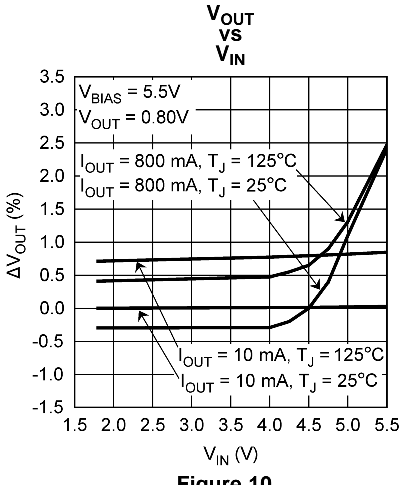


Figure 10.

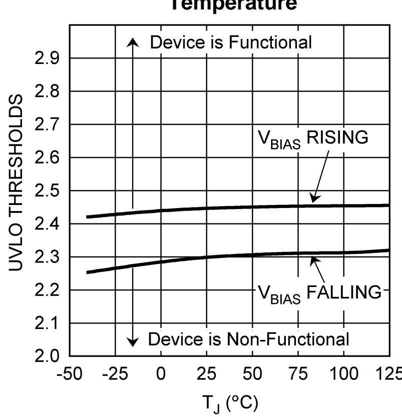


Figure 11.

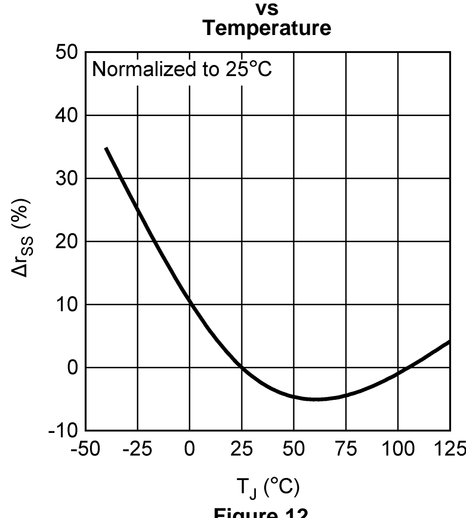


Figure 12.

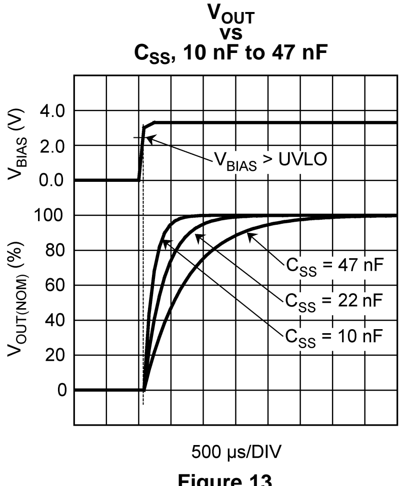


Figure 13.

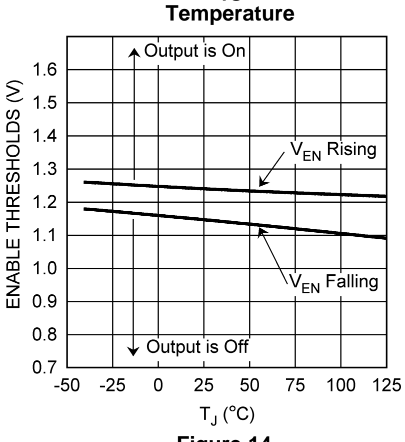


Figure 14.

Copyright © 2007–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified: T_J = 25°C, R1 = 1.40 kΩ, R2 = 1.00 kΩ, C_{FF}= 180 pF, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = 10 µF Ceramic, C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, , C_{SS} = Open.

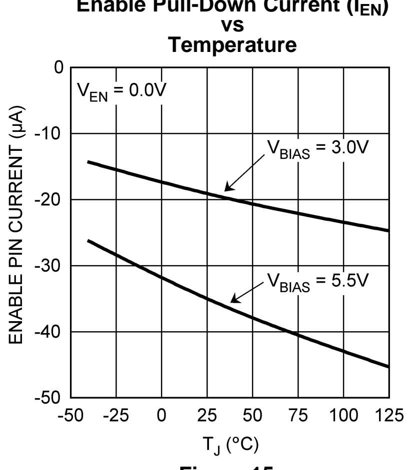


Figure 15.

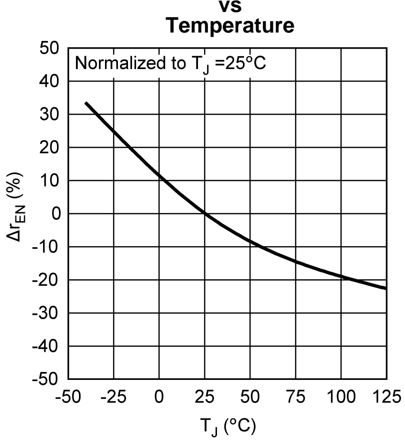


Figure 16.

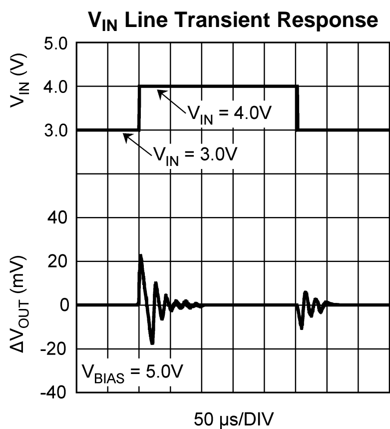


Figure 17.

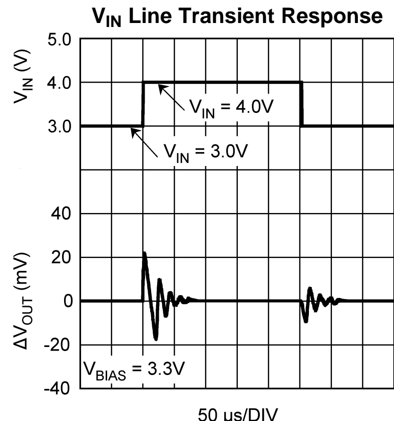


Figure 18.

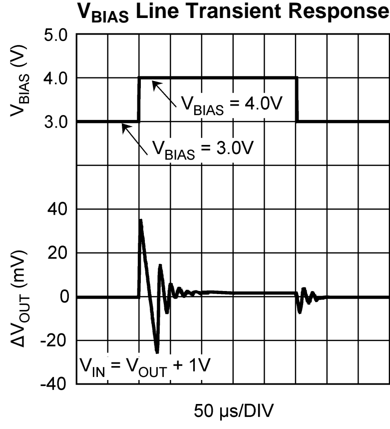


Figure 19.

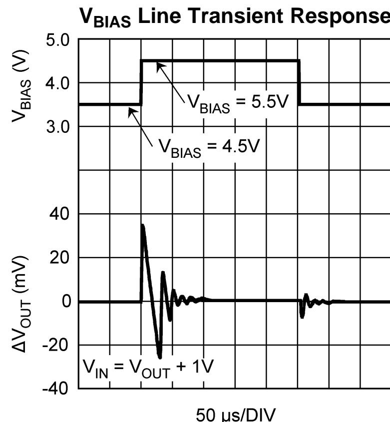


Figure 20.

 Copyright © 2007–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified: T_J = 25°C, R1 = 1.40 kΩ, R2 = 1.00 kΩ, C_{FF}= 180 pF, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = 10 µF Ceramic, C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, , C_{SS} = Open.

Load Transient Response, C_{OUT} = 10 µF Ceramic

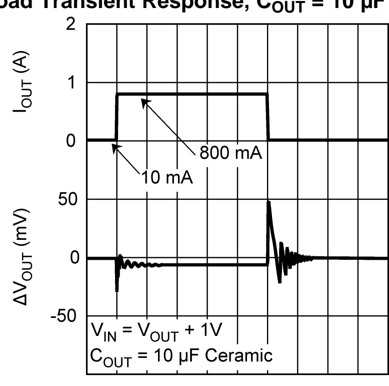


Figure 21.

Load Transient Response, C_{OUT} = 10 µF Ceramic

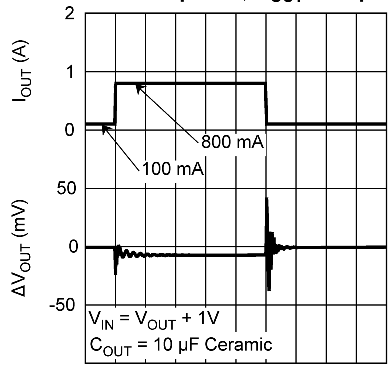


Figure 22.

Load Transient Response, C_{OUT} = 47 µF Ceramic

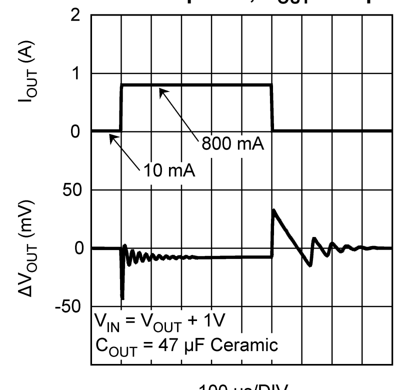


Figure 23.

Load Transient Response, C_{OUT} = 47 µF Ceramic

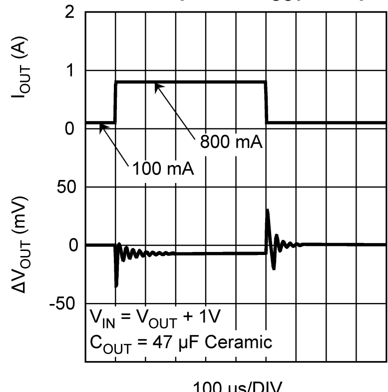


Figure 24.

Load Transient Response, C_{OUT} = 68 µF Tantalum

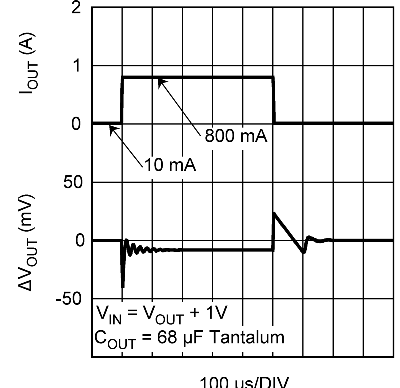


Figure 25.

Load Transient Response, C_{OUT} = 68 µF Tantalum

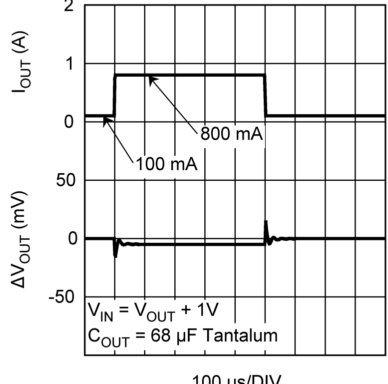


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified: T_J = 25°C, R1 = 1.40 kΩ, R2 = 1.00 kΩ, C_{FF}= 180 pF, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = 10 µF Ceramic, C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, , C_{SS} = Open.

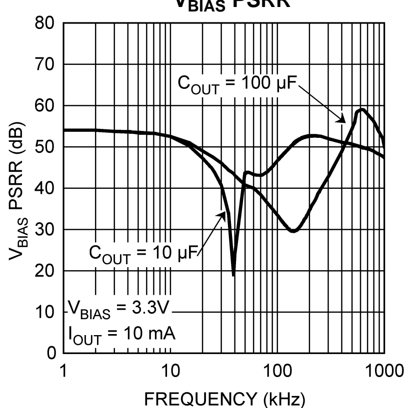


Figure 27.

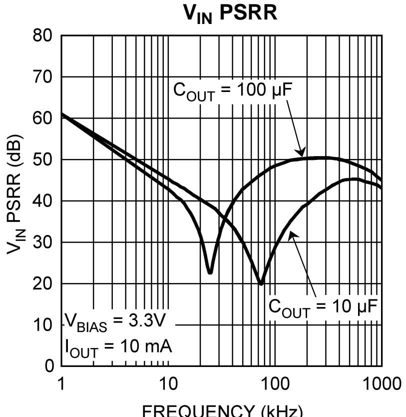


Figure 28.

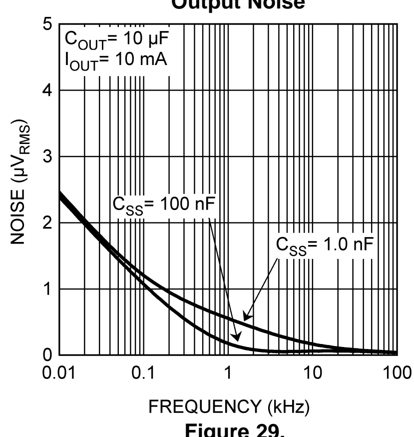


Figure 29.

Copyright © 2007–2013, Texas Instruments Incorporated

BLOCK DIAGRAM

LP38851-ADJ

IN
OUT
BIAS
Under-Voltage
Lock-Out
Thermal
Shut Down
r_{EN}
EN
Enable
1.2V
ADJ
r_{SS}
SS
V_{REF}
I_{LIMIT}
0.5V
GND

APPLICATION INFORMATION

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in TYPICAL APPLICATION CIRCUIT.

Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the IC and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 µF ceramic capacitor at the output will allow unlimited capacitance, Tantalum and/or Aluminum, to be added in parallel.

Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

Bias Capacitor

The capacitor on the bias pin must be at least 1 µF, and can be any good quality capacitor (ceramic is recommended).

Feed Forward Capacitor, C_{FF} (Refer to TYPICAL APPLICATION CIRCUIT)

When using a ceramic capacitor for C_{OUT}, the typical ESR value will be too small to provide any meaningful positive phase compensation, F_Z, to offset the internal negative phase shifts in the gain loop.

$$F_Z = 1 / (2 \times \pi \times C_{OUT} \times ESR) \quad (1)$$

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor, C_{FF}, in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (2)$$

For optimum load transient response select C_{FF} so the zero frequency, F_Z, falls between 500 kHz and 750 kHz.

$$C_{FF} = 1 / (2 \times \pi \times R1 \times F_Z) \quad (3)$$

The phase lead provided by C_{FF} diminishes as the DC gain approaches unity, or V_{OUT} approaches V_{ADJ}. This is because C_{FF} also forms a pole with a frequency of:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times (R1 \parallel R2)) \quad (4)$$

It's important to note that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero mover closer together. The phase lead provided from C_{FF} diminishes quickly as the output voltage is reduced, and has no effect when V_{OUT} = V_{ADJ}. For this reason, relying on this compensation technique alone is adequate only for higher output voltages. For the LP38851, the practical minimum V_{OUT} is 0.8V when a ceramic capacitor is used for C_{OUT}.

Copyright © 2007–2013, Texas Instruments Incorporated

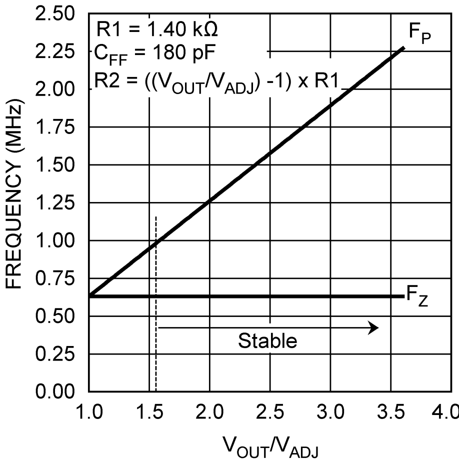


Figure 30. F_{ZERO} and F_{POLE} vs Gain

SETTING THE OUTPUT VOLTAGE (Refer to TYPICAL APPLICATION CIRCUIT)

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times \left(1 + \left(\frac{R1}{R2}\right)\right) \quad (5)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{ADJ} is specified, the use of low quality resistors for R1 and R2 can easily produce a V_{OUT} value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 10 kΩ. This is to prevent internal parasitic capacitances on the ADJ pin from interfering with the F_Z pole set by R1 and C_{FF}.

$$((R1 \times R2) / (R1 + R2)) \le 10\ k\Omega \quad (6)$$

Table 1 lists some suggested, best fit, standard ±1% resistor values for R1 and R2, and a standard ±10% capacitor values for C_{FF}, for a range of V_{OUT} values. Other values of R1, R2, and C_{FF} are available that will give similar results.

Table 1.

V_{OUT}	R1	R2	C_{FF}	F_Z
0.8V	1.07 kΩ	1.78 kΩ	220 pF	676 kHz
0.9V	1.50 kΩ	1.87 kΩ	180 pF	589 kHz
1.00V	1.00 kΩ	1.00 kΩ	270 pF	589 kHz
1.1V	1.65 kΩ	1.37 kΩ	150 pF	643 kHz
1.2V	1.40 kΩ	1.00 kΩ	180 pF	631 kHz
1.3V	1.15 kΩ	715 Ω	220 pF	629 kHz
1.4V	1.07 kΩ	590 Ω	220 pF	676 kHz
1.5V	2.00 kΩ	1.00 kΩ	120pF	663 kHz
1.6V	1.65 kΩ	750 Ω	150 pF	643 kHz
1.7V	2.55 kΩ	1.07 kΩ	100 pF	624 kHz
1.8V	2.94 kΩ	1.13 kΩ	82 pF	660 kHz

Copyright © 2007–2013, Texas Instruments Incorporated

Please refer to Application Note AN-1378 (SNVA112) for additional information on how resistor tolerances affect the calculated V_{OUT} value.

INPUT VOLTAGE

The input voltage (V_{IN}) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least V_{OUT} + V_{DO}, and no higher than whatever value is used for V_{BIAS}.

For applications where V_{BIAS} is higher than 4.5V, V_{IN} must be no greater than 4.5V, otherwise output voltage accuracy may be affected.

BIAS VOLTAGE

The bias voltage (V_{BIAS}) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. When V_{OUT} is set to 1.20V, or less, V_{BIAS} may be anywhere in the operating range of 3.0V to 5.5V. If V_{OUT} is set higher than 1.20V , V_{BIAS} must be between 4.5V and 5.5V to ensure proper operation of the device.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the Under-Voltage Lock-Out (UVLO) threshold of approximately 2.45V.

As the bias voltage rises above the UVLO threshold the device control circuitry becomes active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the Minimum Operating Rating value of 3.0V the device will be functional, but the operating parameters will not be within the specified limits.

SUPPLY SEQUENCING

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed.

One practical limitation is that the Soft-Start circuit starts charging C_{SS} when both V_{BIAS} rises above the UVLO threshold and the Enable pin is above the $V_{EN(ON)}$ threshold. If the application of V_{IN} is delayed beyond this point the benefits of Soft-Start will be compromised.

In any case, the output voltage cannot be specified until both V_{IN} and V_{BIAS} are within the range of specified operating values.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this diode clamp.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold, or when the Enable pin is held low.

When V_{BIAS} is above the UVLO threshold, and the Enable pin is above the $V_{EN(ON)}$ threshold, the control circuitry is active and will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin , limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided.

Copyright © 2007–2013, Texas Instruments Incorporated

SOFT-START

The LP38851 incorporates a Soft-Start function that reduces the start-up current surge into the output capacitor (C_{OUT}) by allowing V_{OUT} to rise slowly to the final value. This is accomplished by controlling V_{REF} at the SS pin. The soft-start timing capacitor (C_{SS}) is internally held to ground until both V_{BIAS} rises above the Under-Voltage Lock-Out threshold (ULVO) and the Enable pin is higher than the $V_{EN(ON)}$ threshold.

V_{REF} will rise at an RC rate defined by the internal resistance of the SS pin (r_{SS}), and the external capacitor connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

$$\text{Soft-Start Time} = C_{SS} \times r_{SS} \times 5 \quad (7)$$

Since the V_{OUT} rise will be exponential, not linear, the in-rush current will peak during the first time constant (τ), and V_{OUT} will require four additional time constants (4τ) to reach the final value (5τ) .

After achieving normal operation, should either V_{BIAS} fall below the ULVO threshold, or the Enable pin fall below the $V_{EN(OFF)}$ threshold, the device output will be disabled and the Soft-Start capacitor (C_{SS}) discharge circuit will become active. The C_{SS} discharge circuit will remain active until V_{BIAS} falls to 500 mV (typical). When V_{BIAS} falls below 500 mV (typical), the C_{SS} discharge circuit will cease to function due to a lack of sufficient biasing to the control circuitry.

Since V_{REF} appears on the SS pin, any leakage through C_{SS} will cause V_{REF} to fall, and thus affect V_{OUT}. A leakage of 50 nA (about 10 MΩ) through C_{SS} will cause V_{OUT} to be approximately 0.1% lower than nominal, while a leakage of 500 nA (about 1 MΩ) will cause V_{OUT} to be approximately 1% lower than nominal. Typical ceramic capacitors will have a factor of 10X difference in leakage between 25°C and 85°C, so the maximum ambient temperature must be included in the capacitor selection process.

Typical C_{SS} values will be in the range of 1 nF to 100 nF, providing typical Soft-Start times in the range of 70 µs to 7 ms (5τ). Values less than 1 nF can be used, but the Soft-Start effect will be minimal. Values larger than 100 nF will provide soft-start, but may not be fully discharged if V_{BIAS} falls from the UVLVO threshold to less than 500 mV in less than 100 µs.

Figure 31 shows the relationship between the C_{OUT} value and a typical C_{SS} value.

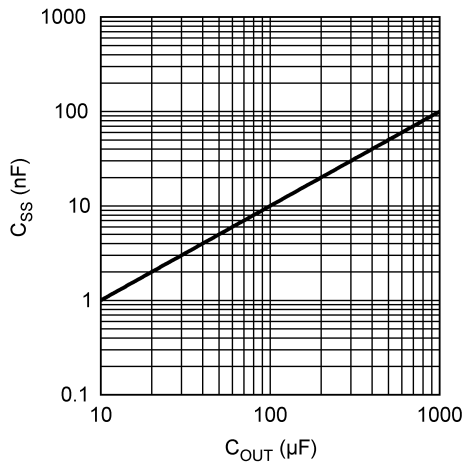


Figure 31. Typical C_{SS} vs C_{OUT} Values

The C_{SS} capacitor must be connected to a clean ground path back to the device ground pin. No components, other than C_{SS}, should be connected to the SS pin, as there could be adverse effects to V_{OUT}.

If the Soft-Start function is not needed the SS pin should be left open, although some minimal capacitance value is always recommended.

Copyright © 2007–2013, Texas Instruments Incorporated

ENABLE OPERATION

The Enable pin (EN) provides a mechanism to enable, or disable, the regulator output stage. The Enable pin has an internal pull-up, through a typical 160 kΩ resistor, to V_{BIAS}.

If the Enable pin is actively driven, pulling the Enable pin above the V_{EN} threshold of 1.25V (typical) will turn the regulator output on, while pulling the Enable pin below the V_{EN} threshold will turn the regulator output off. There is approximately 100 mV of hysteresis built into the Enable threshold provide noise immunity.

If the Enable function is not needed this pin should be left open, or connected directly to V_{BIAS}. If the Enable pin is left open, stray capacitance on this pin must be minimized, otherwise the output turn-on will be delayed while the stray capacitance is charged through the internal resistance (r_{EN}).

POWER DISSIPATION AND HEAT-SINKING

Additional copper area for heat-sinking may be required depending on the maximum device dissipation (P_D) and the maximum anticipated ambient temperature (T_A) for the device. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (8)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)}$$

where

- $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS} (9)

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)}$$

where

- $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN} (10)

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (11)$$

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature (T_A) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$) .

$$\Delta_J = T_{J(MAX)} - T_{A(MAX)} \quad (12)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} \leq \frac{\Delta T_J}{P_D} \quad (13)$$

Heat-Sinking The SFM Package

The SFM package has a θ_{JA} rating of 60°C/W and a θ_{JC} rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow. If the needed θ_{JA}, as calculated above, is greater than or equal to 60°C/W then no additional heat-sinking is required since the package can safely dissipate the heat and not exceed the operating $T_{J(MAX)}$. If the needed θ_{JA} is less than 60°C/W then additional heat-sinking is needed.

The thermal resistance of a SFM package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for PFM package.

The heat-sink to be used in the application should have a heat-sink to ambient thermal resistance, θ_{HA}:

$$\theta_{HA} \leq \theta_{JA} - (\theta_{CH} + \theta_{JC})$$

Copyright © 2007–2013, Texas Instruments Incorporated

$$\theta_{HA} \leq \theta_{JA} - (\theta_{CH} + \theta_{JC})$$

where

- θ_{JA} is the required total thermal resistance from the junction to the ambient air, θ_{CH} is the thermal resistance from the case to the surface of the heart-sink
- θ_{JC} is the thermal resistance from the junction to the surface of the case (14)

For this equation, θ_{JC} is about 3°C/W for a SFM package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. Consult the heat-sink manufacturer datasheet for details and recommendations.

Heat-Sinking The PFM Package

The PFM package has a θ_{JA} rating of 60°C/W, and a θ_{JC} rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The PFM package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat sinking. Figure 32 shows a curve for the θ_{JA} of PFM package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat-sinking.

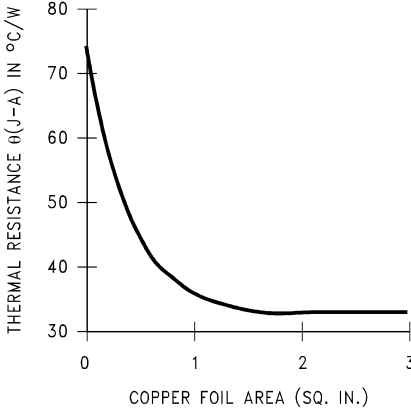


Figure 32. θ_{JA} vs Copper (1 Ounce) Area for the PFM package

Figure 32 shows that increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the PFM package mounted to a PCB is 32°C/W.

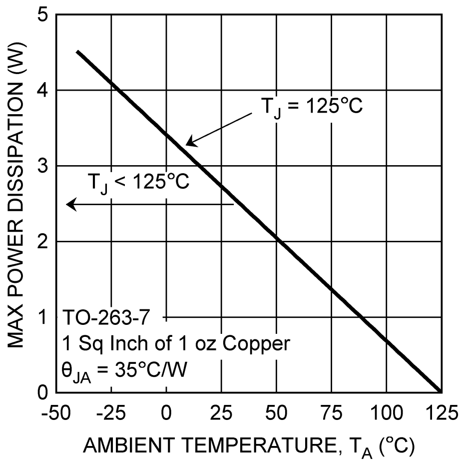


Figure 33. Maximum Power Dissipation vs Ambient Temperature for the PFM Package

Figure 33 shows the maximum allowable power dissipation for PFM packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

Heat-Sinking The SO PowerPad Package

The LP38851MR package has a $θ_{JA}$ rating of 168°C/W, and a $θ_{JC}$ rating of 11°C/W. The $θ_{JA}$ rating of 168°C/W includes the device DAP soldered to an area of 0.008 square inches (0.09 in x 0.09 in) of 1 ounce copper, with no airflow.

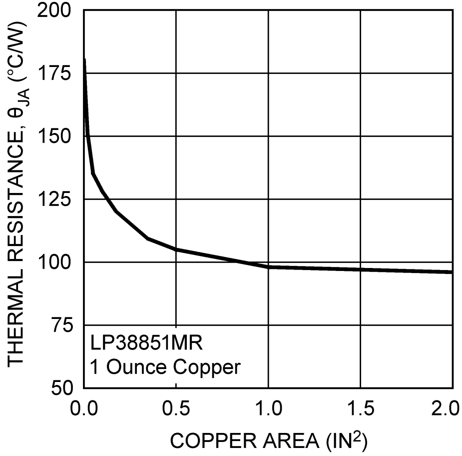


Figure 34. $θ_{JA}$ vs Copper (1 Ounce) Area for the SO PowerPad Package

Increasing the copper area soldered to the DAP to 1 square inch of 1 ounce copper, using a dog-bone type layout, will improve the $θ_{JA}$ rating to 98°C/W. Figure 34 shows that increasing the copper area beyond 1 square inch produces very little improvement.

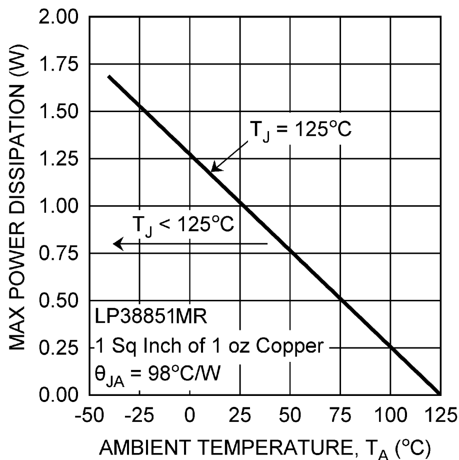


Figure 35. Maximum Power Dissipation vs Ambient Temperature for the SO PowerPad Package

Figure 35 shows the maximum allowable power dissipation for the SO PowerPad package for a range of ambient temperatures, assuming $θ_{JA}$ is 98°C/W and the maximum junction temperature is 125°C.

Copyright © 2007–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38851MR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L38851 MRADJ	Samples
LP38851MRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L38851 MRADJ	Samples
LP38851S-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTW	7	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP38851S -ADJ	Samples
LP38851SX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTW	7	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP38851S -ADJ	Samples
LP38851T-ADJ/NOPB	ACTIVE	TO-220	NDZ	7	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP38851T -ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

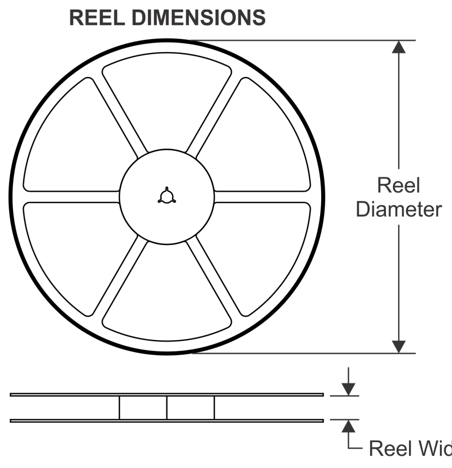
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

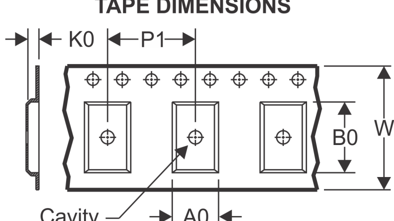
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

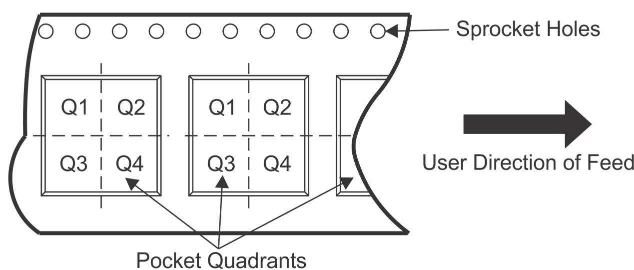


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

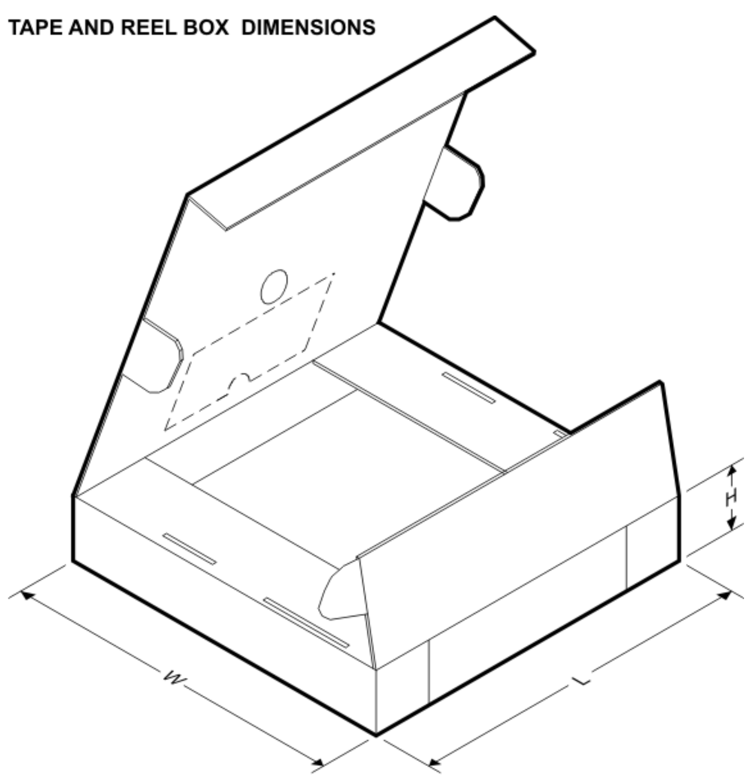
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38851MRX-ADJ/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP38851SX-ADJ/NOPB	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38851MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP38851SX-ADJ/NOPB	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0

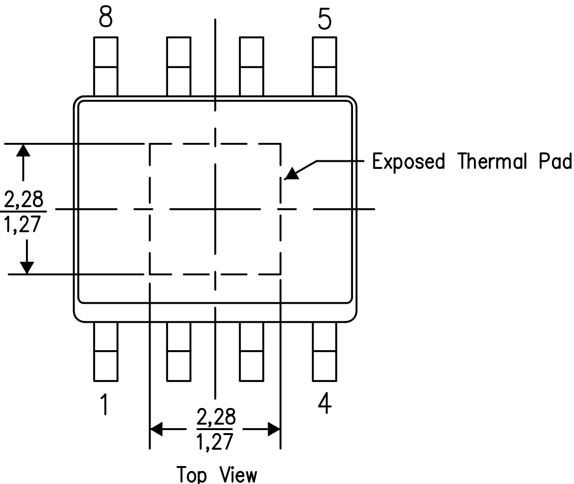
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

0,127mm Thick Stencil Design Example
Reference table below for other
solder stencil thicknesses
(Note E)

4x1,5
1,27
solder mask
over copper
6xø0,33
2,28
2,94
5,75
3x1,5
2,28
4,89
Example Solder Mask
Defined Pad
(See Note C, D)
Non Solder Mask Defined Pad
Example Solder Mask Opening
(Note F)
0,5
2,2
Pad Geometry
(Note C)
0,07
All Around

0,45
1,27
2,15
2,28
Y
2,28
X
5,75

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

4208951-2/D 04/12

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

LAND PATTERN EXAMPLE
SCALE:10X

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

(2.34)
BASED ON
0.125 THICK
STENCIL

8X (1.55)

1

(R0.05) TYP

8

8X (0.6)

SYMM
℄

(2.34)
BASED ON
0.125 THICK
STENCIL

6X (1.27)

4

5

METAL COVERED
BY SOLDER MASK

SYMM
℄

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

(5.4)

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

NDZ0007B

.108 ±.005
[2.74 ±0.12]

6X .050 ±.010
[1.27 ±0.25]

7

.400 +.010 -.005
[10.16 +0.25 -0.12]

7X .030 ±.005
[0.76 ±0.12]

1

∅ .151 ±.002
[3.84 ±0.05]

.342 ±.010
[8.69 ±0.25]

PIN 1 ID

R.040 TYP
[1.02]

7X .015 +.007 -.001
[0.38 +0.17 -0.02]

.248 ±.010
[6.3 ±0.25]

7°

7°

4X .200 ±.010
[5.08 ±0.25]

.180 ±.005
[4.57 ±0.12]

.050 ±.002
[1.27 ±0.05]

TAPER SIDES 1°

3X .113 +.010 -.015
[2.86 +0.25 -0.38]

0°-6°

4X .555 ±.010
[14.1 ±0.25]

4X .700 ±.010
[17.78 ±0.25]

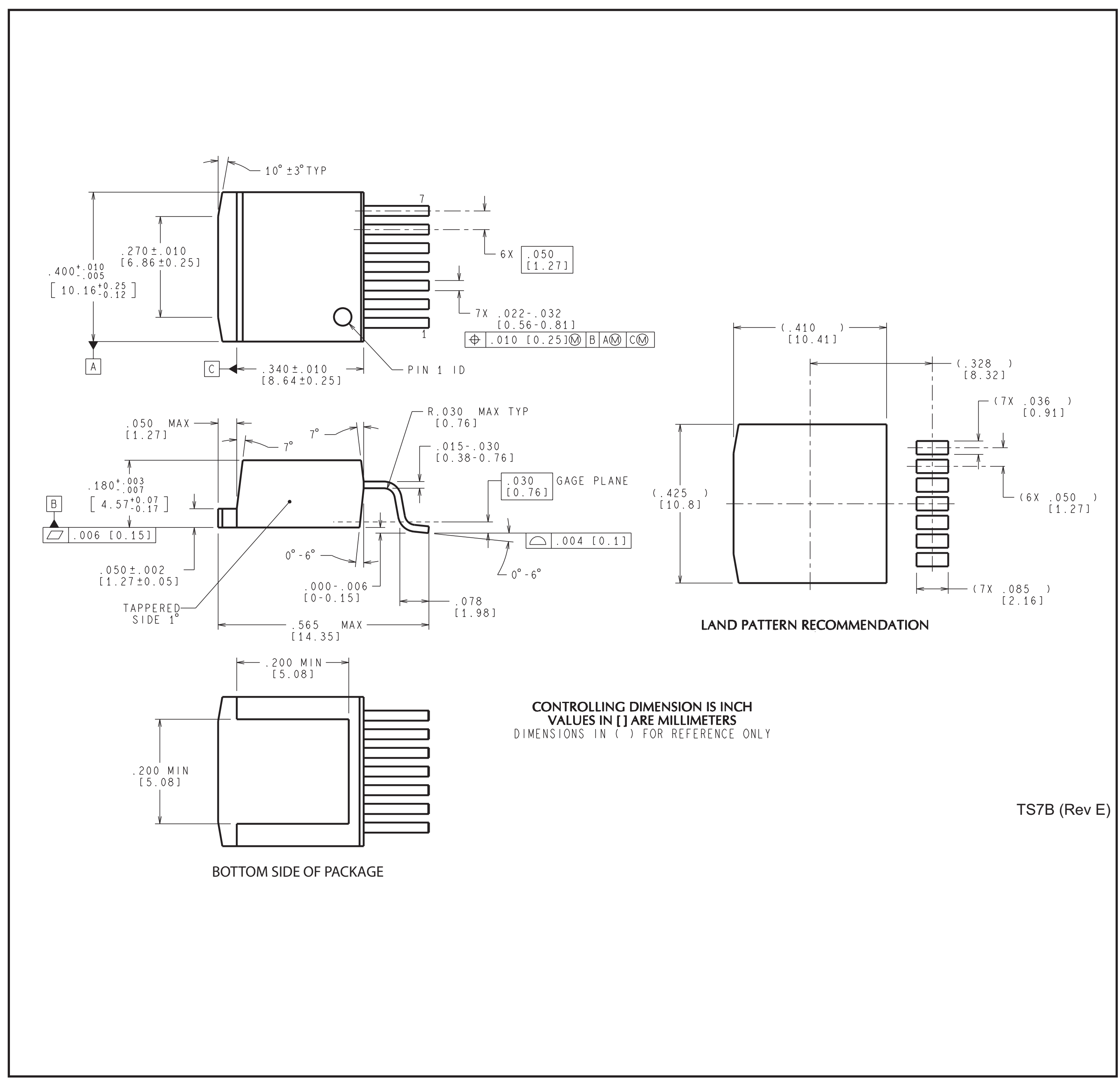
4X .850 ±.010
[21.59 ±0.25]

3X .856 ±.010
[21.74 ±0.25]

TA07B (Rev E)

CONTROLING DIMENSIONS IS INCH
VALUES IN [ ] ARE MILLIMETERS

KTW0007B



TS7B (Rev E)

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LP38851MRX-ADJ/NOPB on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management