

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC245F, TC74VHC245FK

## Octal Bus Transceiver

The TC74VHC245 is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ( $\overline{G}$ ) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

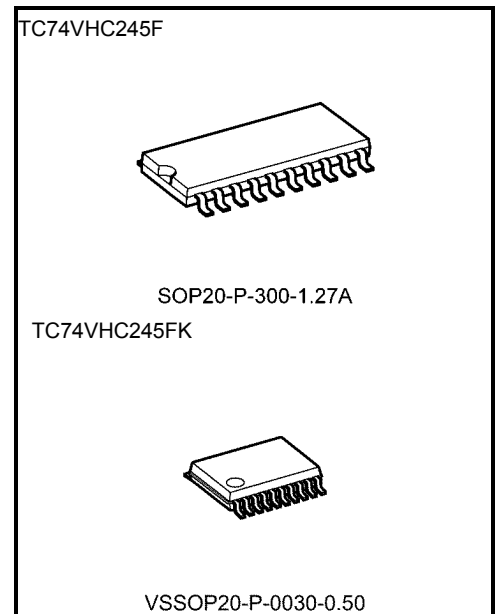
### Features (Note 1) (Note 2) (Note 3)

- High speed:  $t_{pd} = 4.0 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \text{ }\mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC (opr)} = 2 \text{ V to } 5.5 \text{ V}$
- Low noise:  $V_{OLP} = 1.0 \text{ V (max)}$
- Pin and function compatible with 74ALS245

Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Note 3: A parasitic diode is formed between the bus and VCC terminals. Therefore bus terminal can not be used to interface 5 V to 3 V systems directly.

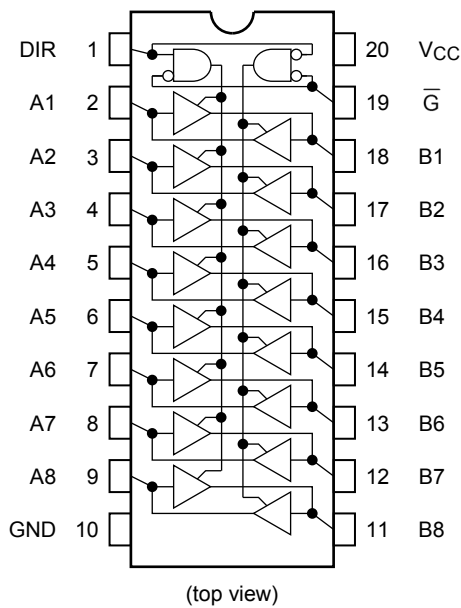


Weight

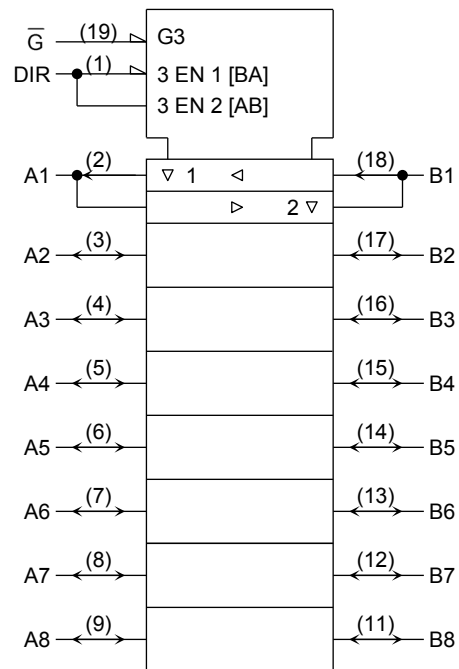
SOP20-P-300-1.27A	: 0.22 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Start of commercial production  
1991-05

### Pin Assignment



### IEC Logic Symbol



### Truth Table

Inputs		Function		Output
$\overline{G}$	DIR	A Bus	B Bus	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don't care

Z: High impedance

### Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage (DIR, $\overline{G}$ )	$V_{IN}$	-0.5 to 7.0	V
DC bus I/O voltage	$V_{I/O}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0 to 5.5	V
Input voltage (DIR, $\overline{G}$ )	V <sub>IN</sub>	0 to 5.5	V
Bus I/O voltage	V <sub>I/O</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V <sub>CC</sub> = 3.3 ± 0.3 V) 0 to 20 (V <sub>CC</sub> = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V<sub>CC</sub> or GND. Please connect both bus inputs and the bus outputs with V<sub>CC</sub> or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

### Electrical Characteristics

#### DC Characteristics

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit											
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max										
High-level input voltage	V <sub>IH</sub>	—	2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V										
Low-level input voltage	V <sub>IL</sub>	—	2.0 3.0 to 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V										
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V									
				3.0	2.9	3.0	—	2.9	—										
				4.5	4.4	4.5	—	4.4	—										
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	—	0.1	V									
				3.0	—	0.0	0.1	—	0.1										
				4.5	—	0.0	0.1	—	0.1										
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	μA										
										Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation delay time	$t_{pLH}$	—	$3.3 \pm 0.3$	15	—	5.8	8.4	1.0	10.0	ns
				50	—	8.3	11.9	1.0	13.5	
	$5.0 \pm 0.5$		15	—	4.0	5.5	1.0	6.5		
			50	—	5.5	7.5	1.0	8.5		
3-state output enable time	$t_{pZL}$	$R_L = 1 \text{ k}\Omega$	$3.3 \pm 0.3$	15	—	8.5	13.2	1.0	15.5	ns
				50	—	11.0	16.7	1.0	19.0	
	$5.0 \pm 0.5$		15	—	5.8	8.5	1.0	10.0		
			50	—	7.3	10.6	1.0	12.0		
3-state output disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1 \text{ k}\Omega$	$3.3 \pm 0.3$	50	—	11.5	15.8	1.0	18.0	ns
			$5.0 \pm 0.5$	50	—	7.0	9.7	1.0	11.0	
Output to output skew	$t_{osLH}$ $t_{osHL}$	(Note 1)	$3.3 \pm 0.3$	50	—	—	1.5	—	1.5	ns
			$5.0 \pm 0.5$	50	—	—	1.0	—	1.0	
Input capacitance	$C_{IN}$	DIR, $\bar{G}$	—	—	—	4	10	—	10	pF
Bus input capacitance	$C_{I/O}$	An, Bn	—	—	—	8	—	—	—	pF
Power dissipation capacitance	CPD	(Note 2)	—	—	—	21	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

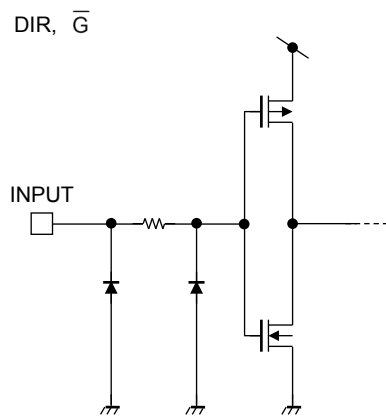
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

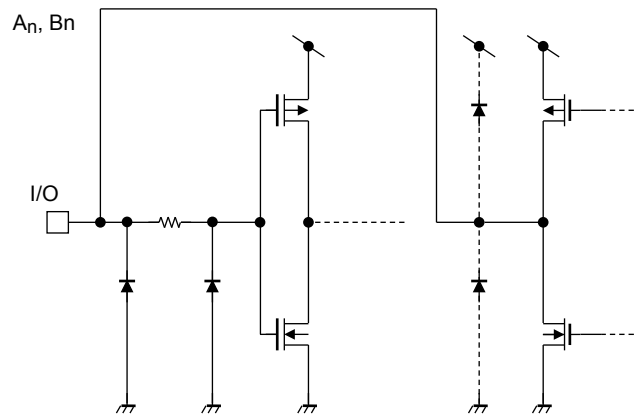
### Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$ ) (Note)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Max	
Quiet output maximum dynamic VOL	VOLP	$C_L = 50 \text{ pF}$	5.0	0.7	1.0	V
Quiet output minimum dynamic VOL	VOLV	$C_L = 50 \text{ pF}$	5.0	-0.7	-1.0	V
Minimum high level dynamic input voltage	$V_{IHD}$	$C_L = 50 \text{ pF}$	5.0	—	3.5	V
Maximum low level dynamic input voltage	$V_{ILD}$	$C_L = 50 \text{ pF}$	5.0	—	1.5	V

### Input Equivalent Circuit



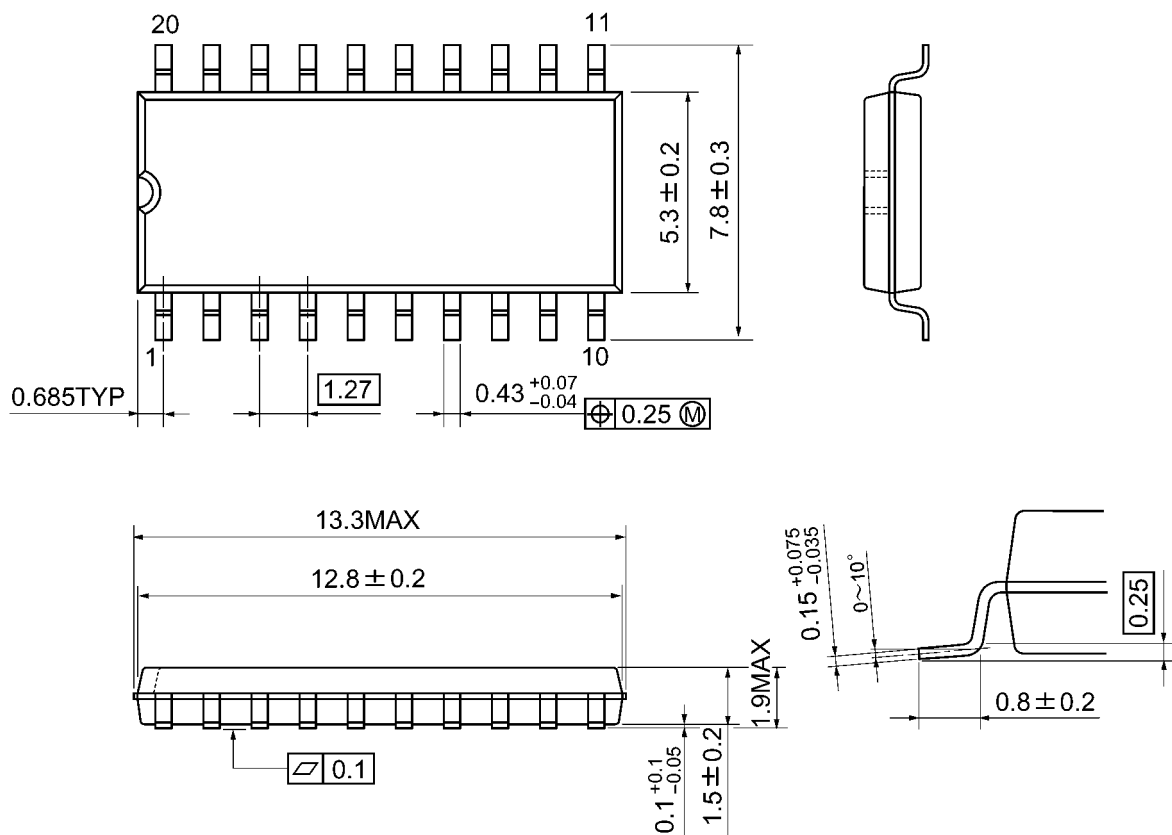
### Bus Terminal Equivalent Circuit



### Package Dimensions

SOP20-P-300-1.27A

Unit: mm

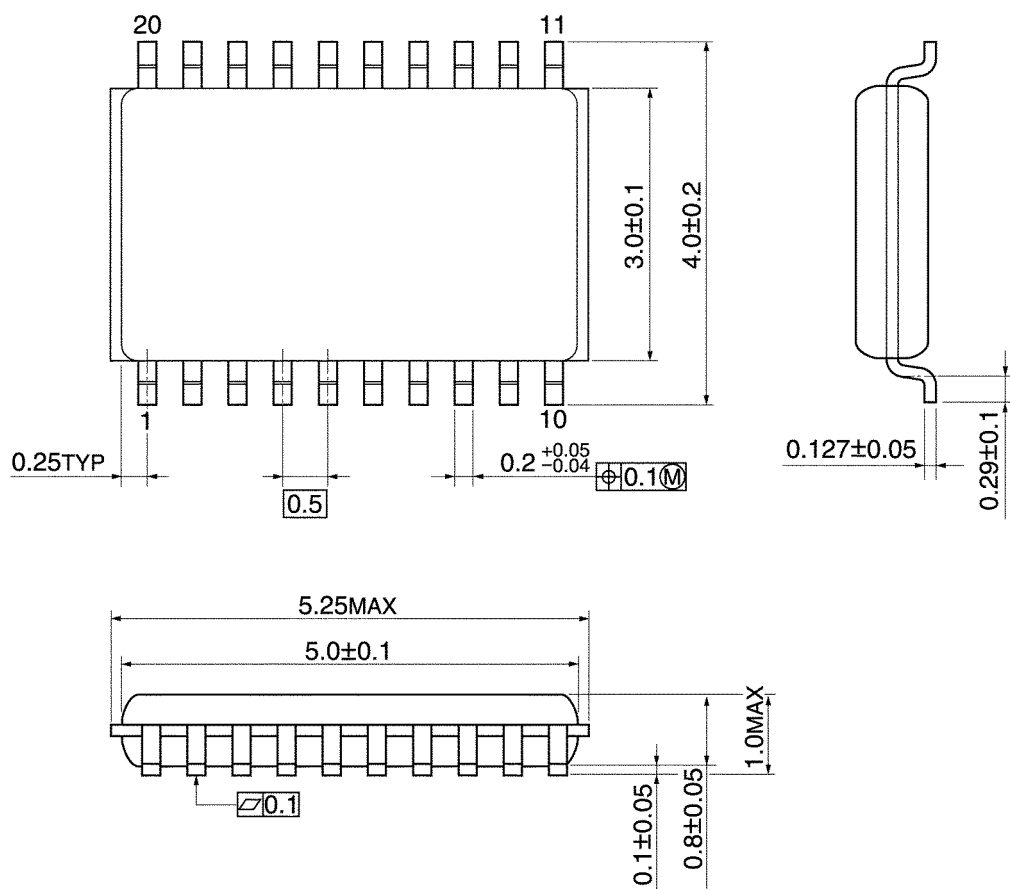


Weight: 0.22 g (typ.)

### Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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