



# THE DATASHEET OF FQD4N20LTM



# FQD4N20L / FQU4N20L

## 200V LOGIC N-Channel MOSFET

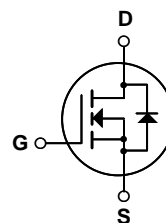
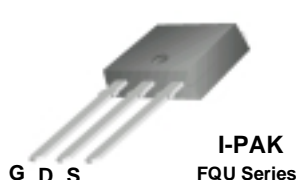
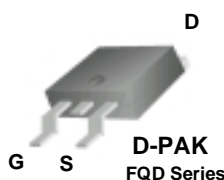
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, and motor control.

### Features

- 3.2A, 200V,  $R_{DS(on)} = 1.35\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 4.0 nC)
- Low  $C_{rss}$  ( typical 6.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirement allowing direct operation from logic drivers



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD4N20L / FQU4N20L	Units
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	3.2	A
		2.02	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	12.8	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	52	mJ
$I_{AR}$	Avalanche Current (Note 1)	3.2	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	30	W
		0.24	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	4.17	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.16	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.6\text{ A}$	--	1.10	1.35	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 1.6\text{ A}$	--	1.13	1.40	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 1.6\text{ A}$ (Note 4)	--	3.0	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	240	310	pF
$C_{oss}$	Output Capacitance		--	36	45	pF
$C_{rss}$	Reverse Transfer Capacitance		--	6	8	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 3.8\text{ A},$ $R_G = 25\ \Omega$  (Note 4, 5)	--	7	25	ns
$t_r$	Turn-On Rise Time		--	70	150	ns
$t_{d(off)}$	Turn-Off Delay Time		--	15	40	ns
$t_f$	Turn-Off Fall Time		--	40	90	ns
$Q_g$	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 3.8\text{ A},$ $V_{GS} = 5\text{ V}$  (Note 4, 5)	--	4.0	5.2	nC
$Q_{gs}$	Gate-Source Charge		--	1.0	--	nC
$Q_{gd}$	Gate-Drain Charge		--	1.9	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	3.2	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	12.8	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.2\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 3.8\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	90	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.25	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 7.6\text{ mH}, I_{AS} = 3.2\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 3.8\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

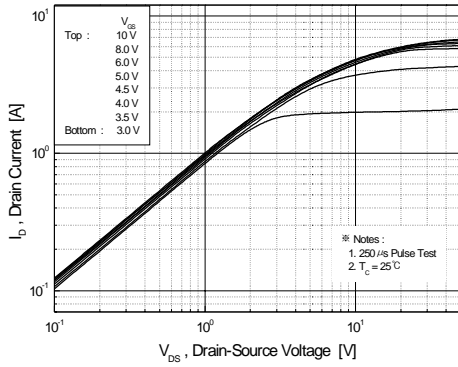


Figure 1. On-Region Characteristics

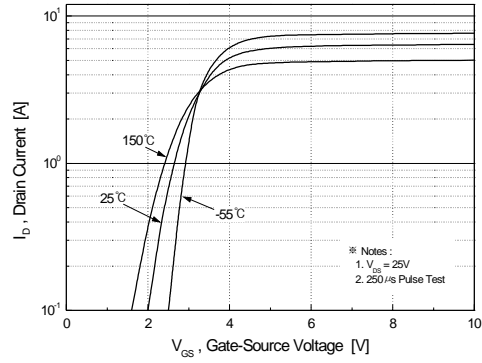


Figure 2. Transfer Characteristics

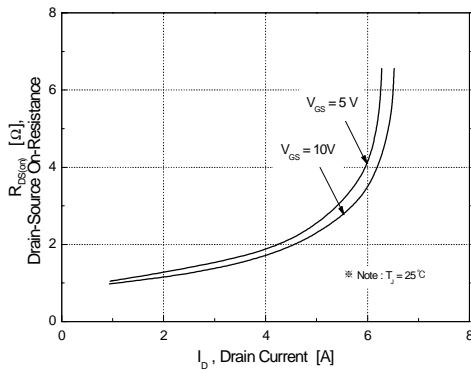


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

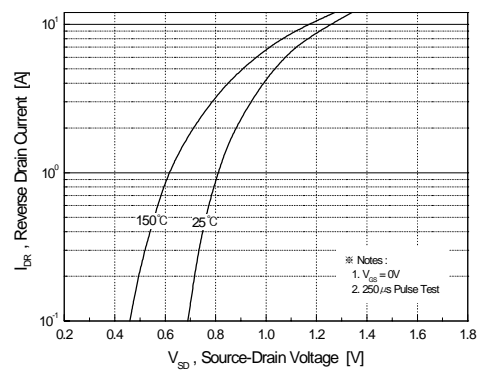


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

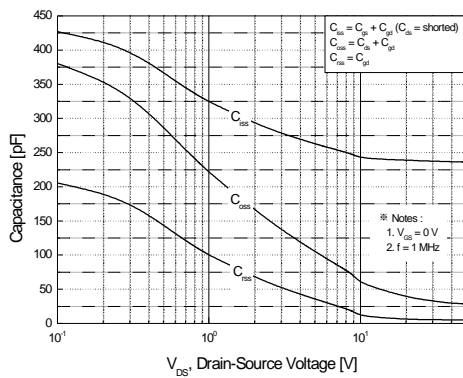


Figure 5. Capacitance Characteristics

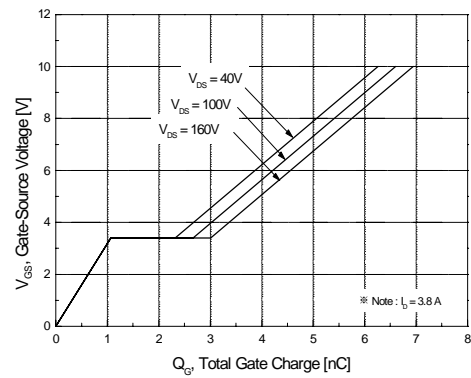
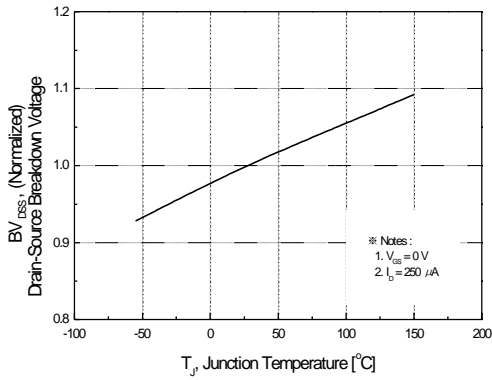
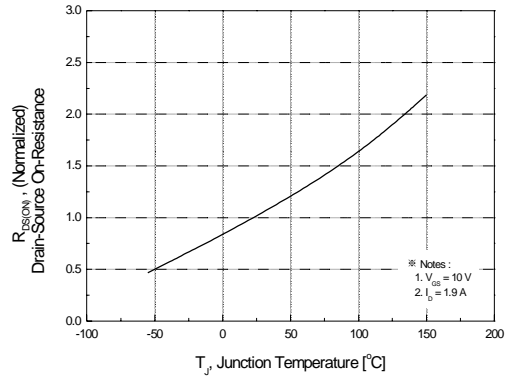


Figure 6. Gate Charge Characteristics

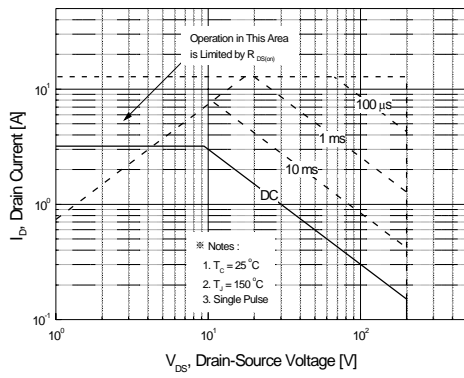
**Typical Characteristics** (Continued)



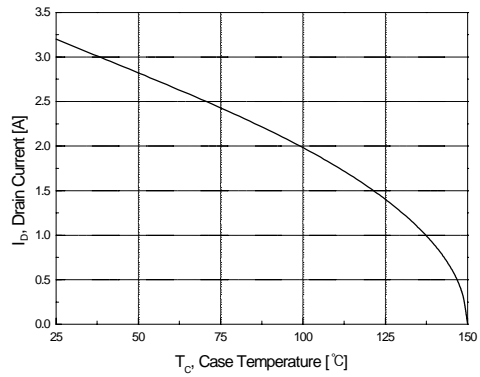
**Figure 7. Breakdown Voltage Variation vs. Temperature**



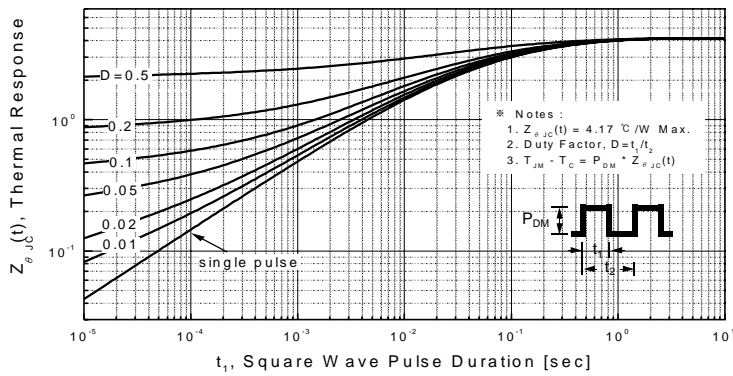
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

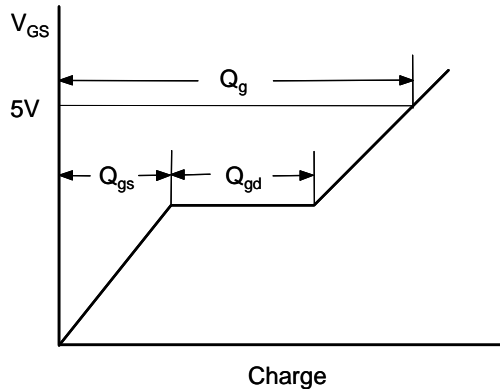
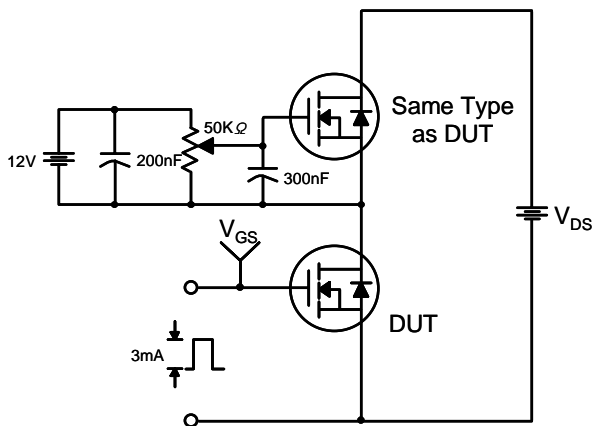


**Figure 10. Maximum Drain Current vs. Case Temperature**

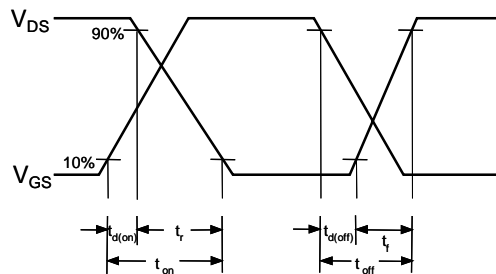
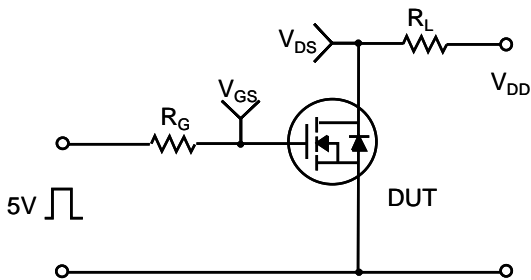


**Figure 11. Transient Thermal Response Curve**

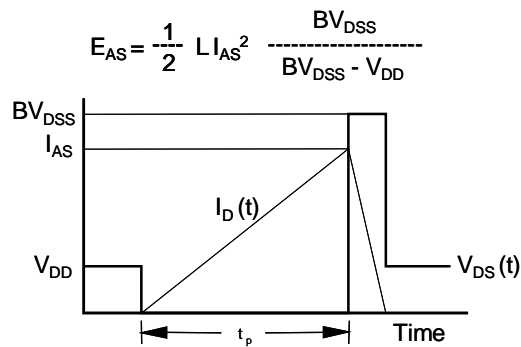
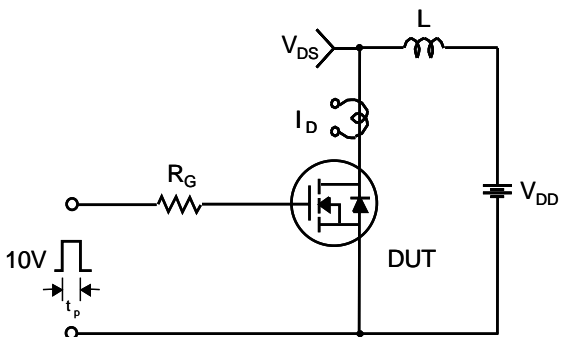
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



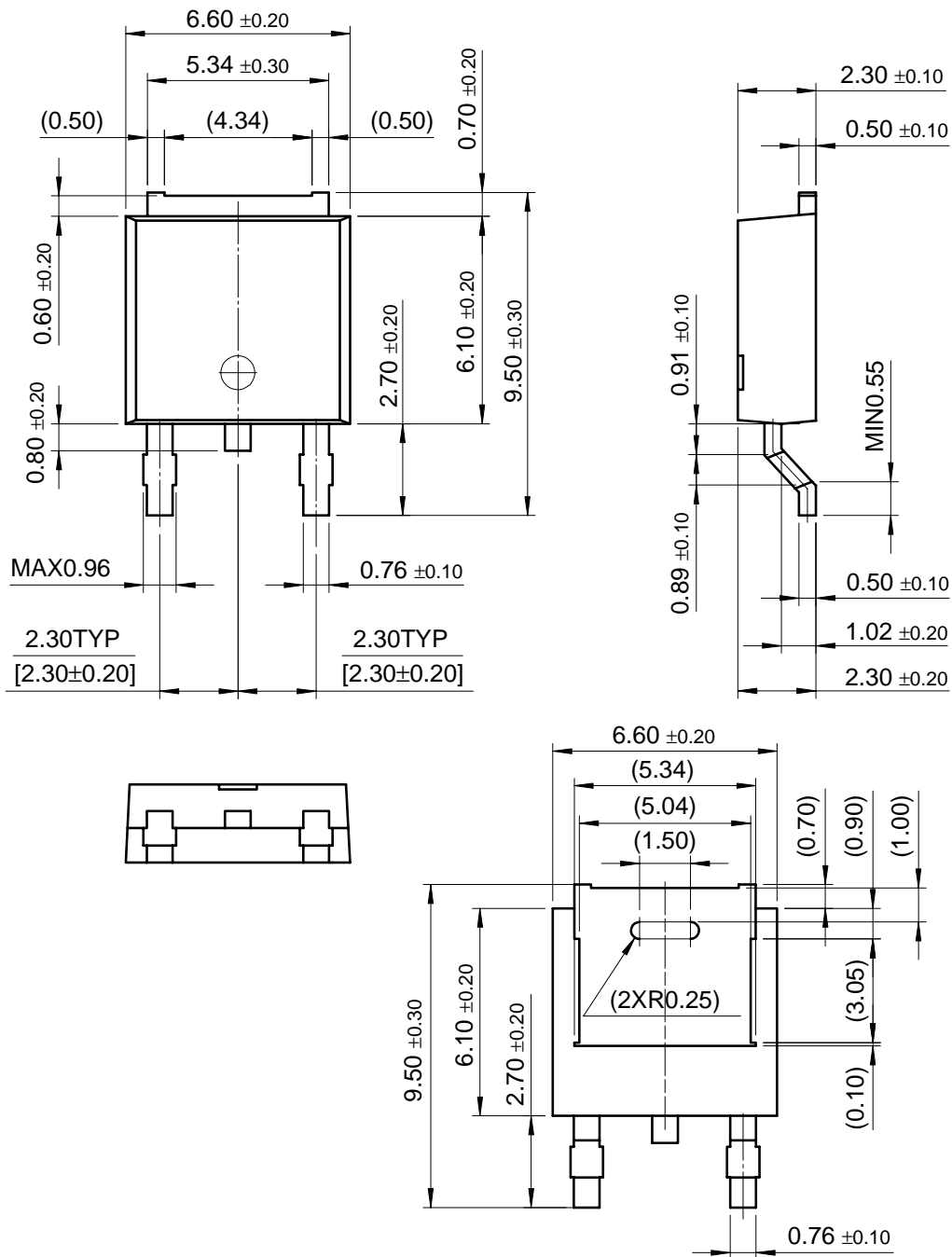
**Unclamped Inductive Switching Test Circuit & Waveforms**





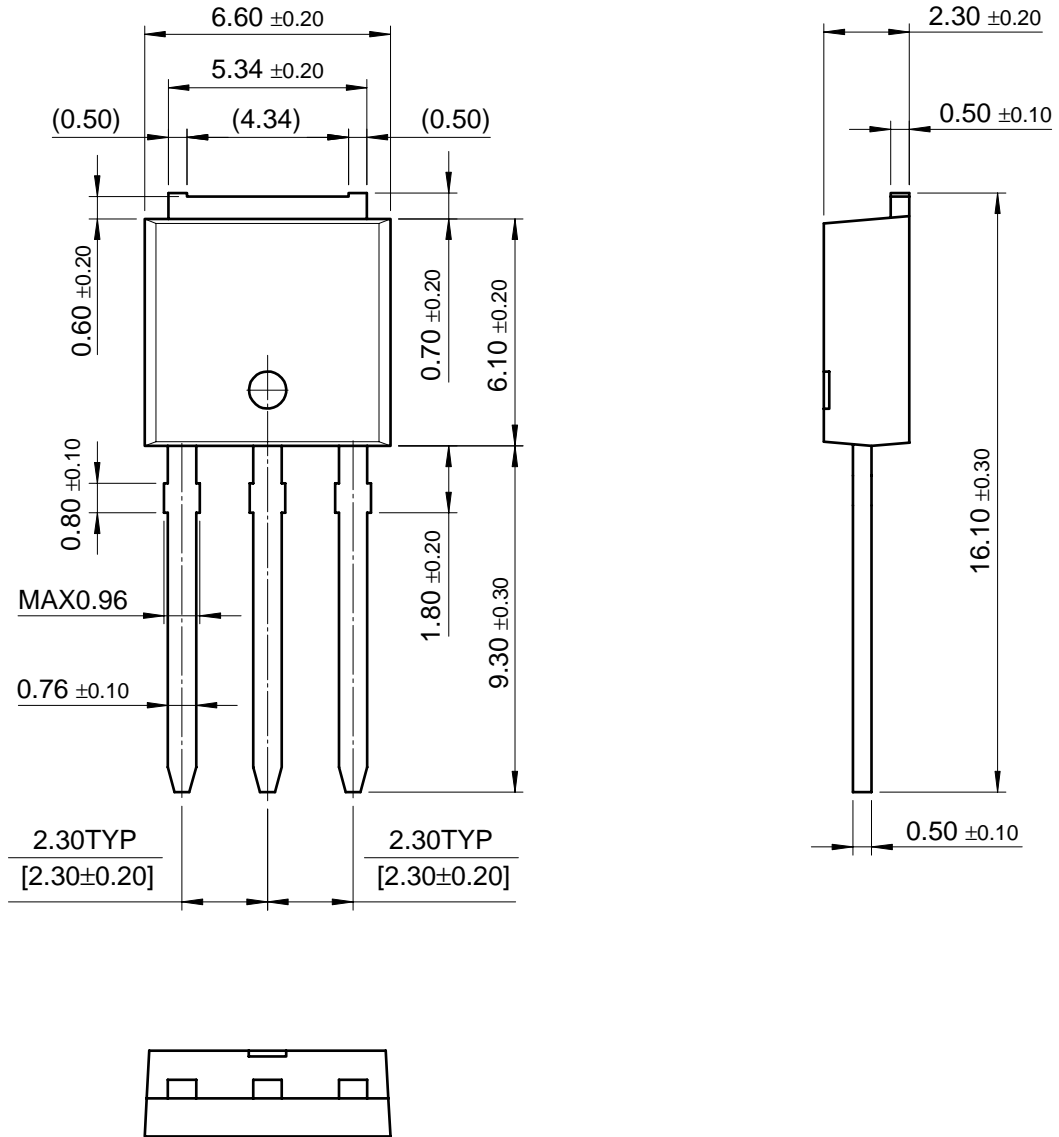
Package Dimensions

DPAK



Package Dimensions (Continued)

# IPAK



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