THE DATASHEET OF

SC4905BIMSTRT

SC4905A/B
High Performance Voltage Mode PWM Controller

Description

The SC4905A/B is a 10 pin BICMOS primary side voltage mode controller for use in Isolated DC-DC and off-line switching power supplies. It is a highly integrated solution, requiring few external components. The device features a high speed oscillator with integrated feed forward compensation, accurately programmable maximum duty cycle, voltage mode of operation, line voltage monitoring, supply UVLO, low start up current, low voltage current limit threshold and user accessible reference.

The SC4905A/B device operates at a fixed frequency, highly desirable for Telecom applications. Features a separate SYNC pin which simplifies synchronization to an external clock. Feeding the oscillator of one device to the SYNC of another forces biphase operation (180 degrees apart) which reduces input ripple and filter size.

The SC4905A has a typical turn-on threshold of 4.4V and the SC4905B has a typical turn-on threshold of about 11.6 volts.

These devices are available in the 10 lead MSOP package.

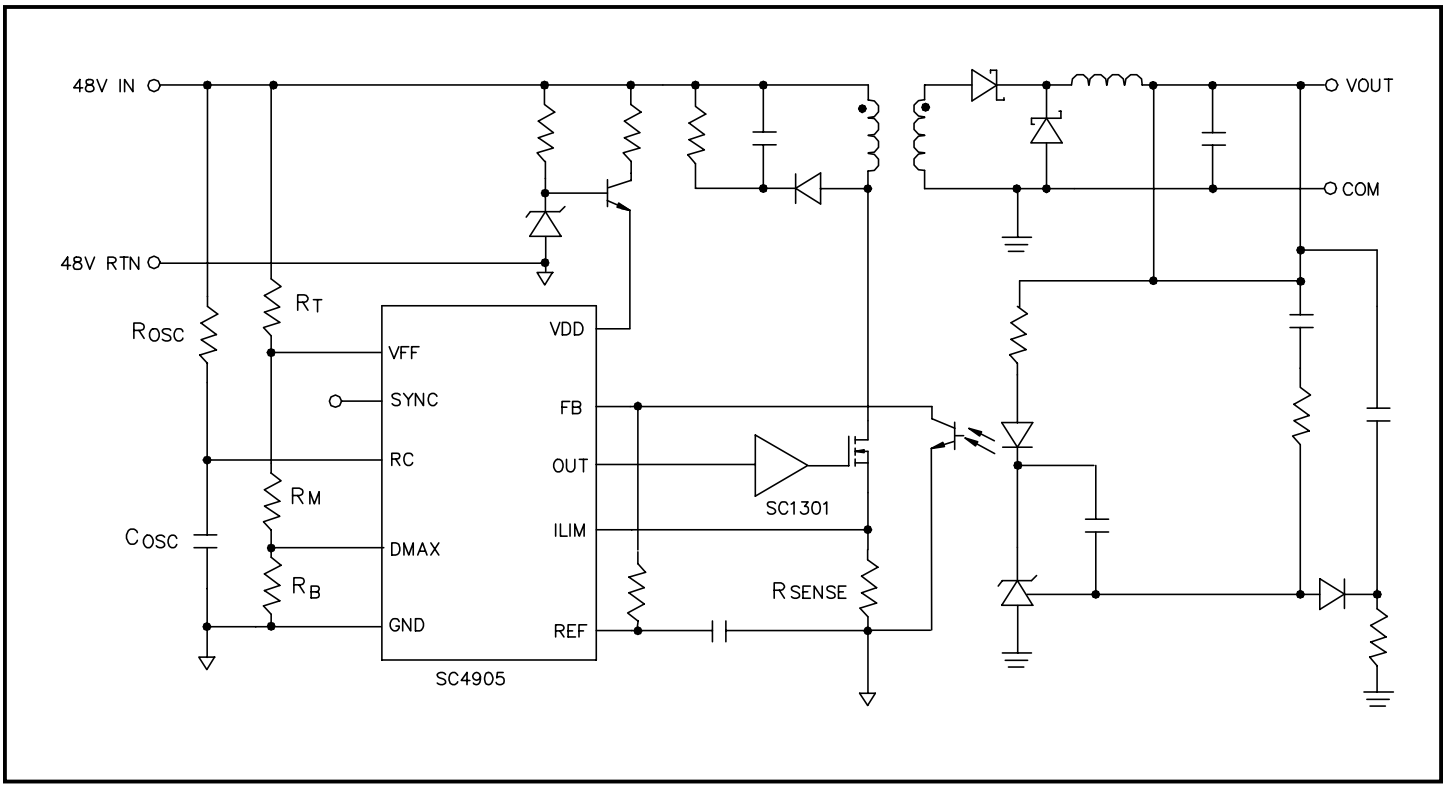
Features

- Operation to 1MHz
- Accurate programmable maximum duty cycle
- Integrated oscillator/voltage feed forward compensation
- Line voltage monitoring
- External frequency synchronization
- Bi-phase mode of operation for ripple reduction
- Under 100µA start-up current
- Accessible reference voltage
- VDD undervoltage lockout
- -40°C to 105°C operating temperature
- 10-Pin MSOP Lead-free package available. Fully WEEE and RoHS compliant

Applications

- Telecom equipment and power supplies
- Networking power supplies
- Power over LAN applications
- Industrial power supplies
- Isolated power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage		18	V
Input Voltage (RC, ILIM)		-0.3 to VREF + 0.3	V
Input Voltage (VFF)		-0.3 to VREF + 0.7	V
Input Current (VFF)		2	mA
Input Voltage (FB)		-0.3 to VREF + 0.7	V
Output Current (REF) DC		5	mA
OUT		-0.3 to VREF + 0.3	V
Power Dissipation		180	mW
Storage Temperature Range	T_{STG}	-65 to +150	°C
Junction Temperature	T_J	-55 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	°C
ESD Rating (Human Body Model)	ESD	2	KV

Electrical Characteristics

Unless otherwise specified, V_{DD} = 12V, V_{IN} = 48V, R_{OSC} = 499k, C_{OSC} = 220pF, R_T = 280k, R_M = 2k, R_B = 8.25k, C_{VDD} = 0.1uF, Ta = Tj = -40 to 105 °C.

Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Curent Section					
Startup Current	V_{DD} = UVLO Start - 1, VDD Comparator Off			100	µA
I_{DD} Active	V_{DD} = Comparator On, Oscillator Running		3.5	4.2	mA
Line Under Voltage Lockout					
Start Threshold	Voltage measured at V_{FF} pin	1.164	1.200	1.236	V
Hysteresis		85	100	115	mV
I_{IB} (VFF)	V_{FF} = 1.2V +/- 3%	-300		300	nA
Oscillator Section					
Maximum Frequency	V_{FF} = 1.2V to 4.8V	0.8	1.0	1.2	MHz
CT Peak Voltage (1)	V_{FF} = 1.2V		1.2		V
	V_{FF} = 3.6V		3.6		V
CT Valley Voltage (1)			200		mV
Sync/CLOCK					
Clock SYNC Threshold		.45 *V_{FF}	.50 *V_{FF}	.55 *V_{FF}	V
Sync Input Detect Time (1)	F_{SYNC} > Fosc		50		nS

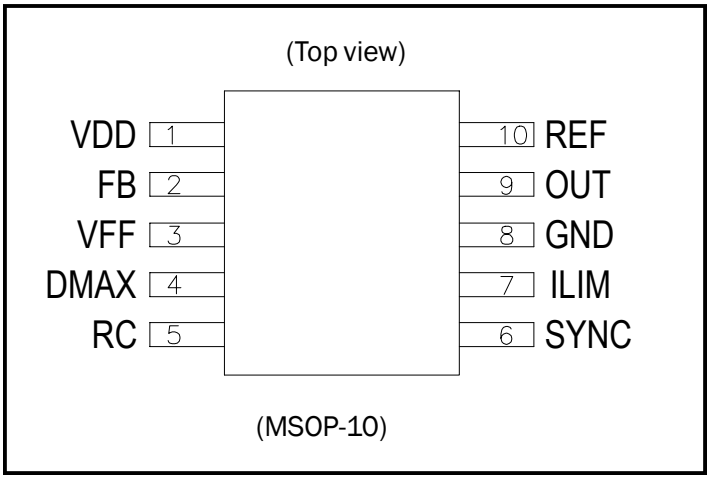
Electrical Characteristics (Cont.)

Unless otherwise specified, V_{DD} = 12V, V_{IN} = 48V, R_{OSC} = 499k, C_{OSC} = 220pF, R_T = 280k, R_M = 2k, R_B = 8.25k, C_{VDD} = 0.1uF, Ta = Tj = -40 to 105 °C.

Parameter	Test Conditions	Min	Typ	Max	Unit
Sync/CLOCK (Cont.)					
Sync Frequency (1)			1.2 *F_{OSC}		Hz
Current Limit Section					
Input Bias Current		0		-2	µA
Current Limit Threshold		170	200	230	mV
Propagation Delay, ILIM to OUT (1)	50mV Overdrive		35		ns
VREF Section					
VREF (A version)	0 - 5mA	-3%	4	+3%	V
VREF (B version)	0 - 5mA	-3%	5	+3%	V
VDD UVLO Section (A version)					
Start Threshold		4.1	4.4	4.6	V
Hysteresis			200	300	mV
VDD UVLO Section (B version)					
Start Threshold		11	11.6	12	V
Hysteresis			3.6	4	V
Pulse Width Modulator Section					
FB Input current	V_{FB} = 0V to Vref			1	uA
Minimum Duty Cycle (1)	V_{FB} < 500mV			0	%
Maximum Duty Cycle	V_{DMAX} = V_{FF} , V_{FB} = Vref		95		%
PWM Gain (1)	V_{FF} = 3.6		27.5		%/V
Propagation Delay, PWM to OUT (1)			75		ns
Output					
Output VSAT Low	I_{OUT} = 1mA			500	mV
Output VSAT High	I_{OUT} = 1mA	VREF - 0.5			V
Rise Time (1)	C_{OUT} = 20pF		10		ns
Fall Time (1)	C_{OUT} = 20pF		10		ns

Note 1: Guaranteed by design. Not 100% tested in production.

Pin Configuration



Ordering Information

Part Number	Package(1)	Temp. Range (T_A)
SC4905AIMSTR	MSOP-10	-40°C to 105°C
SC4905AIMSTRT(2)		
SC4905BIMSTR		
SC4905BIMSTRT(2)		

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

VDD: The supply input for the device. Once VDD has exceeded the UVLO limit, the internal reference, oscillator, drivers and logic are powered up. This pin should be bypassed with a low ESR capacitance right at the IC pin to minimize noise problems, and to ensure proper operation.

FB: Input to the PWM comparator with an offset voltage of 700mV. The feedback analog signal from the output of an error amplifier or an Optoisolator will be connected to this pin to provide regulation.

VFF: The VFF pin provides the controller with a voltage proportional to the power supply input voltage to achieve feed-forward function. RM plus RB in conjunction with RT will set the Vff level (see page 1 circuit).

$$VFF = \frac{(R_B + R_M)}{(R_T + R_B + R_M)} \times VIN$$

DMAX: Programmable duty cycle is achieved via resistive divider from the VFF. The duty cycle percentage is set by the ratio of the divider RM, and RB (see page 1 circuit) from the VFF signal. When RM is shorted, maximum duty cycle of 100% is achieved. RM plus RB in conjunction with RT will also be used as the divider to set the Vff level.

$$DutyCycle\% = \frac{VDMAX}{VFF}$$

RC: The oscillator programming pin. The oscillator should be referenced to Vin to achieve the line feed forward function. Only two components are required to program the oscillator, a resistor R_{OSC} (tied to the Vin and RC), and a capacitor C_{OSC} (tied to the RC and GND). Since the peak oscillator voltage is VFF, constant frequency operation is maintained over the full power supply. When the DMAX pin is shorted to the VFF pin, the oscillator can run at the largest duty cycle possible.
Following formula can be used for a close approximation of the Oscillator Frequency.

$$F_{OSC} \cong \frac{\left(Vin - \frac{VFF}{2}\right)}{(R_{OSC} \bullet C_{OSC} \bullet VFF \bullet 1.05)}$$

Where VFF is the voltage at the VFF pin at a given Vin, frequency is in Hertz, resistance in ohms, and capacitance in farads.
The recommended range if timing resistors is between 10 kohm and 500kohm and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10 kohm should be avoided.
Refer to layout guide lines on page 12 to achieve best results.

SYNC: SYNC is a positive edge triggered input with a threshold precisely set to

0.5*VFF

In the Bi-Phase operation mode SYNC pins should be connected to the Cosc (Timing Capacitors) of the other controller. This will force a 180° out of phase operation. (see page9).
In a single controller operation, SYNC could be grounded or connected to an external synchronization clock with Frequency higher than the on board oscillator Frequency (see page 2).

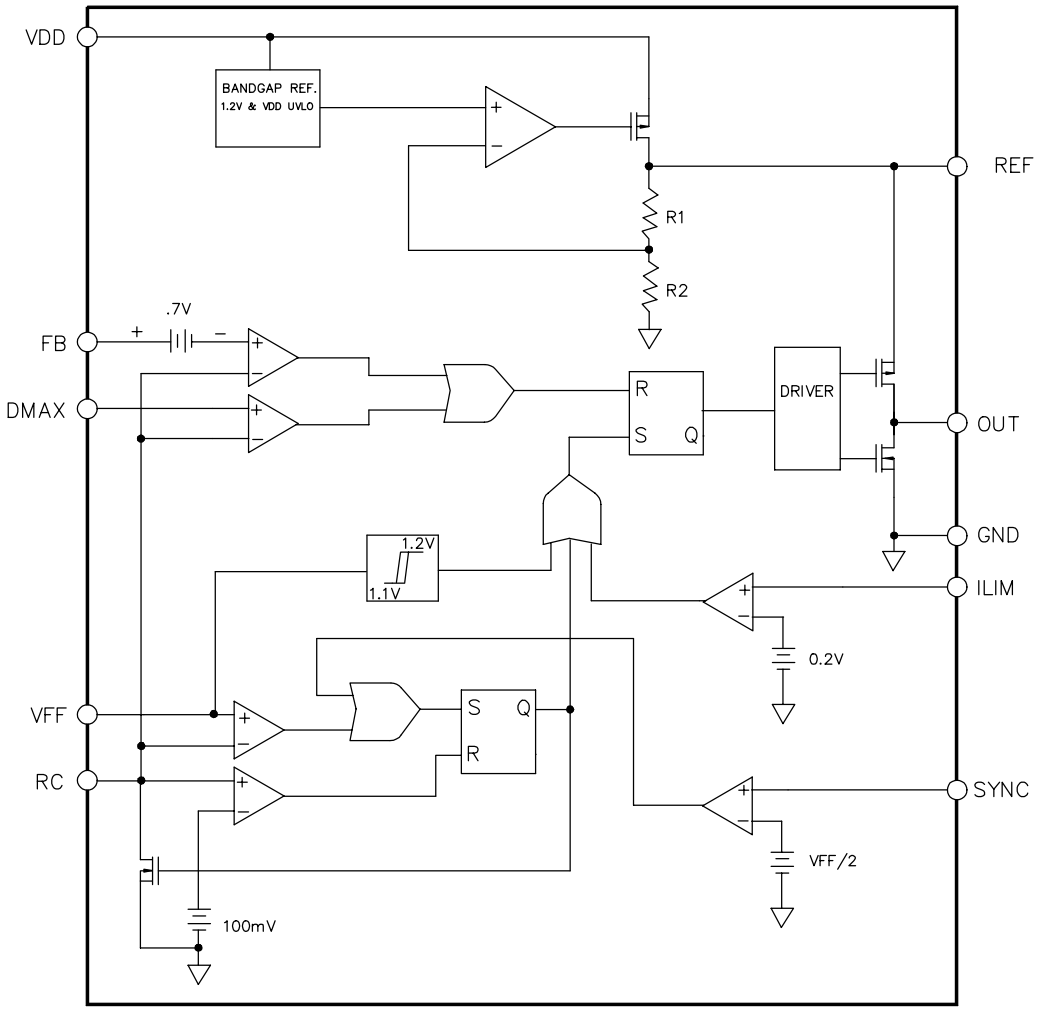
ILIM: Current sense input is provided via the ILIM pin. The current sense input from a sense resistor provides a pulse by pulse current limit by terminating the PWM pulse when the input is above 180mV.

GND: Device power and analog ground. Careful attention should be paid to the layout of the ground planes (see page 12).

OUT: The output is intended to drive an external FET driver or other high impedance circuit. The output voltage swings from GND to Vref with a typical output impedance of 500Ω.

REF: The REF pin provides a 4 or 5V user accessible voltage reference. This pin should be decoupled with a 1µF capacitor.

Block Diagram

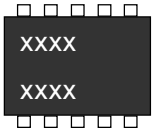


Marking Information

SC4905AIMSTR SC4905BIMSTR

Top Mark

Bottom Mark



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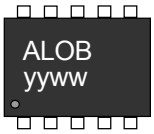

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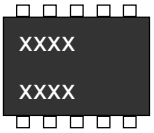


yyww = Date Code (Example: 0012)
xxxx = Semtech Lot No. (Example: E901 01-1)
xxxx

THEORY OF OPERATION

The SC4905 is a versatile 10 pin BICMOS primary side voltage mode controller optimized for applications requiring minimum space such as isolated DC-DC and off-line switching power supplies.
The device contains all of the control and drive circuity required for isolated or non-isolated power supplies, where an external error amplifier is used. Fixed oscillator frequency up to 1MHz can be programmed by an external RC network.
The SC4905 is a voltage mode controller, utilizing a feed forward scheme to accommodate for any variations in the input supply voltage resulting in a duty cycle adjustment. This feed forward action results in an improved dynamic performance of the converter.
The SC4905 also provides a programmable maximum duty cycle to prevent core saturation when a transformer is used. As an added level of protection, SC4905 provides a cycle by cycle peak current limit during an over current condition.

SUPPLY

A single supply, VDD is used to provide the bias for the internal reference, oscillator, drivers, and logic circuitry of the SC4905.

PWM CONTROLLER

The SC4905 is a BICMOS primary side voltage mode controller for use in isolated DC-DC and off-line switching power supplies. It is a highly integrated solution, requiring few external components.
The device features a high speed oscillator with integrated feed forward compensation, accurately programmable maximum duty cycle, voltage mode of operation, line voltage monitoring, supply UVLO, low start-up current, low voltage current limit threshold and user accessible reference.
Two voltage options are available for the SC4905. The SC4905A version has a typical VDD under voltage of 4.4V, and a 4V reference, while the SC4905B version provides a 11.6V VDD UVLO, and a 5V reference.
The Oscillator frequency is programmed by a resistor and a capacitor network connected to the line supply voltage . Any variations in the input supply voltage result in a duty cycle adjustment, provided by the change of the oscillator peak voltage via the VFF pin.
This feed forward action provides an immediate duty cycle adjustment while maintaining a constant oscillator frequency.
A maximum duty cycle can be programmed by connecting a resistor divider from the VFF to the DMAX pin. The scaling of the VFF signal will set the maximum duty cycle percentage.
An external error amplifier will provide the error signal to the FB pin of the SC4905.
A current sense input is provided via the ILIM pin. The current sense input from a sense resistor is used for the peak current limit comparator.
Once VDD has exceeded the UVLO (VDD under voltage lock out) limit, the internal reference, oscillator, drivers and logic are powered up.
SYNC is a positive edge triggered input with a threshold set to 0.5*VFF.
By connecting a faster external control signal to the SYNC pin, the internal oscillator frequency will be synchronized to the positive edge of the external control signal. In a single controller operation, SYNC could be grounded or connected to an external synchronization clock within the SYNC frequency (see page 3).
In the Bi-Phase operation mode a very unique oscillator is utilized to allow two SC4905 to be synchronized together and work out of phase. This feature is setup by simple connection of the SYNC input to the RC pin of the other part. The fastest oscillator automatically becomes the master, forcing the two PWMs to operate out of phase. This feature minimizes the input and output ripples, and reduces stress on the capacitors.

Device	Typical Vdd UVLO	Typical Reference Voltage
SC4905A	4.4V	4V
SC4905B	11.6V	5V

Application Information (Cont.)

VDD UNDER VOLTAGE LOCK OUT

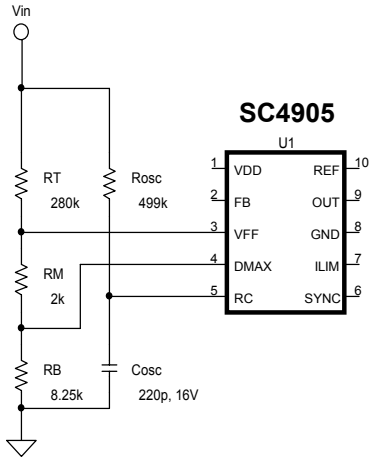
According to the application, and the voltages available, the SC4905A (UVLO = 4.4V), or the SC4905B (UVLO = 11.6V) can be used to provide the VDD undervoltage lock out function to ensure the converters controlled start up.
Before the VDD UVLO has been reached, the internal reference, oscillator, OUT driver, and logic are disabled.

REFERENCE

A 4V (SC4905A) or a 5V(SC4905B) reference voltage is available that can be used to source a typical current up to 5mA to the external circuitry. The REF can be used to provide the feed back circuitry with a regulated bias.

OSCILLATOR

The oscillator frequency is set by connecting a RC network as shown below.



The oscillator has a ramp voltage that will track the voltage at the VFF pin (1.2V<VFF<3.6V). The oscillator peak voltage is derived by charging the oscillator capacitor (Cosc) to the VFF voltage via the oscillator resistor (Rosc). The bias current to charge the Cosc is controlled by the Rosc. Once the RC pin has reached the VFF voltage, the oscillator ramp is discharged by an internal switch hence creating the triangle oscillator ramp.

Since the Rosc is referenced to the input supply voltage, any variation in the supply is directly translated into a variation in the duty cycle, while maintaining the fixed frequency operation.
Following equation can be used to calculate the oscillator frequency:

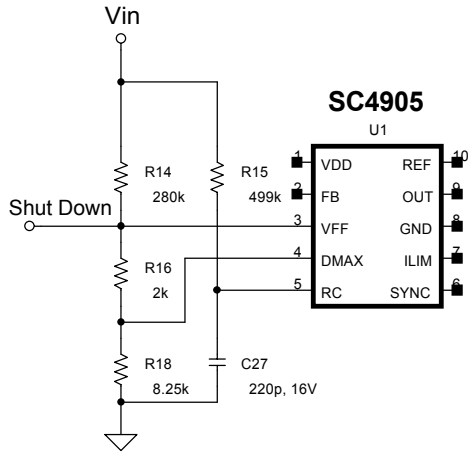
$$F_{OSC} \cong \frac{\left(Vin - \frac{VFF}{2}\right)}{(R_{OSC} \bullet C_{OSC} \bullet VFF \bullet 1.05)}$$

The recommended range if timing resistors is between 10 kohm and 500kohm and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10 kohm should be avoided.

Application Information (Cont.)

FEED FORWARD & MAXIMUM DUTY CYCLE

The feed forward function provided by the SC4905 will improve the dynamic performance of the converter in response to the changes in the input supply.
In voltage mode controllers without the voltage feed forward circuitry, any changes in the input supply will cause an error in the output voltage which is sensed by the error amplifier and eventually is translated to an adjustment in the duty cycle by the controller. This delay in the response will cause the slower dynamic performance of the converter.
This problem is resolved by sensing the input supply line and making the adjustment in the duty cycle immediately at the PWM controller.



The SC4905 uses the input supply line as the bias for the oscillator circuitry, and the VFF pin. Any changes in the line will cause the ramp peak voltage to be adjusted to the VFF pin voltage while maintaining the oscillator frequency unchanged.
The VFF pin can also be used to shut down the SC4905 if it is pulled down to GND by an open collector circuitry. This can be useful for overvoltage protection or other control signals.
The SC4905 also provides a programmable duty cycle, that can be set by an external voltage divider from the VFF pin. The ratio of the divider will determine the programmed duty cycle allowed.

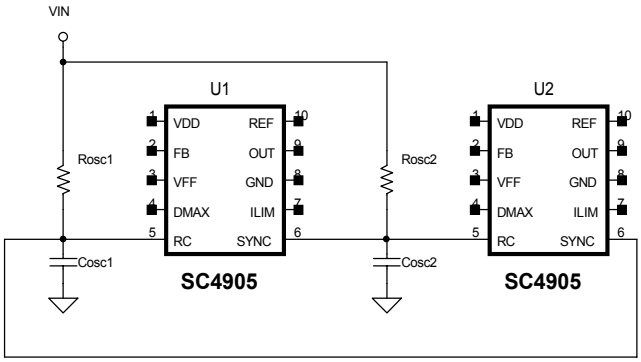
$$\text{DutyCycle}\% = \frac{\text{VDMAX}}{\text{VFF}}$$

If the application does not require an upper limit on the duty cycle, the VFF pin should be connected to the DMAX pin. In this mode, the duty cycle will be allowed to increase to the maximum limit of about 100%.

SYNC/Bi-Phase operation

In noise sensitive applications where synchronization of the oscillator frequency to a reference frequency is required, the SYNC pin can accept the external clock.By connecting an external control signal to the SYNC pin, the Internal oscillator frequency will be synchronized to the positive edge of the external control signal. SYNC is a positive edge triggered input with a threshold set to 0.5*VFF.

In a single controller operation, SYNC chould be grounded or connected to an external synchronization clock within the SYNC frequency (see page 3).

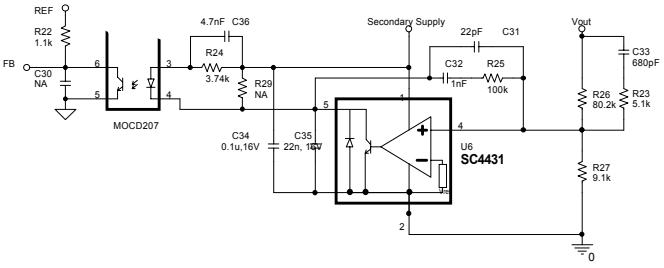


In the Bi-Phase operation mode a very unique oscillator is utilized to allow two SC4905 to be synchronized together and work out of phase. This feature is setup by simple connection of the SYNC input to the RC pin of the other part. The fastest oscillator automatically becomes the master, forcing the two PWMs to operate out of phase. This feature minimizes the input and output ripples, and reduces stress on the capacitors.

Application Information (Cont.)

FEED BACK

The error signal from the output of an external Error amplifier such as SC431 or SC4431 is applied to the inverting input of the PWM comparator at the FB pin either directly or via an opto coupler for the Isolated applications. For best stability keep the FB trace length as short as possible.

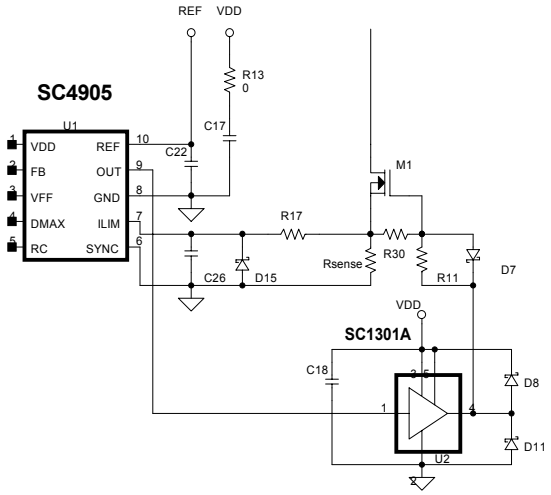


The signal at the FB pin is then compared to the ramp signal from the RC pin and the OUT gate drive signal is generated.

Voltages below 600mV at the FB pin, will produce a 0% duty cycle at the OUT drive. Maximum duty cycle is produced when VFB-600mV>VFF. The FB signal range is from 600mv to 4V.

OVER CURRENT

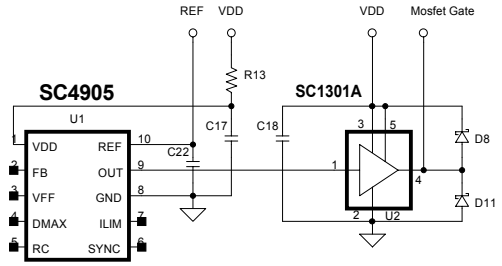
A pulse by pulse current limit is provided by the SC4905. The current information is sensed at the ILIM pin and compared to a peak current limit level of 180mV. If the 180mV limit is exceeded, the OUT pulse is terminated.



GATE DRIVERS

OUT is a CMOS gate drive output stage that is supplied from REF and provides a peak source/sink current of about 1mA. The output stage is capable of driving the logic input of external MOSFET Drivers and is switched at the oscillator frequency. When the voltage on the RC pin is rising,, the output is high.

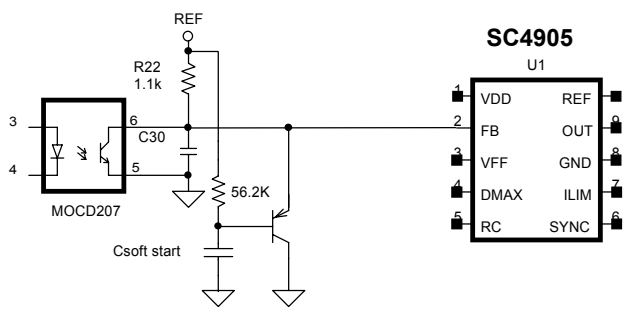
It should be noted that if high speed/high current drivers such as the SC1301 are used, careful layout must be followed in order to minimize stary inductance, which might cause negative voltages at the output of the drivers. This negative voltage can be clamped to reasonable level by placing a small Schottky diode directly at the output of the driver as shown below.



SOFT START

During start up of the converter, the discharged output capacitor, and the load current demand large supply current requirements. To avoid this a soft start scheme is usually implemented where the duty cycle of the regulator is gradually increased from 0% until the soft start duration is elapsed.

Programmable soft start duration can implemented externally by utilizing a simple external circuitry shown below.



Approximate soft start duration can be calculated as below:

Application Information (Cont.)

START UP SEQUENCE

Initially during the power up, the SC4905 is in the under voltage lock out condition. As the VDD supply exceeds the UVLO limit of the SC4905 and the VFF pin exceeds the line under voltage lock out of about 1.2V, the internal reference, oscillator, and logic circuitry are powered up.

The OUT driver is not enabled until the line under voltage lock out limit is reached. At that point, once the FB pin has reached above 600mV, the output driver is enabled. As the output voltage starts to increase, the error signal from the error amplifier starts to decrease. If isolation is required, the error amplifier output can drive the LED of the opto isolator. The output of the opto is connected in a common emitter configuration with a pull up resistor to a reference voltage connected to the FB pin of the SC4905. The voltage level at the FB pin provides the duty cycle necessary to achieve regulation.

Application Information (Cont.)

LAYOUT GUIDELINES

Careful attention to layout requirements are necessary for successful implementation of the SC4905 PWM controller.

High currents switching are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used. The number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the FET must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between FETs and the Transformer should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI.

4) The output capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only. Connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC4905 is best placed over a quiet ground plane area. Avoid pulse currents in the Cin FET loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the VDD supply capacitor(s). Under no circumstances should GND be returned to a ground inside the Cin and FET loop. This can be achieved by making a star connection between the quiet GND planes that the SC4905 will be connected to and the noisy high current GND planes connected to the FETs.

6) The feed back connection between the error amplifier and the FB pin should be kept as short as possible, and the GND connections should be to the quiet GND used for the SC4905.

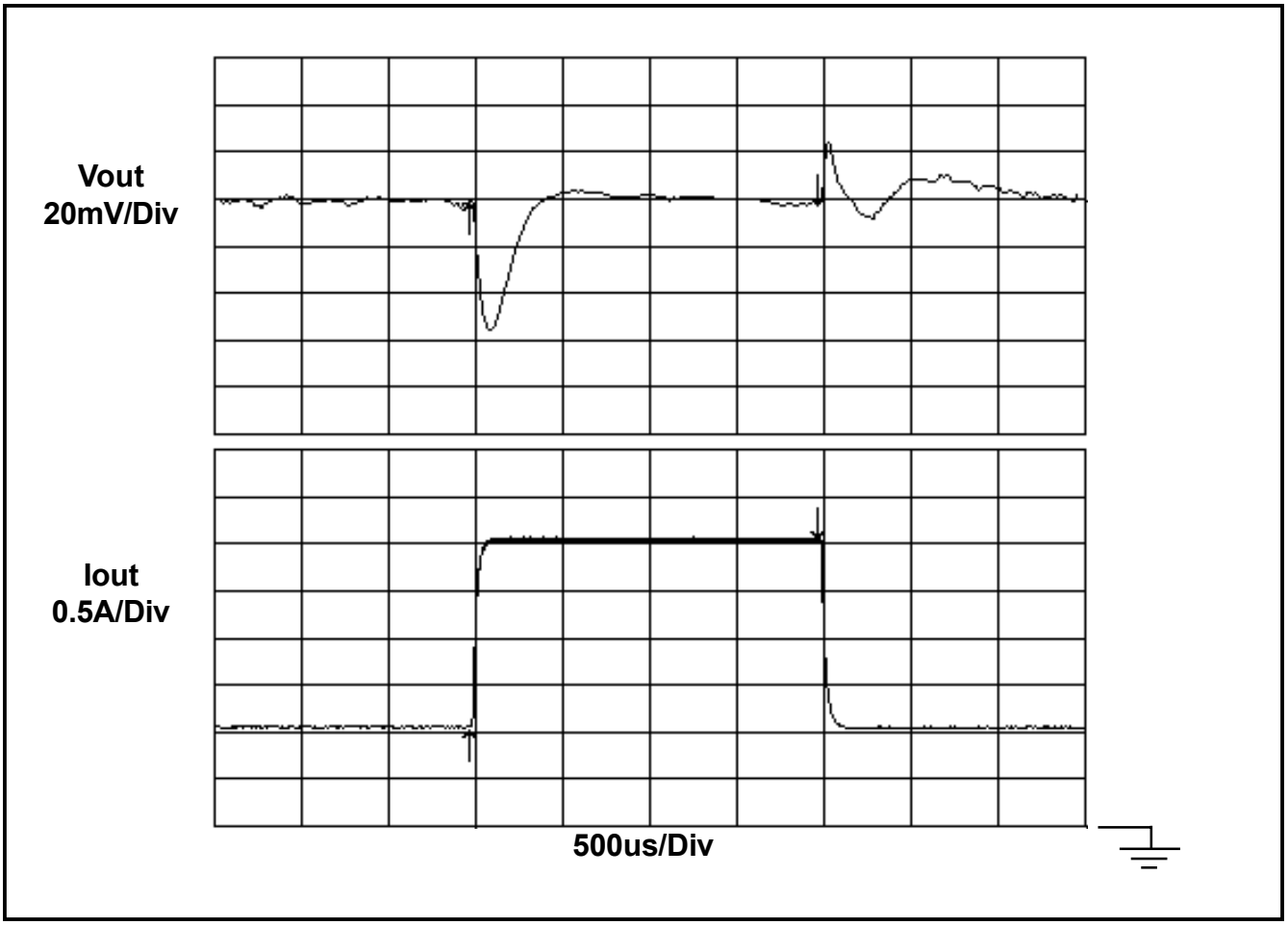
7) If an opto isolator is used for isolation, quiet primary and secondary ground planes should be used. Same precautions should be followed for the primary GND plane as mentioned in item 5 mentioned above. For the secondary GND plane, the GND plane method mentioned in item 4 should be followed.

8) All the noise sensitive components such as VFF, DMAX resistive divider, reference by pass capacitor, VDD bypass capacitor, current sensing circuitry, feedback circuitry, and the oscillator resistor/capacitor network should be connected as close as possible to the SC4905. The GND return should be connected to the quiet SC4905 GND plane.

9) The connection from the OUT of the SC4905 should be minimized to avoid any stray inductance. If the layout can not be optomized due to constraints, a small Schottky diode maybe connected from the OUT pin to the ground directly at the IC. This will clamp excessive negative voltages at the IC. If drivers are used, the Schottky diodes should be connected directly at the IC, from the output of the driver to the driver ground.

10) If the SYNC function is not used, the SYNC pin should be grounded at the SC4905 GND to avoid noise pick up.

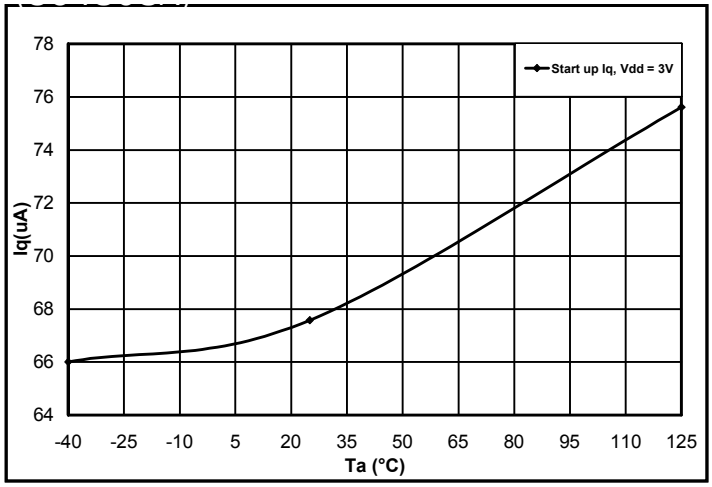
Typical Step Load



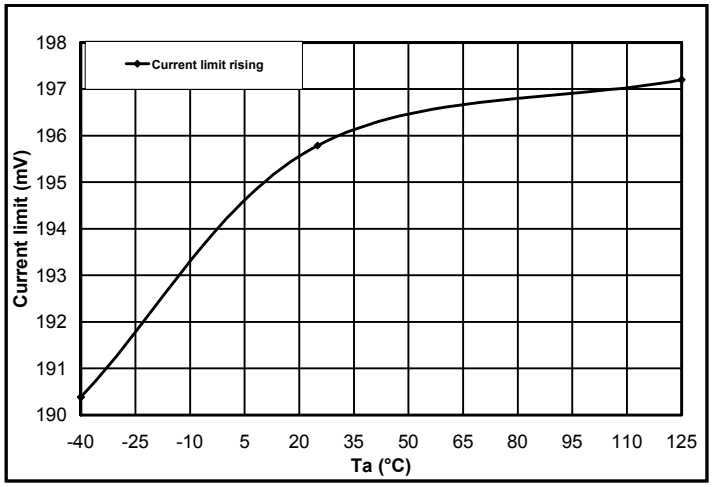
Cout = 6X100uF (600uF) Tantalum

Typical SC4905 Forward converter Step Load plot at Vin = 48V, Vout = 12V, Step = 50% to 75% Iout, Fosc = 245kHz

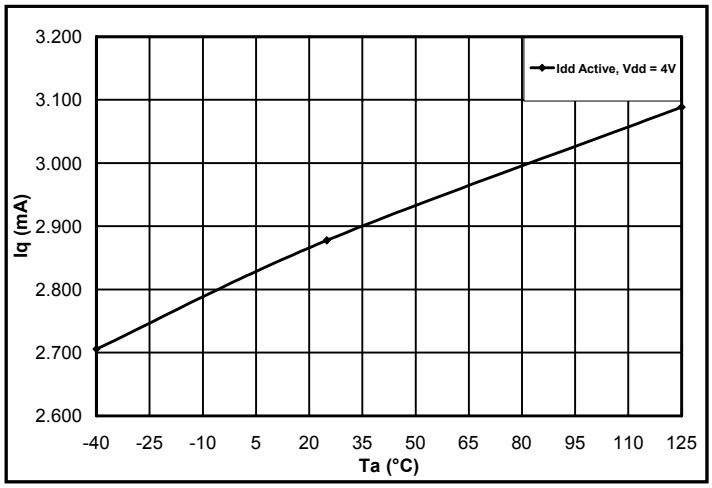
SC4905A Typical Characteristics



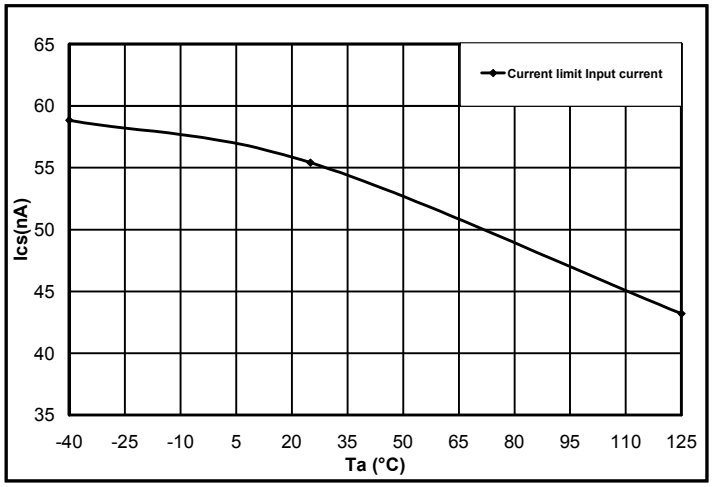
Iq (start up) vs. Temperature



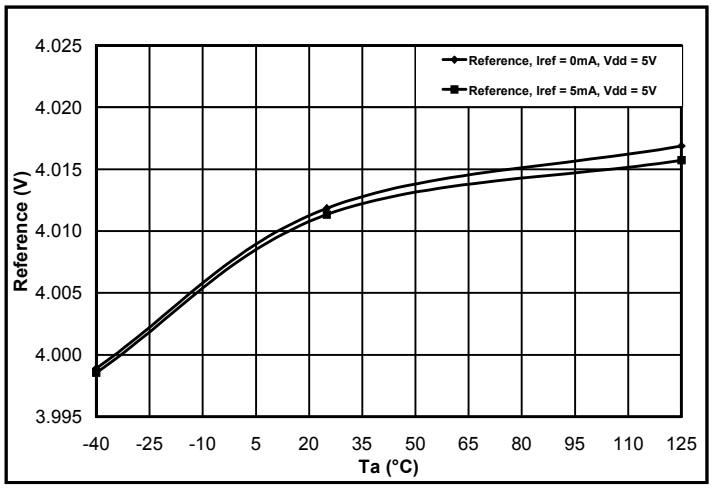
Current Limit vs. Temperature



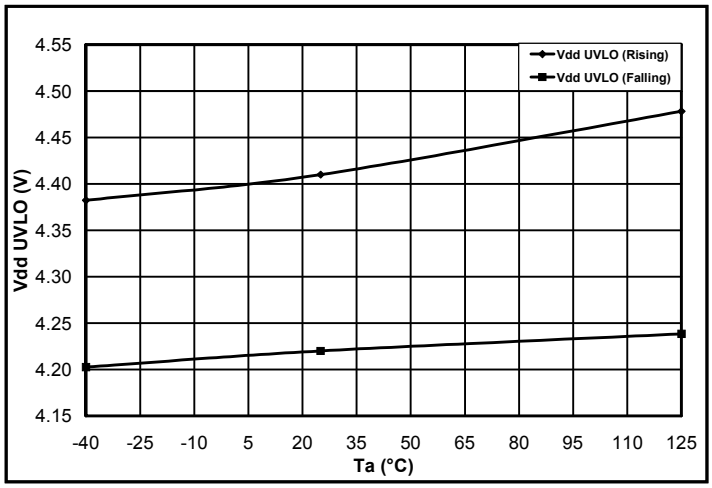
Idd (operating) vs. Temperature



Current Limit bias current vs. Temperature

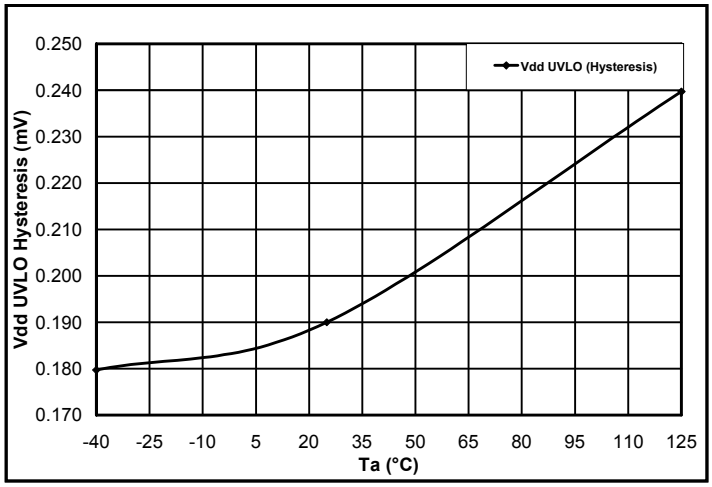


Reference vs. Temperature

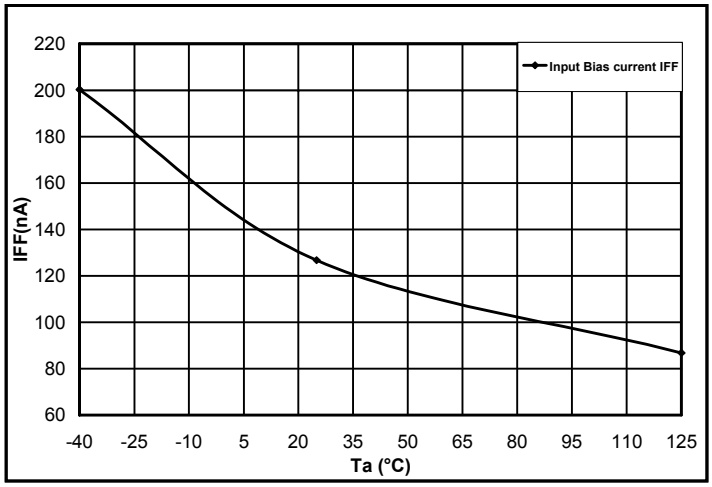


Vdd UVLO vs. Temperature

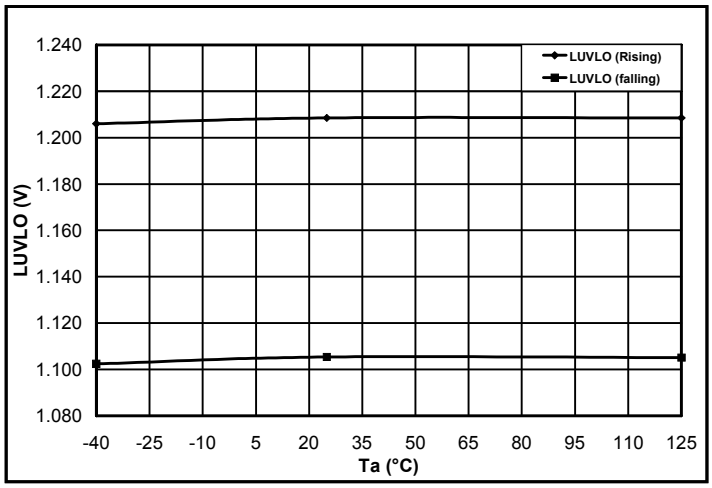
SC4905A Typical Characteristics (Cont.)



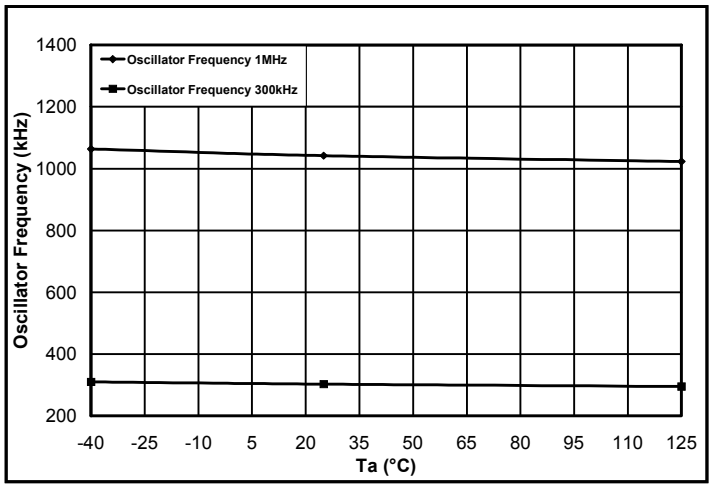
Vdd UVLO Hysteresis vs. Temperature



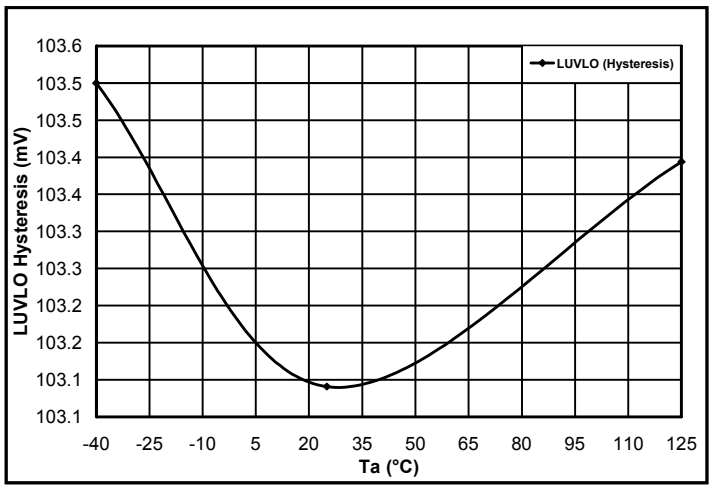
Vff pin leakage current vs. Temperature



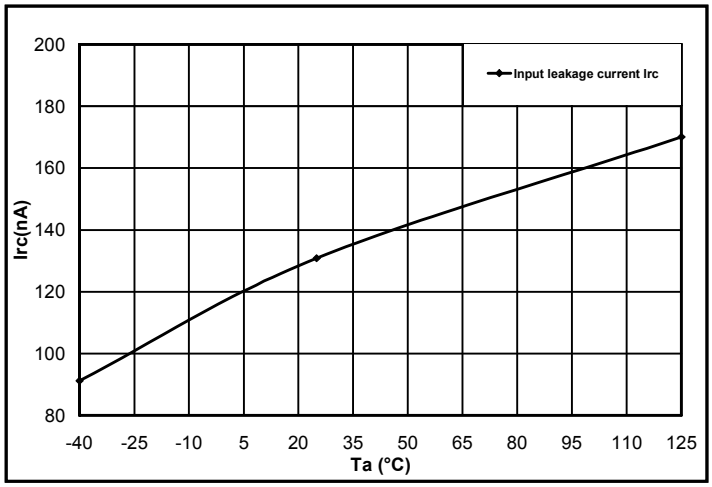
Line UVLO vs. Temperature



Oscillator Frequency vs. Temperature

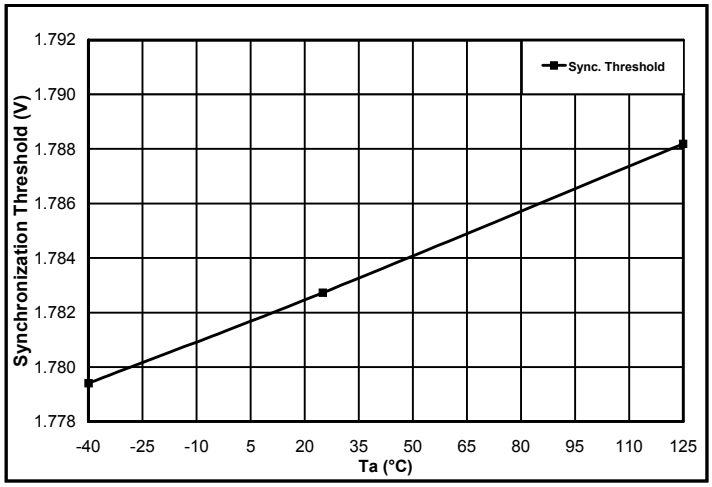


Line UVLO Hysteresis vs. Temperature

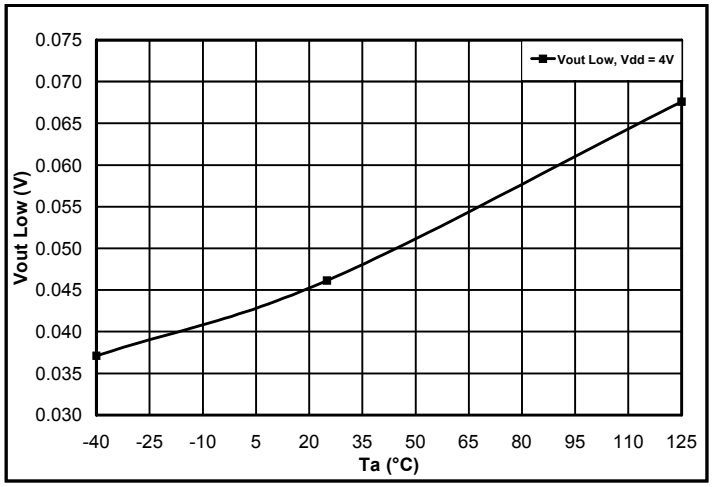


RC pin leakage current vs. Temperature

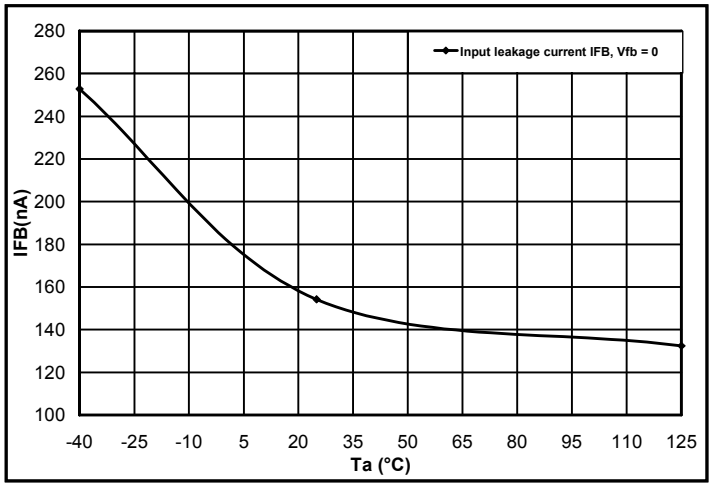
SC4905A Typical Characteristics (Cont.)



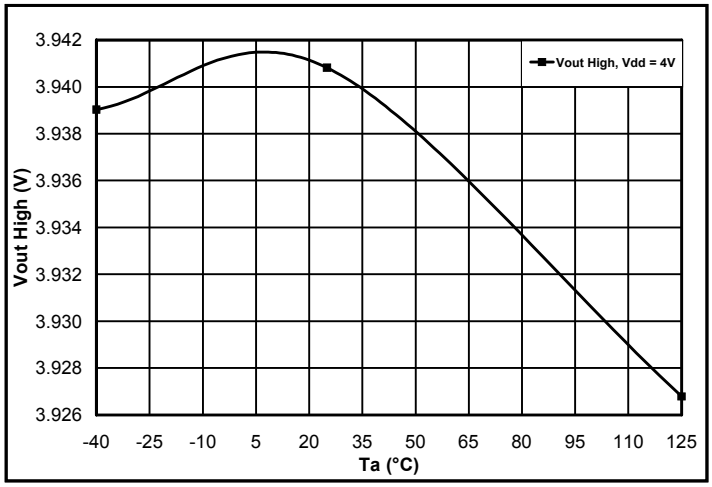
Synchronization Threshold vs. Temperature



VOUT Low vs. Temperature

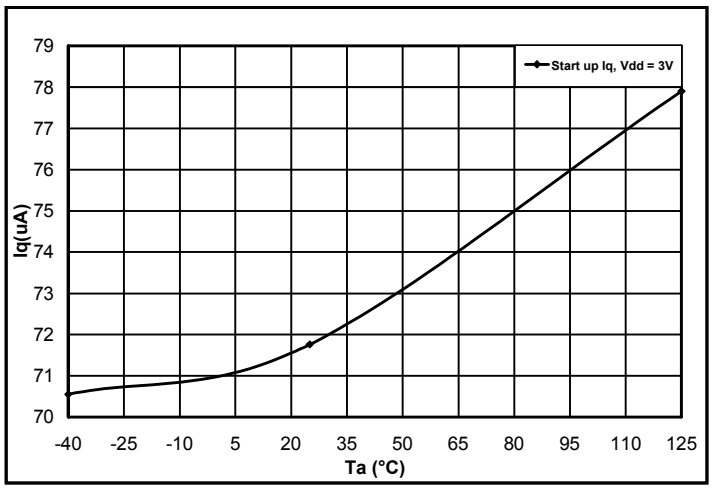


FB pin leakage current vs. Temperature

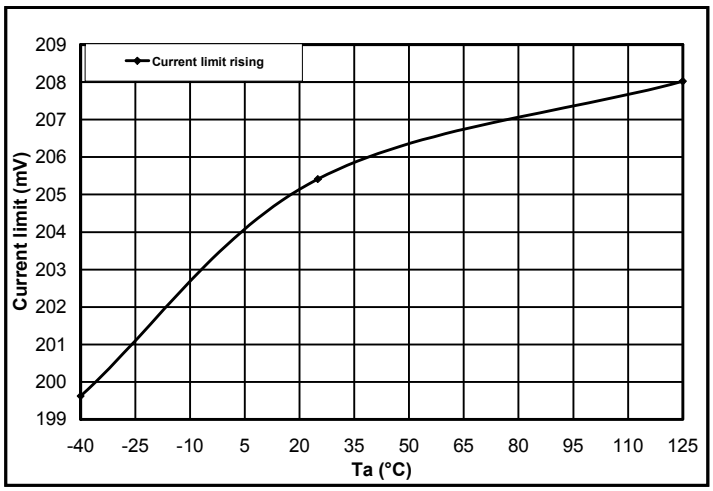


VOUT high vs. Temperature

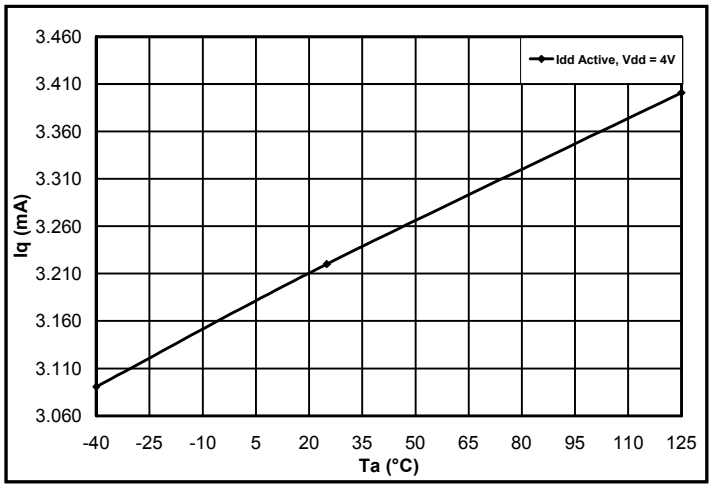
SC4905B Typical Characteristics



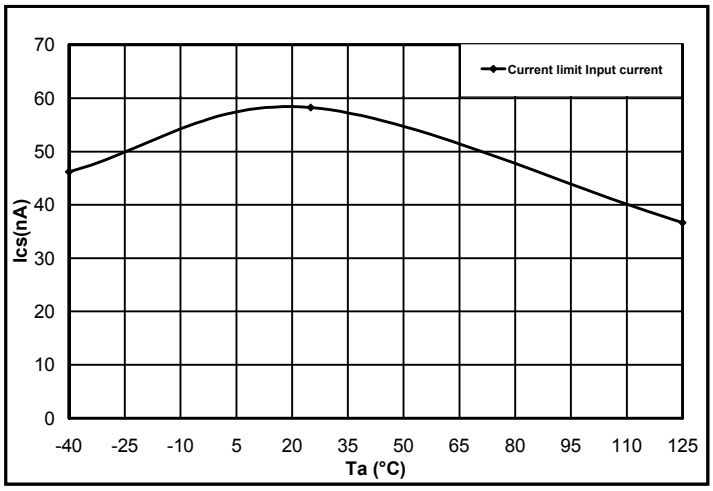
Iq (start up) vs. Temperature



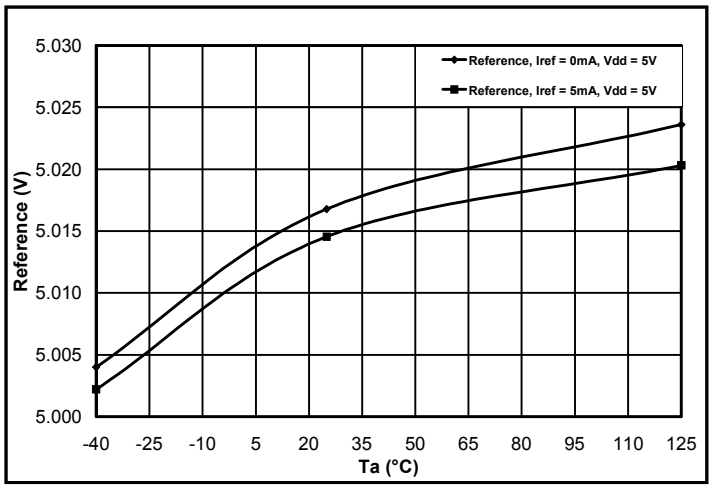
Current Limit vs. Temperature



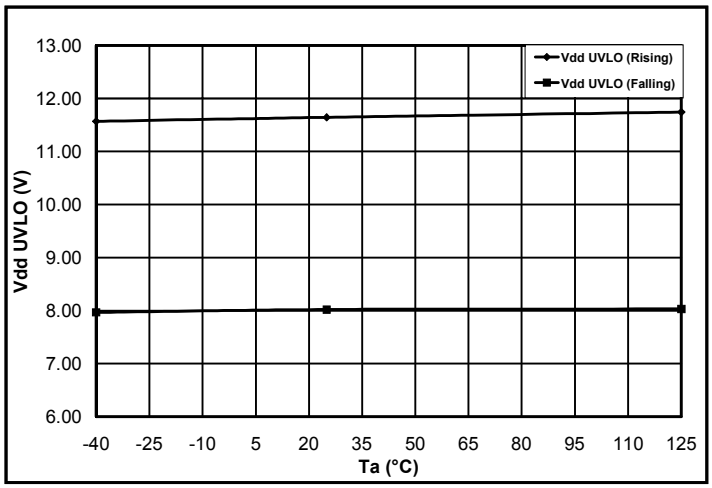
Idd (operating) vs. Temperature



Current Limit bias current vs. Temperature

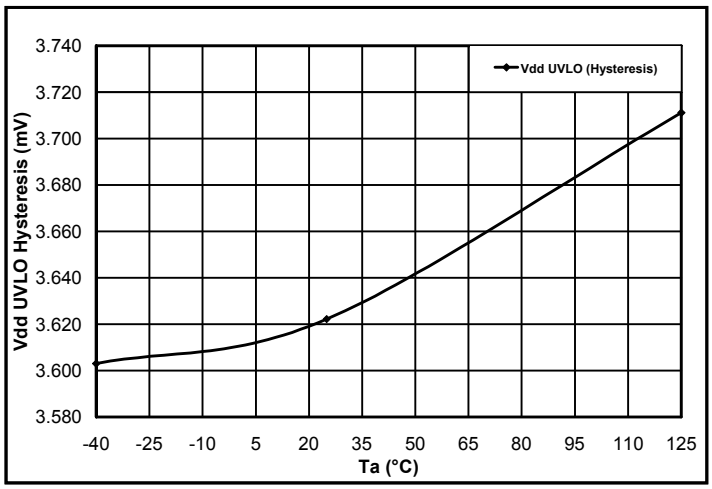


Reference vs. Temperature

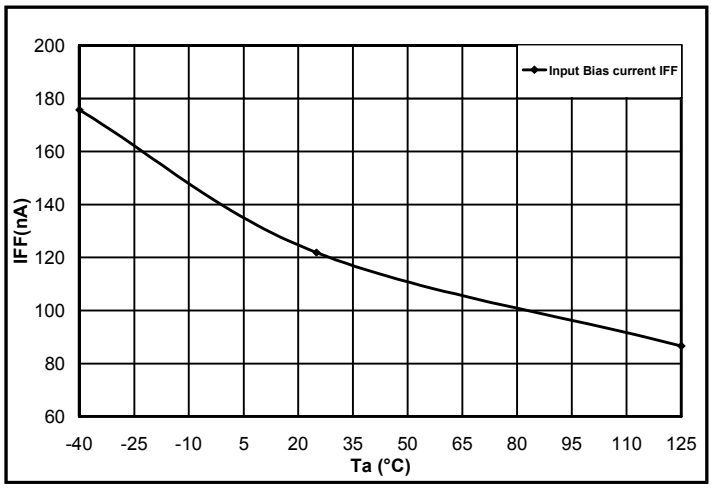


Vdd UVLO vs. Temperature

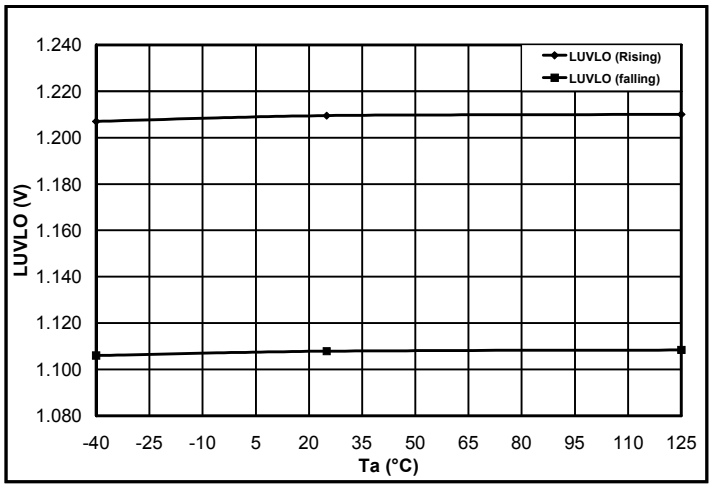
SC4905B Typical Characteristics (Cont.)



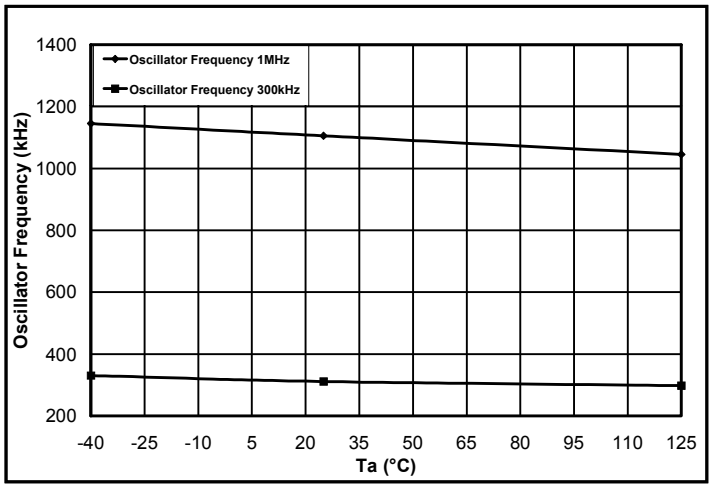
Vdd UVLO Hysteresis vs. Temperature



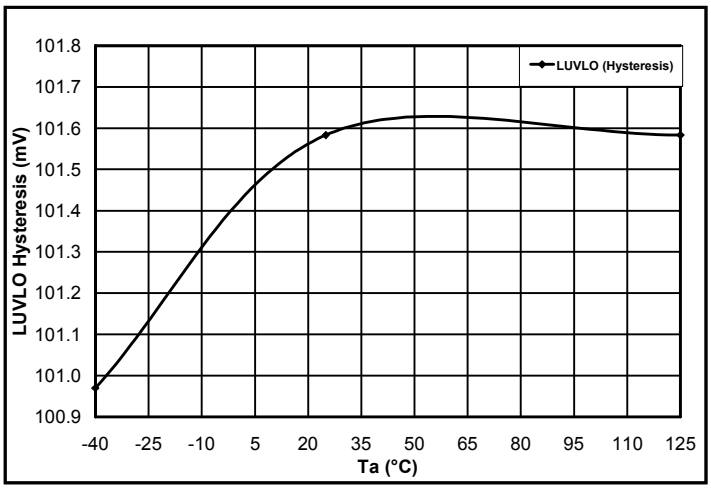
Vff pin leakage current vs. Temperature



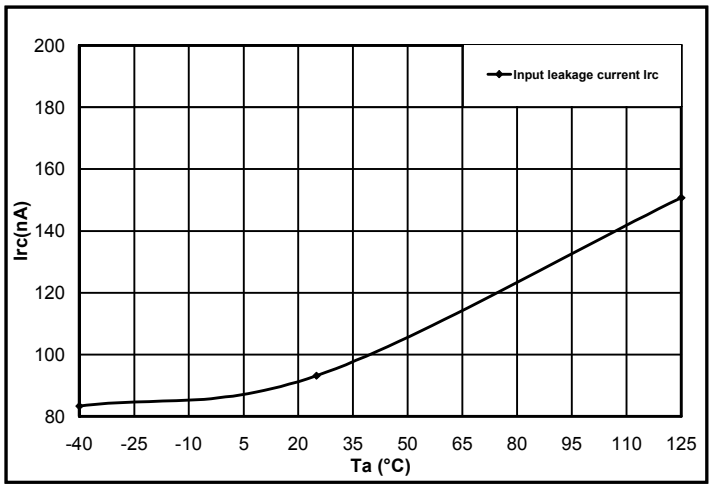
Line UVLO vs. Temperature



Oscillator Frequency vs. Temperature

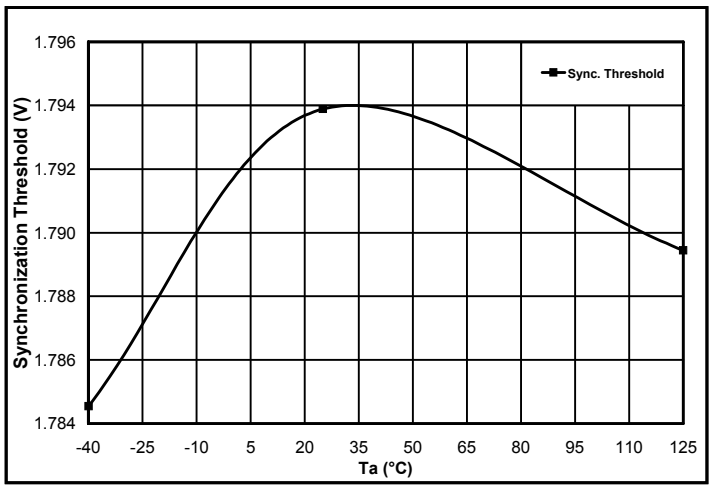


Line UVLO Hysteresis vs. Temperature

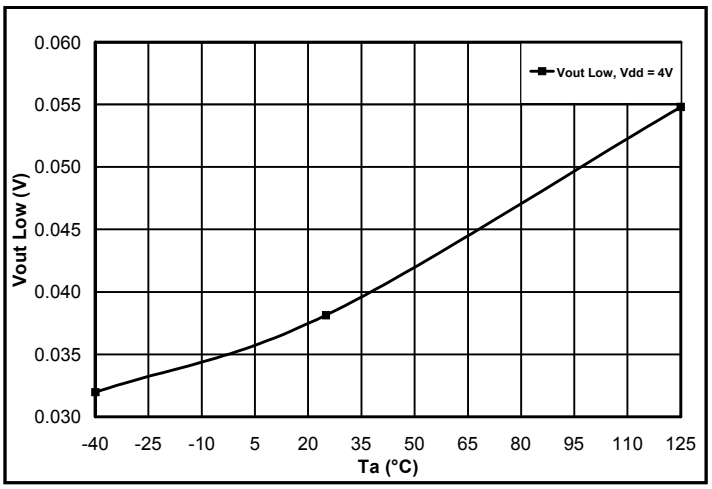


RC pin leakage current vs. Temperature

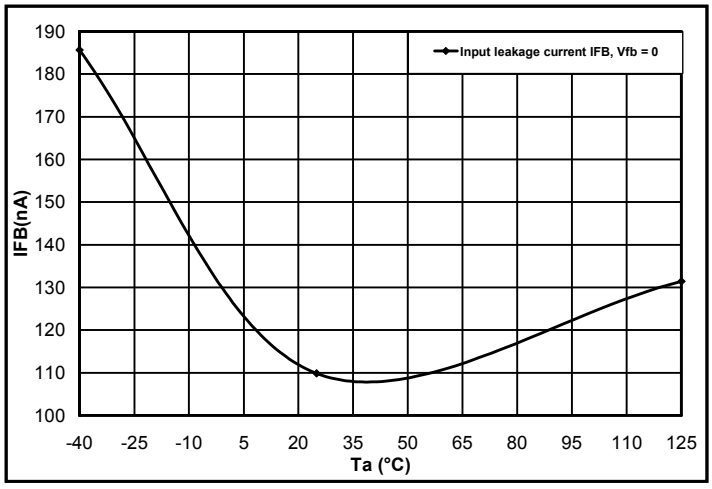
SC4905B Typical Characteristics (Cont.)



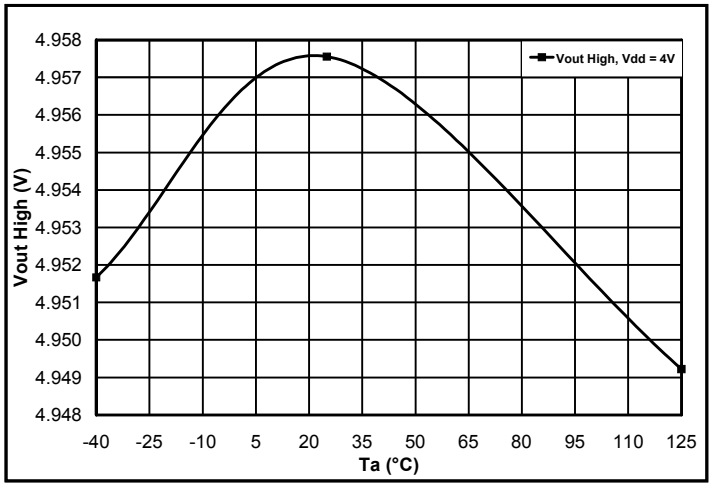
Synchronization Threshold vs. Temperature



Vout Low vs. Temperature

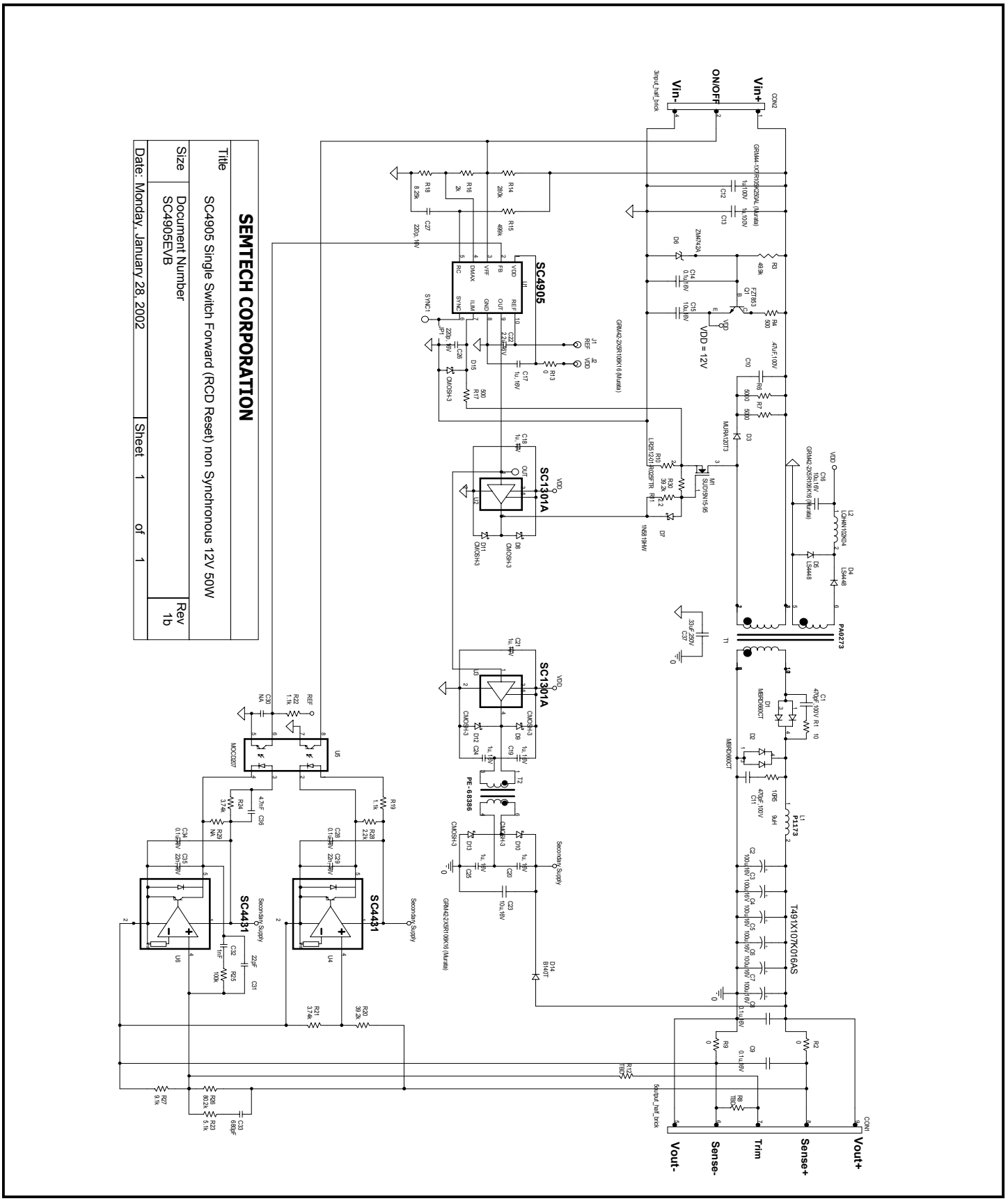


FB pin leakage current vs. Temperature



Vout high vs. Temperature

Evaluation Board Schematics

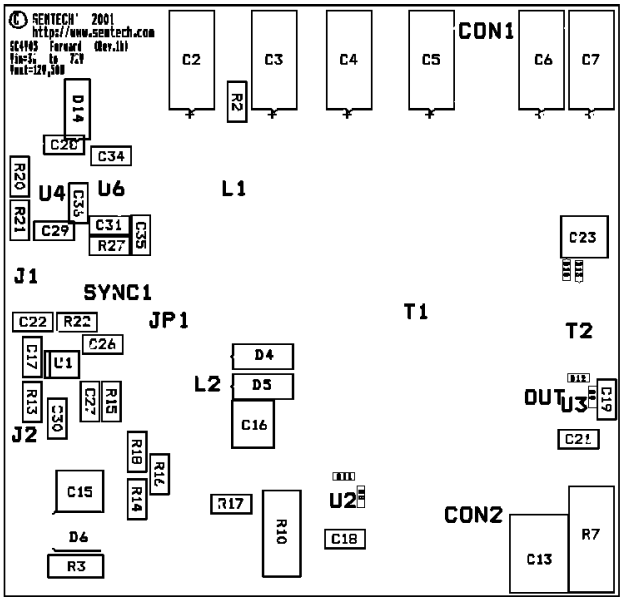


Evaluation Board Bill of Materials

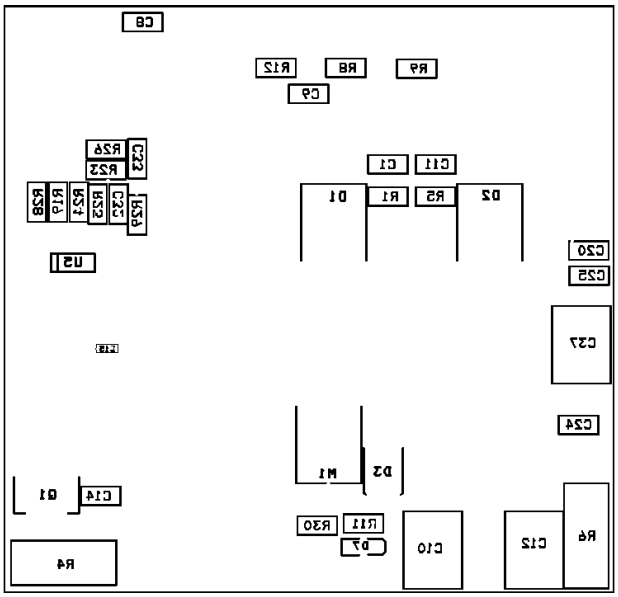
Revised: Monday, March 8, 2003
SC4905 Single Switch Forward (RCD Reset) non Synchronous 12V 50W
Bill Of Materials Revised: January 28,2002 Revision: 1b

Item	Quantity	Reference	Part	Manufacturer #	Foot Print
1	1	CON1	5output_half_brick		CON\5OUTPUT_HALF_BRICK
2	1	CON2	3input_half_brick		CON\3INPUT_HALF_BRICK
3	2	C11,C1	470pF,100V		SM/C_0805
4	6	C2,C3,C4,C5,C6,C7	100u,16V		EEJL1CD476R
5	5	C8,C9,C14,C28,C34	0.1u,16V		SM/C_0805
6	1	C10	.47uF,100V	GHM1545X7R474K250 (Murata)	SM/C_2220
7	2	C12,C13	1u,100V	GRM44-1X7R105K250AL (Murata)	SM/C_2220
8	3	C15,C16,C23	10u,16V	GRM42-2X5R106K16 (Murata)	SM/C_1210_GRM
9	7	C17,C18,C19,C20,C21,C24, C25	1u, 16V		SM/C_0805
10	1	C22	2.2u, 16V		SM/C_0805
11	2	C26,C27	220p, 16V		SM/C_0805
12	2	C29,C35	22n, 16V		SM/C_0805
13	1	C30	NA		SM/C_0805
14	1	C31	22pF		SM/C_0805
15	1	C32	1nF		SM/C_0805
16	1	C33	680pF		SM/C_0805
17	1	C36	4.7nF		SM/C_0805
18	1	C37	.33uF,250V	C4532X7R2E334K (TDK)	SM/C_2220
19	2	D1,D2	MBRD660CT		DIODE_DPAK
20	1	D3	MURA120T3		SM/DO214AA
21	2	D4,D5	LS4448		SM/DO213AC
22	1	D6	ZM4742A	ZM4742A (Diodes Inc.)	SMB/DO214
23	1	D7	1N5819HW		SOD123
24	7	D8,D9,D10,D11,D12,D13, D15	CMOSH-3	CMOSH-3 (Central Semiconductor)	SOD523
25	1	D14	B140T		SM/DO213AC
26	1	JP1	short		VIA\2P
27	1	J1	REF		ED5052
28	1	J2	VDD		ED5052
29	1	L1	9uH	P1173.123T (Pulse)	P1173
30	1	L2	LQH4N102K04	LQH4N102K04 (Murata)	SDIP0302
31	1	M1	SUD15N15-95	SUD15N15-95 (Vishay)	DPAKFET
32	1	OUT	OUT		ED5052
33	1	Q1	FZT853	FZT853 (Zetex)	SM/SOT223_BCEC
34	2	R5,R1	10		SM/R_0805
35	3	R2,R9,R13	0		SM/R_0805
36	1	R3	49.9k		SM/R_1206
37	1	R4	500	MRC1-100-5000-F-7	SM/R_1210_MCR
38	2	R6,R7	5000	MRC1-100-5001-F-7	SM/R_1210_MCR
39	2	R8,R12	TBD		SM/R_0805
40	1	R10	LR2512-01-R025FTR	LR2512-01-R025FTR (IRC)	ERJL1W
41	1	R11	2.2		SM/R_0805
42	1	R14	280k		SM/R_0805
43	1	R15	499k		SM/R_0805
44	1	R16	2k		SM/R_0805
45	1	R17	500		SM/R_0805
46	1	R18	8.25k		SM/R_0805
47	2	R22,R19	1.1k		SM/R_0805
48	2	R20,R30	39.2k		SM/R_0805
49	2	R24,R21	3.74k		SM/R_0805
50	1	R23	5.1k		SM/R_0805
51	1	R25	100k		SM/R_0805
52	1	R26	80.2k		SM/R_0805
53	1	R27	9.1k		SM/R_0805
54	1	R28	2.2k		SM/R_0805
55	1	R29	NA		SM/R_0805
56	1	SYNC1	SYNC		ED5052
57	1	T1	PA0273	PA0273 (Pulse)	PA0273
58	1	T2	PE-68386	PE-68386 (Pulse)	PE-68386
59	1	U1	SC4905	SC4905 (Semtech)	MSOP10
60	2	U2,U3	SC1301A	SC1301A (Semtech)	SOT23_5PIN
61	2	U4,U6	SC4431	SC4431 (Semtech)	SOT23_5PIN
62	1	U5	MOCD207	MOCD207(Fairchild)	SO-8

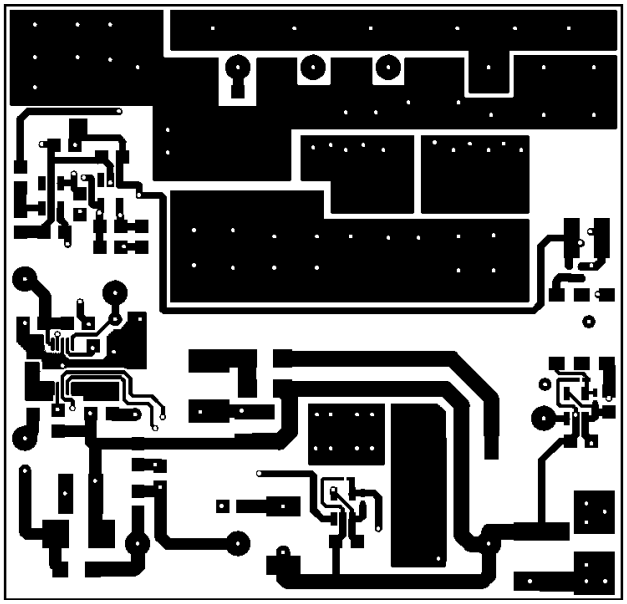
Evaluation Board Gerber Plots



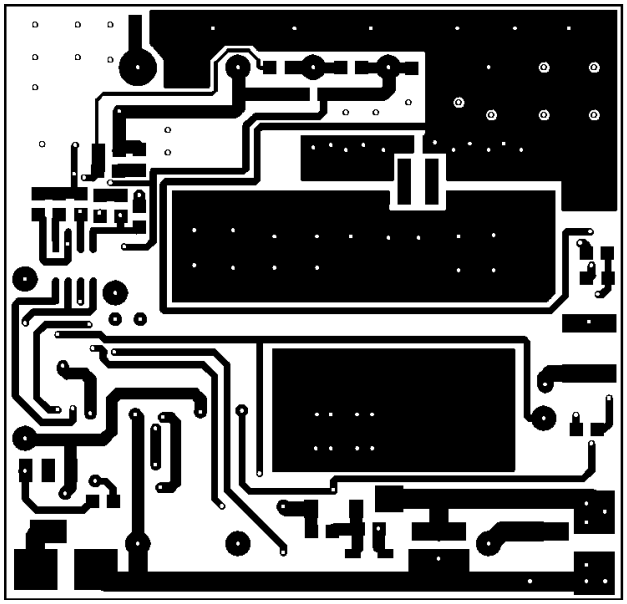
Board Layout Assembly Top



Board Layout Assembly Bottom

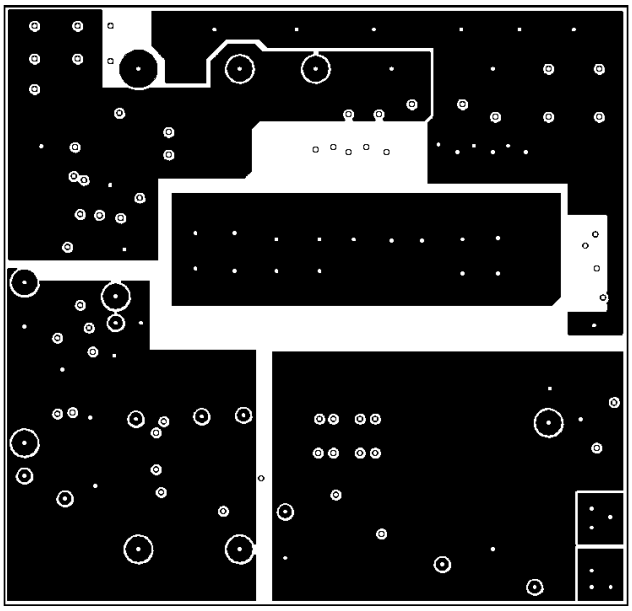


Board Layout Top

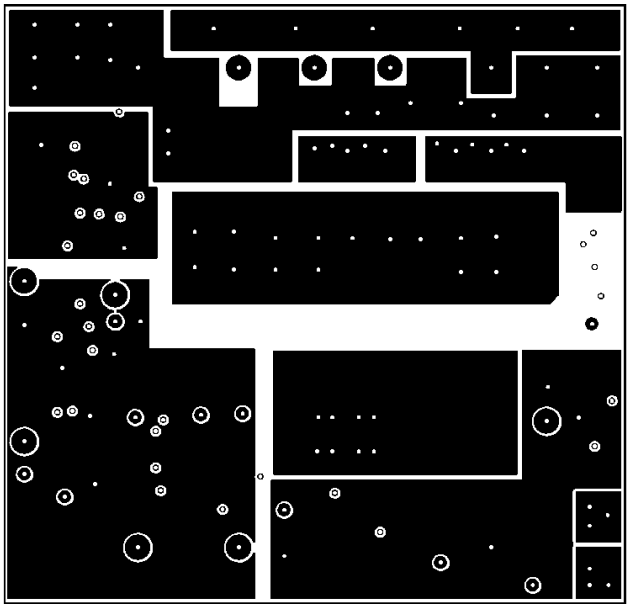


Board Layout Bottom

Evaluation Board Gerber Plots

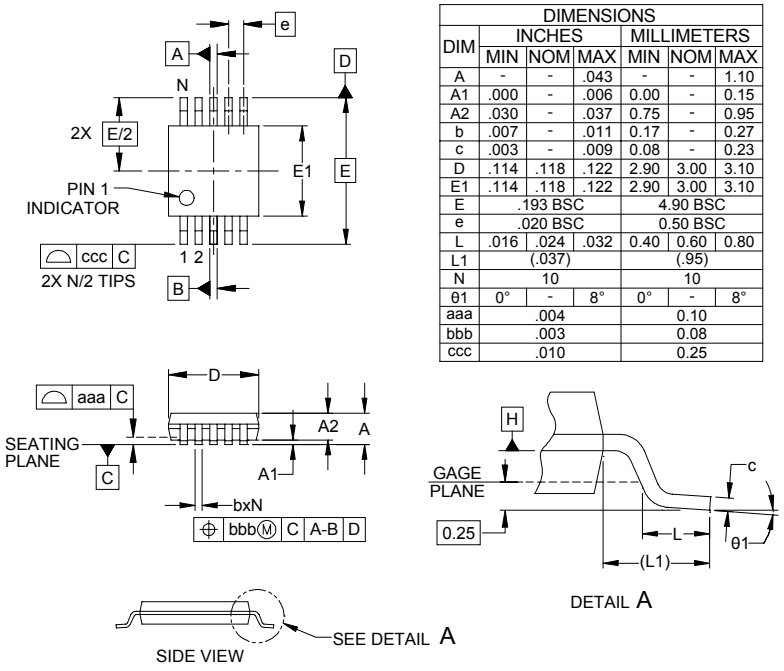


Board Layout INNER1



Board Layout INNER2

Outline Drawing - MSOP-10

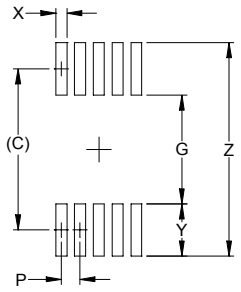


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

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- Shortage Management
- Alternative Solution
- Excess Inventory Management