



# THE DATASHEET OF STF7N52DK3

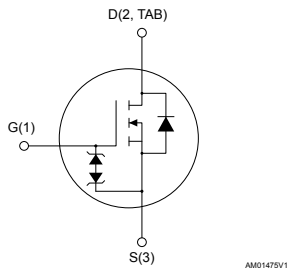


## N-channel 525 V, 0.95 $\Omega$ typ., 6 A, SuperFREDmesh3™ Power MOSFETs in DPAK and TO-220FP packages



DPAK

TO-220FP



AM01475V1

### Features

Order codes	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STD7N52DK3	525 V	1.15 $\Omega$	6 A	90 W
STF7N52DK3				25 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

These devices are developed using the revolutionary N-channel SuperFREDmesh3™ technology. They associate all advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with a fast body-drain recovery diode. Such series complements the FDmesh™ advanced technology.

#### Product status links

[STD7N52DK3](#)
[STF7N52DK3](#)

#### Product summary

##### STD7N52DK3

Order code	STD7N52DK3
Marking	7N52DK3
Package	DPAK
Packing	Tape and reel

##### STF7N52DK3

Order code	STF7N52DK3
Marking	7N52DK3
Package	TO-220FP
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$V_{DS}$	Drain-source voltage	525		V
$V_{GS}$	Gate-source voltage	±30		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	6	6 <sup>(1)</sup>	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	4	4 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	24	24 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	90	25	W
$I_{AR}^{(3)}$	Avalanche current, repetitive or non-repetitive	3		A
$E_{AS}^{(4)}$	Single pulse avalanche energy	110		mJ
$dv/dt^{(5)}$	Peak diode recovery voltage slope	20		V/ns
$di/dt^{(5)}$	Diode reverse recovery current slope	400		A/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ , $T_C = 25\text{ °C}$ )		2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150		°C
$T_J$	Operating junction temperature range			

1. This value is limited by maximum junction temperature.
2. Pulse width is limited by safe operating area.
3. Pulse width is limited by  $T_{Jmax}$ .
4. Starting  $T_J = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$
5.  $I_{SD} \leq 6\text{ A}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case	1.39	5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	°C/W

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2oz Cu board.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	525			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 525\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 525\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$		0.95	1.15	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	870	-	$\text{pF}$
$C_{oss}$	Output capacitance			70		
$C_{rss}$	Reverse transfer capacitance			13		
$C_{oss(tr)}^{(1)}$	Time-related equivalent output capacitance	$V_{DS} = 0\text{ to }420\text{ V}$ , $V_{GS} = 0\text{ V}$	-	53	-	$\text{pF}$
$C_{oss(er)}^{(2)}$	Energy-related equivalent output capacitance			74		
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 420\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 17. Test circuit for gate charge behavior)	-	33	-	$\text{nC}$
$Q_{gs}$	Gate-source charge			5		
$Q_{gd}$	Gate-drain charge			19		

1.  $C_{oss(tr)}$  is defined as the constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 420 V.

2.  $C_{oss(er)}$  is defined as the constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 420 V.

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$		12		
$t_r$	Rise time			12		
$t_{d(off)}$	Turn-off delay time	(see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	37	-	$\text{ns}$
$t_f$	Fall time			19		

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$I_{SD}$	Source-drain current		-		6	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				24		
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V	
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	110		ns	
$Q_{rr}$	Reverse recovery charge			0.44			μC
$I_{RRM}$	Reverse recovery current			8			
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ °C}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	140		ns	
$Q_{rr}$	Reverse recovery charge			0.68			μC
$I_{RRM}$	Reverse recovery current			10			

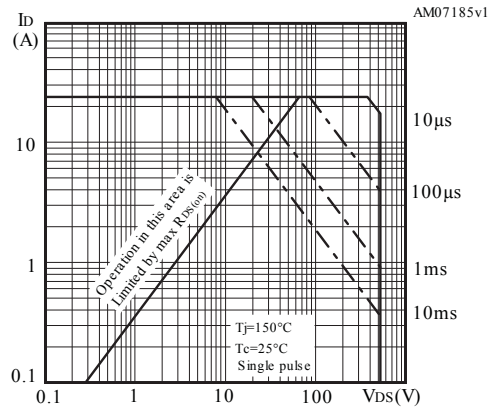
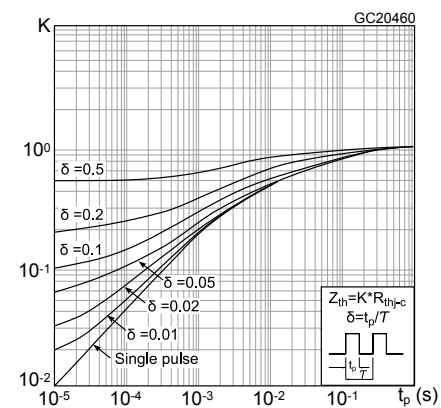
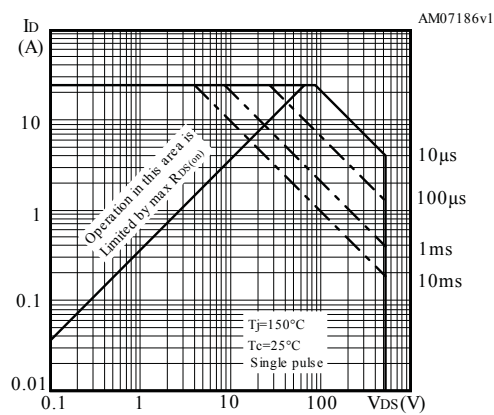
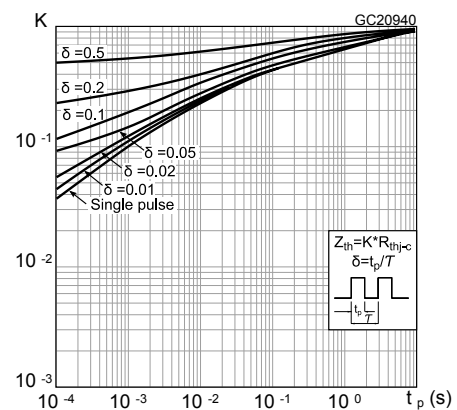
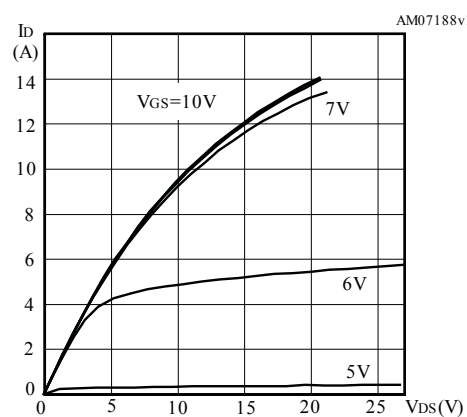
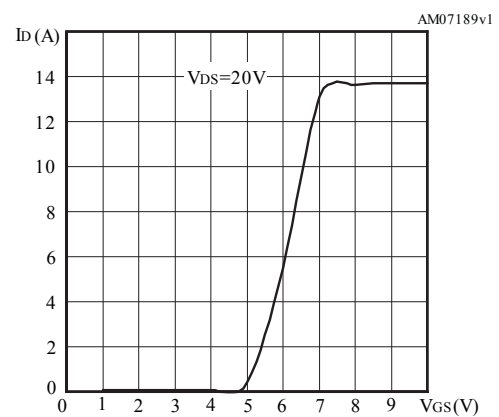
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%.

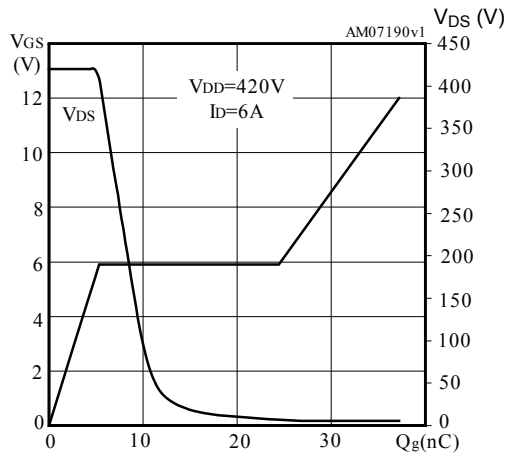
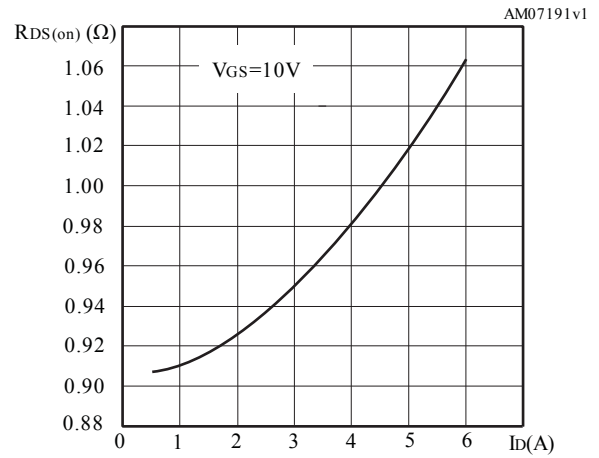
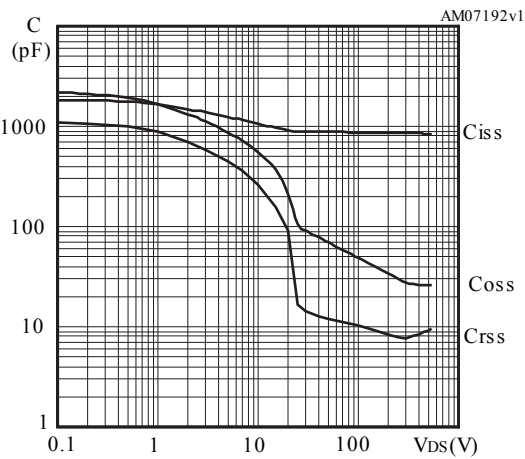
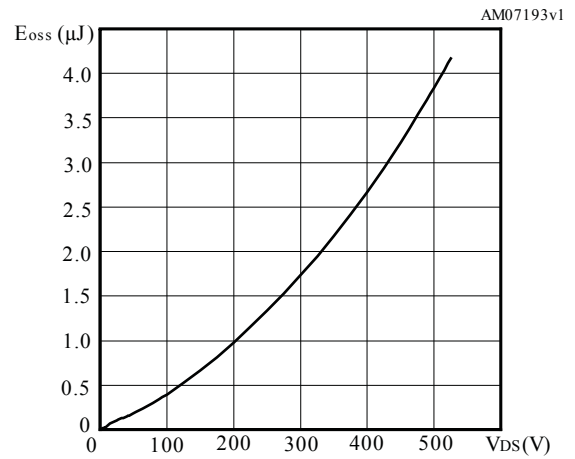
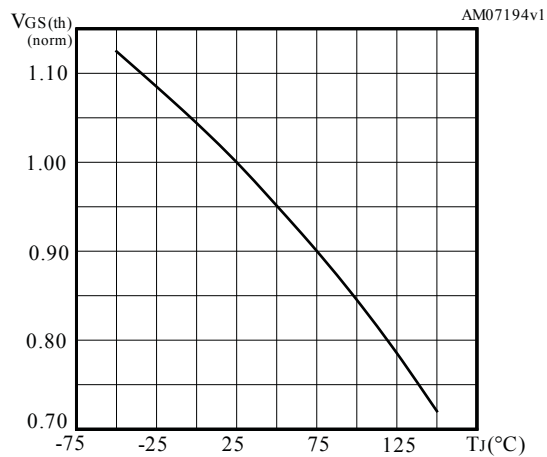
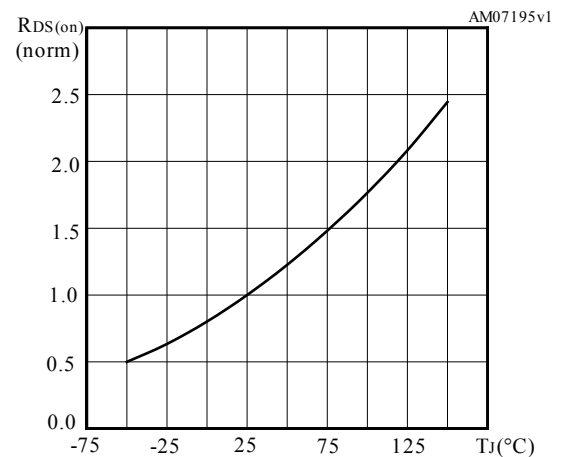
**Table 7. Gate-source Zener diode**

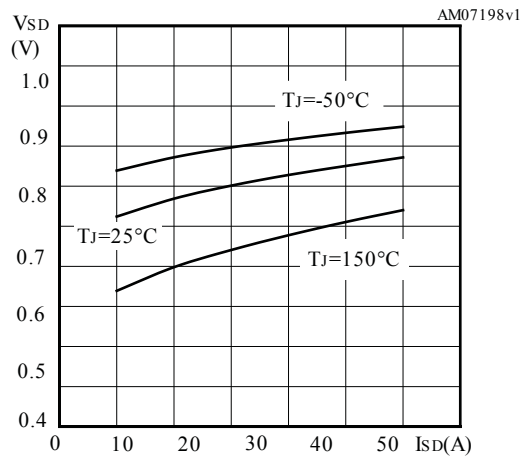
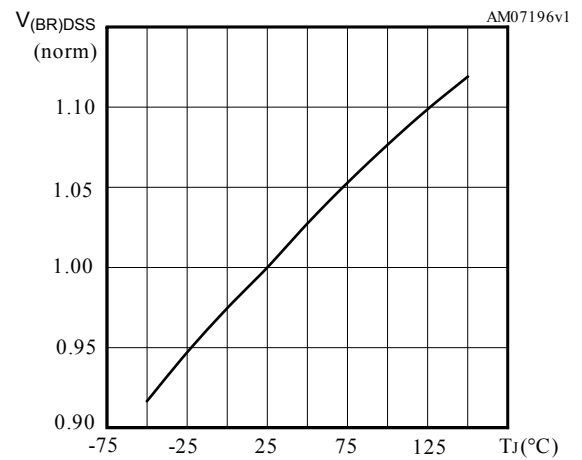
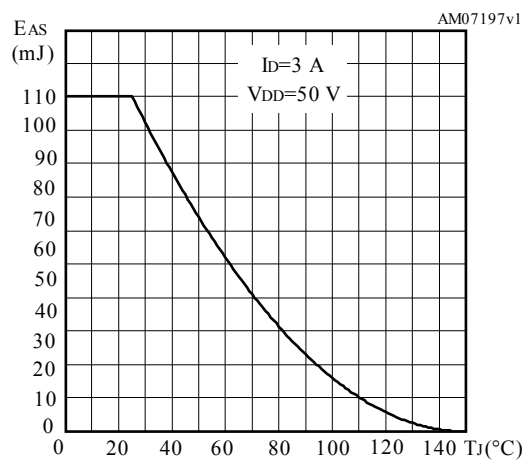
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

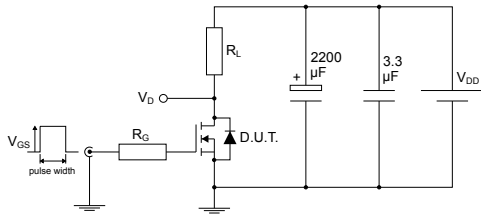
## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area for DPAK**

**Figure 2. Thermal impedance for DPAK**

**Figure 3. Safe operating area for TO-220FP**

**Figure 4. Thermal impedance for TO-220FP**

**Figure 5. Output characteristics**

**Figure 6. Transfer characteristics**


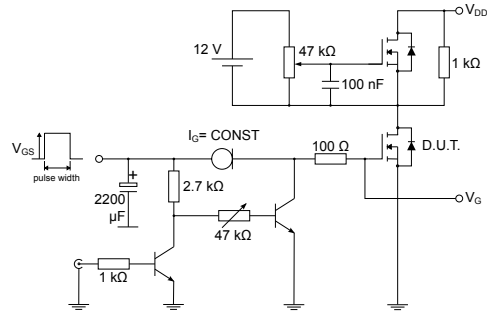
**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Static drain-source on-resistance**

**Figure 9. Capacitance variations**

**Figure 10. Output capacitance stored energy**

**Figure 11. Normalized gate threshold voltage vs temperature**

**Figure 12. Normalized on-resistance vs temperature**


**Figure 13. Source-drain diode forward characteristics**

**Figure 14. Normalized V<sub>(BR)DSS</sub> vs temperature**

**Figure 15. Maximum avalanche energy vs starting T<sub>J</sub>**


### 3 Test circuits

**Figure 16. Test circuit for resistive load switching times**


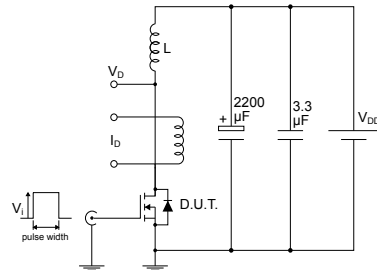
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**Figure 17. Test circuit for gate charge behavior**


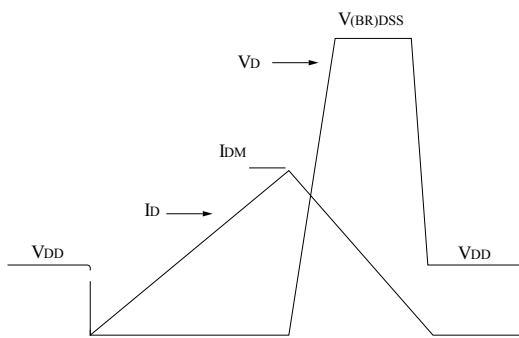
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**Figure 18. Test circuit for inductive load switching and diode recovery times**

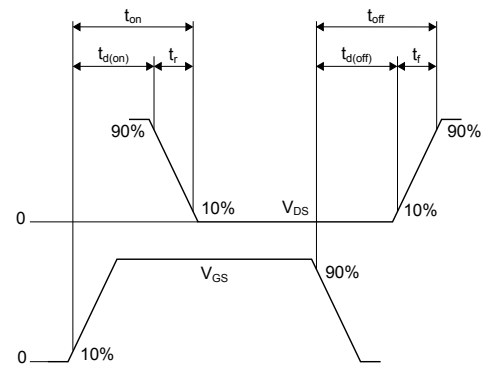

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**Figure 19. Unclamped inductive load test circuit**


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**Figure 20. Unclamped inductive waveform**


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**Figure 21. Switching time waveform**


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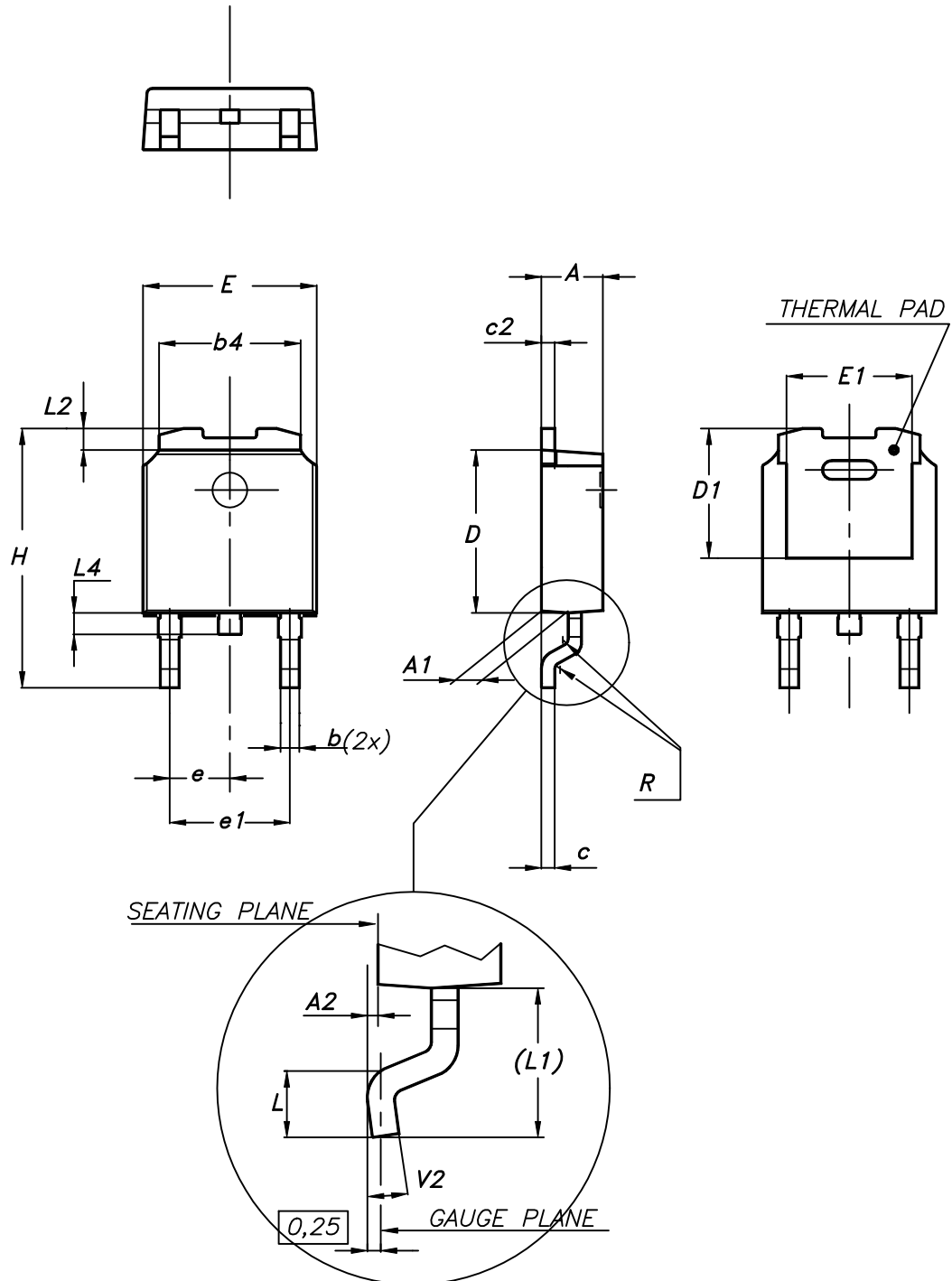
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

#### 4.1 DPAK (TO-252) type A2 package information

Figure 22. DPAK (TO-252) type A2 package outline

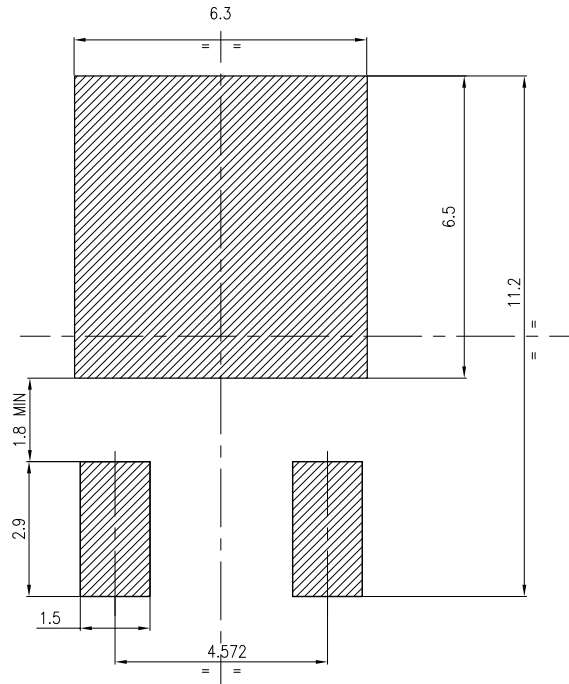


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**Table 8. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

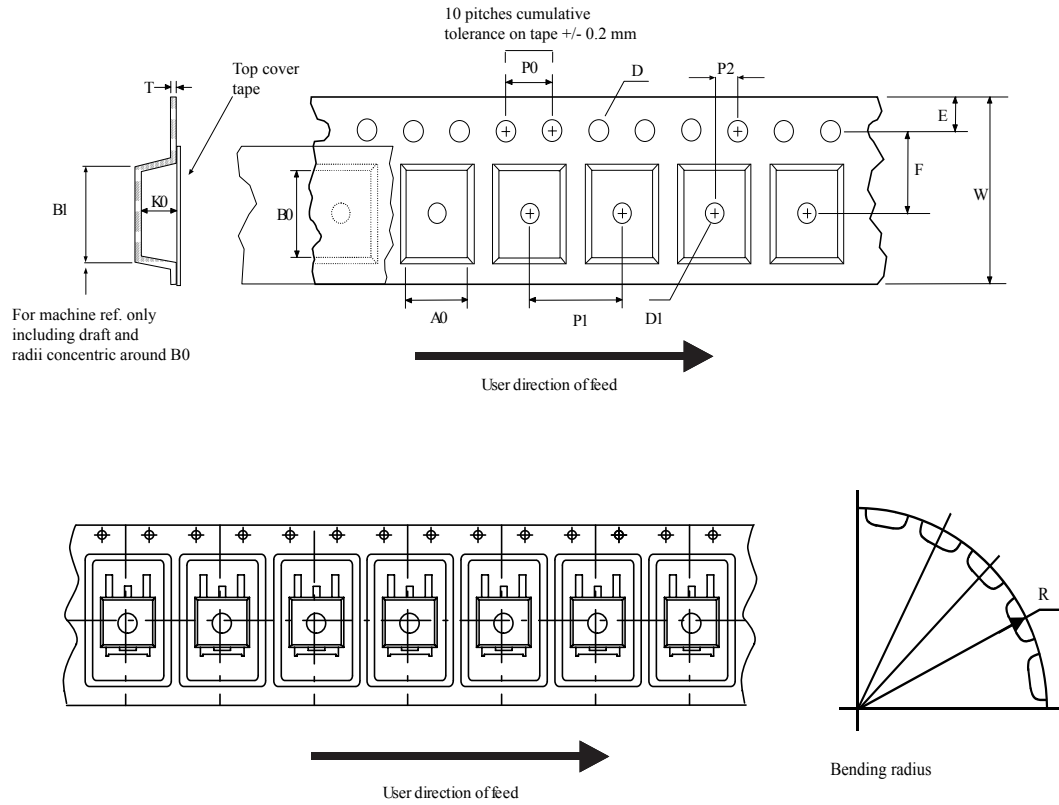
Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)



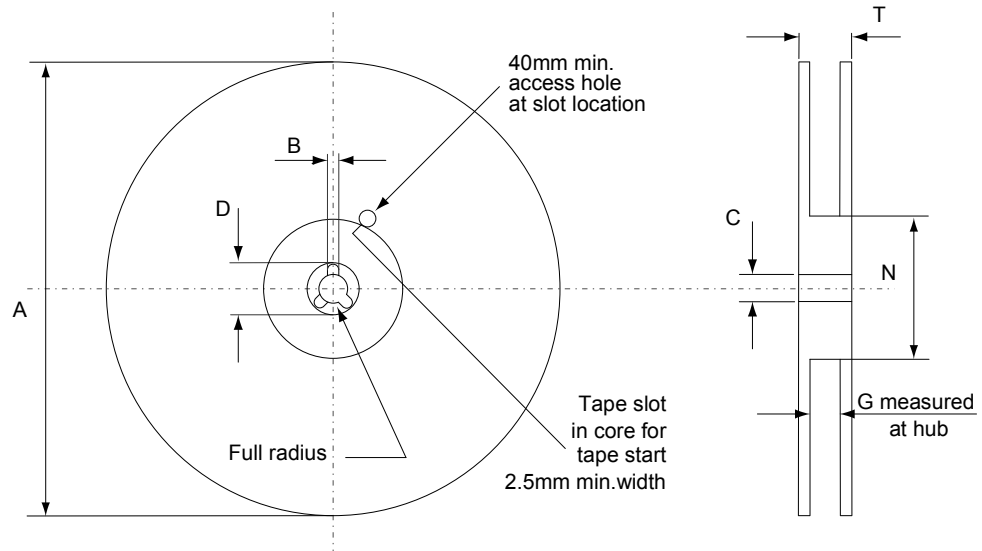
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## 4.2 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



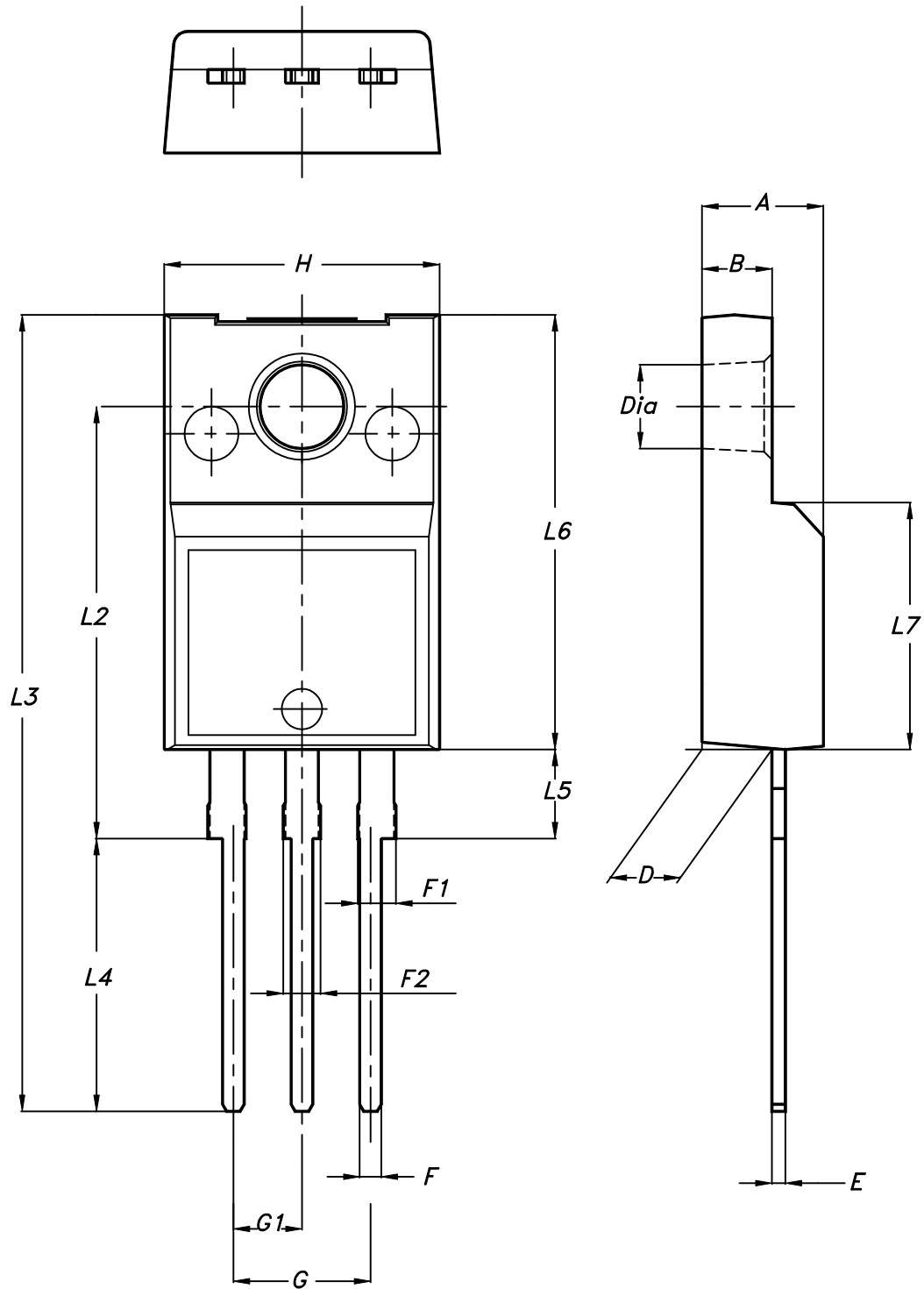
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**Figure 25. DPAK (TO-252) reel outline**


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**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

**4.3 TO-220FP package information**
**Figure 26. TO-220FP package outline**


7012510\_Rev\_12\_B

**Table 10. TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## Revision history

**Table 11. Document revision history**

Date	Version	Changes
09-Oct-2009	1	First release
20-Oct-2010	2	Document status promoted from preliminary data to datasheet
01-Oct-2018	3	The part number STP7N52DK3 has been moved to a separate datasheet and the document has been updated accordingly. Updated <a href="#">Section 4 Package information</a> . Minor text changes

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