



**THE DATASHEET OF  
BUK7277-55A,118**





# BUK7277-55A

N-channel TrenchMOS standard level FET

12 June 2014

Product data sheet

## 1. General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

## 2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

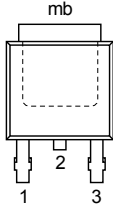
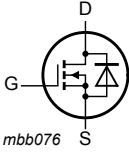
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	55	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	18	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	51	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 175\text{ °C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	-	154	m $\Omega$
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	65	77	m $\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 6\text{ A}; V_{sup} \leq 55\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	-	36	mJ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>DPAK (SOT428)</b></p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7277-55A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7277-55A	BUK7277-55A

## 8. Limiting values

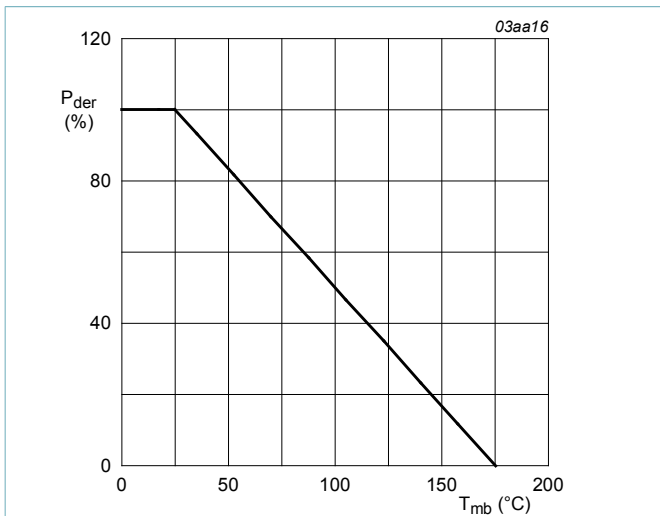
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	51	W
$I_D$	drain current	$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 2</a>	-	13	A
		$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	18	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 3</a>	[1]	73	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C

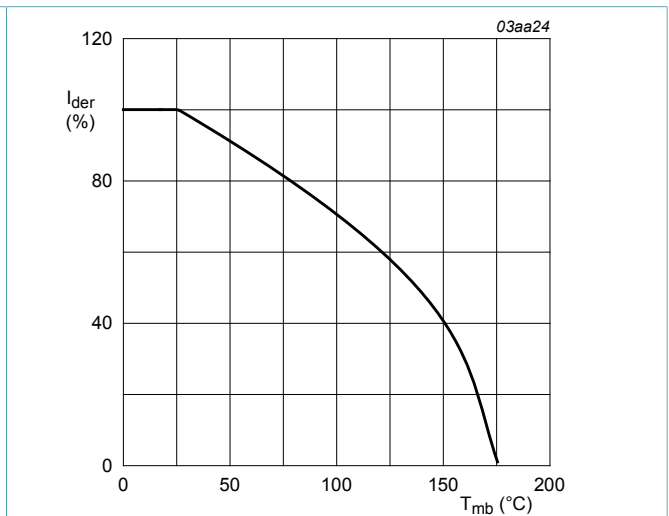
Symbol	Parameter	Conditions	Min	Max	Unit
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	18	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	73	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 6\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; unclamped	-	36	mJ

[1] Peak drain current is limited by chip, not package.



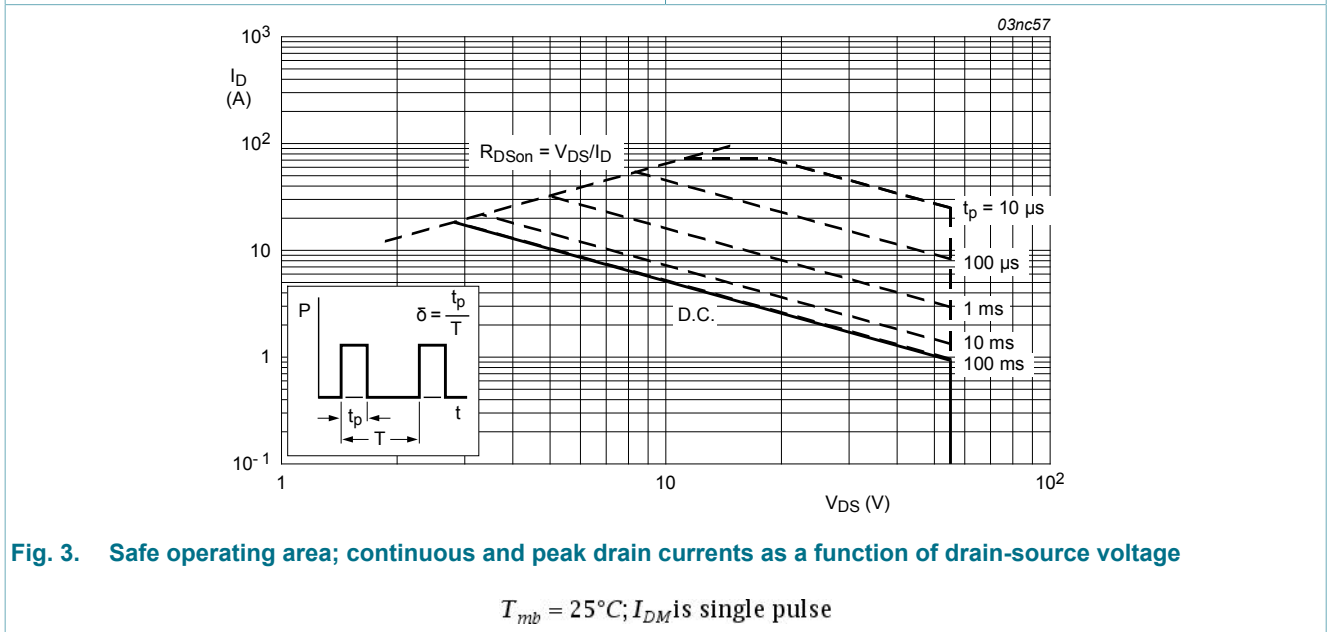
**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$



**Fig. 2. Normalized continuous drain current as a function of mounting base temperature**

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25\text{ °C}$ ;  $I_{DM}$  is single pulse

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	-	2.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	71.4	-	K/W

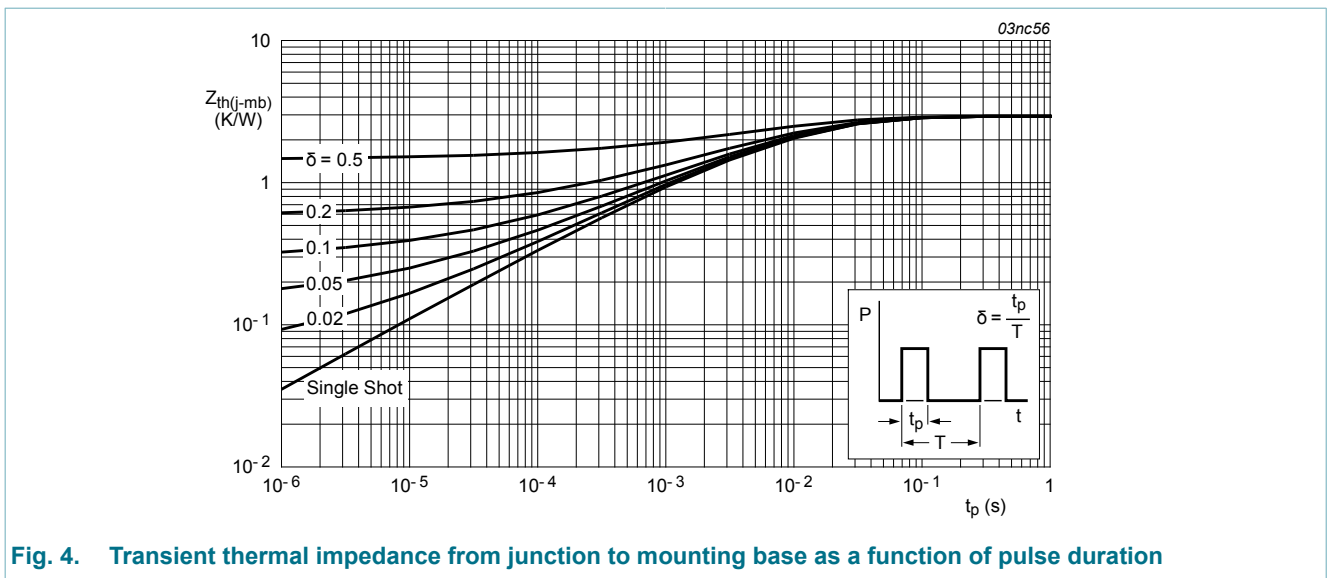


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

### 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	-	4.4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	-	154	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	65	77	mΩ
<b>Dynamic characteristics</b>						
C <sub>iSS</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a>	-	316	422	pF
C <sub>oss</sub>	output capacitance		-	92	110	pF
C <sub>rSS</sub>	reverse transfer capacitance		-	64	87	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω; T <sub>j</sub> = 25 °C	-	10	-	ns
t <sub>r</sub>	rise time		-	50	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	70	-	ns
t <sub>f</sub>	fall time		-	40	-	ns
L <sub>D</sub>	internal drain inductance	measured from drain lead from package to centre of die; T <sub>j</sub> = 25 °C	-	2.5	-	nH
L <sub>S</sub>	internal source inductance	measured from source lead from package to source bond pad; T <sub>j</sub> = 25 °C	-	7.5	-	nH
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C	-	32	-	ns
Q <sub>r</sub>	recovered charge		-	120	-	nC

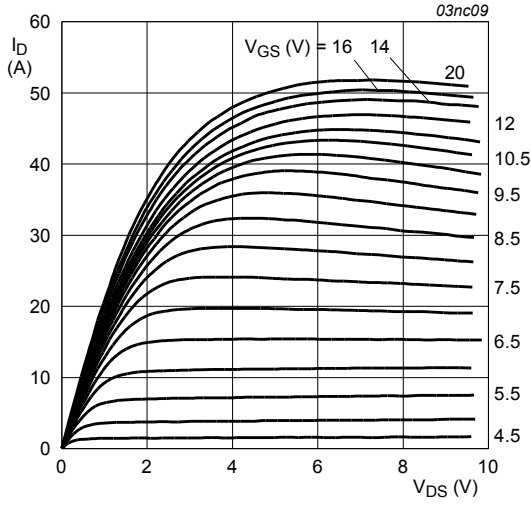


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

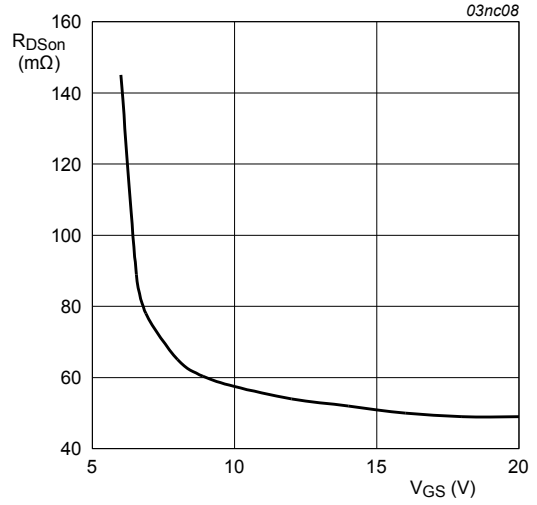


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

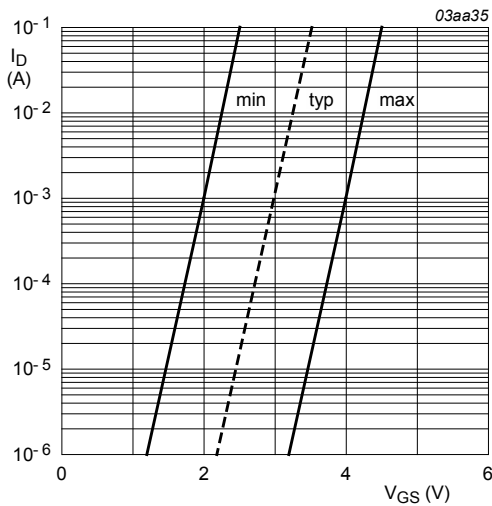


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

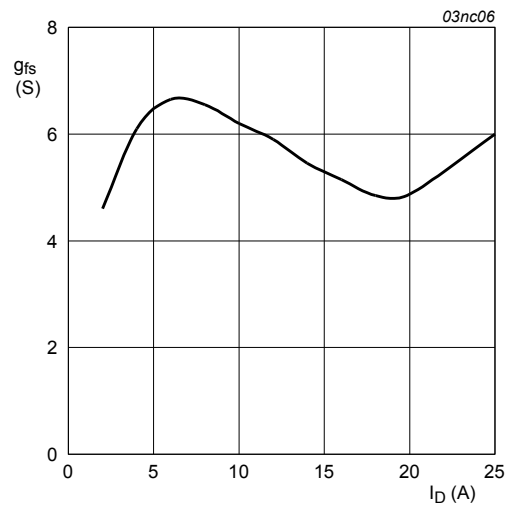


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

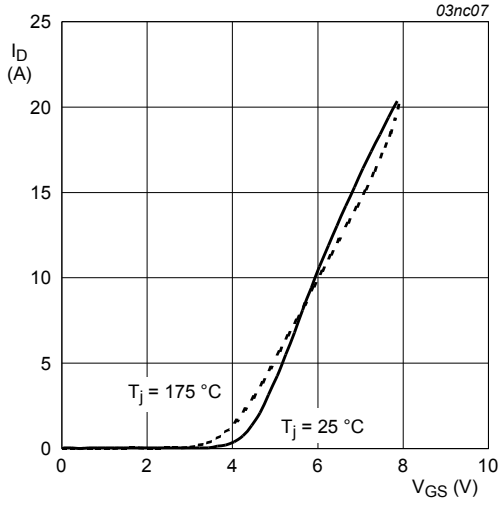


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} = 25V$$

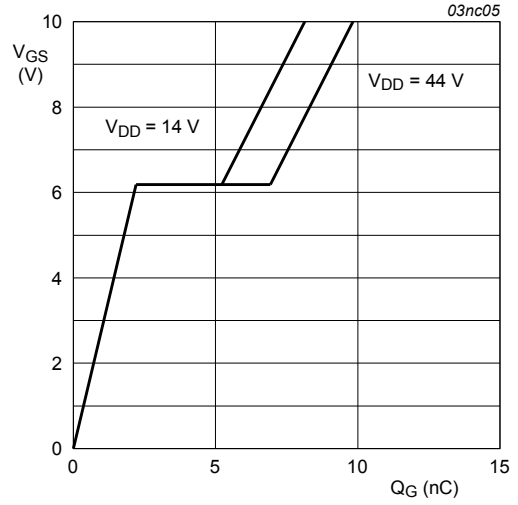


Fig. 10. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 10A$$

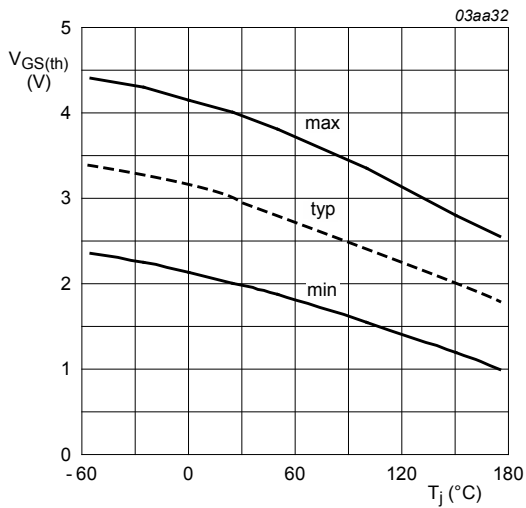


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1mA; V_{DS} = V_{GS}$$

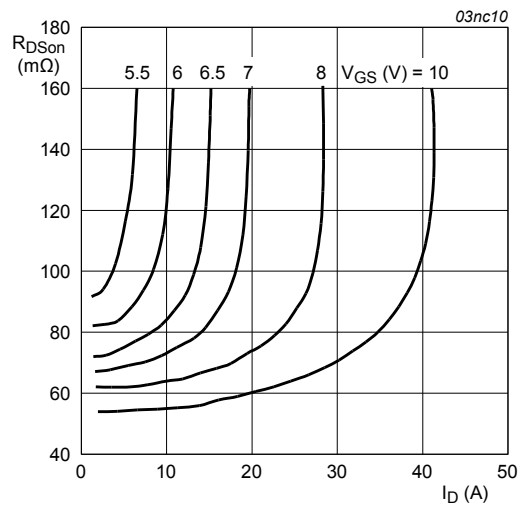
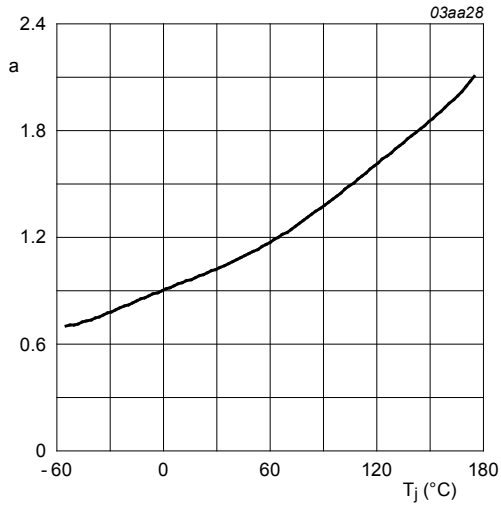


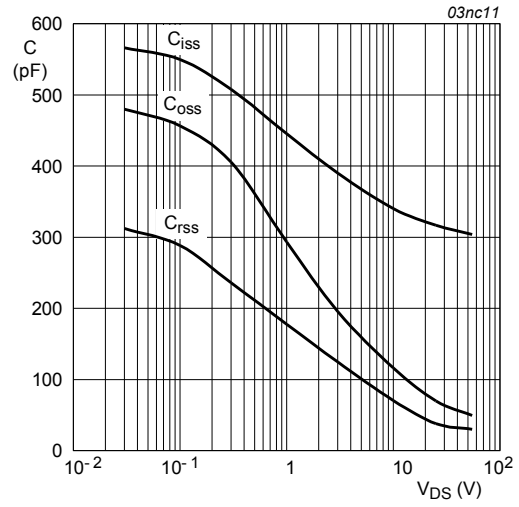
Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}C$$



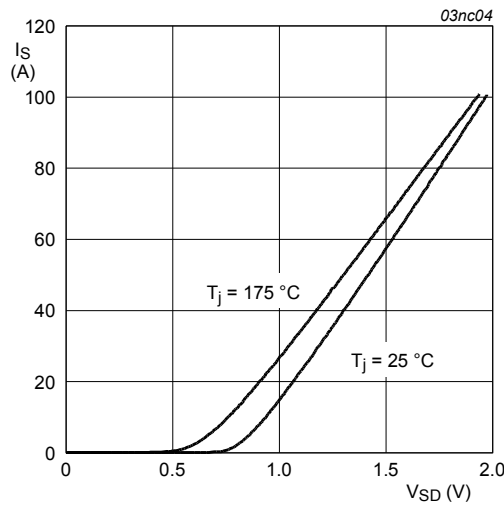
**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



**Fig. 14. Input, output and reverse capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0V; f = 1MHz$$

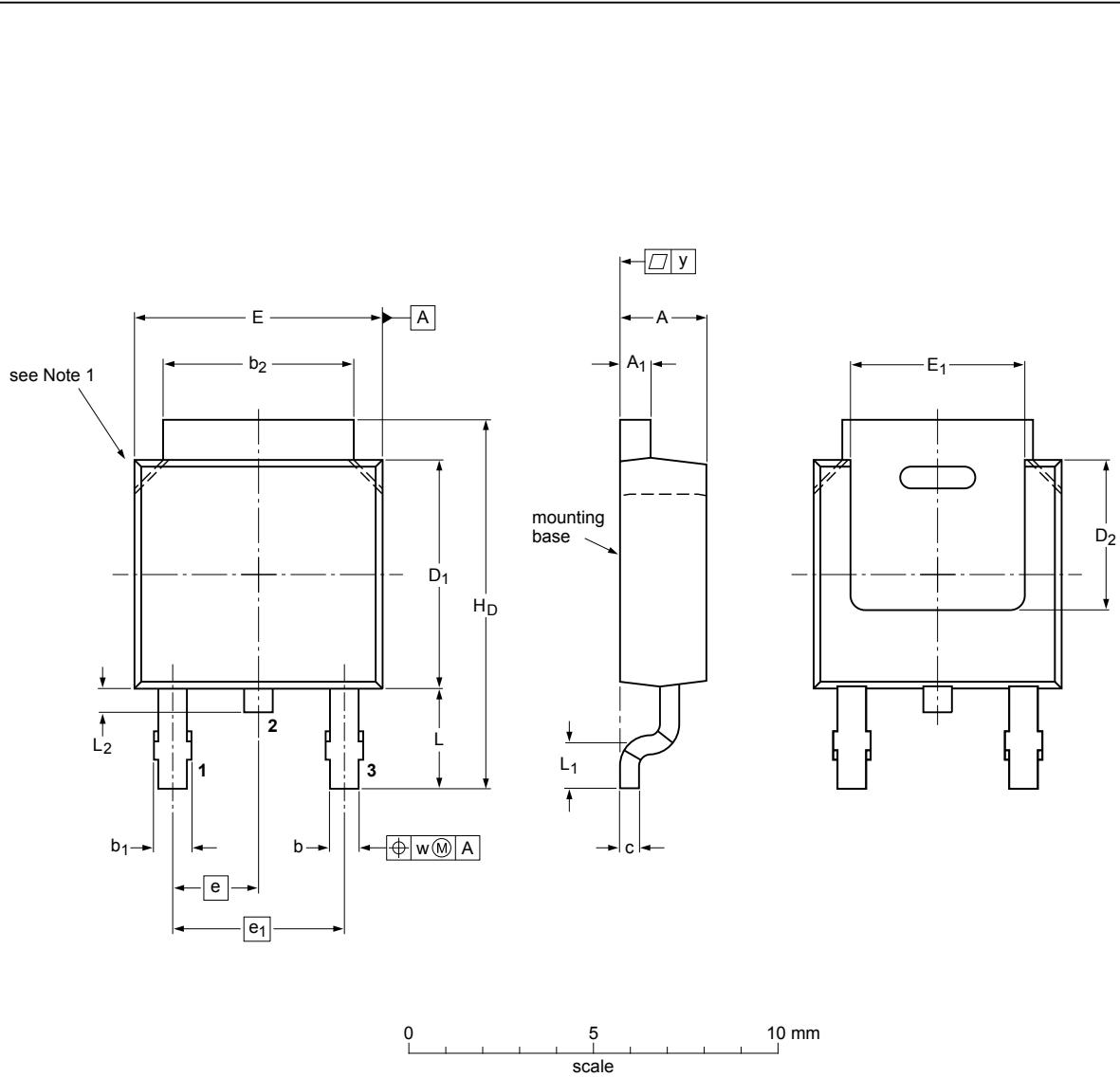


**Fig. 15. Reverse diode current as a function of reverse diode voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	H <sub>D</sub>	L	L <sub>1</sub>	L <sub>2</sub>	w	y
mm	max	2.38	0.93	0.89	1.1	5.46	0.56	6.22		6.73			10.4	2.95		0.9		0.2
	nom										2.285	4.57					0.2	
	min	2.22	0.46	0.71	0.9	5.00	0.20	5.98	4.0	6.47	4.45		9.6	2.55	0.5	0.5		

Note

1. Plastic body may have 45° chamfer.

sot428\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT428		TO-252	SC-63		06-03-16 14-06-10

Fig. 16. Package outline DPAK (SOT428)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
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