



**THE DATASHEET OF  
TPS76801QPWPREP**



# TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP TPS76828-EP, TPS76830-EP, TPS76833-EP, TPS76850-EP, TPS76801-EP FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

SGLS011B – MARCH 2003 – REVISED DECEMBER 2008

## FEATURES

- 1-A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Down to 230 mV at 1 A (TPS76850)
- Ultralow 85- $\mu$ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power Good (See TPS767xx for Power-On Reset With 200-ms Delay Option)
- 20-Pin TSSOP (PWP)PowerPAD™ Package
- Thermal Shutdown Protection

## description

This device is designed to have a fast transient response and be stable with 10- $\mu$ F low ESR capacitors. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76850) and is directly proportional to the output current. Additionally, since the PMOS pass element is a

voltage-driven device, the quiescent current is very low and independent of output loading (typically 85  $\mu$ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to  $\overline{\text{EN}}$  (enable) shuts down the regulator, reducing the quiescent current to less than 1  $\mu$ A at  $T_J = 25^\circ\text{C}$ .

Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

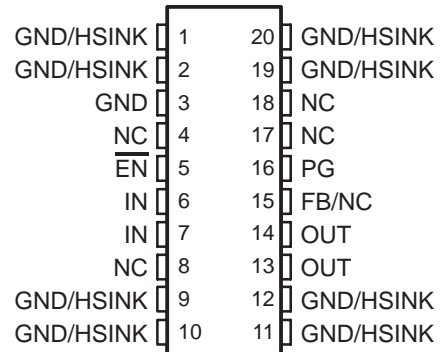
The TPS768xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS768xx family is available in a 20-pin PWP package.

## SUPPORTS DEFENSE, AEROSPACE AND MEDICAL APPLICATION

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ( $-55^\circ\text{C}/125^\circ\text{C}$ ) Temperature Range†
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

† Additional temperature ranges are available – contact factory.

### PWP PACKAGE (TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



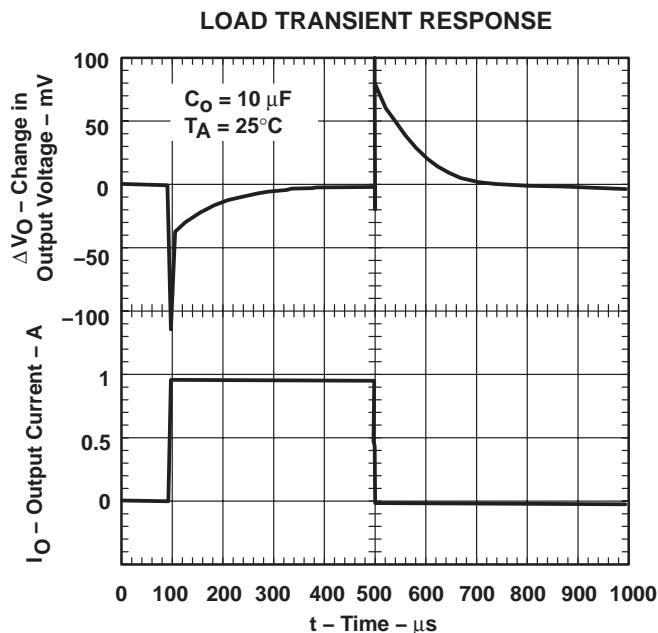
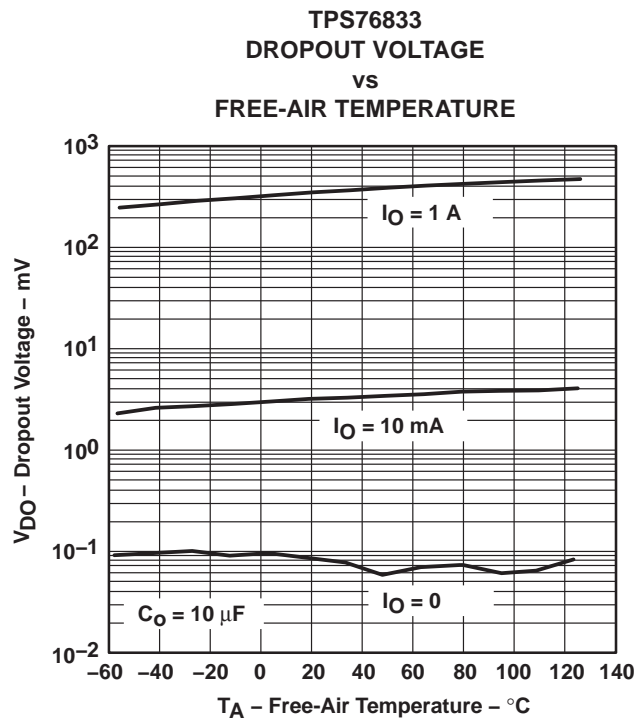
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**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP  
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description (continued)



**ORDERING INFORMATION†**

T <sub>J</sub>	OUTPUT VOLTAGE (V)	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	TYP				
-40°C to 125°C	5.0	TSSOP - PWP	Tape and reel	TPS76850QPWPREP	76850EP
	3.3			TPS76833QPWPREP	76833EP
	3.0			TPS76830QPWPREP§	76830EP§
	2.8			TPS76828QPWPREP§	76828EP§
	2.7			TPS76827QPWPREP§	76827EP§
	2.5			TPS76825QPWPREP	76825EP
	1.8			TPS76818QPWPREP	76818EP
	1.5			TPS76815QPWPREP	76815EP
	Adjustable 1.2 V to 5.5 V			TPS76801QPWPREP	76801EP
	-55°C to 125°C			Adjustable 1.2 V to 5.5 V	TSSOP - PWP
5.0		TPS76850MPWPREP	76850ME		

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ This device is Product Preview.

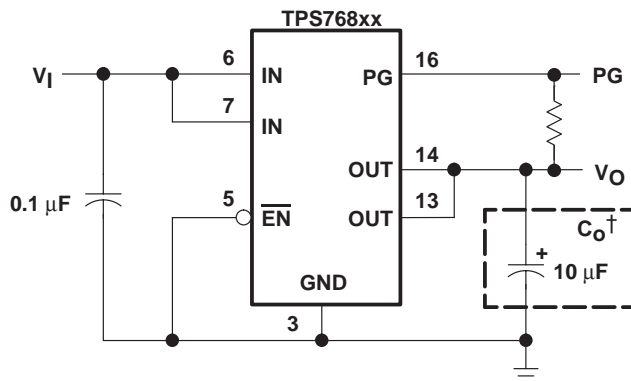
The TPS76801 is programmable using an external resistor divider (see application information). The PWP package is available taped and reeled. Note R suffix to the device type (e.g., TPS76801QPWPREP).



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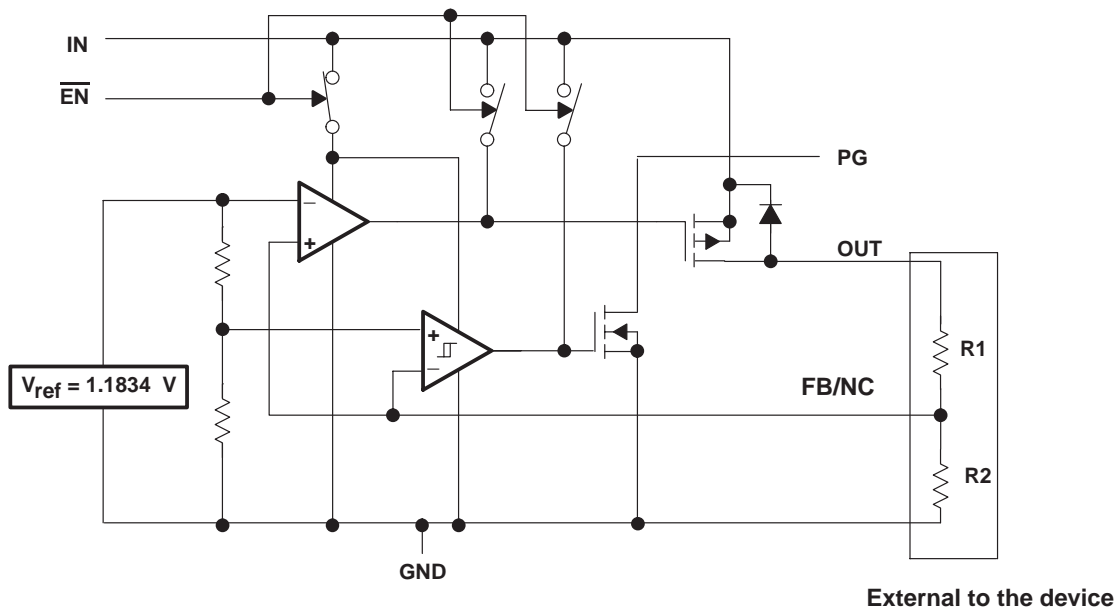
description (continued)



† See application information section for capacitor selection details.

**Figure 1. Typical Application Configuration (For Fixed Output Options)**

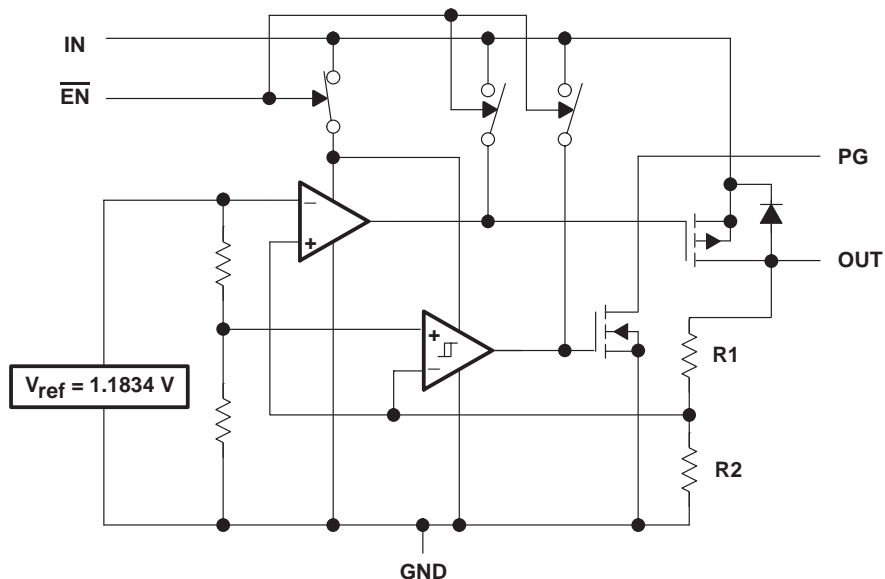
functional block diagram—adjustable version



**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP  
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**functional block diagram—fixed-voltage version**



**Terminal Functions**

**PWP Package**

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND/HSINK	1		Ground/heatsink
GND/HSINK	2		Ground/heatsink
GND	3		LDO ground
NC	4		No connect
$\overline{\text{EN}}$	5	I	Enable input
IN	6	I	Input
IN	7	I	Input
NC	8		No connect
GND/HSINK	9		Ground/heatsink
GND/HSINK	10		Ground/heatsink
GND/HSINK	11		Ground/heatsink
GND/HSINK	12		Ground/heatsink
OUT	13	O	Regulated output voltage
OUT	14	O	Regulated output voltage
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
PG	16	O	PG output
NC	17		No connect
NC	18		No connect
GND/HSINK	19		Ground/heatsink
GND/HSINK	20		Ground/heatsink

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Input voltage range <sup>‡</sup> , $V_I$ .....	-0.3 V to 13.5 V
Voltage range at $\overline{EN}$ .....	-0.3 V to $V_I + 0.3$ V
Maximum PG voltage .....	16.5 V
Peak output current .....	Internally limited
Continuous total power dissipation .....	See dissipation rating table
Output voltage, $V_O$ (OUT, FB) .....	7 V
Operating virtual junction temperature range, $T_J$ .....	-40°C to 125°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
ESD rating, HBM .....	2 kV

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup> All voltage values are with respect to network terminal ground.

**DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES**

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP <sup>§</sup>	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP <sup>¶</sup>	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

<sup>§</sup> This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in<sup>2</sup>).

<sup>¶</sup> This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in<sup>2</sup>) and layers 3 and 6 at 100% coverage (6 in<sup>2</sup>). For more information, refer to TI technical brief SLMA002.

**recommended operating conditions**

	MIN	MAX	UNIT
Input voltage, $V_I$ <sup>#</sup>	2.7	10	V
Output voltage range, $V_O$	1.2	5.5	V
Output current, $I_O$ (see Note 1)	0	1.0	A
Operating virtual junction temperature, $T_J$ (see Note 1)	-40	125	°C

<sup>#</sup> To calculate the minimum input voltage for your maximum output current, use the following equation:  $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$ .

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



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electrical characteristics over recommended operating free-air temperature range,  
 $V_I = V_O(\text{typ}) + 1 \text{ V}$ ,  $I_O = 1 \text{ mA}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 10 \mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 $\mu\text{A}$ to 1 A load) (see Note 2)	TPS76801	$5.5 \text{ V} \geq V_O \geq 1.5 \text{ V}$ , $T_J = 25^\circ\text{C}$	$V_O$			V
		$5.5 \text{ V} \geq V_O \geq 1.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	$0.98V_O$	$1.02V_O$		
	TPS76815	$T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.5			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.470	1.530		
	TPS76818	$T_J = 25^\circ\text{C}$ , $2.8 \text{ V} < V_{IN} < 10 \text{ V}$	1.8			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.8 \text{ V} < V_{IN} < 10 \text{ V}$	1.764	1.836		
	TPS76825	$T_J = 25^\circ\text{C}$ , $3.5 \text{ V} < V_{IN} < 10 \text{ V}$	2.5			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.5 \text{ V} < V_{IN} < 10 \text{ V}$	2.450	2.550		
	TPS76827	$T_J = 25^\circ\text{C}$ , $3.7 \text{ V} < V_{IN} < 10 \text{ V}$	2.7			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.7 \text{ V} < V_{IN} < 10 \text{ V}$	2.646	2.754		
	TPS76828	$T_J = 25^\circ\text{C}$ , $3.8 \text{ V} < V_{IN} < 10 \text{ V}$	2.8			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.8 \text{ V} < V_{IN} < 10 \text{ V}$	2.744	2.856		
	TPS76830	$T_J = 25^\circ\text{C}$ , $4 \text{ V} < V_{IN} < 10 \text{ V}$	3.0			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $4 \text{ V} < V_{IN} < 10 \text{ V}$	2.940	3.060		
	TPS76833	$T_J = 25^\circ\text{C}$ , $4.3 \text{ V} < V_{IN} < 10 \text{ V}$	3.3			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $4.3 \text{ V} < V_{IN} < 10 \text{ V}$	3.234	3.366		
	TPS76850	$T_J = 25^\circ\text{C}$ , $6 \text{ V} < V_{IN} < 10 \text{ V}$	5.0			
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $6 \text{ V} < V_{IN} < 10 \text{ V}$	4.900	5.100		
Quiescent current (GND current) $\overline{\text{EN}} = 0 \text{ V}$ , (see Note 2)		$10 \mu\text{A} < I_O < 1 \text{ A}$ , $T_J = 25^\circ\text{C}$	85			$\mu\text{A}$
		$I_O = 1 \text{ A}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	125			
Output voltage line regulation ( $\Delta V_O/V_O$ ) (see Notes 2 and 3)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$ , $T_J = 25^\circ\text{C}$	0.01			%/V
Load regulation			3			mV
Output noise voltage (TPS76818)		$\text{BW} = 200 \text{ Hz}$ to $100 \text{ kHz}$ , $C_O = 10 \mu\text{F}$ , $I_C = 1 \text{ A}$ , $T_J = 25^\circ\text{C}$	55			$\mu\text{V}_{\text{rms}}$
Output current limit		$V_O = 0 \text{ V}$	1.7	2		A
Thermal shutdown junction temperature			150			$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_I$ , $T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_I < 10 \text{ V}$	1			$\mu\text{A}$
		$\overline{\text{EN}} = V_I$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.7 \text{ V} < V_I < 10 \text{ V}$	10			$\mu\text{A}$
FB input current	TPS76801	$\text{FB} = 1.5 \text{ V}$	2			nA
High level enable input voltage			1.7			V
Low level enable input voltage			0.9			V
Power supply ripple rejection (see Note 2)		$f = 1 \text{ KHz}$ , $T_J = 25^\circ\text{C}$	$C_O = 10 \mu\text{F}$ , 60			dB

NOTES: 2. Minimum IN operating voltage is 2.7 V or  $V_O(\text{typ}) + 1 \text{ V}$ , whichever is greater. Maximum IN voltage 10 V.  
 3. If  $V_O \leq 1.8 \text{ V}$  then  $V_{I\text{max}} = 10 \text{ V}$ ,  $V_{I\text{min}} = 2.7 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{I\text{max}} - 2.7 \text{ V})}{100} \times 1000$$

If  $V_O \geq 2.5 \text{ V}$  then  $V_{I\text{max}} = 10 \text{ V}$ ,  $V_{I\text{min}} = V_O + 1 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{I\text{max}} - (V_O + 1 \text{ V}))}{100} \times 1000$$



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electrical characteristics over recommended operating free-air temperature range,  
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 1 \text{ mA}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 10 \mu\text{F}$  (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG	Minimum input voltage for valid PG	$I_{O(\text{PG})} = 300 \mu\text{A}$		1.1		V
	Trip threshold voltage	$V_O$ decreasing	92		98	% $V_O$
	Hysteresis voltage	Measured at $V_O$		0.5		% $V_O$
	Output low voltage	$V_I = 2.7 \text{ V}$ , $I_{O(\text{PG})} = 1 \text{ mA}$		0.15	0.4	V
	Leakage current	$V_{(\text{PG})} = 5 \text{ V}$			1	$\mu\text{A}$
Input current ( $\overline{\text{EN}}$ )		$\overline{\text{EN}} = 0 \text{ V}$	-1	0	1	$\mu\text{A}$
		$\overline{\text{EN}} = V_I$	-1		1	
Dropout voltage (see Note 4)	TPS76828	$I_O = 1 \text{ A}$ , $T_J = 25^\circ\text{C}$		500		mV
		$I_O = 1 \text{ A}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			825	
	TPS76830	$I_O = 1 \text{ A}$ , $T_J = 25^\circ\text{C}$		450		
		$I_O = 1 \text{ A}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			675	
	TPS76833	$I_O = 1 \text{ A}$ , $T_J = 25^\circ\text{C}$		350		
		$I_O = 1 \text{ A}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			575	
	TPS76850	$I_O = 1 \text{ A}$ , $T_J = 25^\circ\text{C}$		230		
		$I_O = 1 \text{ A}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			380	

NOTE 4:  $I_N$  voltage equals  $V_{O(\text{typ})} - 100 \text{ mV}$ ; TPS76801 output voltage set to 3.3 V nominal with external resistor divider. TPS76815, TPS76818, TPS76825, and TPS76827 dropout voltage limited by input voltage range limitations (i.e., TPS76830 input voltage needs to drop to 2.9 V for purpose of this test).

## TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
$V_O$	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8, 9
	Power supply ripple rejection	vs Frequency	10
	Output spectral noise density	vs Frequency	11
	Input voltage (min)	vs Output voltage	12
$Z_O$	Output impedance	vs Frequency	13
$V_{DO}$	Dropout voltage	vs Free-air temperature	14
	Line transient response		15, 17
	Load transient response		16, 18
$V_O$	Output voltage	vs Time	19
	Dropout voltage	vs Input voltage	20
	Equivalent series resistance (ESR)	vs Output current	22 – 25

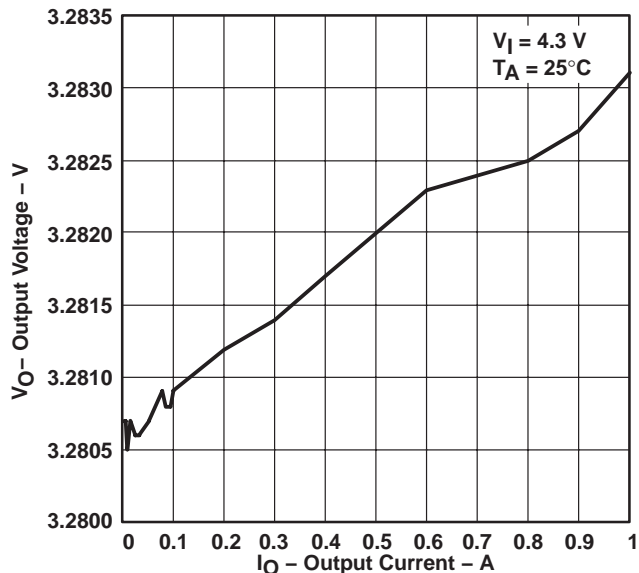


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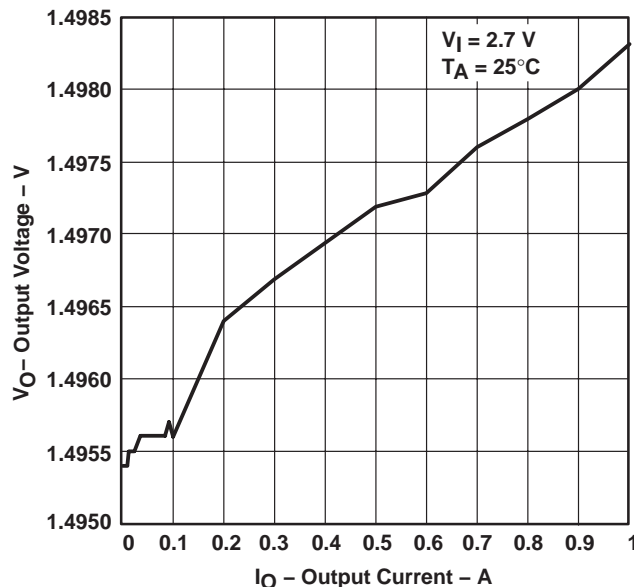
**TYPICAL CHARACTERISTICS**

**TPS76833  
 OUTPUT VOLTAGE  
 vs  
 OUTPUT CURRENT**



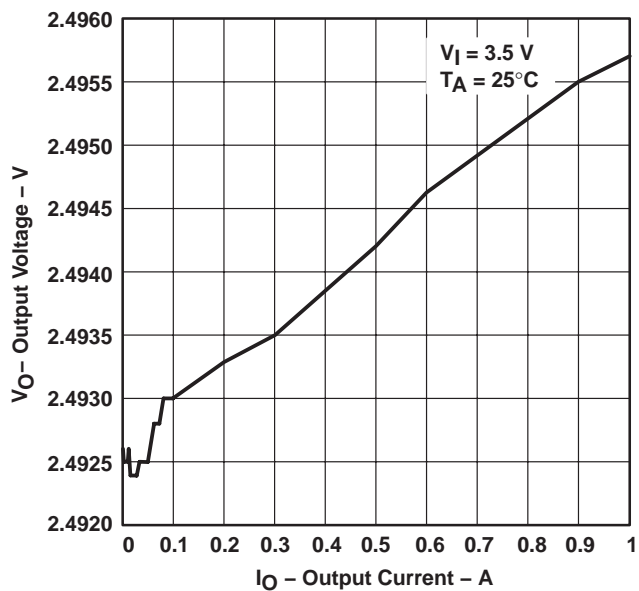
**Figure 2**

**TPS76815  
 OUTPUT VOLTAGE  
 vs  
 OUTPUT CURRENT**



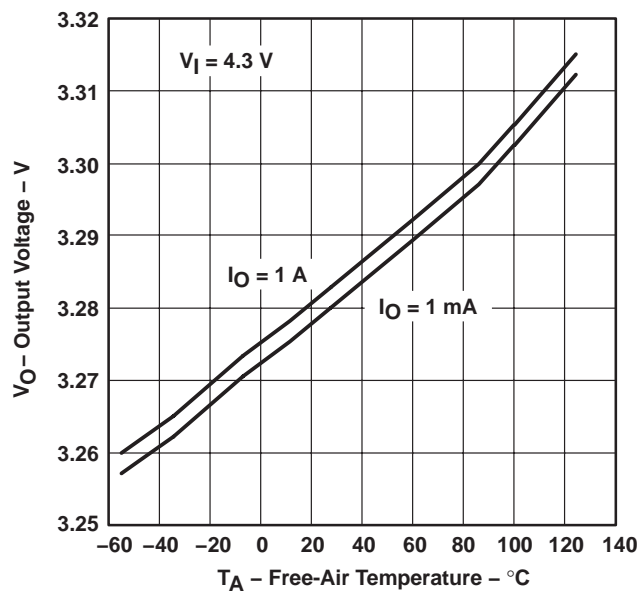
**Figure 3**

**TPS76825  
 OUTPUT VOLTAGE  
 vs  
 OUTPUT CURRENT**



**Figure 4**

**TPS76833  
 OUTPUT VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE**



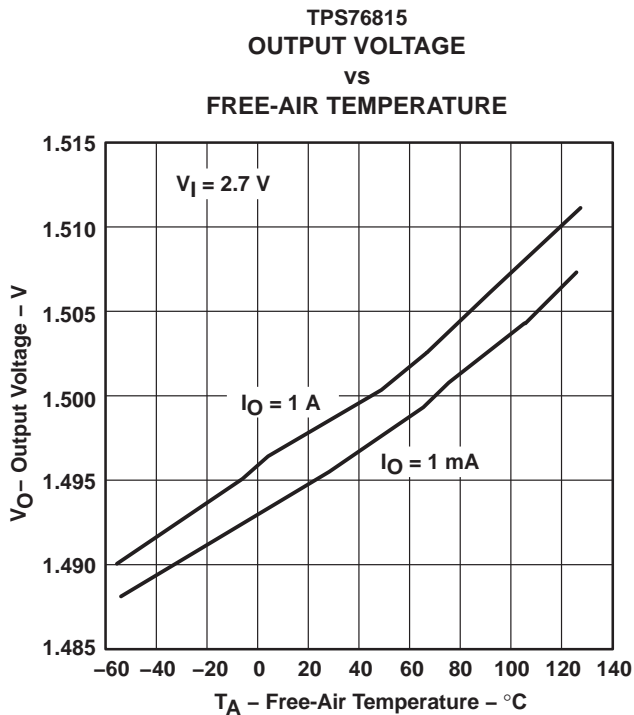
**Figure 5**



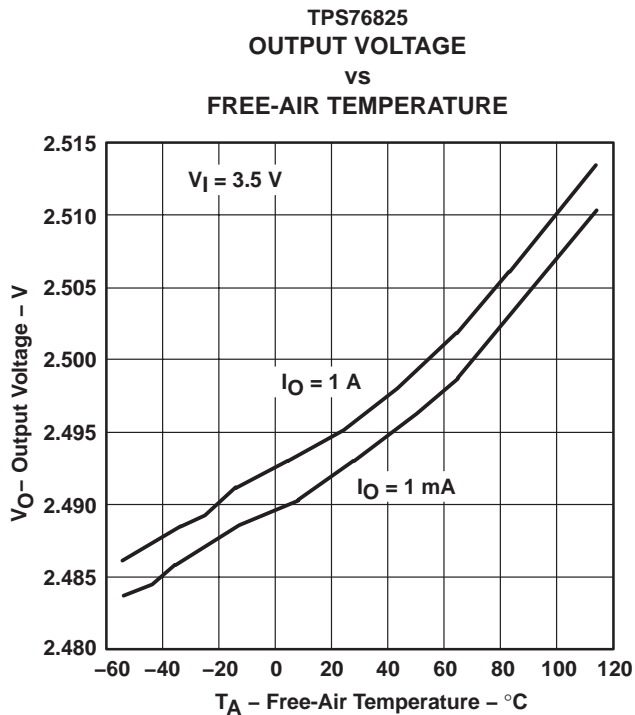
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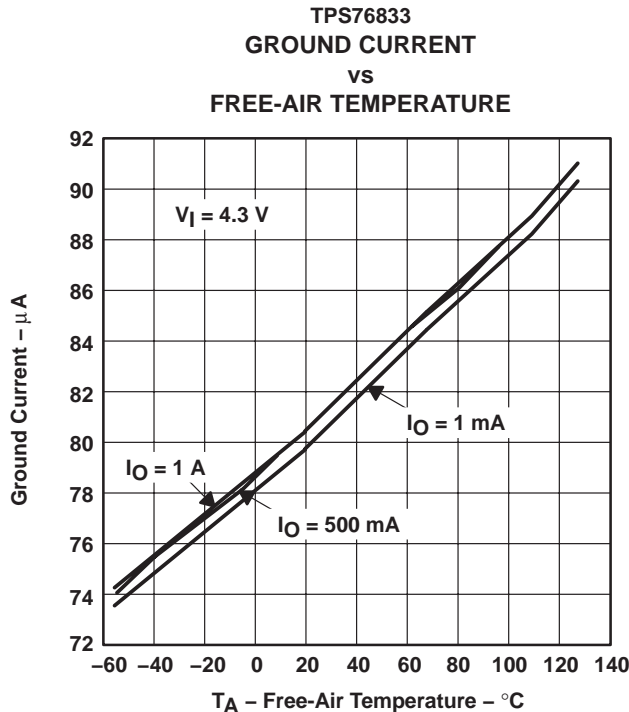
**TYPICAL CHARACTERISTICS**



**Figure 6**



**Figure 7**



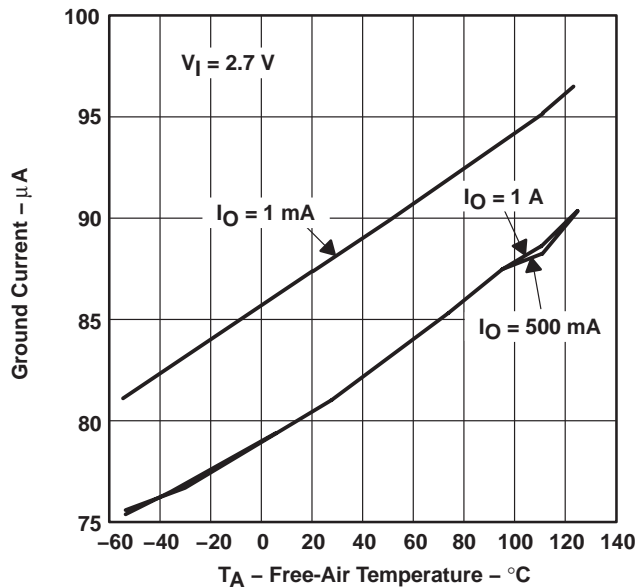
**Figure 8**

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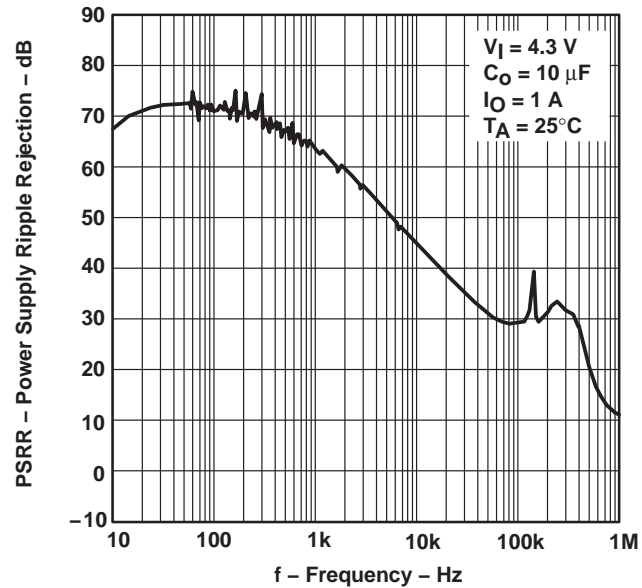
**TYPICAL CHARACTERISTICS**

**TPS76815  
 GROUND CURRENT  
 VS  
 FREE-AIR TEMPERATURE**



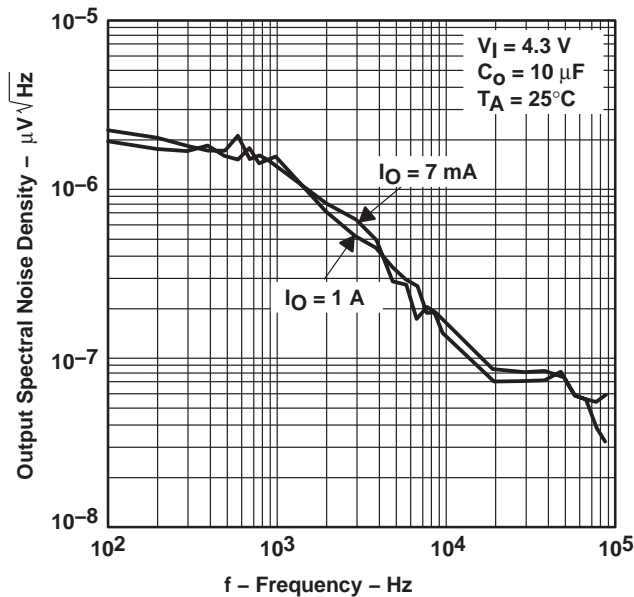
**Figure 9**

**TPS76833  
 POWER SUPPLY RIPPLE REJECTION  
 VS  
 FREQUENCY**



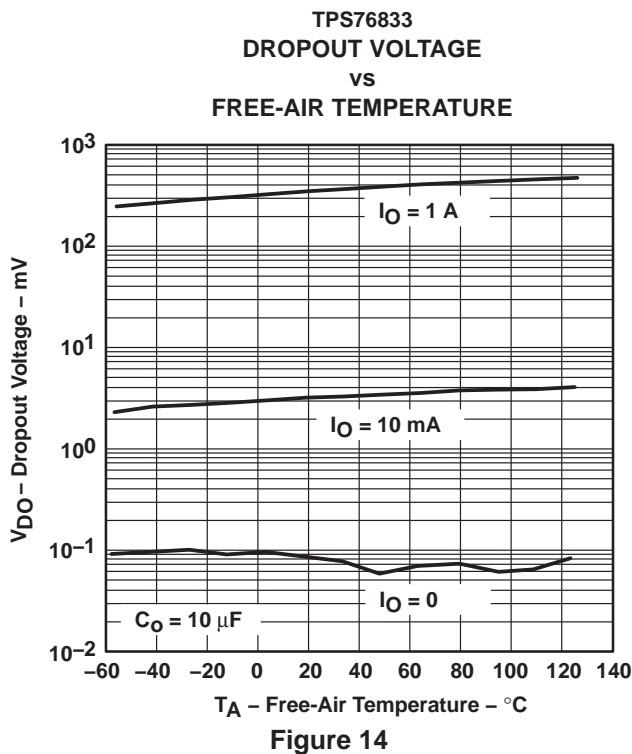
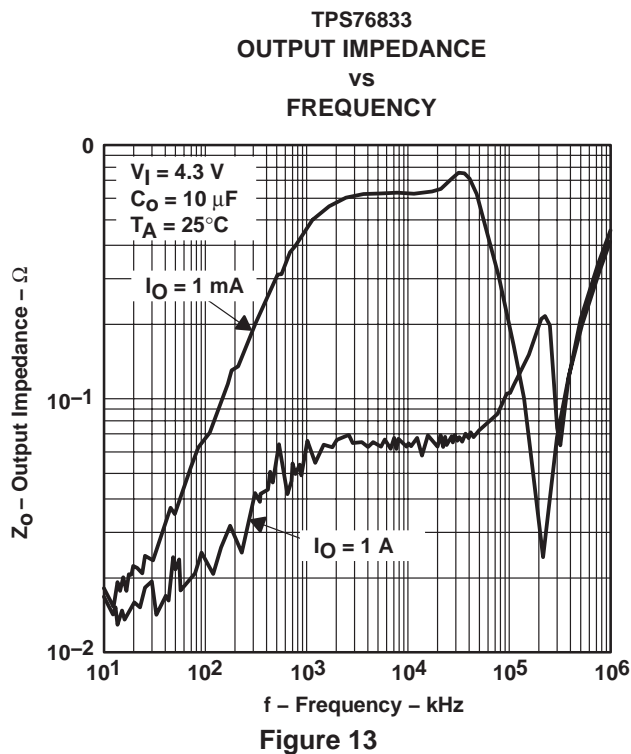
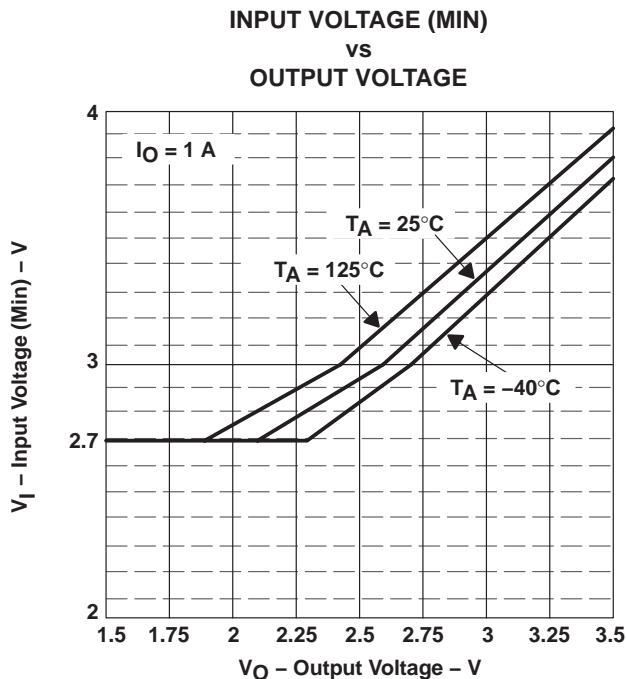
**Figure 10**

**TPS76833  
 OUTPUT SPECTRAL NOISE DENSITY  
 VS  
 FREQUENCY**



**Figure 11**

TYPICAL CHARACTERISTICS



TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP  
 TPS76828-EP, TPS76830-EP, TPS76833-EP, TPS76850-EP, TPS76801-EP  
**FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

SGLS011B – MARCH 2003 – REVISED DECEMBER 2008

TYPICAL CHARACTERISTICS

TPS76815  
 LINE TRANSIENT RESPONSE

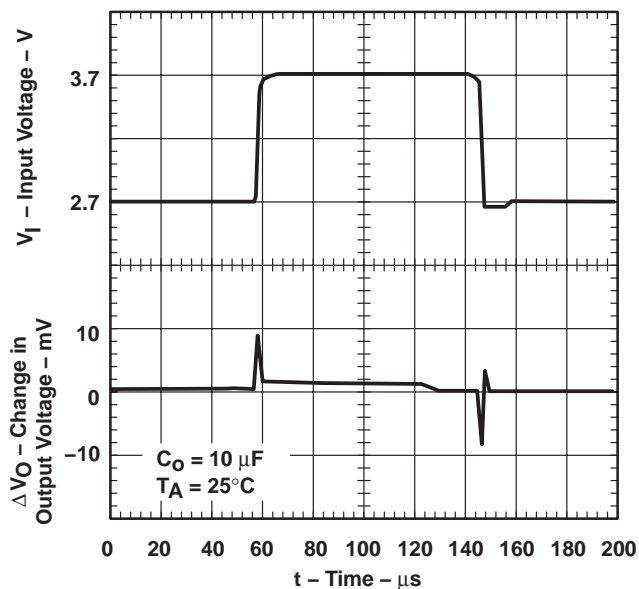


Figure 15

TPS76815  
 LOAD TRANSIENT RESPONSE

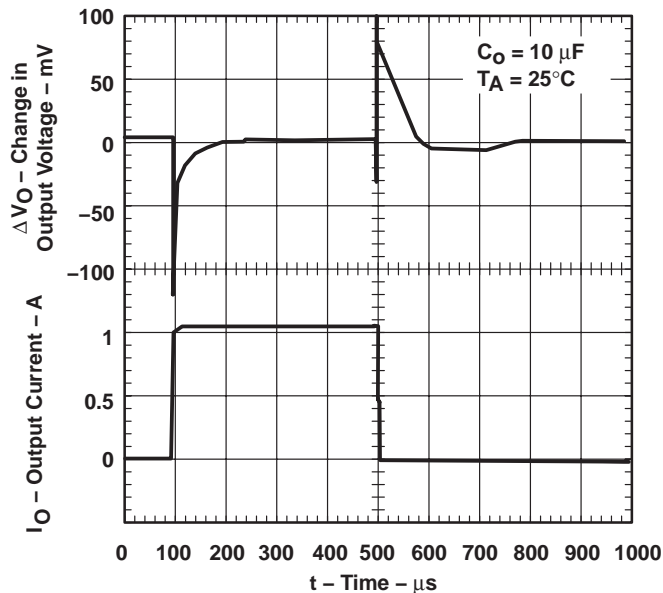


Figure 16

TPS76833  
 LINE TRANSIENT RESPONSE

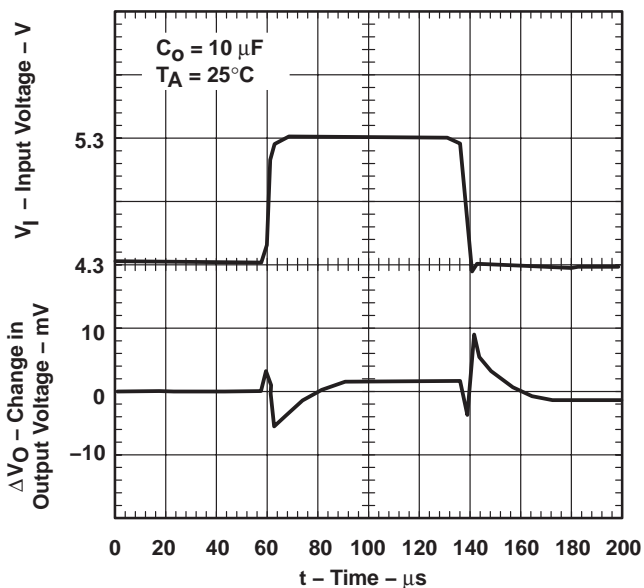


Figure 17

TPS76833  
 LOAD TRANSIENT RESPONSE

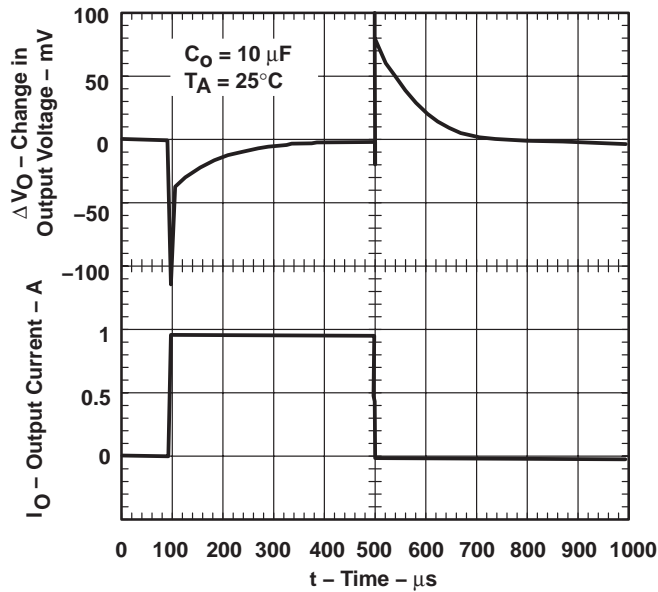


Figure 18

TYPICAL CHARACTERISTICS

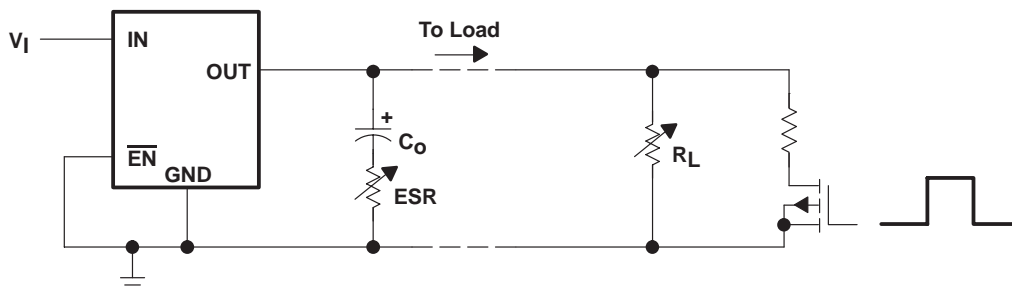
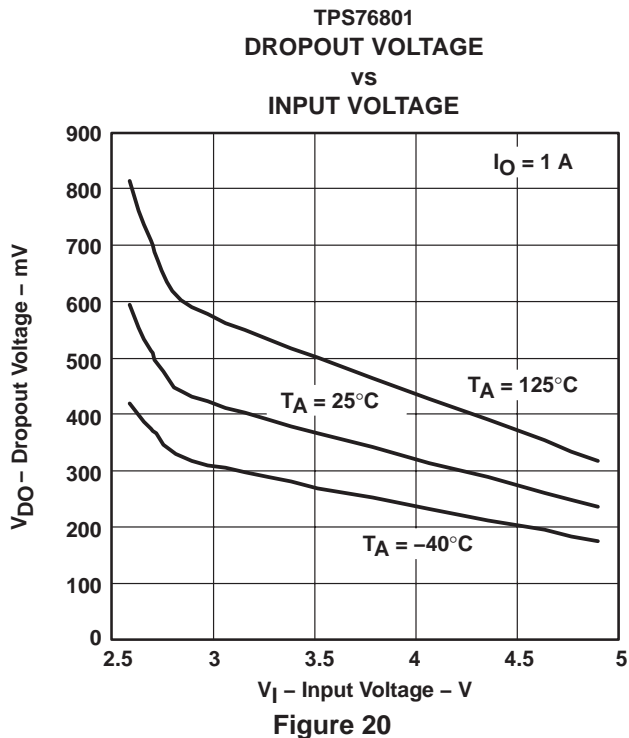
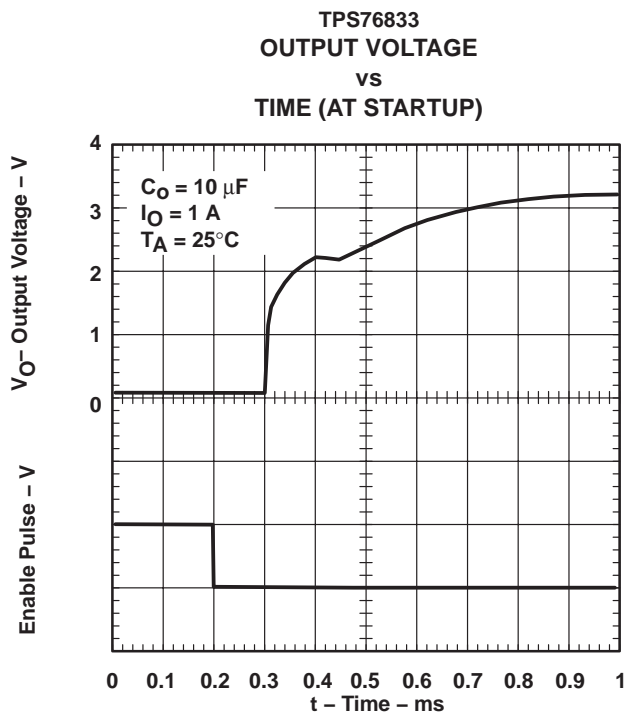
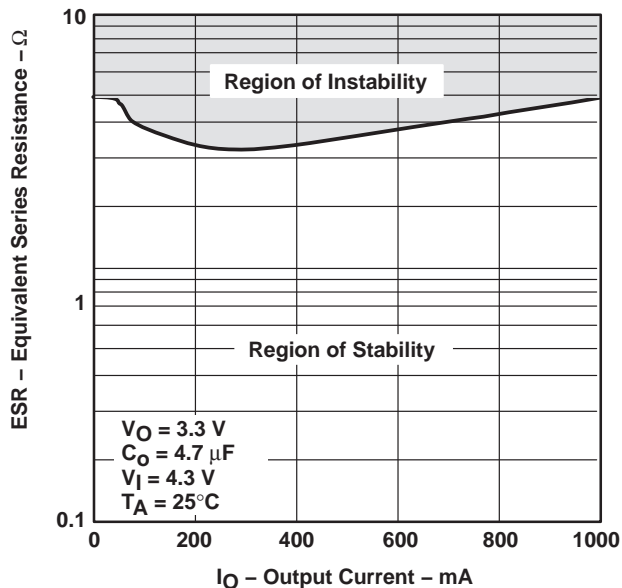


Figure 21. Test Circuit for Typical Regions of Stability (Figures 22 through 25) (Fixed Output Options)

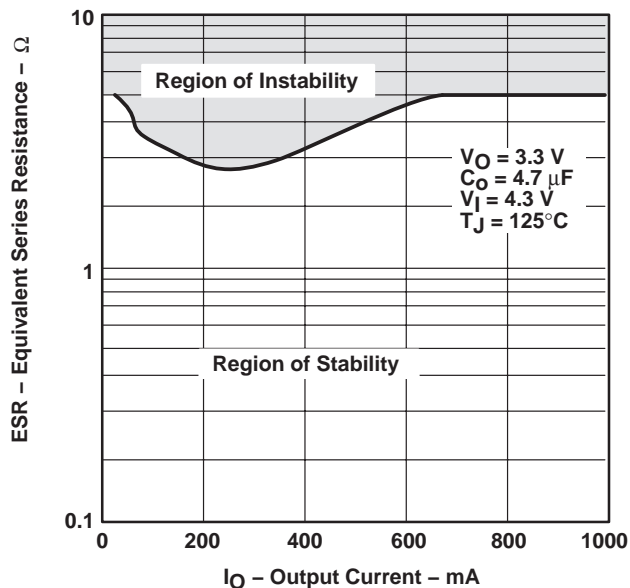
**TYPICAL CHARACTERISTICS**

TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT



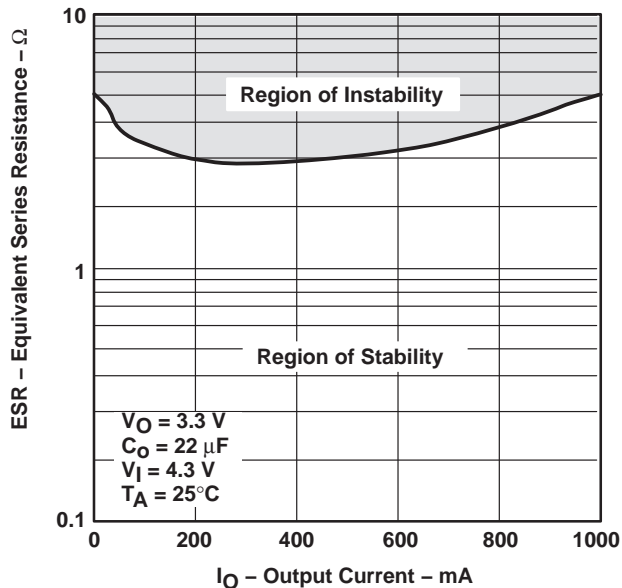
**Figure 22**

TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT



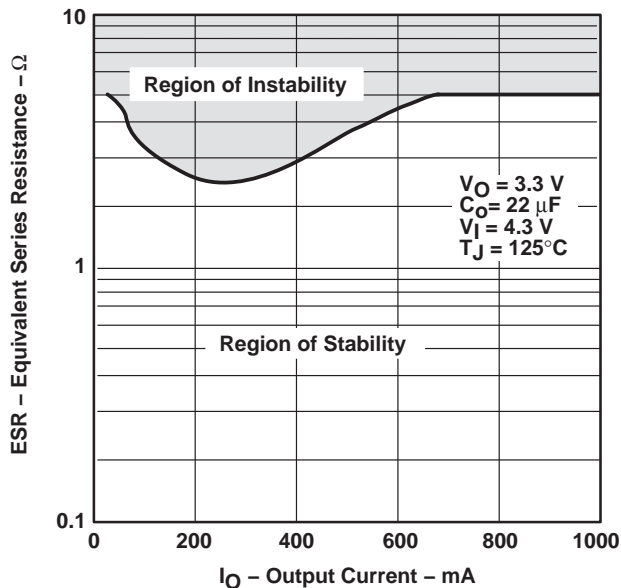
**Figure 23**

TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT



**Figure 24**

TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT



**Figure 25**

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

**TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76827-EP  
TPS76828-EP, TPS76830-EP, TPS76833-EP, TPS76850-EP, TPS76801-EP  
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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## APPLICATION INFORMATION

The TPS768xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and offers an adjustable device, the TPS76801 (adjustable from 1.2 V to 5.5 V).

### device operation

The TPS768xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ( $I_B = I_C/\beta$ ). The TPS768xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in  $\beta$  forces an increase in  $I_B$  to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS768xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS768xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2  $\mu$ A. If the shutdown feature is not used,  $\overline{EN}$  should be tied to ground.

### minimum load requirements

The TPS768xx family is stable even at zero load; no minimum load is required for operation.

### FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as shown in Figure 27. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

### external capacitor requirements

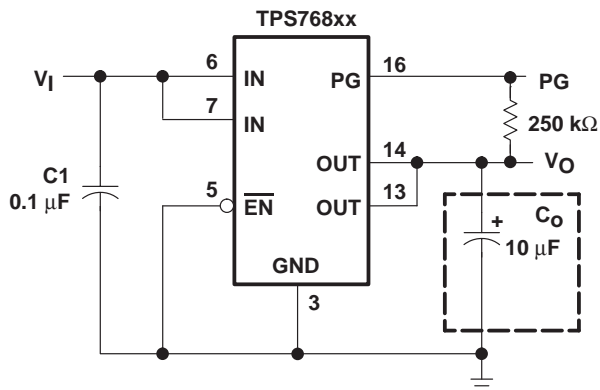
An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047  $\mu$ F or larger) improves load transient response and noise rejection if the TPS768xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS768xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10  $\mu$ F and the ESR (equivalent series resistance) must be between 50 m $\Omega$  and 1.5  $\Omega$ . Capacitor values 10  $\mu$ F or larger are acceptable, provided the ESR is less than 1.5  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10  $\mu$ F surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.



**APPLICATION INFORMATION**

**external capacitor requirements (continued)**



**Figure 26. Typical Application Circuit (Fixed Versions)**

**programming the TPS76801 adjustable LDO regulator**

The output voltage of the TPS76801 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

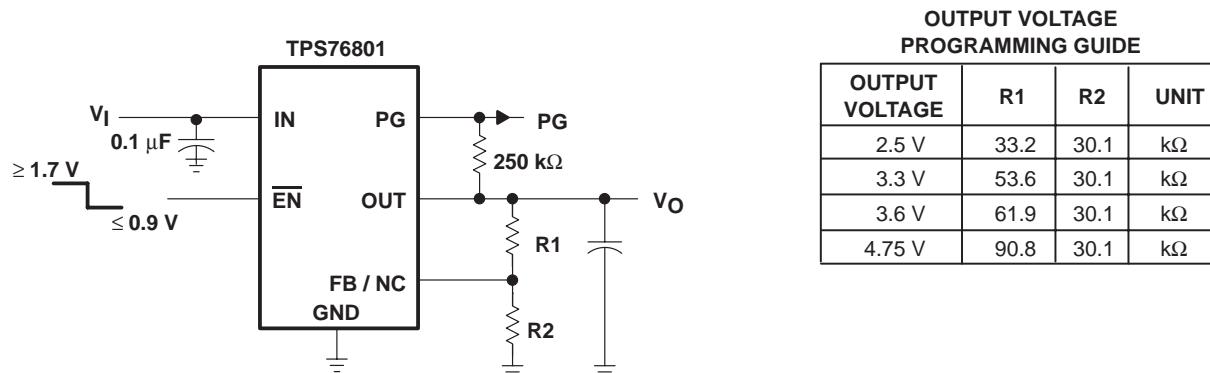
$$V_O = V_{ref} \times \left( 1 + \frac{R1}{R2} \right) \tag{1}$$

Where:

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left( \frac{V_O}{V_{ref}} - 1 \right) \times R2 \tag{2}$$



**Figure 27. TPS76801 Adjustable LDO Regulator Programming**

## APPLICATION INFORMATION

### power-good indicator

The TPS768xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

### regulator protection

The TPS768xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS768xx also features internal current limiting and thermal protection. During normal operation, the TPS768xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature.

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76801MPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	76801ME	<a href="#">Samples</a>
TPS76801QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76801QE	<a href="#">Samples</a>
TPS76815QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76815QE	<a href="#">Samples</a>
TPS76818QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76818QE	<a href="#">Samples</a>
TPS76825QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76825QE	<a href="#">Samples</a>
TPS76833QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76833QE	<a href="#">Samples</a>
TPS76850MPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	76850ME	<a href="#">Samples</a>
TPS76850QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76850QE	<a href="#">Samples</a>
V62/03632-01XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76801QE	<a href="#">Samples</a>
V62/03632-02XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76815QE	<a href="#">Samples</a>
V62/03632-03XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76818QE	<a href="#">Samples</a>
V62/03632-04XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76825QE	<a href="#">Samples</a>
V62/03632-08XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76833QE	<a href="#">Samples</a>
V62/03632-09XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	76850QE	<a href="#">Samples</a>
V62/03632-10XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	76801ME	<a href="#">Samples</a>
V62/03632-11XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	76850ME	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS76801-EP, TPS76815-EP, TPS76818-EP, TPS76825-EP, TPS76833-EP, TPS76850-EP :**

● Catalog: [TPS76801](#), [TPS76815](#), [TPS76818](#), [TPS76825](#), [TPS76833](#), [TPS76850](#)

● Automotive: [TPS76801-Q1](#), [TPS76815-Q1](#), [TPS76818-Q1](#), [TPS76825-Q1](#), [TPS76833-Q1](#), [TPS76850-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76801MPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76801QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76815QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76818QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76825QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76833QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76850MPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76850QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

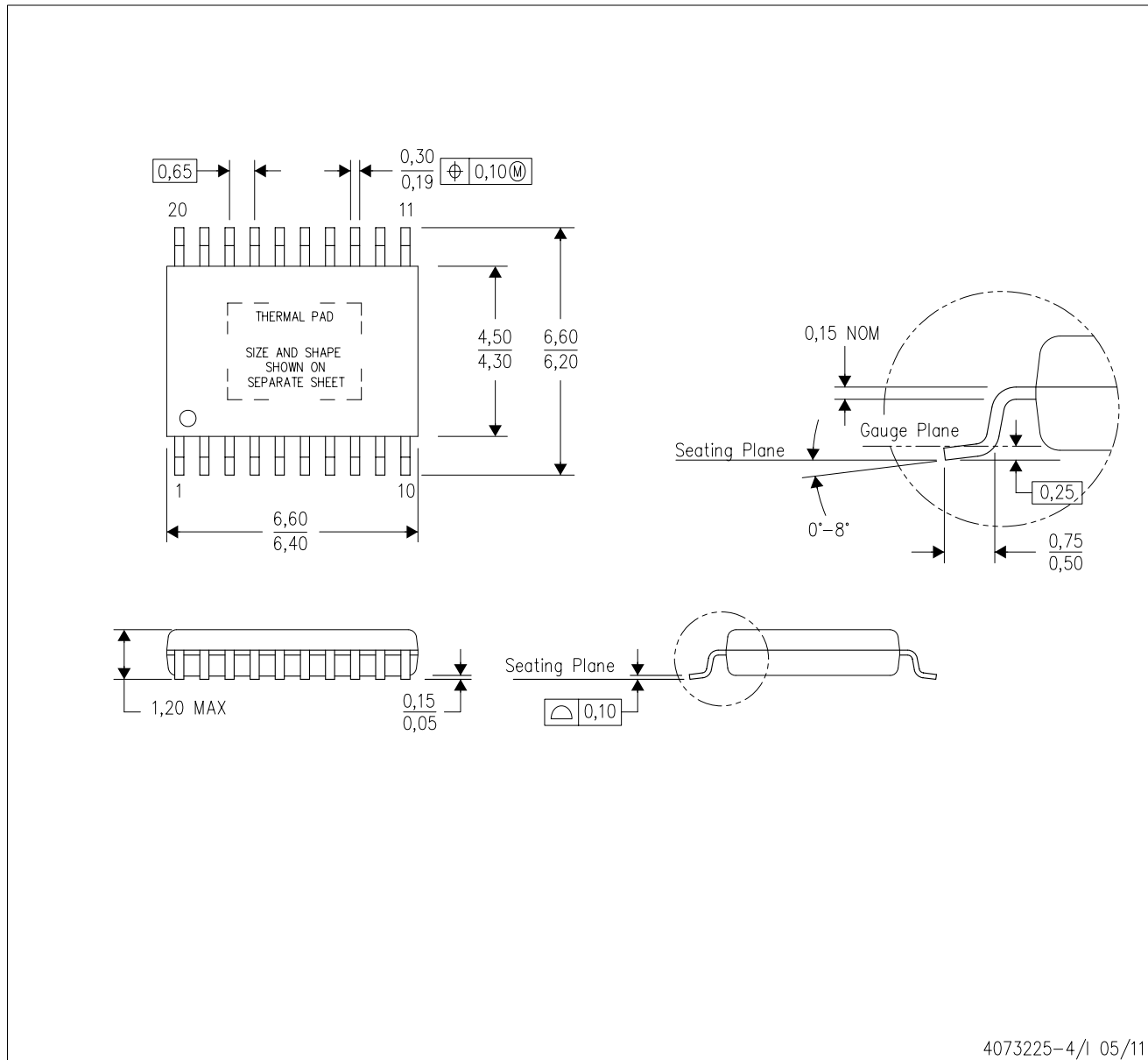

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76801MPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76801QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76815QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76818QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76825QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76833QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76850MPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76850QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0

# MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

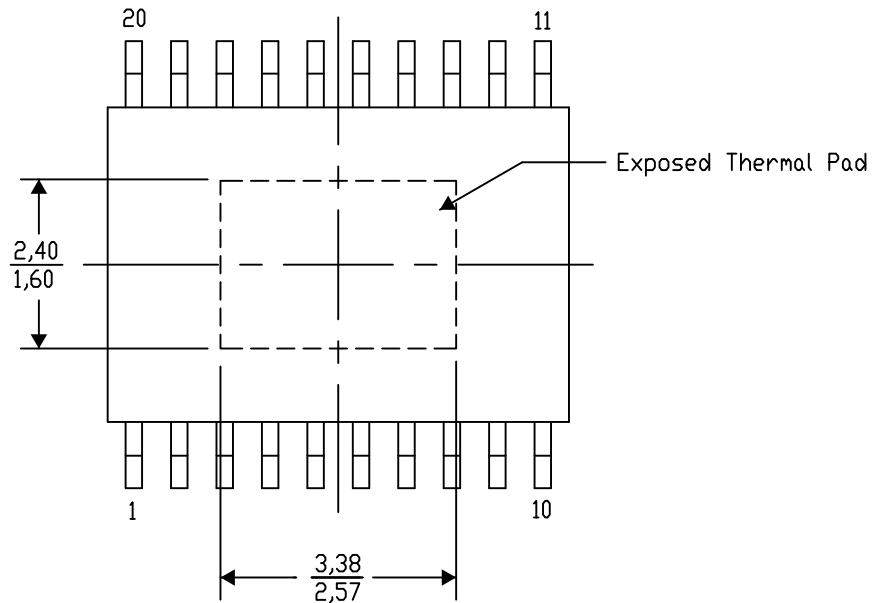
### PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

#### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

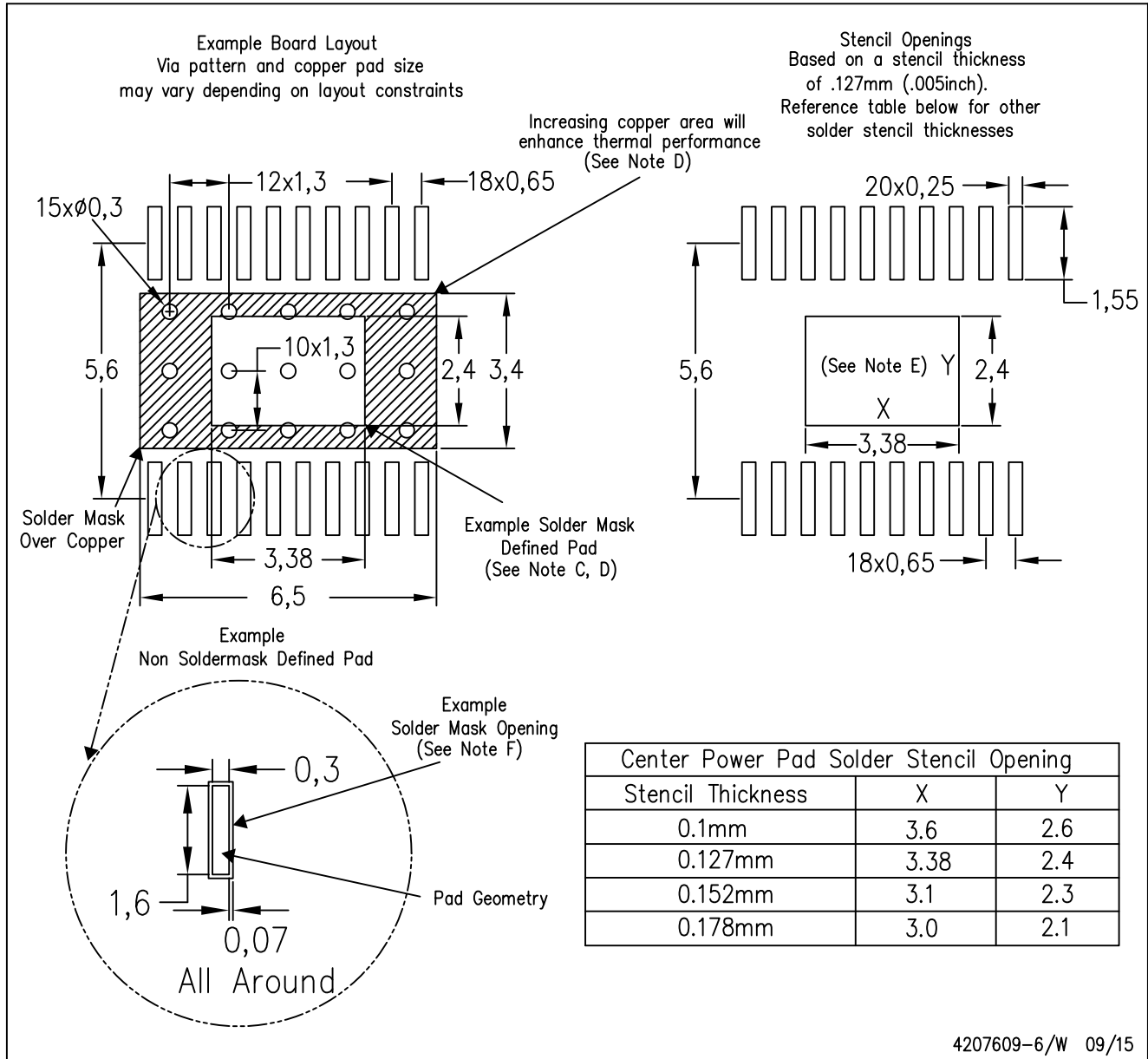
4206332-13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## THERMAL PAD MECHANICAL DATA

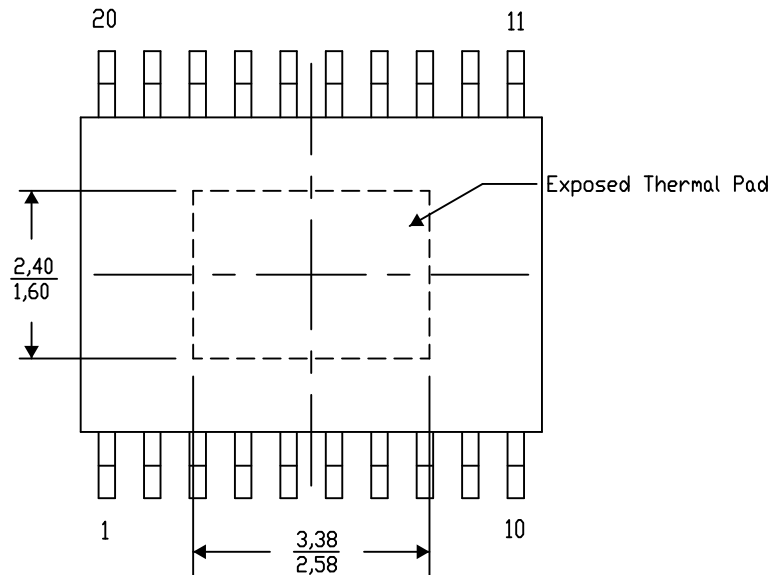
### PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

#### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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