THE DATASHEET OF

ADM8616WCYAKSZ-RL7

Low Voltage Supervisory Circuits with Watchdog Timer in 4-Lead SC70

Data Sheet

ADM8616/ADM8617

FEATURES

- Precision 1.8 V to 5 V power supply monitoring
- 9 $\overline{\text{RESET}}$ threshold options
  - 1.58 V to 4.63 V
- 4 $\overline{\text{RESET}}$ timeout options
  - 1 ms, 20 ms, 140 ms, 1120 ms
- 3 watchdog timeout options
  - 6.3 ms, 102 ms, 1.6 sec
- $\overline{\text{RESET}}$ output stages
  - Push-pull active-low (ADM8616)
  - Open-drain active-low (ADM8617)
- Low power consumption (5 µA)
- Guaranteed reset output valid to V_{CC} = 1 V
- Power supply glitch immunity
- Specified over −40°C to +85°C temperature range
- 4-lead SC70 package

APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

FUNCTIONAL BLOCK DIAGRAM

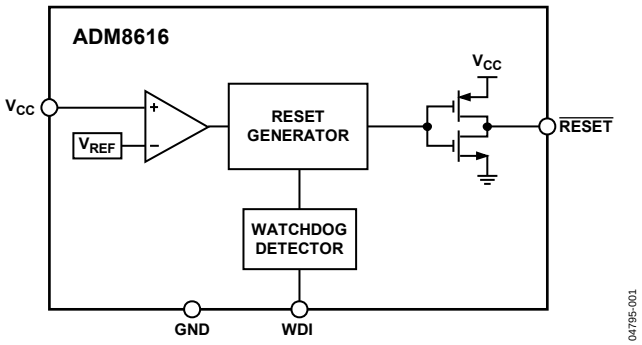

Figure 1.

GENERAL DESCRIPTION

The ADM8616/ADM8617 are supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. A power-on reset signal generates when the supply voltage rises to a preset threshold level. The ADM8616/ADM8617 have an on-chip watchdog timer that can reset the microprocessor if it fails to strobe within a preset timeout period.

Each part is available in the following nine reset threshold options: 1.58 V, 1.67 V, 2.19 V, 2.32 V, 2.63 V, 2.93 V, 3.08 V, 4.38 V, and 4.63 V. There are four reset timeout options: 1 ms, 20 ms, 140 ms, and 1120 ms. There are also three possible watchdog timeouts available: 6.3 ms, 102 ms, and 1.6 sec. Not all device options are released for sale as standard models. See the Ordering Guide for details.

The parts differ in terms of reset output configuration. The ADM8616 is active-low with a push-pull output, while the ADM8617 is active-low with an open-drain output.

The ADM8616/ADM8617 are available in 4-lead SC70 packages and typically consume only 5 µA, making them suitable for use in low power, portable applications.

Rev. C

Document Feedback

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REVISION HISTORY

2/2018—Rev. B to Rev. C

Changes to General Description Section ... 1
Added Note 1, Table 1 ... 3
Moved Ordering Guide ... 10
Changes to Figure 16 and Ordering Guide ... 10

1/2007—Rev. A to Rev. B

Changes to Functional Block Diagram ... 1

11/2006—Rev. 0 to Rev. A

Changes to Ordering Guide ... 10

6/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	
Supply Current		10	20	µA	V_{CC} = 5.5 V
		5	12	µA	V_{CC} = 3.6 V
$\overline{\text{RESET}}$ THRESHOLD VOLTAGE[1]					
ADM861xL	4.50	4.63	4.75	V	
ADM861xM	4.25	4.38	4.50	V	
ADM861xT	3.00	3.08	3.15	V	
ADM861xS	2.85	2.93	3.00	V	
ADM861xR	2.55	2.63	2.70	V	
ADM861xZ	2.25	2.32	2.38	V	
ADM861xY	2.12	2.19	2.25	V	
ADM861xW	1.62	1.67	1.71	V	
ADM861xV	1.52	1.58	1.62	V	
$\overline{\text{RESET}}$ THRESHOLD TEMPERATURE COEFFICIENT		40		ppm/°C	
$\overline{\text{RESET}}$ THRESHOLD HYSTERESIS		2 × V_{TH}		mV	
$\overline{\text{RESET}}$ TIMEOUT PERIOD[1]					
ADM861xxA	1	1.4	2	ms	
ADM861xxB	20	28	40	ms	
ADM861xxC	140	200	280	ms	
ADM861xxD	1120	1600	2240	ms	
V_{CC} TO $\overline{\text{RESET}}$ DELAY		40		µs	V_{CC} falling at 1 mV/µs
$\overline{\text{RESET}}$ OUTPUT VOLTAGE					
VOL (Open-Drain and Push-Pull)			0.3	V	V_{CC} ≥ 1.0 V, I_{SINK} = 50 µA
			0.3	V	V_{CC} ≥ 1.2 V, I_{SINK} = 100 µA
			0.3	V	V_{CC} ≥ 2.7 V, I_{SINK} = 1.2 mA
			0.4	V	V_{CC} ≥ 4.5 V, I_{SINK} = 3.2 mA
VOH (Push-Pull Only)	0.8 × V_{CC}			V	V_{CC} ≥ 2.7 V, I_{SOURCE} = 500 µA
	V_{CC} − 1.5			V	V_{CC} ≥ 4.5 V, I_{SOURCE} = 800 µA
$\overline{\text{RESET}}$ Rise Time		5	25	ns	From 10% to 90% V_{CC}, C_L = 5 pF, V_{CC} = 3.3 V
Open-Drain $\overline{\text{RESET}}$ Output Leakage Current			1	µA	
WATCHDOG INPUT					
Watchdog Timeout Period[1]					
ADM861xxxW	4.3	6.3	9.3	ms	
ADM861xxxX	71	102	153	ms	
ADM861xxxY	1.12	1.6	2.4	sec	
WDI Pulse Width	50			ns	V_{IL} = 0.3 × V_{CC}, V_{IH} = 0.7 × V_{CC}
WDI Input Threshold				V	
VIL			0.3 × V_{CC}		
VIH	0.7 × V_{CC}			V	
WDI Input Current		120	160	µA	V_{WDI} = V_{CC}
	−20	−15		µA	V_{WDI} = 0

[1] Not all device options are released for sale as standard models. See the Ordering Guide for details.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
$\overline{RESET}$	−0.3 V to +6 V
Output Current ($\overline{RESET}$)	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance, SC70	146°C/W
Soldering Temperature	
Sn/Pb	240°C, 30 sec
Pb-Free	260°C, 40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

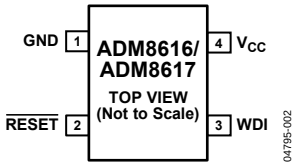

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground.
2	$\overline{\text{RESET}}$	Active-Low $\overline{\text{RESET}}$ Output. Asserted whenever V_{CC} is below the reset threshold (V_{TH}). Push-Pull Output Stage for ADM8616. Open-Drain Output Stage for ADM8617.
3	WDI	Watchdog Input. Generates a $\overline{\text{RESET}}$ if the logic level on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin, or if a reset is generated. Leave floating to disable the watchdog timer.
4	V_{CC}	Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

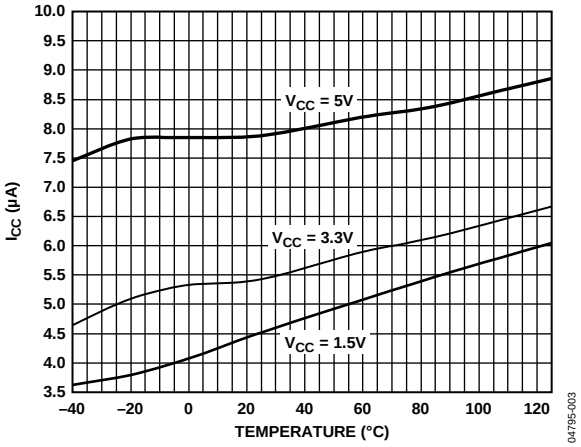

Figure 3. Supply Current vs. Temperature

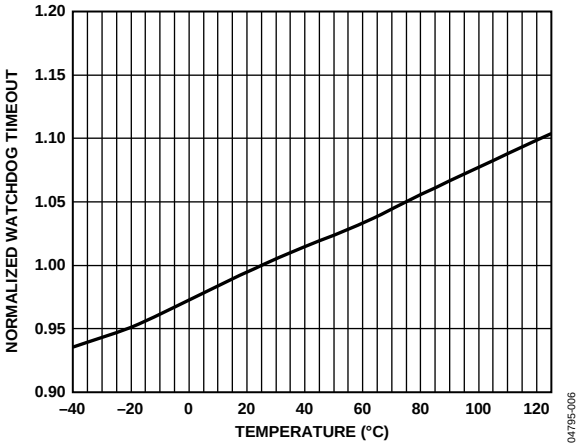

Figure 6. Normalized Watchdog Timeout Period vs. Temperature

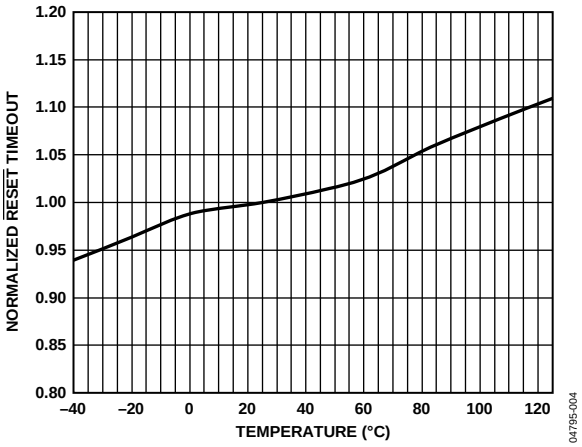

Figure 4. Normalized $\overline{RESET}$ Timeout Period vs. Temperature

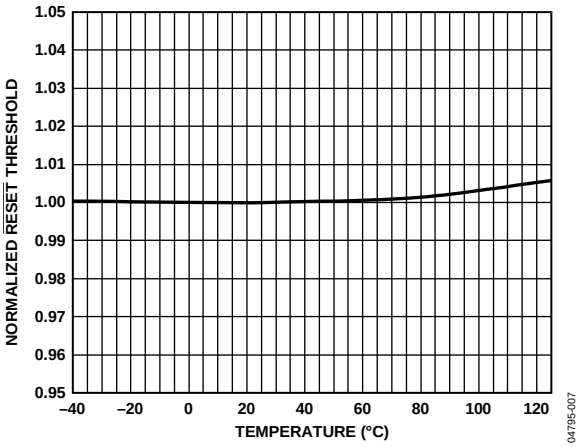

Figure 7. Normalized $\overline{RESET}$ Threshold vs. Temperature

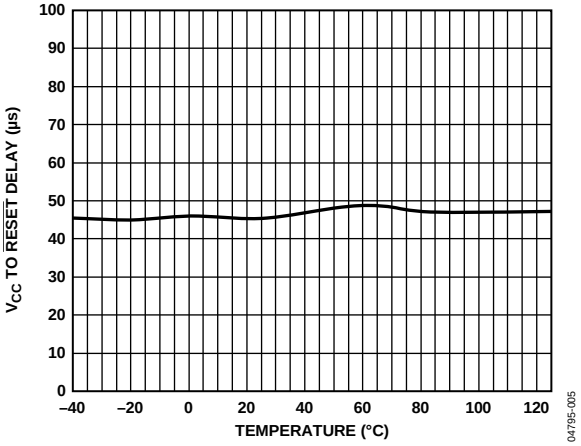

Figure 5. V_{CC} to $\overline{RESET}$ Output Delay vs. Temperature

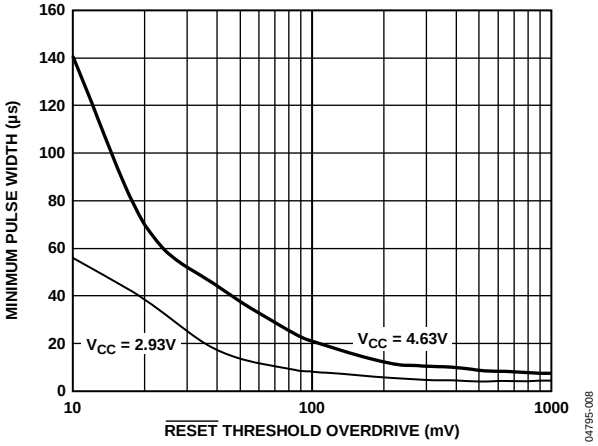

Figure 8. Maximum V_{CC} Transient Duration vs. $\overline{RESET}$ Threshold Overdrive

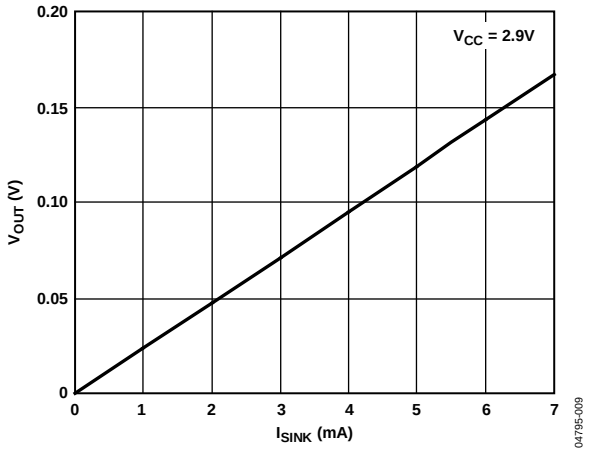

Figure 9. Voltage Output Low vs. I_{SINK}

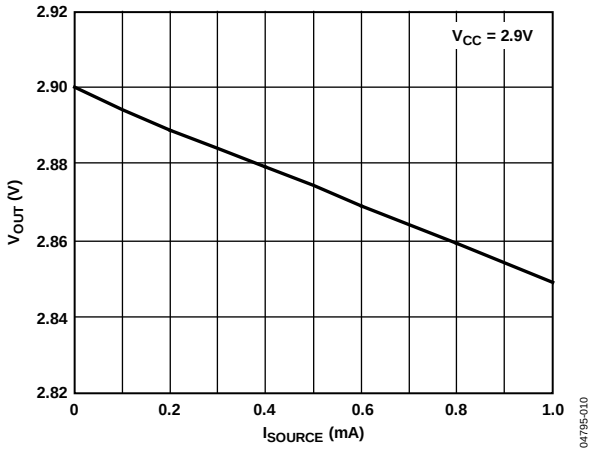

Figure 10. Voltage Output High vs. I_{SOURCE}

CIRCUIT DESCRIPTION

The ADM8616/ADM8617 provide microprocessor supply voltage supervision by controlling the microprocessors $\overline{\text{RESET}}$ input. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a $\overline{\text{RESET}}$ signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout $\overline{\text{RESET}}$ after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer. By including watchdog strobe instructions in microprocessor code, a watchdog timer can detect if the microprocessor code breaks down or becomes stuck in an infinite loop. If this happens, the watchdog timer asserts a $\overline{\text{RESET}}$ pulse that restarts the microprocessor in a known state.

RESET OUTPUT

The ADM8616 features an active-low, push-pull $\overline{\text{RESET}}$ output, while the ADM8617 features an active-low, open-drain $\overline{\text{RESET}}$ output. The $\overline{\text{RESET}}$ signal is guaranteed to be logic low and logic high, respectively, for V_{CC} down to 1 V.

The $\overline{\text{RESET}}$ output is asserted when V_{CC} is below the $\overline{\text{RESET}}$ threshold (V_{TH}), or when WDI is not serviced within the watchdog timeout period (t_{WD}). $\overline{\text{RESET}}$ remains asserted for the duration of the $\overline{\text{RESET}}$ active timeout period (t_{RP}) after V_{CC} rises above the $\overline{\text{RESET}}$ threshold or after the watchdog timer times out. Figure 11 illustrates the behavior of the $\overline{\text{RESET}}$ outputs.

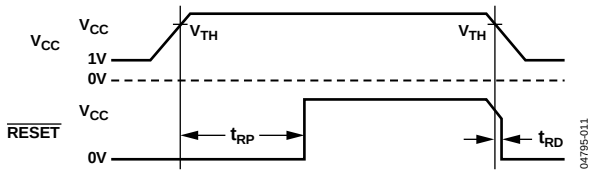

Figure 11. $\overline{\text{RESET}}$ Timing Diagram

WATCHDOG INPUT

The ADM8616/ADM8617 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), $\overline{\text{RESET}}$ is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period, therefore, indicates a code execution error, and the $\overline{\text{RESET}}$ pulse generated restarts the microprocessor in a known state.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a $\overline{\text{RESET}}$ assertion due to an undervoltage condition on V_{CC}. When $\overline{\text{RESET}}$ is asserted, the watchdog timer is cleared and does not begin counting again until $\overline{\text{RESET}}$ deasserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

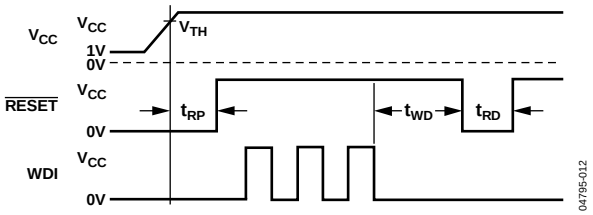

Figure 12. Watchdog Timing Diagram

APPLICATION INFORMATION

WATCHDOG INPUT CURRENT

To minimize watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 160 µA. Pulsing WDI low-high-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the $\overline{\text{RESET}}$ output circuitry so that $\overline{\text{RESET}}$ is not asserted when the watchdog timer times out.

NEGATIVE-GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM8616/ADM8617 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 8 plots V_{CC} transient duration vs. transient magnitude. The curve shows combinations of transient magnitude and duration for which a $\overline{\text{RESET}}$ is not generated for 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a $\overline{\text{RESET}}$, but if the transient is any bigger in magnitude or duration, a $\overline{\text{RESET}}$ is generated. An optional 0.1 µF bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC} = 0 V

The active-low $\overline{\text{RESET}}$ output is guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor, valid outputs for V_{CC} as low as 0 V are possible. The resistor, connected between $\overline{\text{RESET}}$ and ground, pulls the output low when it is unable to sink current. A large resistance, such as 100 kΩ, must be used so that it does not overload the $\overline{\text{RESET}}$ output when V_{CC} is above 1 V.

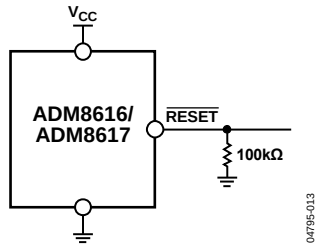

Figure 13. Ensuring $\overline{\text{RESET}}$ Valid to V_{CC} = 0 V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessors watchdog strobe code, quickly switching WDI low to high and then high to low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-high-low WDI pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog does not detect this because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset.

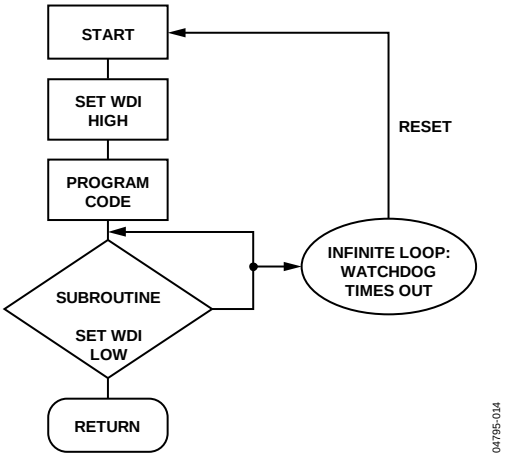

Figure 14. Watchdog Flow Diagram

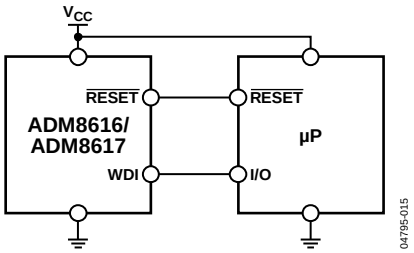

Figure 15. Typical Application Circuit

OUTLINE DIMENSIONS

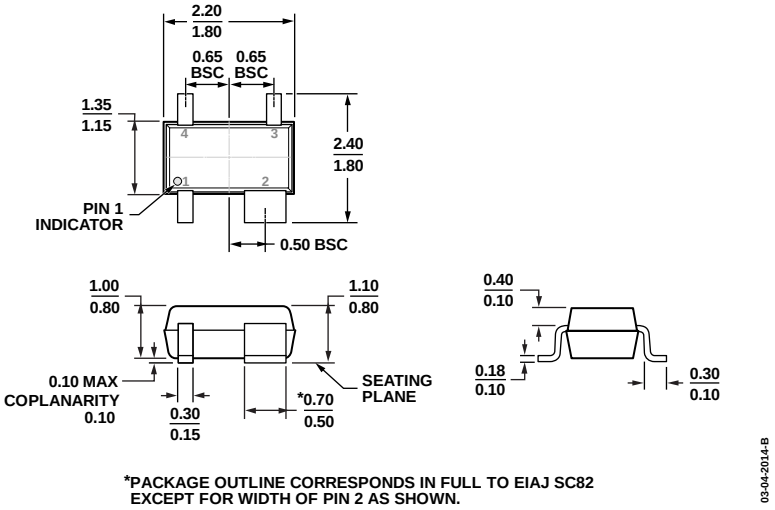

Figure 16. 4-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-4)
Dimensions shown in millimeters

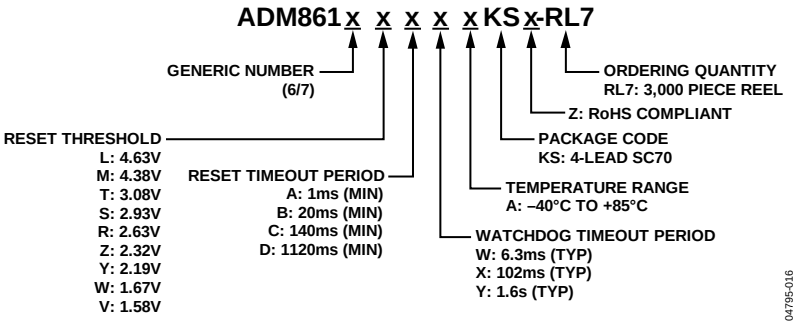

Figure 17. Ordering Code Structure

ORDERING GUIDE

Model[1, 2, 3]	Reset Threshold (V)	Reset Timeout Minimum (ms)	Watchdog Timeout (sec)	Temperature Range	Qty	Package Description	Package Option	Marking Code
ADM8616LCYAKSZ-RL7	4.63	140	1.6	–40°C to +85°C	3,000	4-Lead SC70	KS-4	N0F
ADM8616WCYAKSZ-RL7	1.67	140	1.6	–40°C to +85°C	3,000	4-Lead SC70	KS-4	N0F
ADM8617SAYAKSZ-RL7	2.93	1	1.6	–40°C to +85°C	3,000	4-Lead SC70	KS-4	M4X
ADM8617RCYAKSZ-RL7	2.63	140	1.6	–40°C to +85°C	3,000	4-Lead SC70	KS-4	M4X

[1] The ADM8616/ADM8617 include many device options; however, not all options are released for sale. Released options are called standard models and are listed in the Ordering Guide. The Watchdog Timers page on the Analog Devices website also lists standard models. Contact a sales representative for information on nonstandard models and be aware that samples and production units have very long lead times.
[2] If ordering nonstandard models, complete the ordering code shown in Figure 17 by inserting reset threshold, reset timeout, and watchdog timeout suffixes.
[3] Z = RoHS Compliant Part.

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