



**THE DATASHEET OF  
PSMN1R2-25YLC,115**





# PSMN1R2-25YLC

N-channel 25 V 1.3 m $\Omega$  logic level MOSFET in LFPAK using NextPower technology

Rev. 1 — 2 May 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD and QOSS for high system efficiencies at low and high loads
- Ultra low R<sub>ds(on)</sub> and low parasitic inductance

### 1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	-	25	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	-	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	179	W
T <sub>j</sub>	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	1.35	1.7	m $\Omega$
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	1.05	1.3	m $\Omega$

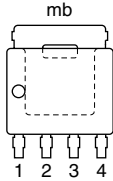
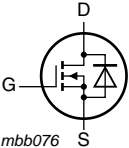
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	8.3	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 15</a> ; see <a href="#">Figure 14</a>	-	31	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

**SOT669 (LPAK;  
Power-SO8)**

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN1R2-25YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 4. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PSMN1R2-25YLC	1C225L

[1] % = placeholder for manufacturing site code.

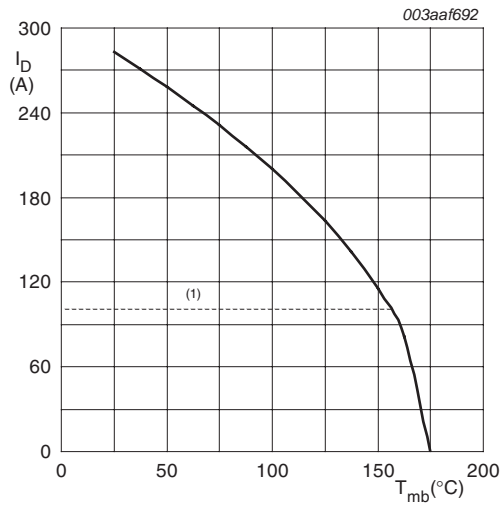
## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

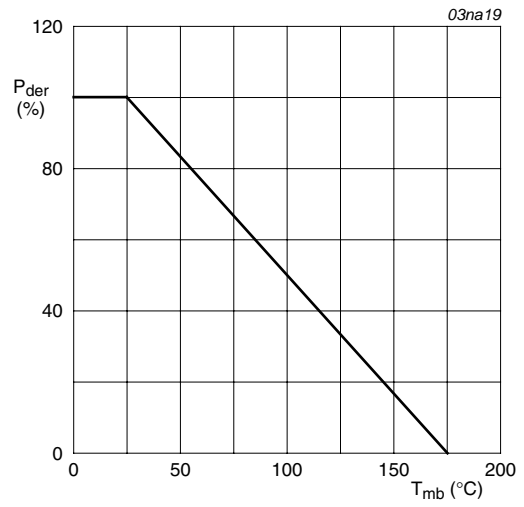
Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V	
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	-	100	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 4</a>	-	1133	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	179	W	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
$T_{sld(M)}$	peak soldering temperature		-	260	°C	
$V_{ESD}$	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	690	-	V	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	100	A	
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	1133	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$ ; see <a href="#">Figure 3</a>	-	178	mJ	

[1] Continuous current is limited by package.



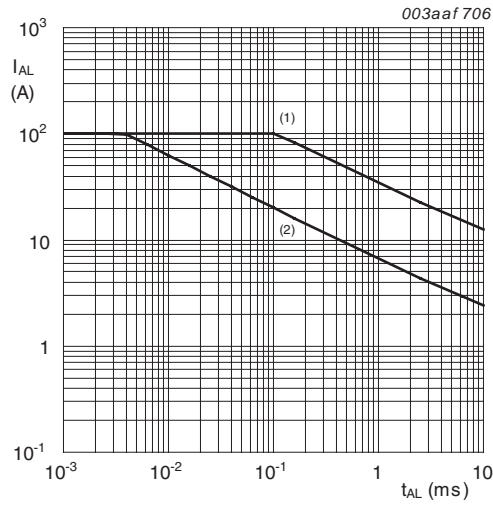
$V_{GS} \geq 10V$ ; (1) Capped at 100A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



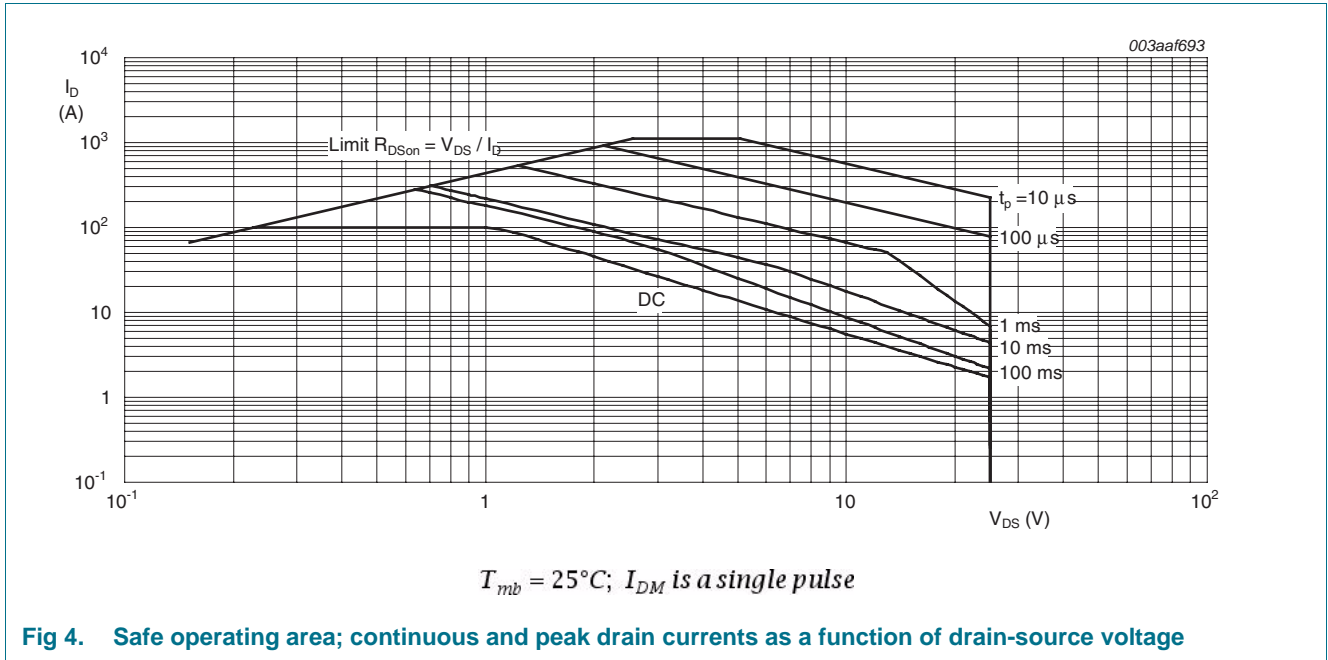
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1)  $T_j (init) = 25^{\circ}C$ ; (2)  $T_j (init) = 100^{\circ}C$

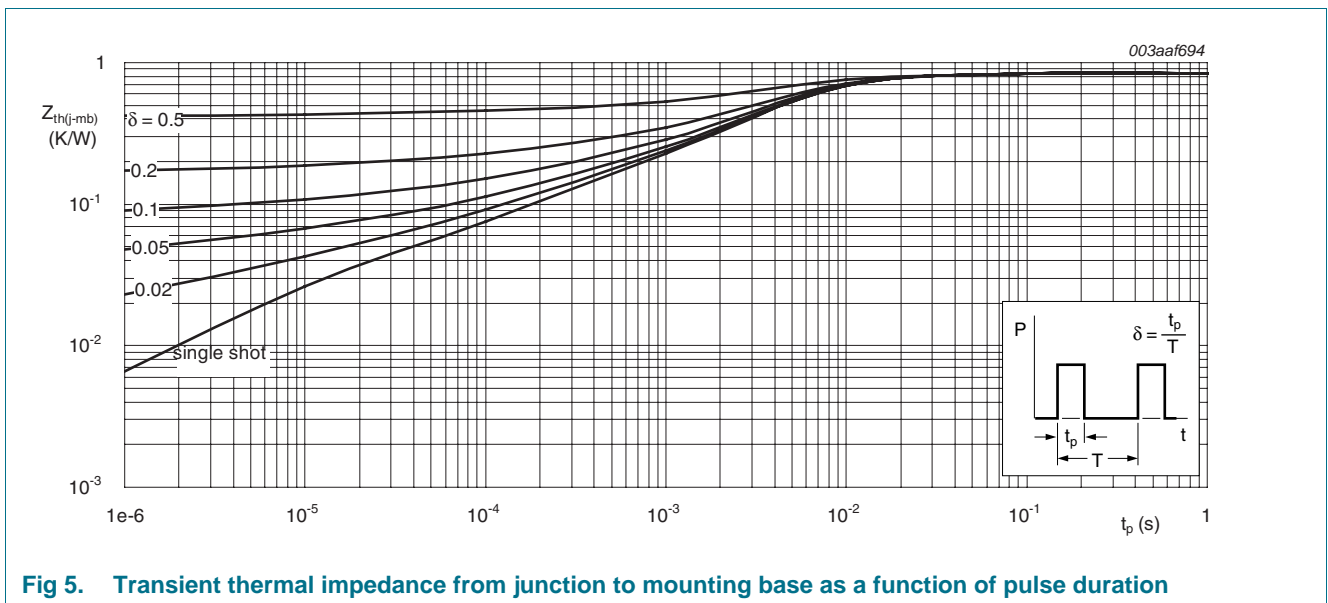
Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	0.71	0.84	K/W



## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	1.05	1.45	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	2.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	1.35	1.7	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	2.75	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	1.05	1.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	2.1	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1	2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	66	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 15</a> ; see <a href="#">Figure 14</a>	-	31	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	65	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	9.7	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3	-	nC
$Q_{GD}$	gate-drain charge		-	8.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	2.5	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	4173	-	pF
$C_{oss}$	output capacitance		-	994	-	pF
$C_{rss}$	reverse transfer capacitance		-	347	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	32	-	ns
$t_r$	rise time		-	42	-	ns
$t_{d(off)}$	turn-off delay time		-	60	-	ns
$t_f$	fall time		-	29	-	ns

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{OSS}$	output charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 12\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$	-	21	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.8	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	41	-	ns
$Q_r$	recovered charge	$V_{DS} = 12\text{ V}$	-	36	-	nC
$t_a$	reverse recovery rise time	$V_{GS} = 0\text{ V}$ ; $I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 18</a>	-	24	-	ns
$t_b$	reverse recovery fall time		-	17	-	ns

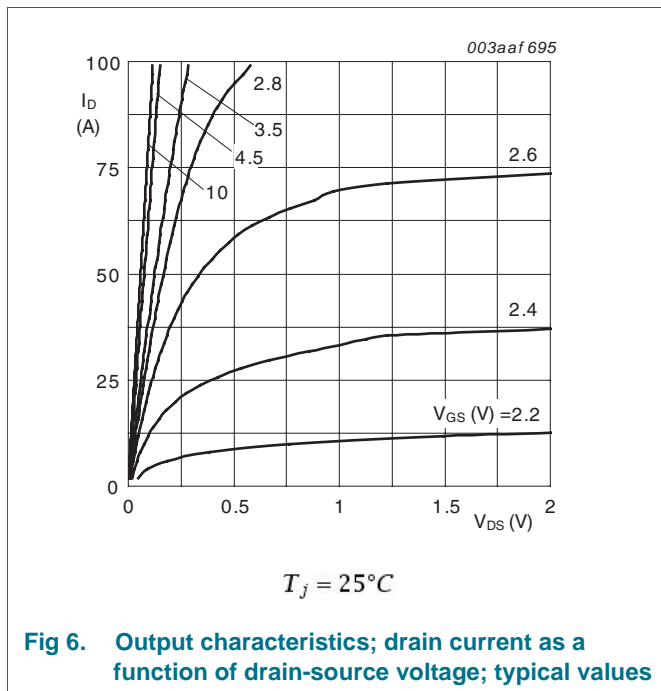


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

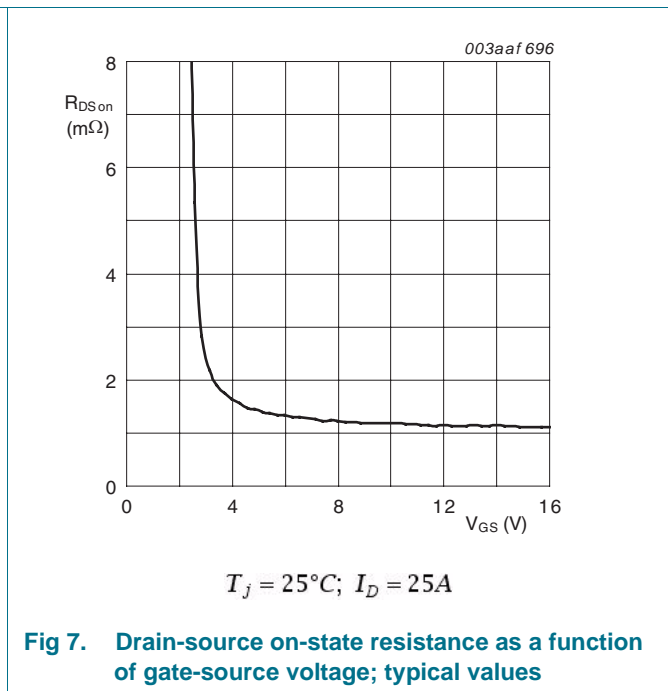
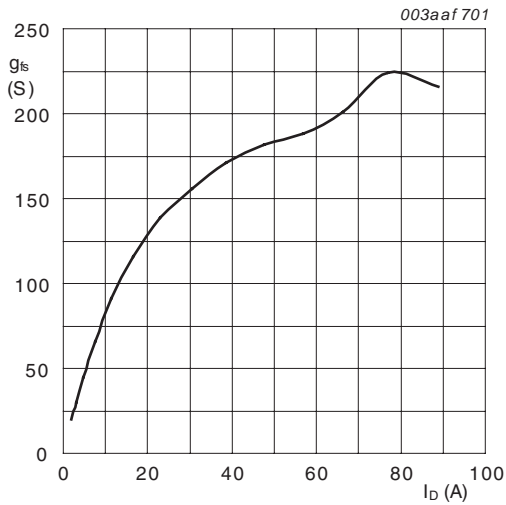
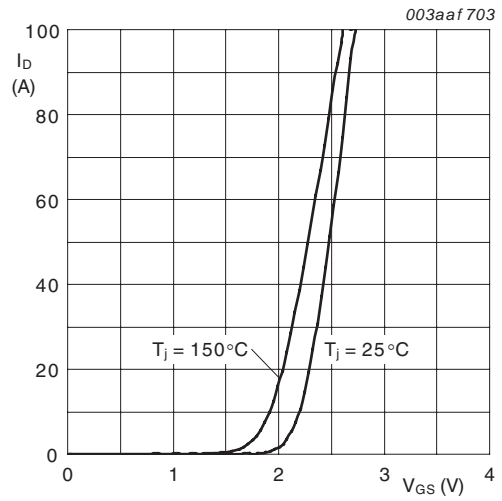


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



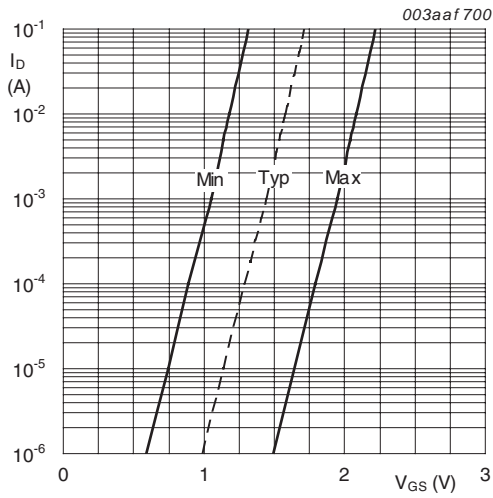
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values



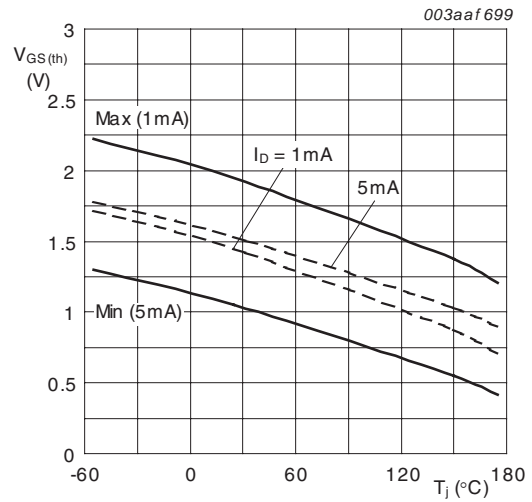
$V_{DS} = 10\text{V}$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature

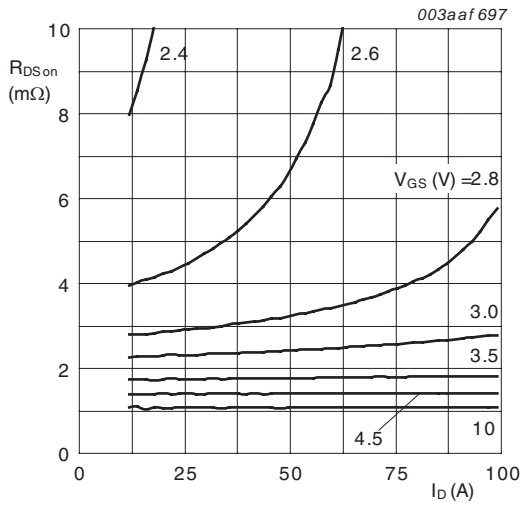
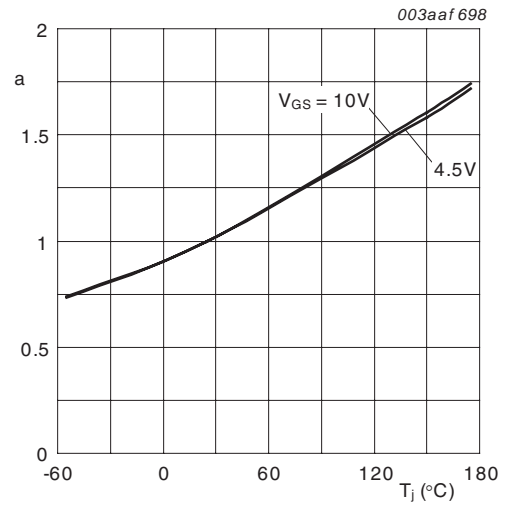


Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

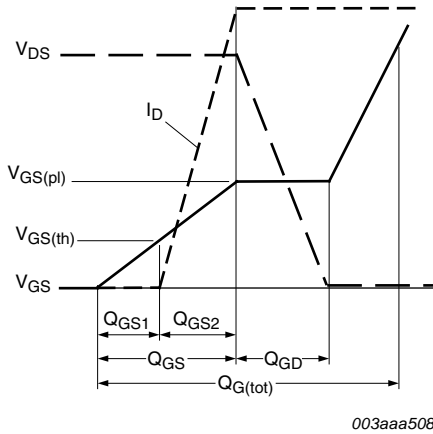


Fig 14. Gate charge waveform definitions

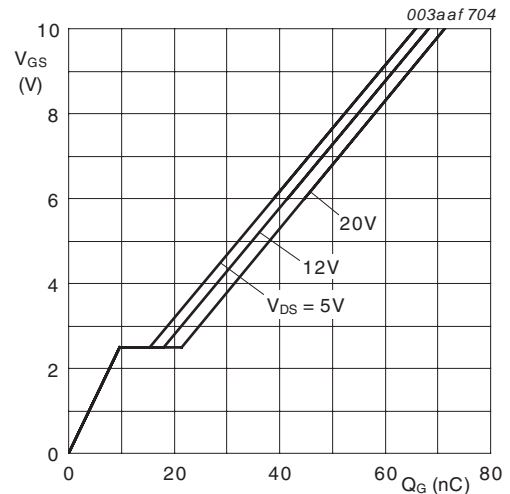
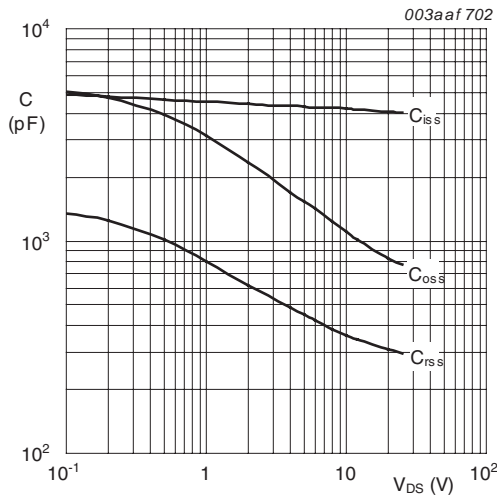
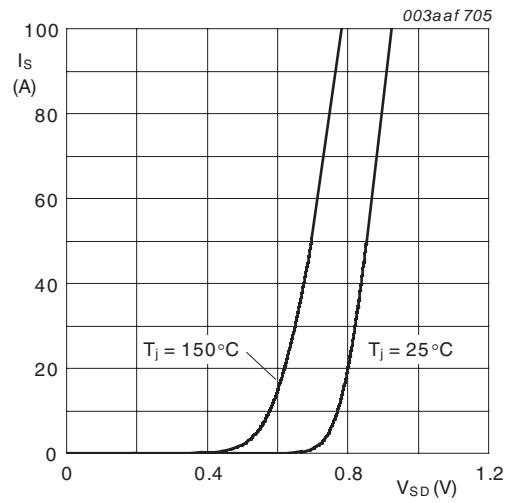


Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 17. Source current as a function of source-drain voltage; typical values

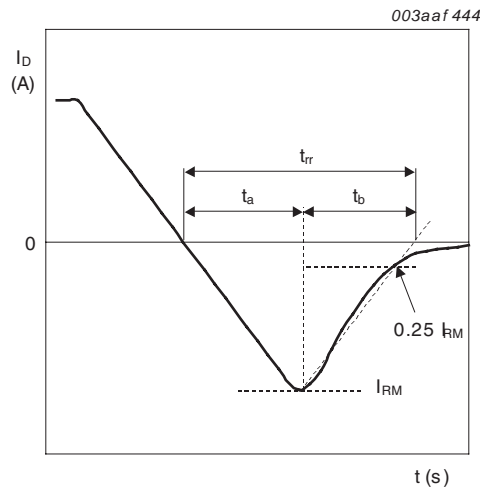


Fig 18. Reverse recovery timing definition

8. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669

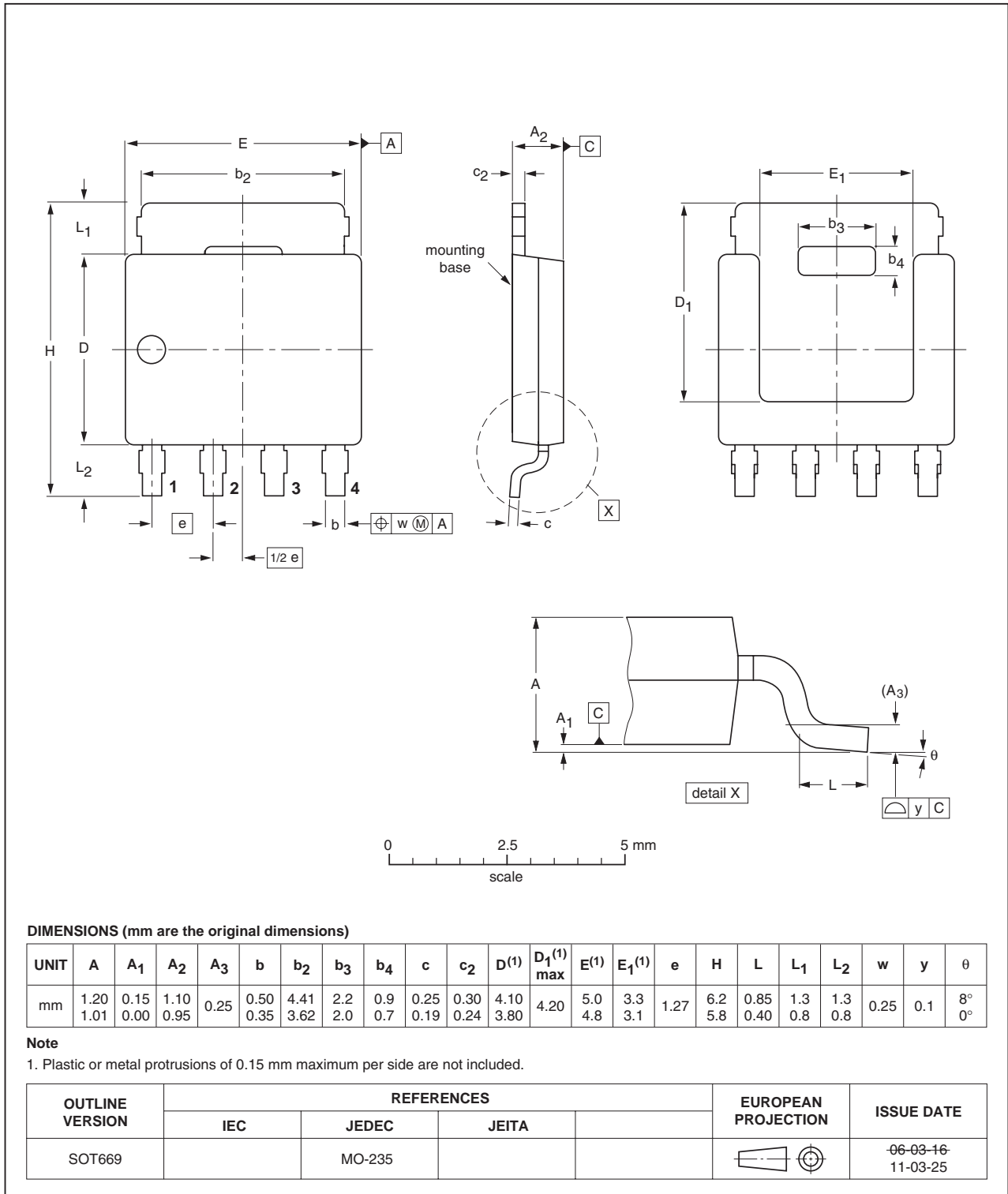


Fig 19. Package outline SOT669 (LPAK; Power-SO8)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R2-25YLC v.1	20110502	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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