



**THE DATASHEET OF
UC2827DW-1G4**



BUCK CURRENT/VOLTAGE FED PUSH-PULL PWM CONTROLLERS

 Check for Samples: [UC2827-1](#), [UC2827-2](#), [UC3827-1](#), [UC3827-2](#)

FEATURES

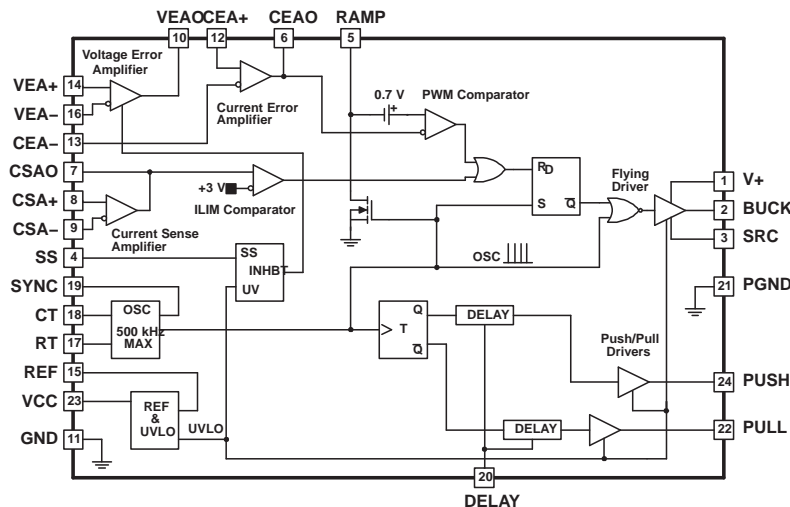
- Ideal for Multiple Output and/or High Voltage Output Voltage Converters
- Up to 500 kHz Operation
- High Voltage, High Current Floating Driver for Buck Converter Stage
- UC3827-1 Current Fed Controller has Push-Pull Drivers with Overlapping Conduction Periods
- UC3827-2 Voltage Fed Controller has Push-Pull Drivers with Nonoverlapping Conduction Periods
- Average Current Mode, Peak Current Mode or Voltage Mode with Input Voltage Feedforward Control for Buck Power Stage
- Wide Bandwidth, Low Offset, Differential Current Sense Amplifier
- Precise Short Circuit Current Control

DESCRIPTION

The UC3827 family of controller devices provides an integrated control solution for cascaded buck and push-pull converters. These converters are known as current fed or voltage fed push-pull converters and are ideally suited for multiple output and/or high voltage output applications. In both current fed and voltage fed modes, the push-pull switches are driven at 50% nominal duty cycles and at one half the switching frequency of the buck stage. In the current fed mode, the two switches are driven with a specified over-lap period to prevent ringing and voltage stress on the devices. In the voltage fed mode, the two switches are driven with a specified gap time between the switches to prevent shorting the transformer across the energy storage capacitor and to prohibit excessive currents flowing through the devices.

The converter's output voltage is regulated by pulse width modulation of the buck switch. The UC3827 contains complete protection and PWM control functions for the buck converter. Easy control of the floating switch is accomplished by the floating drive circuitry. The gate drive waveform is level shifted to support an input voltage up to $72 V_{DC}$.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (CONTINUED)

The UC3827 can be set up in traditional voltage mode control using input voltage feedforward technique or in current mode control. Using current mode control prevents potential core saturation of the push-pull transformer due to mismatches in timing and in component tolerances. With average current mode control, precise control of the inductor current feeding the push-pull stage is possible without the noise sensitivity associated with peak current mode control. The UC3827 average current mode loop can also be connected in parallel with the voltage regulation loop to assist only in fault conditions.

Other valuable features of the UC3827 include bidirectional synchronization capability, user programmable overlap time (UC3827-1), user programmable gap time (UC3827-2), a high bandwidth differential current sense amplifier, and soft start circuitry.

ORDERING INFORMATION⁽¹⁾

T _A = T _J	PUSH-PULL TOPOLOGY	PACKAGES		
		SOIC-24	PDIP-24	PLCC-28
-40°C to 85°C	Current Fed	UC2827DW-1	UC2827N-1	-
	Voltage Fed	UC2827DW-2	UC2827N-2	-
0°C to 70°C	Current Fed	UC3827DW-1	UC3827N-1	UC3827Q-1
	Voltage Fed	UC3827DW-2	UC3827N-2	-

(1) The DW and Q packages are also available taped and reeled. Add a TR suffix to the device type (i.e., UC2827DWTR-1).

THERMAL INFORMATION

THERMAL METRIC		UC2827-1, UC2827-2, UC3827-1, UC3827-2	UC2827-1, UC2827-2, UC3827-1, UC3827-2	UNITS
		N	J	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽¹⁾	60	70 to 80	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽²⁾	30	28	

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

THERMAL INFORMATION

THERMAL METRIC		UC2827-1, UC2827-2, UC3827-1, UC3827-2	UC2827-1, UC2827-2, UC3827-1, UC3827-2	UNITS
		DW	⁽¹⁾ QLCC	
		28 PINS	28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	71 to 83	40 to 65	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	24	30	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		UC2827-1 UC2827-2 UC3827-1 UC3827-2	UNITS
Supply voltage, VCC		20	
Input voltage range	CEAO, CEA+, CEA-, CSAO, CSA+, CSA-, CT, DELAY, PUSH, PULL, RAMP, RT, SS, SYNC, VEA+, VEA0,	-0.3 to 5	V
	V+ and BUCK	90	
	SRC	90-VCC	
BUCK driver	I/O continuous	±250	mA
	I/O peak	±1	A
PUSH/PULL driver	I/O continuous	±200	mA
	I/O peak	±0.8	A
Storage temperature		-65 to 150	°C
Junction temperature		-55 to 150	
Lead temperature (soldering, 10 sec)		300	

(1) Voltages are referenced to ground. Currents are positive into, negative out of the specified terminal. Consult *Packaging* section of databook for thermal limitations and considerations of packages.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{VCC} = 15\text{ V}$, $V_{V+} = 14.3\text{ V}$, $C_{CT} = 340\text{ pF}$, $R_{RT} = 10\text{ k}\Omega$, $R_{DELAY} = 24.3\text{ k}\Omega$, $V_{SRC} = V_{GND} = V_{BUCK} = V_{PUSH} = V_{PULL}$ outputs no load, $T_J = T_A$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
	VCC UVLO, Turn-on		8.3	8.8	9.5	V
	Hysteresis		0.9	1.2	1.5	V
I_{VCC}	Supply current start	$V_{VCC} = 8\text{ V}$			1000	μA
I_{VCC}	Supply current run			32	45	mA
	I_{V+} buck high		0.2	1	2	mA
VOLTAGE ERROR AMPLIFIER						
	I_B			0.5	3	μA
	VIO				10	mV
	AVOL		80	95		dB
	GBW ⁽¹⁾ Gain bandwidth		1	4		MHz
V_{OL}	Low-level output voltage	$I_{VEAO} = 0\text{ }\mu\text{A}$ (No load)		0.3	0.5	V
V_{OH}	High-level output voltage	$I_{VEAO} = 0\text{ }\mu\text{A}$ (No load)	2.85	3	3.20	V
CURRENT SENSE AMPLIFIER						
	I_B			-1	-5	μA
	VIO				5	mV
	AVOL		80	110		dB
	GBW ⁽¹⁾ Gain bandwidth		15	29		MHz
V_{OL}	Low-level output voltage	$I_{CEAO} = 0\text{ }\mu\text{A}$ (No load)		0.25	0.5	V
V_{OH}	High-level output voltage	$I_{CEAO} = 0\text{ }\mu\text{A}$ (No load)	3	3.3		V
	CMRR Common mode range ⁽¹⁾		-0.3		2	V

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, $V_{VCC} = 15\text{ V}$, $V_{V+} = 14.3\text{ V}$, $C_{CT} = 340\text{ pF}$, $R_{RT} = 10\text{ k}\Omega$, $R_{DELAY} = 24.3\text{ k}\Omega$, $V_{SRC} = V_{GND} = V_{BUCK} = V_{PUSH} = V_{PULL}$ outputs no load, $T_J = T_A$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT ERROR AMPLIFIER						
I_B				-1	-5	μA
V_{IO}					10	mV
AV_{OL}			80	110		dB
$GBW^{(2)}$	Gain bandwidth	At 100 kHz, Measure Gain	2	4.5		MHz
V_{OL}		$I_{CEAO} = 0\text{ }\mu\text{A}$ (No Load)		0.25	0.5	V
V_{OH}		$I_{CEAO} = 0\text{ }\mu\text{A}$ (No Load)	3.3	3.5		V
$CMRR$	Common mode range ⁽²⁾		-0.3		5	V
OSCILLATOR SECTION						
f_{OSC}	Frequency		180	220	250	kHz
$I_{CT(dsch)}$	CT discharge current	3.5V at CT when CT removed	5			mA
PWM COMPARATOR						
D_{MAX}	Minimum duty cycle	200 kHz			0%	
D_{MAX}	Maximum duty cycle	200 kHz	85%	91%	95%	
BUCK OUTPUT STAGE						
t_{RISE}	Rise time	1 nF Load ⁽³⁾		40	100	ns
t_{FALL}	Fall time	1 nF, Load		30	80	ns
V_{OH}	High-level output voltage	$I_{BUCK} = -15\text{ mA}$, $V_+ -BUCK^{(4)}$		1.5	2.5	V
		$I_{BUCK} = -150\text{ mA}$, $V_+ -BUCK^{(4)}$		2	2.5	V
V_{OL}	Low-level output voltage	$I_{BUCK} = 15\text{ mA}^{(5)}$		0.2	0.4	V
		$I_{BUCK} = 150\text{ mA}^{(5)}$		0.7	1.2	V
PUSH/PULL OUTPUT STAGES						
t_{RISE}	Rise time	1 nF load		50	100	ns
t_{FALL}	Fall time	1 nF load		35	100	ns
	Overlap time	UCx827-1 1 nF loads ⁽⁶⁾	100	250	400	ns
	Nonoverlapping time ⁽⁷⁾	UCx827-2	100	250	500	ns
V_{OH}	High-level output voltage	$I_{PUSH/PULL} = -10\text{ mA}$, $V_{CC} - PUSH^{(8)}$		2	3	V
		$I_{PUSH/PULL} = -100\text{ mA}$, $V_{CC} - PUSH^{(8)}$		2.5	3	V
V_{OL}	Low-level output voltage	$I_{PUSH/PULL} = 10\text{ mA}^{(8)}$		0.2	0.8	V
		$I_{PUSH/PULL} = 100\text{ mA}^{(8)}$		0.6	1.2	V
REFERENCE						
	Reference voltage		4.8	5	5.2	V
I_{SC}	Short-circuit current	$V_{REF} = 0\text{ V}$	-35	-50	-65	mA
	Line regulation	$0.5\text{ V} < V_{VCC} < 20\text{ V}$		5	20	mV
	Load regulation	$0\text{ mA} < I_O < 10\text{ mA}$		8	20	mV
SOFT START						
V_{OL}	Low-level output voltage saturation	$V_{VCC} = 7\text{ V}$		250	500	mV
I_{SS}	Soft-start current		-5	-12	-25	μA

(2) Ensured by design. Not production tested.

(3) Measure the rise time from when BUCK crosses 1 V until it crosses 9 V.

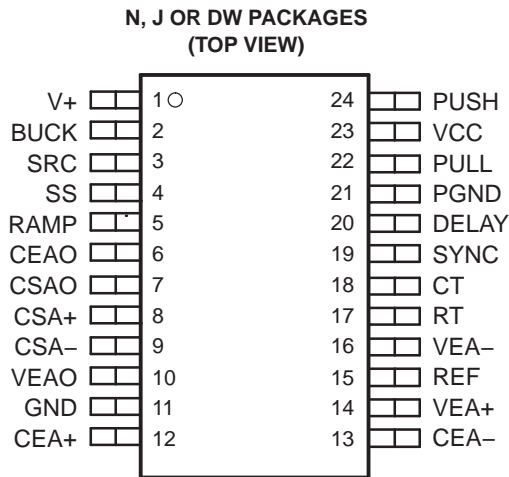
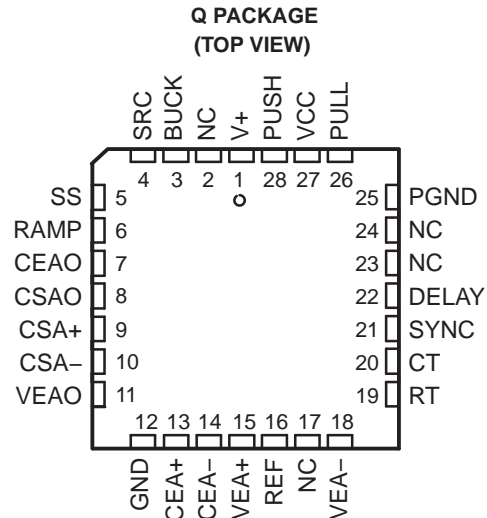
(4) To force BUCK high, force $V_{CSAO} = 2.5\text{ V}$, $V_{CEAO} = 2.5\text{ V}$, a 25-k Ω pulldown resistor from RAMP to ground, and $V_{CT} = 0.5\text{ V}$.

(5) To force BUCK low, force $V_{CSAO} = 2.5\text{ V}$, $V_{CEAO} = 2.5\text{ V}$, a 10-k Ω pulldown resistor from RAMP to ground, and $V_{CT} = 3.5\text{ V}$.

(6) The overlap time is measured from the point at which the rising edge of PUSH/PULL crosses 5 V until the falling edge of PULL/PUSH crosses 5 V.

(7) The non-overlap time is measured from the point at which the falling edge of PUSH/PULL crosses 5 V until the rising edge of PULL/PUSH crosses 5 V.

(8) To toggle PUSH or PULL into a desired state, pulse CT from 0.5 V to 3.5 V. PUSH and PULL toggle on the rising edge of CT.

CONNECTION DIAGRAMS
**DIL-24 (N or J, DW PACKAGES)
(TOP VIEW)**

**PLCC-28 (Q PACKAGE)
(TOP VIEW)**


NC – No internal connection

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	N or DW	Q		
BUCK	2	3	O	Output of the buck PWM controller. The BUCK output is a floating driver, optimized for controlling the gate of an N-channel MOSFET. The peak sink and source currents are 1 A. V _{CC} undervoltage faults disables BUCK to an off condition (low).
CEA+	12	13	I	Non-inverting input of the current error amplifier.
CEA-	13	14	I	Inverting input of the current error amplifier
CEAO	6	7	O	Output of the current error amplifier and the inverting input of the PWM comparator of the buck converter.
CSA+	8	9	I	Noninverting input of the current sense amplifier.
CSA-	9	10	I	Inverting input of the current sense amplifier.
CSAO	7	8	O	Output of the current sense amplifier and the noninverting input of the current limit comparator. When the signal level on this pin exceeds the 3V threshold of the current limit comparator, the buck gate drive pulse is terminated. This feature is useful to implement cycle-by-cycle current limiting for the buck converter.
CT	18	20	I	Provides for the timing capacitor which is connected between CT and GND. The oscillator frequency is set by CT and a resistor RT, connected between pin RT and GND. The CT discharge current is approximately 40 x the bias current through the resistor connected to RT. A practical maximum value for the discharge current is 20 mA. The frequency of the oscillator is given by equation ⁽¹⁾
DELAY	20	22	I	A resistor to GND programs the overlap time of the PUSH and PULL outputs of the UC3827-1 and the dead time of the PUSH and PULL outputs of the UC3827-2. The minimum value of the resistor, R _{DELAY} , is 18 kΩ. The delay or overlap time is given by equation ⁽²⁾
GND	11	12	-	Ground reference for all sensitive setup components not related to driving the outputs. They include all timing, voltage sense, current sense, and bypass components.
PGND	21	25	-	Ground connection for the PUSH and PULL outputs. PGND must be connected to GND at a single point on the printed circuit board. This is imperative to prevent large, high frequency switching currents flowing through the ground metalization inside the device.
PULL	22	26	O	Ground referenced output to drive an N-channel MOSFET. The PULL and the PUSH outputs are driving the two switches of the push-pull converter with complementary signals at close to a 50% duty cycle. Any undervoltage faults will disable PULL to an off condition (low).

$$(1) f_{OSC} = \frac{0.77}{R_{RT} \times C_{CT}} \text{ (Hz)}$$

$$(2) t_{DELAY} = \frac{R_{DELAY}}{200\Omega} \times 10^{-9} \text{ (s)}$$

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	N or DW	Q		
PUSH	24	28	O	Ground referenced output to drive an N-channel MOSFET. The PULL and the PUSH outputs are driving the two switches of the push-pull converter with complementary signals at close to a 50% duty cycle. Any undervoltage faults disables PUSH to an off condition (low).
RAMP	5	6	I	The RAMP voltage, after a 700 mV internal level shift, is fed to the noninverting input of the buck PWM comparator. A resistor to V_{IN} and a capacitor to GND provide an input voltage feedforward signal for the buck controller in voltage mode control. In peak current mode control, the RAMP pin receives the current signal of the buck converter. In an average current mode setup, the RAMP pin has a linearly increasing ramp signal. This waveform may be generated either by connecting RAMP directly to CT, or by connecting both a resistor from VCC to RAMP and a capacitor from RAMP to GND.
REF	15	16	O	The output of the +5V on board reference. Bypass this pin with a capacitor to GND. The reference is off when the chip is in undervoltage lockout mode.
RT	17	19	I	A resistor to GND programs the charge current of the timing capacitor connected to CT. The charge current approximately equals that shown in equation ⁽³⁾ . The charge current should be less than 500 μ A to keep CT's discharge peak current less than 20 mA, which is CT's maximum practical discharge value. The discharge time, which sets the maximum duty cycle, is set internally and is influenced by the charge current.
SRC	3	4	I	The source connection for the floating buck switch. The voltage on the SRC pin can exceed VCC but must be lower than $90 V - V_{VCC}$. Also, during turn-off transients of the buck switch, the voltage at SRC can go to $-2V$.
SS	4	5	O	Soft-start pin requires a capacitor to GND. During soft-start the output of the voltage error amplifier is clamped to the soft-start capacitor voltage which is slowly charged by an internal current source. In UVLO, SS is held low.
SYNC	19	21	I	A bidirectional pin for the oscillator, used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4 V. The SYNC voltage is 3.6 V when the oscillator capacitor, CT, is discharged. Otherwise it is 0 V. If the recommended synchronization circuit is not used, a 1 k Ω or lower value resistor from SYNC to GND may be needed to increase the fall time of the signal at SYNC.
VCC	23	27	I	A voltage source connected to this pin supplies the power for the UC3827. It is recommended to bypass this pin to both GND and PGND ground connections with good quality high frequency capacitors
VEA+	14	15	I	Non-inverting input of the voltage error amplifier
VEA-	16	18	I	Inverting input of the voltage error amplifier
VEAO	10	11	O	Output of the voltage error amplifier
V+	1	1	I	Supply voltage for the buck output. The floating driver of the UC3827 uses the bootstrap technique which requires a reservoir capacitor to store the required energy for the on time of the buck switch. A diode must be connected from VCC to V+ to charge the reservoir capacitor. This diode must be able to withstand V_{IN} . The reservoir capacitor must be connected between V+ and SRC.

(3)
$$I_{RT} = \frac{2.5 V}{R_{RT}}$$

APPLICATION INFORMATION

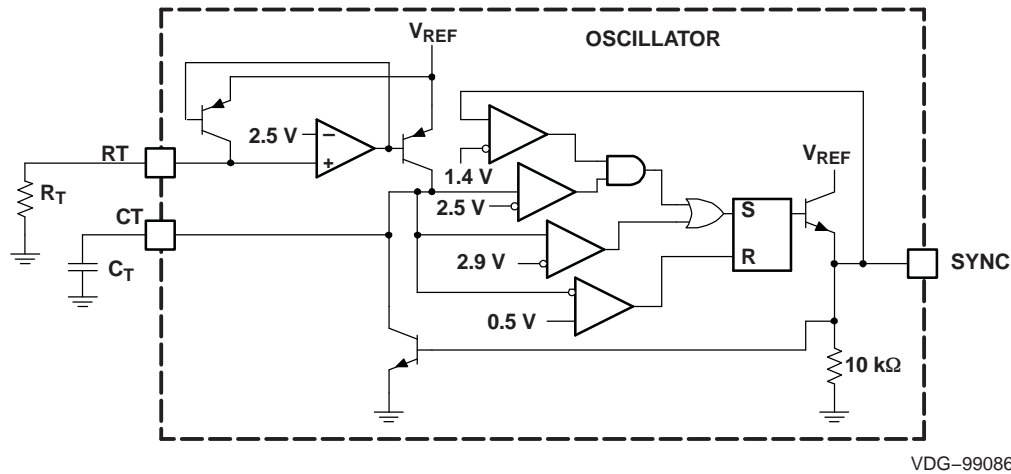


Figure 1. Oscillator Block With External Connections

CIRCUIT BLOCK DESCRIPTION

PWM Oscillator

The oscillator block diagram with external connections is shown in Equation 1. A resistor (R_T) connected to pin RT sets the linear charge current:

$$I_{RT} = \frac{2.5 \text{ V}}{R_{RT}} \quad (1)$$

The timing capacitor (C_{CT}) is linearly charged with the charge current forcing the OSC pin to charge to a 3.4 V threshold. After exceeding this threshold, the RS flip-flop is set driving $CLKSYN$ high and R_{DEAD} low which discharges C_{CT} . C_T continues to discharge until it reaches a 0.5 V threshold and resets the RS flip-flop which repeats the charging sequence as shown in Figure 2

As shown in Figure 3, several oscillators are synchronized to the highest free running frequency by connecting 100 pF capacitors in series with each $CLKSYN$ pin and connecting the other side of the capacitors together forming the $CLKSYN$ bus. The $CLKSYN$ bus is then pulled down to ground with a resistance of approximately 10k. Referring to Figure 1, the synchronization threshold is 1.4 V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5 V. This allows units, once they discharge below 2.5 V, to continue through the current discharge and subsequent charge cycles whether or not other units on the $CLKSYN$ bus are still synchronizing. This requires the frequency of all free running oscillators to be within 17% of each other to assure synchronization.

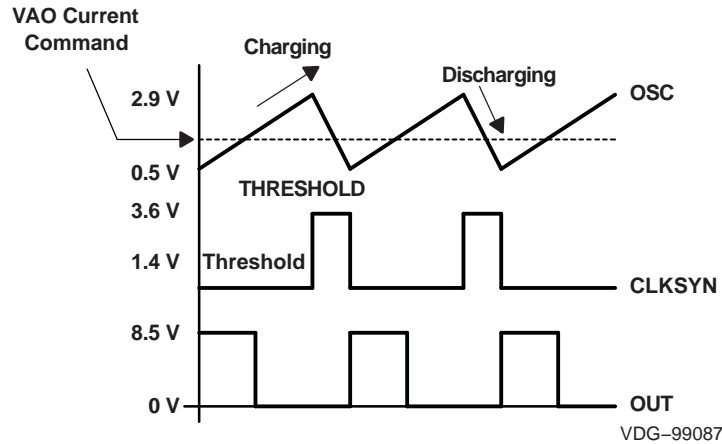


Figure 2. Oscillator and PWM Output Waveform

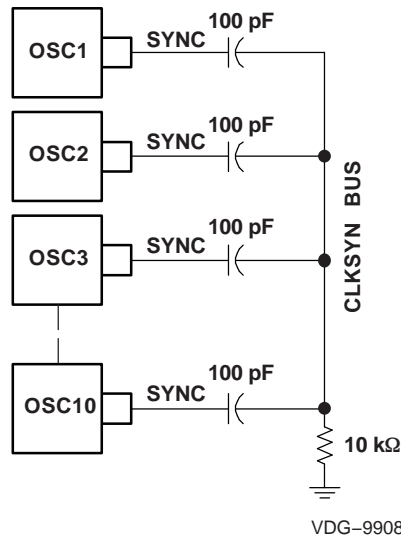


Figure 3. Oscillator Synchronization Connection Diagram

REVISION HISTORY

REVISION	DATE OF CHANGE	DESCRIPTION
SLUS365A	8/2005	Improved CMRR of CSA from (0 - 2 V) to (-0.3 - 2 V) Improved CMRR of CEA from (0 - 5 V) to (-0.3 - 5 V)
SLUS365D	4/2011	Updated the Thermal Information Section

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2827DW-1	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	UC2827DW-1	Samples
UC2827DW-2	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	UC2827DW-2	Samples
UC2827DWTR-1	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	UC2827DW-1	Samples
UC2827DWTR-1G4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	UC2827DW-1	Samples
UC3827DW-1	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	UC3827DW-1	Samples
UC3827DW-2	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	UC3827DW-2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2827DWTR-1	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



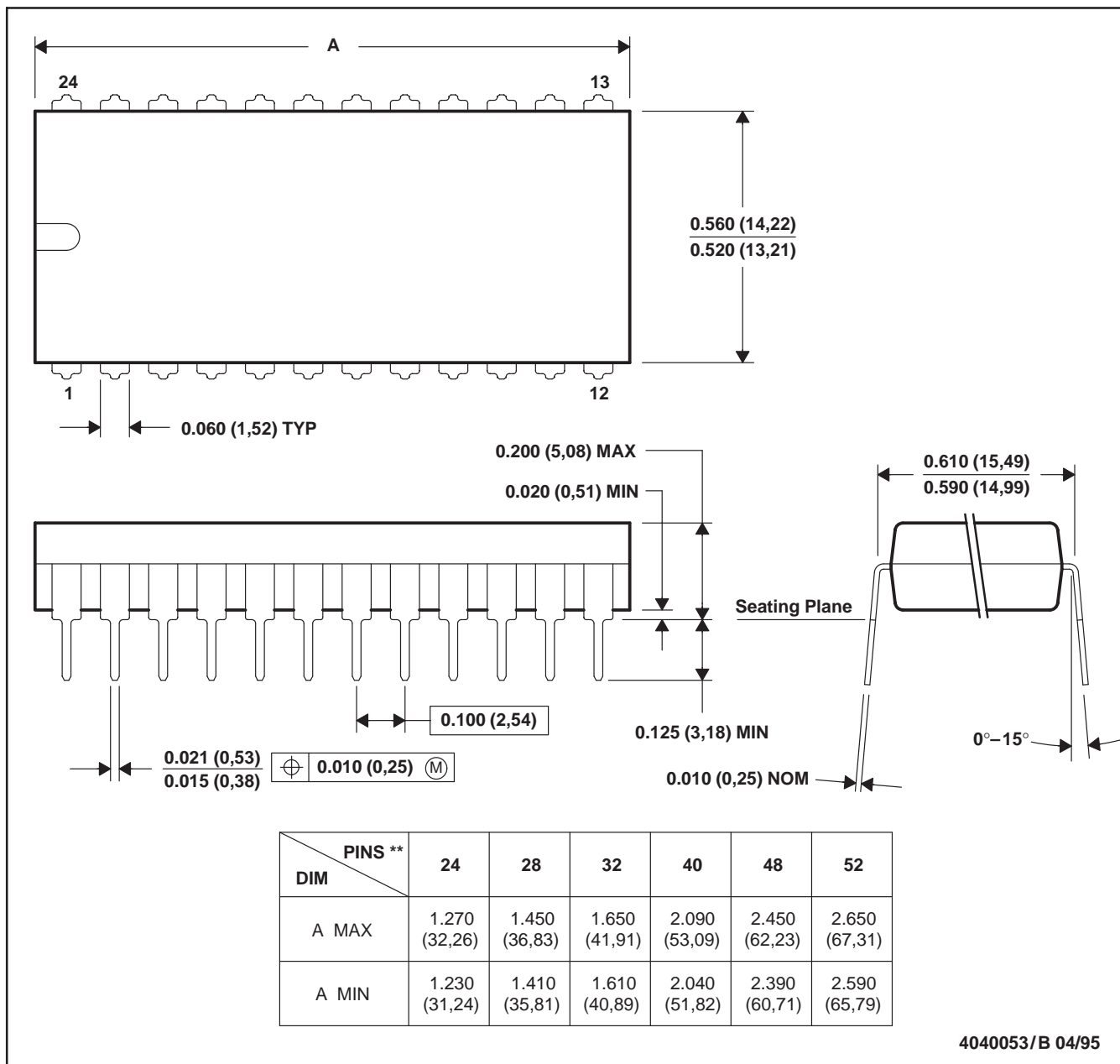
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2827DWTR-1	SOIC	DW	24	2000	367.0	367.0	45.0

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

DW (R-PDSO-G24)

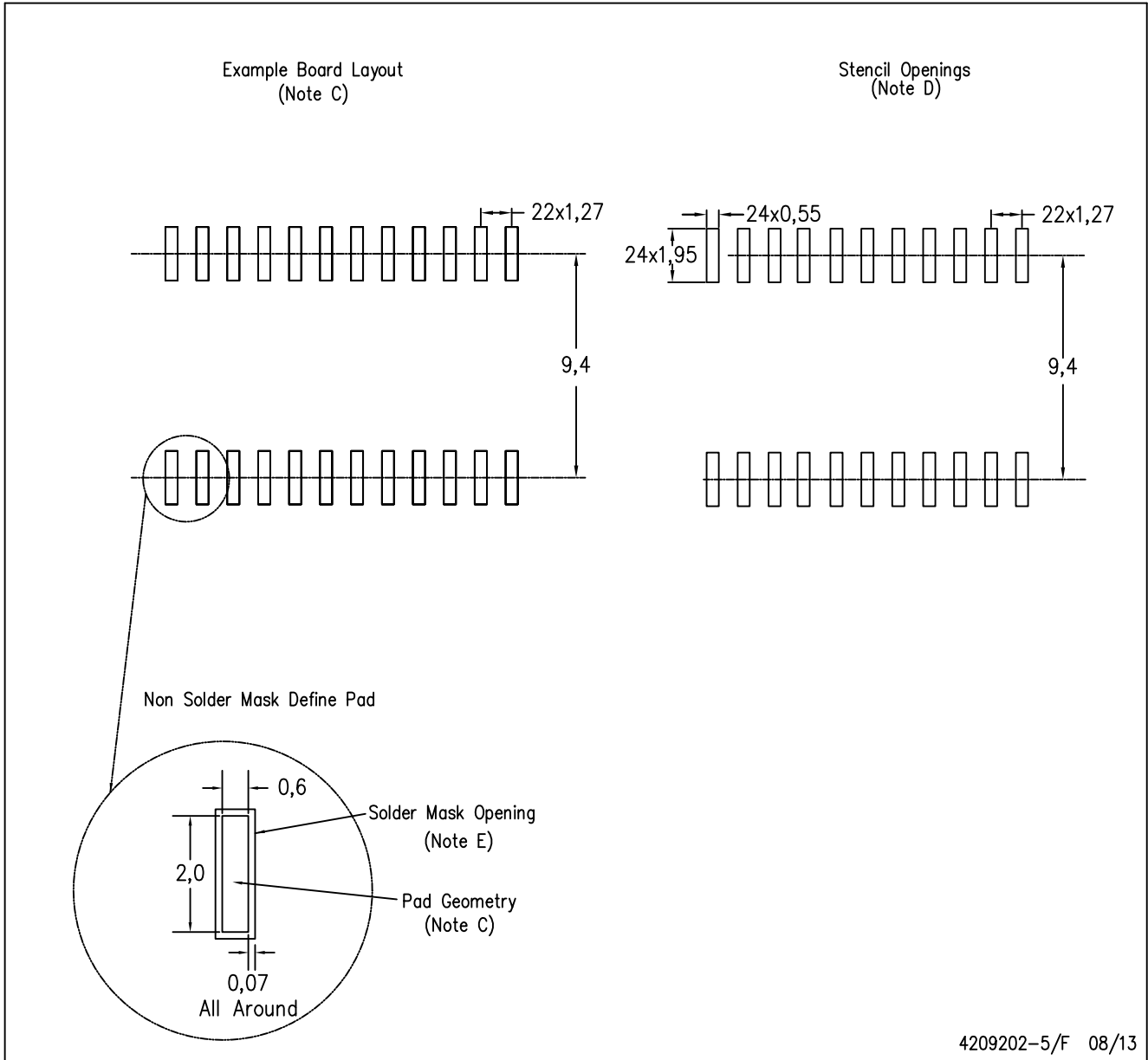
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View UC2827DW-1G4](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management