THE DATASHEET OF

AD9220ARSZ-REEL

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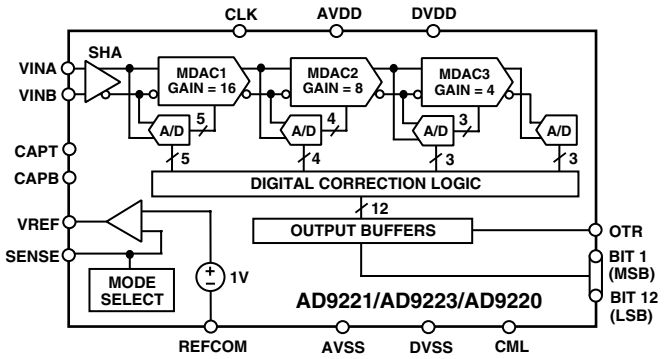
Complete 12-Bit 1.5/3.0/10.0 MSPS Monolithic A/D Converters

AD9221/AD9223/AD9220

FEATURES

Monolithic 12-Bit A/D Converter Product Family
Family Members Are: AD9221, AD9223, and AD9220
Flexible Sampling Rates: 1.5 MSPS, 3.0 MSPS, and 10.0 MSPS
Low Power Dissipation: 59 mW, 100 mW, and 250 mW
Single 5 V Supply
Integral Nonlinearity Error: 0.5 LSB
Differential Nonlinearity Error: 0.3 LSB
Input Referred Noise: 0.09 LSB
Complete On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 70 dB
Spurious-Free Dynamic Range: 86 dB
Out-of-Range Indicator
Straight Binary Output Data
28-Lead SOIC and 28-Lead SSOP

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9221, AD9223, and AD9220 are a generation of high performance, single supply 12-bit analog-to-digital converters. Each device exhibits true 12-bit linearity and temperature drift performance[1] as well as 11.5-bit or better ac performance.[2] The AD9221/AD9223/AD9220 share the same interface options, package, and pinout. Thus, the product family provides an upward or downward component selection path based on performance, sample rate and power. The devices differ with respect to their specified sampling rate, and power consumption, which is reflected in their dynamic performance over frequency.

The AD9221/AD9223/AD9220 combine a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid and monolithic implementations at a fraction of the power consumption and cost. Each device is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and-hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. The devices use a multistage differential pipelined architecture with digital output error correction logic to provide 12-bit accuracy at the specified data rates and to guarantee no missing codes over the full operating temperature range.

The input of the AD9221/AD9223/AD9220 is highly flexible, allowing for easy interfacing to imaging, communications, medical, and data-acquisition systems. A truly differential input structure allows for both single-ended and differential input interfaces of varying input spans. The sample-and-hold amplifier (SHA) is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels as well as sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. Also, the AD9221/AD9223/AD9220 is well suited for communication systems employing Direct-IF down conversion since the SHA in the differential input mode can achieve excellent dynamic performance *far beyond* its specified Nyquist frequency.[2]

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9221/AD9223/AD9220 family offers a complete single-chip sampling 12-bit, analog-to-digital conversion function in pin compatible 28-lead SOIC and SSOP packages.

Flexible Sampling Rates—The AD9221, AD9223, and AD9220 offer sampling rates of 1.5 MSPS, 3.0 MSPS, and 10.0 MSPS, respectively.

Low Power and Single Supply—The AD9221, AD9223, and AD9220 consume only 59 mW, 100 mW, and 250 mW, respectively, on a single 5 V power supply.

Excellent DC Performance Over Temperature—The AD9221/AD9223/AD9220 provide 12-bit linearity and temperature drift performance.[1]

Excellent AC Performance and Low Noise—The AD9221/AD9223/AD9220 provide better than 11.3 ENOB performance and have an input referred noise of 0.09 LSB rms.[2]

Flexible Analog Input Range—The versatile on-board sample-and-hold (SHA) can be configured for either single-ended or differential inputs of varying input spans.

NOTES
[1]Excluding internal voltage reference.
[2]Depends on the analog input configuration.

REV. E

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
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AD9221/AD9223/AD9220–SPECIFICATIONS

DC SPECIFICATIONS

(AVDD = 5 V, DVDD = 5 V, f_{SAMPLE} = Max Conversion Rate, V_{REF} = 2.5 V, VINB = 2.5 V, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD9221	AD9223	AD9220	Unit
RESOLUTION	12	12	12	Bits min
MAX CONVERSION RATE	1.5	3	10	MHz min
INPUT REFERRED NOISE (TYP)				
V_{REF} = 1 V	0.23	0.23	0.23	LSB rms typ
V_{REF} = 2.5 V	0.09	0.09	0.09	LSB rms typ
ACCURACY				
Integral Nonlinearity (INL)	±0.4	±0.5	±0.5	LSB typ
	±1.25	±1.25	±1.25	LSB max
Differential Nonlinearity (DNL)	±0.3	±0.3	±0.3	LSB typ
	±0.75	±0.75	±0.75	LSB max
INL[1]	±0.6	±0.6	±0.7	LSB typ
DNL[1]	±0.3	±0.3	±0.35	LSB typ
No Missing Codes	12	12	12	Bits Guaranteed
Zero Error (@ 25°C)	±0.3	±0.3	±0.3	% FSR max
Gain Error (@ 25°C)[2]	±1.5	±1.5	±1.5	% FSR max
Gain Error (@ 25°C)[3]	±0.75	±0.75	±0.75	% FSR max
TEMPERATURE DRIFT				
Zero Error	±2	±2	±2	ppm/°C typ
Gain Error[2]	±26	±26	±26	ppm/°C typ
Gain Error[3]	±0.4	±0.4	±0.4	ppm/°C typ
POWER SUPPLY REJECTION				
AVDD, DVDD (+5 V ± 0.25 V)	±0.06	±0.06	±0.06	% FSR max
ANALOG INPUT				
Input Span (with V_{REF} = 1.0 V)	2	2	2	V p-p min
Input Span (with V_{REF} = 2.5 V)	5	5	5	V p-p max
Input (VINA or VINB) Range	0	0	0	V min
	AVDD	AVDD	AVDD	V max
Input Capacitance	16	16	16	pF typ
INTERNAL VOLTAGE REFERENCE				
Output Voltage (1 V Mode)	1	1	1	V typ
Output Voltage Tolerance (1 V Mode)	±14	±14	±14	mV max
Output Voltage (2.5 V Mode)	2.5	2.5	2.5	V typ
Output Voltage Tolerance (2.5 V Mode)	±35	±35	±35	mV max
Load Regulation[4]	2.0	2.0	2.0	mV max
REFERENCE INPUT RESISTANCE	5	5	5	kΩ typ
POWER SUPPLIES				
Supply Voltages				
AVDD	5	5	5	V (±5% AVDD Operating)
DVDD	2.7 to 5.25	2.7 to 5.25	2.7 to 5.25	V
Supply Current				
IAVDD	14.0	26	58	mA max
	11.8	20	51	mA typ
IDVDD	0.5	0.5	4.0	mA max
	0.02	0.02	<1.0	mA typ
POWER CONSUMPTION	59.0	100	254	mW typ
	70.0	130	310	mW max

NOTES

[1]V_{REF} = 1 V.

[2]Including internal reference.

[3]Excluding internal reference.

[4]Load regulation with 1 mA load current (in addition to that required by the AD9221/AD9223/AD9220).

Specification subject to change without notice.

AC SPECIFICATIONS

(AVDD = 5 V, DVDD= 5 V, f_{SAMPLE} = Max Conversion Rate, V_{REF} = 1.0 V, VINB = 2.5 V, DC Coupled/Single-Ended Input T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD9221	AD9223	AD9220	Unit
MAX CONVERSION RATE	1.5	3.0	10.0	MHz min
DYNAMIC PERFORMANCE				
Input Test Frequency 1 (VINA = –0.5 dBFS)	100	500	1000	kHz
Signal-to-Noise and Distortion (SINAD)	70.0	70.0	70	dB typ
	69.0	68.5	68.5	dB min
Effective Number of Bits (ENOBs)	11.3	11.3	11.3	dB typ
	11.2	11.1	11.1	dB min
Signal-to-Noise Ratio (SNR)	70.2	70.0	70.2	dB typ
	69.0	68.5	69.0	dB min
Total Harmonic Distortion (THD)	–83.4	–83.4	–83.7	dB typ
	–77.5	–76.0	–76.0	dB max
Spurious Free Dynamic Range (SFDR)	86.0	87.5	88.0	dB typ
	79.0	77.5	77.5	dB max
Input Test Frequency 2 (VINA = –0.5 dBFS)	0.50	1.50	5.0	MHz
Signal-to-Noise and Distortion (SINAD)	69.9	69.4	67.0	dB typ
	69.0	68.0	65.0	dB min
Effective Number of Bits (ENOBs)	11.3	11.2	10.8	dB typ
	11.2	11.1	10.5	dB min
Signal-to-Noise Ratio (SNR)	70.1	69.7	68.8	dB typ
	69.0	68.5	67.5	dB min
Total Harmonic Distortion (THD)	–83.4	–82.9	–72.0	dB typ
	–77.5	–75.0	–68.0	dB max
Spurious Free Dynamic Range (SFDR)	86.0	85.7	75.0	dB typ
	79.0	76.0	69.0	dB max
Full Power Bandwidth	25	40	60	MHz typ
Small Signal Bandwidth	25	40	60	MHz typ
Aperture Delay	1	1	1	ns typ
Aperture Jitter	4	4	4	ps rms typ
Acquisition to Full-Scale Step	125	43	30	ns typ

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

(AVDD = 5 V, DVDD = 5 V, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol		Unit
CLOCK INPUT			
High Level Input Voltage	V_{IH}	3.5	V min
Low Level Input Voltage	V_{IL}	1.0	V max
High Level Input Current (V_{IN} = DVDD)	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
DVDD = 5 V			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	4.5	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	0.1	V max
DVDD = 3 V			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	2.95	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.80	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	0.05	V max
Output Capacitance	C_{OUT}	5	pF typ

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AVDD = 5 V, DVDD = 5 V, C_L = 20 pF)

Parameter	Symbol	AD9221	AD9223	AD9220	Unit
Clock Period*	t_C	667	333	100	ns min
CLOCK Pulsewidth High	t_{CH}	300	150	45	ns min
CLOCK Pulsewidth Low	t_{CL}	300	150	45	ns min
Output Delay	t_{OD}	8	8	8	ns min
		13	13	13	ns typ
		19	19	19	ns max
Pipeline Delay (Latency)		3	3	3	Clock Cycles

*The clock period may be extended to 1 ms without degradation in specified performance @ 25°C.

Specifications subject to change without notice.

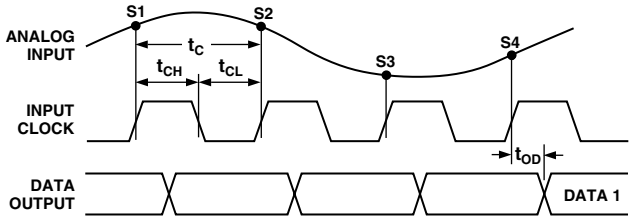


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
REFCOM	AVSS	–0.3	+0.3	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
VINA, VINB	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead SOIC

θ_{JA} = 71.4°C/W

θ_{JC} = 23°C/W

28-Lead SSOP

θ_{JA} = 63.3°C/W

θ_{JC} = 23°C/W

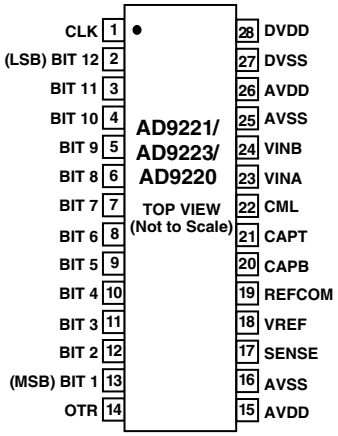
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9221AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9223AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9220AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9221ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9223ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9220ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9221-EB		Evaluation Board	
AD9223-EB		Evaluation Board	
AD9220-EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9221/AD9223/AD9220 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1	CLK	Clock Input Pin
2	BIT 12	Least Significant Data Bit (LSB)
3–12	BITS 11–2	Data Output Bit
13	BIT 1	Most Significant Data Bit (MSB)
14	OTR	Out of Range
15, 26	AVDD	5 V Analog Supply
16, 25	AVSS	Analog Ground
17	SENSE	Reference Select
18	VREF	Reference I/O
19	REFCOM	Reference Common
20	CAPB	Noise Reduction Pin
21	CAPT	Noise Reduction Pin
22	CML	Common-Mode Level (Midsupply)
23	VINA	Analog Input Pin (+)
24	VINB	Analog Input Pin (–)
27	DVSS	Digital Ground
28	DVDD	3 V to 5 V Digital Supply

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

Zero Error
The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Aperture Jitter
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

Aperture Delay
Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = \left(SINAD - 1.76\right) / 6.02$$

it is possible to get a measure of performance expressed as *N*, the effective number of bits.

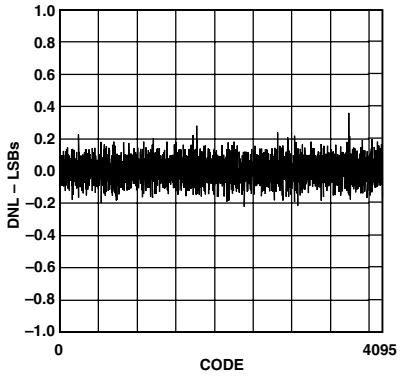
Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

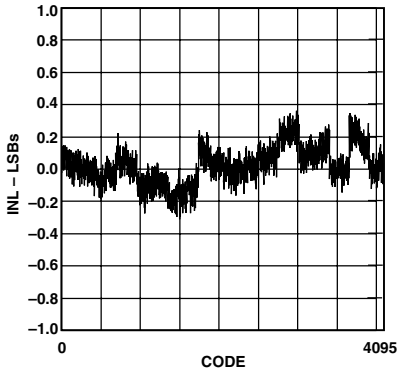
Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious Free Dynamic Range (SFDR)
SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

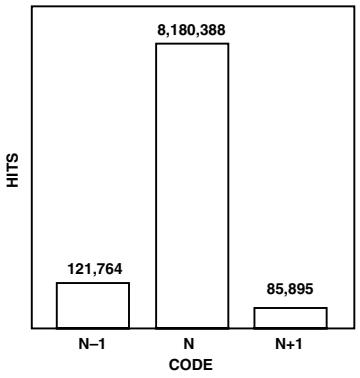
AD9221–Typical Performance Characteristics (AVDD = 5 V, DVDD = 5 V, f_{SAMPLE} = 1.5 MSPS, T_A = 25°C)



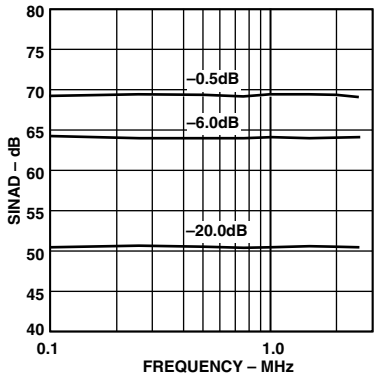
TPC 1. Typical DNL



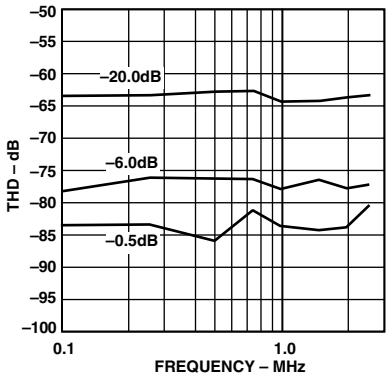
TPC 2. Typical INL



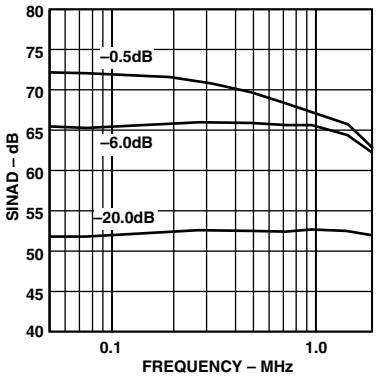
TPC 3. "Grounded-Input" Histogram (Input Span = 2 V p-p)



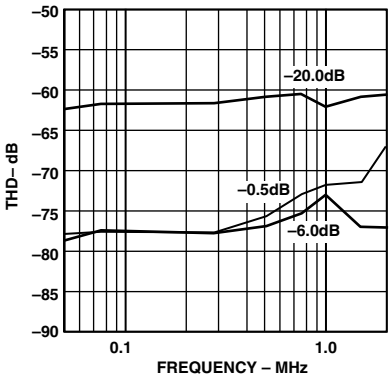
TPC 4. SINAD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)



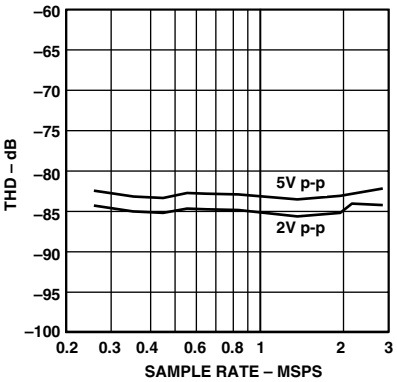
TPC 5. THD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)



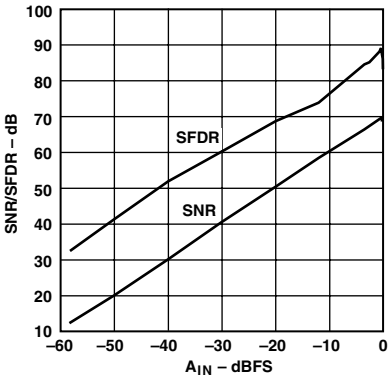
TPC 6. SINAD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)



TPC 7. THD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)

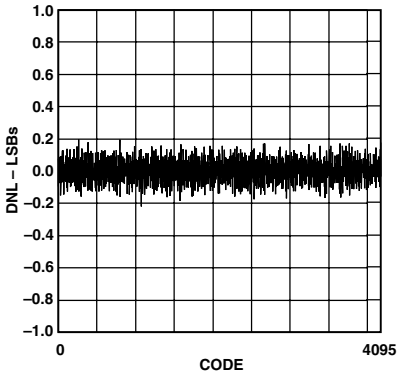


TPC 8. THD vs. Sample Rate (A_{IN} = –0.5 dB, f_{IN} = 500 kHz, V_{CM} = 2.5 V)

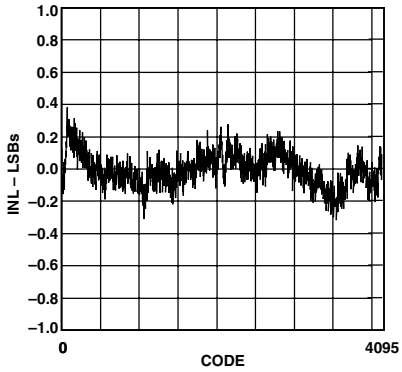


TPC 9. SNR/SFDR vs. A_{IN} (Input Amplitude) (f_{IN} = 500 kHz, Input Span = 2 V p-p, V_{CM} = 2.5 V)

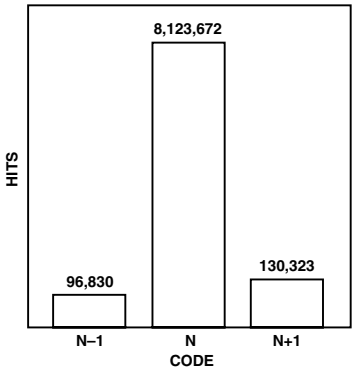
AD9223–Typical Performance Characteristics (AVDD = 5 V, DVDD = 5 V, f_{SAMPLE} = 3.0 MSPS, T_A = 25°C)



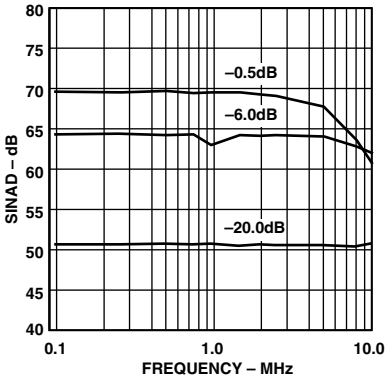
TPC 10. Typical DNL



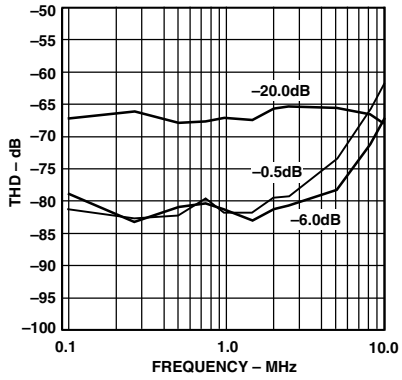
TPC 11. Typical INL



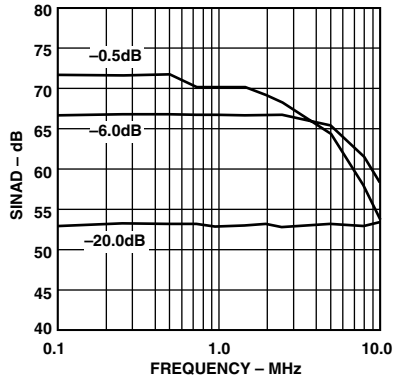
TPC 12. "Grounded-Input" Histogram (Input Span = 2 V p-p)



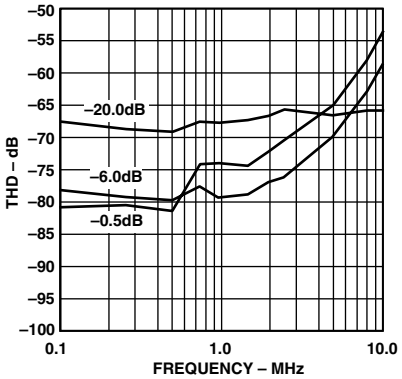
TPC 13. SINAD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)



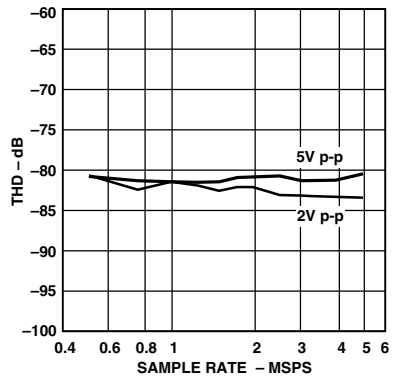
TPC 14. THD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)



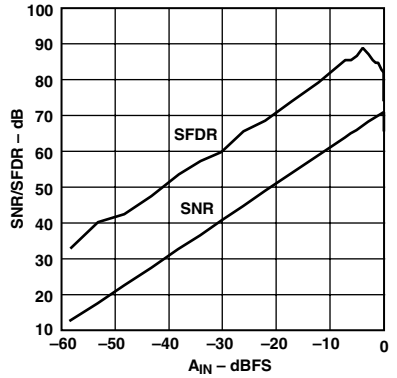
TPC 15. SINAD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)



TPC 16. THD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)

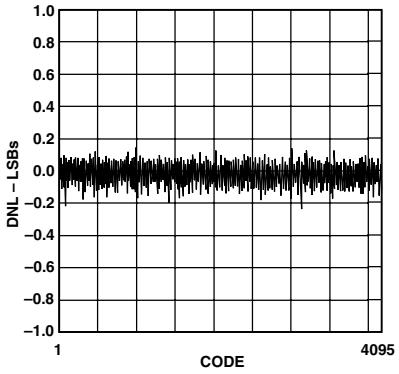


TPC 17. THD vs. Sample Rate (A_{IN} = –0.5 dB, f_{IN} = 500 kHz, V_{CM} = 2.5 V)

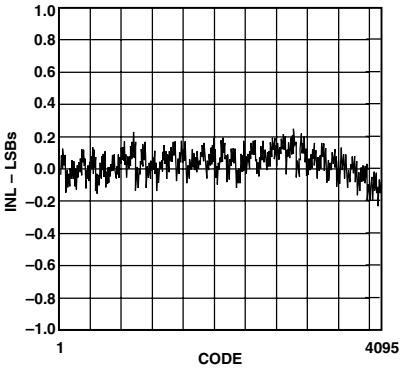


TPC 18. SNR/SFDR vs. A_{IN} (Input Amplitude) (f_{IN} = 1.5 MHz, Input Span = 2 V p-p, V_{CM} = 2.5 V)

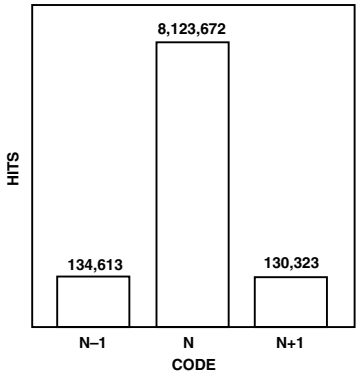
AD9220–Typical Performance Characteristics (AVDD = 5 V, DVDD = 5 V, f_{SAMPLE} = 10 MSPS, T_A = 25°C)



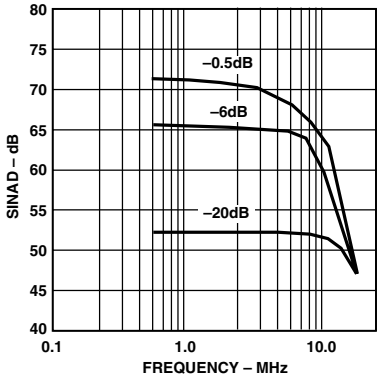
TPC 19. Typical DNL



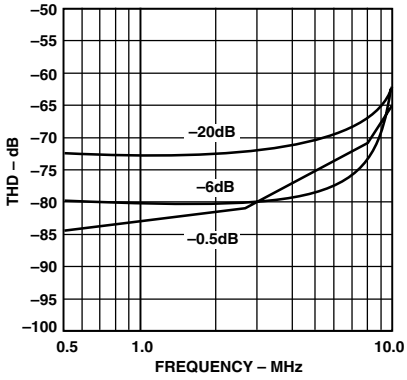
TPC 20. Typical INL



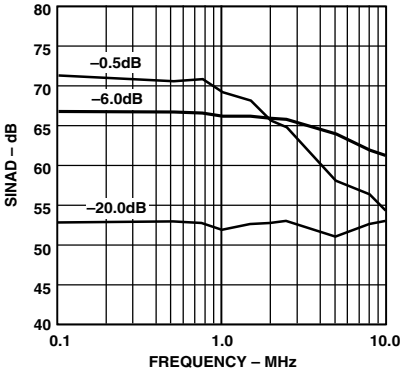
TPC 21. "Grounded-Input" Histogram (Input Span = 2 V p-p)



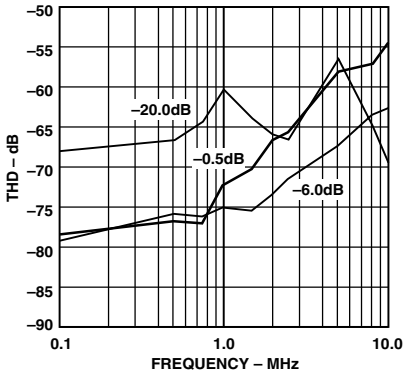
TPC 22. SINAD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)



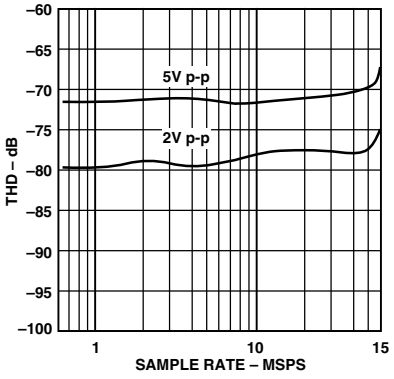
TPC 23. THD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)



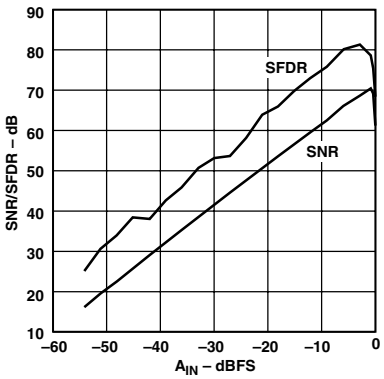
TPC 24. SINAD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)



TPC 25. THD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)



TPC 26. THD vs. Clock Frequency (A_{IN} = –0.5 dB, f_{IN} = 1.0 MHz, V_{CM} = 2.5 V)



TPC 27. SNR/SFDR vs. A_{IN} (Input Amplitude) (f_{IN} = 5.0 MHz, Input Span = 2 V p-p, V_{CM} = 2.5 V)

INTRODUCTION

The AD9221/AD9223/AD9220 are members of a high performance, complete single-supply 12-bit ADC product family based on the same CMOS pipelined architecture. The product family allows the system designer an upward or downward component selection path based on dynamic performance, sample rate, and power. The analog input range of the AD9221/AD9223/AD9220 is highly flexible, allowing for both single-ended or differential inputs of varying amplitudes that can be ac or dc coupled. Each device shares the same interface options, pinout, and package offering.

The AD9221/AD9223/AD9220 utilize a four-stage pipeline architecture with a wideband input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last stage, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This latency is not a concern in most applications. The digital output, together with the out-of-range indicator (OTR), is latched into an output buffer to drive the output pins. The output drivers can be configured to interface with 5 V or 3.3 V logic families.

The AD9221/AD9223/AD9220 use both edges of the clock in their internal timing circuitry (see Figure 1 and Specifications for exact timing requirements). The A/D samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock), the input SHA is in the sample mode; during the clock high time, it is in hold. System disturbances just prior to the rising edge of the clock and/or excessive clock jitter may cause the input SHA to acquire the wrong value, and should be minimized.

The internal circuitry of both the input SHA and individual pipeline stages of each member of the product family are optimized for both power dissipation and performance. An inherent trade-off exists between the input SHA's dynamic performance and its power dissipation. Figures 2 and 3 show this trade-off by comparing the full-power bandwidth and settling time of the AD9221/AD9223/AD9220. Both figures reveal that higher full-power bandwidths and faster settling times are achieved at the expense of an increase in power dissipation. Similarly, a trade-off exists between the sampling rate and the power dissipated in each stage.

As previously stated, the AD9221, AD9223, and AD9220 are similar in most aspects except for the specified sampling rate, power consumption, and dynamic performance. The product family is highly flexible, providing several different input ranges and interface options. As a result, many of the application issues and trade-offs associated with these resulting configurations are also similar. The data sheet is structured such that the designer can make an informed decision in selecting the proper A/D and optimizing its performance to fit the specific application.

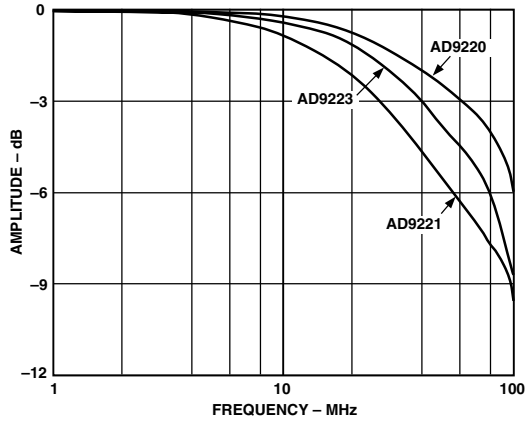


Figure 2. Full-Power Bandwidth

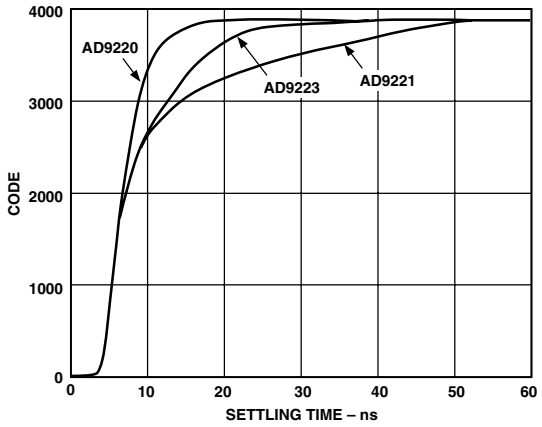


Figure 3. Settling Time

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 4, a simplified model of the AD9221/AD9223/AD9220, highlights the relationship between the analog inputs, VINA, VINB, and the reference voltage, VREF. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the A/D core. The minimum input voltage to the A/D core is automatically defined to be –VREF.

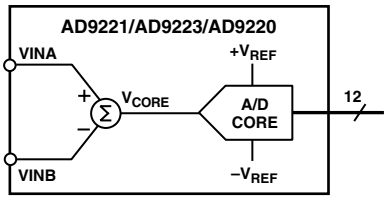


Figure 4. AD9221/AD9223/AD9220 Equivalent Functional Input Circuit

The addition of a differential input structure gives the user an additional level of flexibility that is not possible with traditional flash converters. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D's input structure allows the dc offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the A/D core is the difference of the voltages applied at the *VINA* and *VINB* input pins. Therefore, the equation,

$$V_{CORE} = VINA - VINB \quad (1)$$

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE}, must satisfy the condition,

$$-VREF \le V_{CORE} \le VREF \quad (2)$$

where *VREF* is the voltage at the *VREF* pin.

While an infinite combination of VINA and VINB inputs exist that satisfy Equation 2, there is an additional limitation placed on the inputs by the power supply voltages of the AD9221/AD9223/AD9220. The power supplies bound the valid operating range for VINA and VINB. The condition,

$$\begin{aligned} AVSS - 0.3V < VINA < AVDD + 0.3V \\ AVSS - 0.3V < VINB < AVDD + 0.3V \end{aligned} \quad (3)$$

where *AVSS* is nominally 0 V and *AVDD* is nominally 5 V, defines this requirement. Thus, the range of valid inputs for VINA and VINB is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationship between VINA, VINB, VREF and the digital output of the AD9221/AD9223/AD9220, see Table IV.

Refer to Table I and Table II at the end of this section for a summary of both the various analog input and reference configurations.

ANALOG INPUT OPERATION

Figure 5 shows the equivalent analog input of the AD9221/AD9223/AD9220, which consists of a differential sample-and-hold amplifier (SHA). The differential input structure of the SHA is highly flexible, allowing the devices to be easily configured for either a differential or single-ended input. The dc offset, or common-mode voltage, of the input(s) can be set to accommodate either single-supply or dual-supply systems. Also, note that the analog inputs, VINA and VINB, are interchangeable with the exception that reversing the inputs to the VINA and VINB pins results in a polarity inversion.

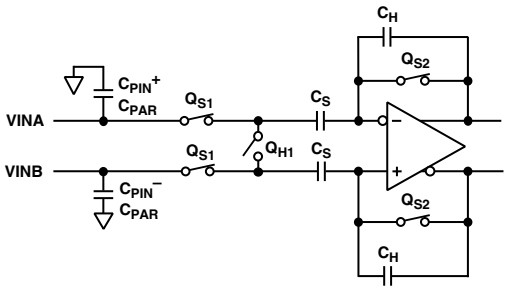


Figure 5. AD9221/AD9223/AD9220 Simplified Input Circuit

The SHA's optimum *distortion* performance for a differential or single-ended input is achieved under the following two conditions: (1) the common-mode voltage is centered around midsupply (i.e., AVDD/2 or approximately 2.5 V) and (2) the input signal voltage span of the SHA is set at its lowest (i.e., 2 V input span). This is due to the sampling switches, Q_{S1}, being CMOS switches whose R_{ON} resistance is very low but has some signal dependency that causes frequency dependent ac distortion while the SHA is in the track mode. The R_{ON} resistance of a CMOS switch is typically lowest at its midsupply but increases symmetrically as the input signal approaches either AVDD or AVSS. A lower input signal voltage span centered at midsupply reduces the degree of R_{ON} modulation.

Figure 6 compares the AD9221/AD9223/AD9220's THD vs. frequency performance for a 2 V input span with a common-mode voltage of 1 V and 2.5 V. Note how each A/D with a common-mode voltage of 1 V exhibits a similar degradation in THD performance at higher frequencies (i.e., beyond 750 kHz). Similarly, note how the THD performance at lower frequencies becomes less sensitive to the common-mode voltage. As the input frequency approaches dc, the distortion will be dominated by static nonlinearities such as INL and DNL. It is important to note that these dc static nonlinearities are independent of any R_{ON} modulation.

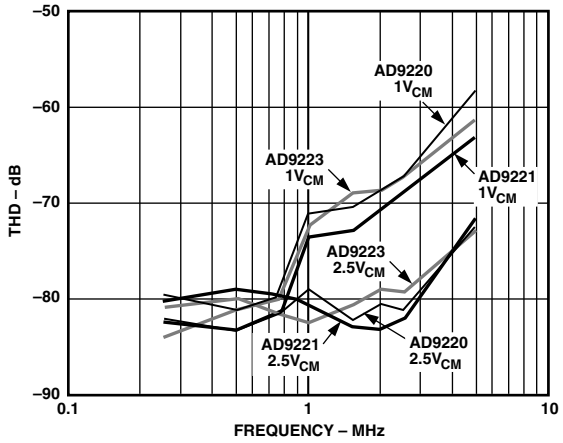


Figure 6. AD9221/AD9223/AD9220 THD vs. Frequency for V_{CM} = 2.5 V and 1.0 V (A_{IN} = –0.5 dB, Input Span = 2.0 V p-p)

Due to the high degree of symmetry within the SHA topology, a significant improvement in distortion performance for differential input signals with frequencies up to and beyond Nyquist can be realized. This inherent symmetry provides excellent cancellation of both common-mode distortion and noise. Also, the required input signal voltage span is reduced by a half, which further reduces the degree of R_{ON} modulation and its effects on distortion.

The optimum noise and dc linearity performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 5 V input span) and matched input impedance for VINA and VINB. Note that only a slight degradation in dc linearity performance exists between the 2 V and 5 V input span as specified in the AD9221/AD9223/AD9220 DC Specifications.

Referring to Figure 5, the differential SHA is implemented using a switched-capacitor topology. Therefore, its input impedance and its subsequent effects on the input drive source should be understood to maximize the converter's performance. The combination of the pin capacitance, C_{PIN}, parasitic capacitance, C_{PAR}, and sampling capacitance, C_S, is typically less than 16 pF. When the SHA goes into track mode, the input source must charge or discharge the voltage stored on C_S to the new input voltage. This action of charging and discharging C_S, averaged over a period of time and for a given sampling frequency, f_S, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period (i.e., $T = 1/f_S$), the input impedance is dynamic and therefore certain precautions on the input drive source should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that gets drawn by C_H from the input drive source. It can be shown that if C_S is allowed to fully charge up to the input voltage before switches Q_{S1} are opened, then the average current into the input is the same as if there were a resistor of $1/(C_S f_S)$ ohms connected between the inputs. This means that the input impedance is inversely proportional to the converter's sample rate. Since C_S is only 4 pF, this resistive component is typically much larger than that of the drive source (i.e., 25 kΩ at f_S = 10 MSPS).

If one considers the SHA's input impedance over a sampling period, it appears as a dynamic input impedance to the input drive source. When the SHA goes into the track mode, the input source should ideally provide the charging current through R_{ON} of switch Q_{S1} in an exponential manner. The requirement of exponential charging means that the most common input source, an op amp, must exhibit a source impedance that is both low and resistive up to and beyond the sampling frequency.

The output impedance of an op amp can be modeled with a series inductor and resistor. When a capacitive load is switched onto the output of the op amp, the output will momentarily drop due to its effective output impedance. As the output recovers, ringing may occur. To remedy the situation, a series resistor can be inserted between the op amp and the SHA input as shown in Figure 7. The series resistance helps isolate the op amp from the switched-capacitor load.

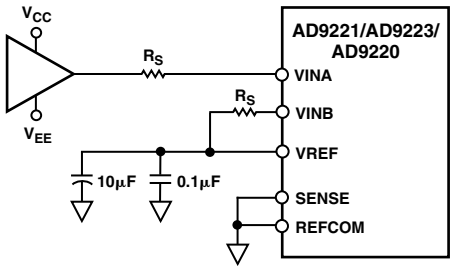


Figure 7. Series Resistor Isolates Switched-Capacitor SHA Input from Op Amp. Matching Resistors Improve SNR Performance

The optimum size of this resistor is dependent on several factors, which include the AD9221/AD9223/AD9220 sampling rate, the selected op amp, and the particular application. *In most applications, a 30 Ω to 50 Ω resistor is sufficient.* However, some applications may require a larger resistor value to reduce the noise bandwidth or possibly limit the fault current in an overvoltage condition. Other applications may require a larger resistor value as part of an antialiasing filter. In any case, since the THD performance is dependent on the series resistance and the above mentioned factors, optimizing this resistor value for a given application is encouraged.

A slight improvement in SNR performance and dc offset performance is achieved by matching the input resistance of VINA and VINB. The degree of improvement is dependent on the resistor value and the sampling rate. For series resistor values greater than 100 Ω, the use of a matching resistor is encouraged.

Figure 8 shows a plot for THD performance versus R_{SERIES} for the AD9221/AD9223/AD9220 at their respective sampling rate and Nyquist frequency. The Nyquist frequency typically represents the worst case scenario for an ADC. In this case, a high speed, high performance amplifier (AD8047) was used as the buffer op amp. Although not shown, the AD9221/AD9223/AD9220 exhibits a slight increase in SNR (i.e. 1 dB to 1.5 dB) as the resistance is increased from 0 kΩ to 2.56 kΩ due to its bandlimiting effect on wideband noise. Conversely, it exhibits slight decrease in SNR (i.e., 0.5 dB to 2 dB) if VINA and VINB do not have a matched input resistance.

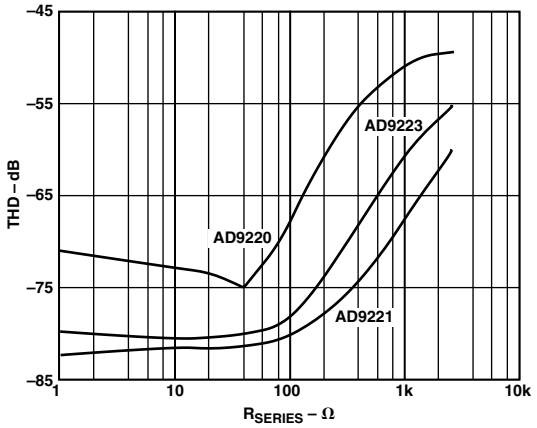


Figure 8. THD vs. R_{SERIES} ($f_{IN} = f_S/2$, A_{IN} = –0.5 dB, Input Span = 2 V p-p, V_{CM} = 2.5 V)

Figure 8 shows that a small R_{SERIES} between 30 Ω and 50 Ω provides the optimum THD performance for the AD9220. Lower values of R_{SERIES} are acceptable for the AD9223 and AD9221 as their lower sampling rates provide a longer transient recovery period for the AD8047. Note that op amps with lower bandwidths will typically have a longer transient recovery period and therefore require a slightly higher value of R_{SERIES} and/or lower sampling rate to achieve the optimum THD performance.

As the value of R_{SERIES} increases, a corresponding increase in distortion is noted. This is due to its interaction with the SHA's parasitic capacitor, C_{PAR}, which has a signal dependency. Thus, the resulting R-C time constant is signal dependent and consequently a source of distortion.

The noise or small-signal bandwidth of the AD9221/AD9223/AD9220 is the same as their full-power bandwidth as shown in Figure 2. For noise sensitive applications, the excessive bandwidth may be detrimental and the addition of a series resistor and/or

shunt capacitor can help limit the wideband noise at the A/D's input by forming a low-pass filter. Note, however, that the combination of this series resistance with the equivalent input capacitance of the AD9221/AD9223/AD9220 should be evaluated for those time-domain applications that are sensitive to the input signal's absolute settling time. In applications where harmonic distortion is not a primary concern, the series resistance may be selected in combination with the SHA's nominal 16 pF of input capacitance to set the filter's 3 dB cutoff frequency.

A better method of reducing the noise bandwidth, while possibly establishing a real pole for an antialiasing filter, is to add some additional shunt capacitance between the input (i.e., VINA and/or VINB) and analog ground. Since this additional shunt capacitance combines with the equivalent input capacitance of the AD9221/AD9223/AD9220, a lower series resistance can be selected to establish the filter's cutoff frequency while not degrading the distortion performance of the device. The shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the hold capacitor, C_H, further reducing current transients seen at the op amp's output.

The effect of this increased capacitive load on the op amp driving the AD9221/AD9223/AD9220 should be evaluated. To optimize performance when noise is the primary consideration, increase the shunt capacitance as much as the transient response of the input signal will allow. Increasing the capacitance too much may adversely affect the op amp's settling time, frequency response, and distortion performance.

REFERENCE OPERATION

The AD9221/AD9223/AD9220 contain an on-board band gap reference that provides a pin-strappable option to generate either a 1 V or 2.5 V output. With the addition of two external resistors, the user can generate reference voltages other than 1 V and 2.5 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. See Table II for a summary of the pin-strapping options for the AD9221/AD9223/AD9220 reference configurations.

Figure 9 shows a simplified model of the internal voltage reference of the AD9221/AD9223/AD9220. A pin-strappable reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin. The voltage on the VREF pin determines the full-scale input span of the A/D. This input span equals,

$$\textit{Full-Scale Input Span} = 2 \times \textit{VREF}$$

The voltage appearing at the VREF pin as well as the state of the internal reference amplifier, A1, are determined by the voltage appearing at the SENSE pin. The logic circuitry contains two comparators that monitor the voltage at the SENSE pin. The comparator with the lowest set point (approximately 0.3 V) controls the position of the switch within the feedback path of A1. If the SENSE pin is tied to REFCOM, the switch is connected to the internal resistor network, thus providing a VREF of 2.5 V. If the SENSE pin is tied to the VREF pin via a short or resistor, the switch is connected to the SENSE pin. A short will provide a VREF of 1.0 V while an external resistor network will provide an alternative VREF between 1.0 V and 2.5 V. The other comparator controls internal circuitry that will disable the reference amplifier if the SENSE pin is tied to AVDD. Disabling the reference amplifier allows the VREF pin to be driven by an external voltage reference.

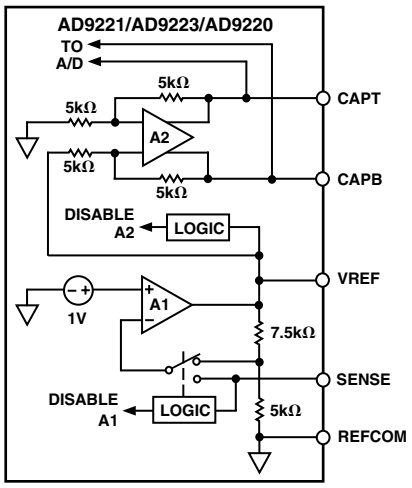


Figure 9. Equivalent Reference Circuit

The actual reference voltages used by the internal circuitry of the AD9221/AD9223/AD9220 appear on the CAPT and CAPB pins. For proper operation when using the internal or an external reference, it is necessary to add a capacitor network to decouple these pins. Figure 10 shows the recommended decoupling network. This capacitive network performs the following three functions: (1) along with the reference amplifier, A2, it provides a low source impedance over a large frequency range to drive the A/D internal circuitry, (2) it provides the necessary compensation for A2, and (3) it band-limits the noise contribution from the reference. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 15 ms and should be evaluated in any power-down mode of operation.

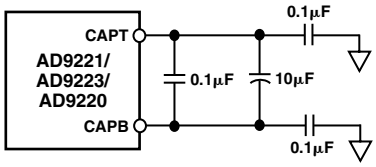


Figure 10. Recommended CAPT/CAPB Decoupling Network

The A/D's input span may be varied dynamically by changing the differential reference voltage appearing across CAPT and CAPB symmetrically around 2.5 V (i.e., midsupply). To change the reference at speeds beyond the capabilities of A2, it will be necessary to drive CAPT and CAPB with two high speed, low noise amplifiers. In this case, both internal amplifiers (i.e., A1 and A2) must be disabled by connecting SENSE to AVDD and VREF to REFCOM, and the capacitive decoupling network removed. The external voltages applied to CAPT and CAPB must be 2.5 V + Input Span/4 and 2.5 V – Input Span/4, respectively, in which the input span can be varied between 2 V and 5 V. Note that those samples within the pipeline A/D during any reference transition will be corrupted and should be discarded.

Table I. Analog Input Configuration Summary

Input Connection	Coupling	Input Span (V)	Input Range (V)		Figure No.	Comments
			VINA*	VINB*		
Single-Ended	DC	2	0 to 2	1	13, 14	Best for stepped input response applications, suboptimum THD, and noise performance. Requires ±5 V op amp.
		2 × VREF	0 to 2 × VREF	VREF	13, 14	Same as above but with improved noise performance due to increase in dynamic range. Headroom/settling time requirements of ±5 V op amp should be evaluated.
		5	0 to 5	2.5	13, 14	Optimum noise performance, excellent THD performance. Requires op amp with VCC > 5 V due to headroom issue.
		2 × VREF	2.5 – VREF to 2.5 + VREF	2.5	24	Optimum THD performance with VREF = 1. Noise to performance improves while THD performance degrades as VREF increases to 2.5 V. Single-supply operation (i.e., 5 V) for many op amps.
Single-Ended	AC	2 or 2 × VREF	0 to 1 or 0 to 2 × VREF	1 or VREF	15	Suboptimum ac performance due to input common-mode level not biased at optimum midsupply level (i.e., 2.5 V).
		5	0 to 5	2.5	15	Optimum noise performance, excellent THD performance, ability to use ±5 V op amp.
		2 × VREF	2.5 – VREF to 2.5 + VREF	2.5	16	Flexible input range, optimum THD performance with VREF = 1. Noise performance improves while THD performance degrades as VREF increases to 2.5 V. Ability to use +5 V or ±5 V op amp.
Differential (via Transformer)	AC	2	2 to 3	3 to 2	19	Optimum full-scale THD and SFDR performance well beyond the A/D's Nyquist frequency. Preferred mode for undersampling applications.
		2 × VREF	2.5 – VREF/2 to 2.5 + VREF/2	2.5 + VREF/2 to 2.5 – VREF/2	19	Same as 2 V to 3 V input range with the exception that full-scale THD and SFDR performance can be traded off for better noise performance. Refer to discussion in AC Coupling and Interface Issue section and Simple AC Interface section.
		5	1.75 to 3.25	3.25 to 1.75	19	Optimum Noise performance. Also, the optimum THD and SFDR performance for "less than" full-scale signals (i.e., –6 dBFS). Refer to discussion in AC Coupling and Interface Issue section and Simple AC Interface section.

*VINA and VINB can be interchanged if signal inversion is required.

Table II. Reference Configuration Summary

Reference Operating Mode	Input Span (VINA–VINB) (V p-p)	Required VREF (V)	Connect	To
INTERNAL	2	1	SENSE	VREF
INTERNAL	5	2.5	SENSE	REFCOM
INTERNAL	2 ≤ SPAN ≤ 5 and SPAN = 2 × VREF	1 ≤ VREF ≤ 2.5 and VREF = (1 + R1/R2)	R1 R2	VREF and SENSE SENSE and REFCOM
EXTERNAL (Nondynamic)	2 ≤ SPAN ≤ 5	1 ≤ VREF ≤ 2.5	SENSE VREF	AVDD EXT. REF.
EXTERNAL (Dynamic)	2 ≤ SPAN ≤ 5	CAPT and CAPB Externally Driven	SENSE VREF EXT. REF. EXT. REF.	AVDD REFCOM CAPT CAPB

DRIVING THE ANALOG INPUTS

Introduction

The AD9221/AD9223/AD9220 has a highly flexible input structure, allowing it to interface with single-ended or differential input interface circuitry. The applications shown in sections Driving the Analog Inputs and Reference Configurations, along with the information presented in Input and Reference Overview of this data sheet, give examples of both single-ended and differential operation. Refer to Tables I and II for a list of the different possible input and reference configurations and their associated figures in the data sheet.

The optimum mode of operation, analog input range, and associated interface circuitry will be determined by the particular application's performance requirements as well as power supply options. For example, a dc coupled single-ended input would be appropriate for most data acquisition and imaging applications. Also, many communication applications that require a dc coupled input for proper demodulation can take advantage of the excellent single-ended distortion performance of the AD9221/AD9223/AD9220. The input span should be configured such that the system's performance objectives and the headroom requirements of the driving op amp are simultaneously met.

Alternatively, the differential mode of operation with a transformer coupled input provides the best THD and SFDR performance over a wide frequency range. This mode of operation should be considered for the most demanding spectral based applications that allow ac coupling (e.g., Direct IF to Digital Conversion).

Single-ended operation requires that VINA be ac- or dc-coupled to the input signal source while VINB of the AD9221/AD9223/AD9220 can be biased to the appropriate voltage corresponding to a midscale code transition. Note that signal inversion may be easily accomplished by transposing VINA and VINB. The rated specifications for the AD9221/AD9223/AD9220 are characterized using single-ended circuitry with input spans of 5 V and 2 V as well as VINB = 2.5 V.

Differential operation requires that VINA and VINB be simultaneously driven with two equal signals that are in and out of phase versions of the input signal. Differential operation of the AD9221/AD9223/AD9220 offers the following benefits: (1) Signal swings are smaller and therefore linearity requirements placed on the input signal source may be easier to achieve, (2) Signal swings are smaller and therefore may allow the use of op amps that may otherwise have been constrained by headroom

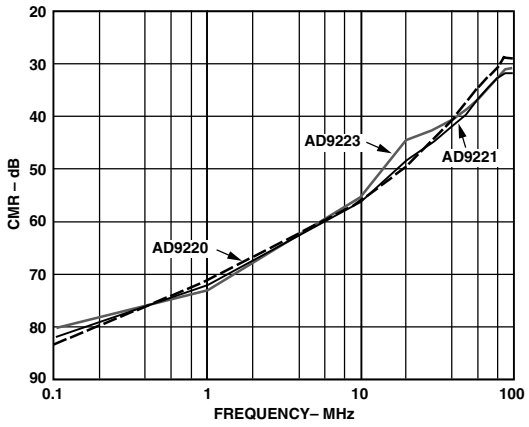


Figure 11. AD9221/AD9223/AD9220 Input CMR vs. Input Frequency

limitations, (3) Differential operation minimizes even-order harmonic products, and (4) Differential operation offers noise immunity based on the device's common-mode rejection. Figure 11 depicts the common-mode rejection of the three devices.

As is typical of most CMOS devices, exceeding the supply limits will turn on internal parasitic diodes, resulting in transient currents within the device. Figure 12 shows a simple means of clamping an ac- or dc-coupled single-ended input with the addition of two series resistors and two diodes. An optional capacitor is shown for ac-coupled applications. Note that a larger series resistor could be used to limit the fault current through D1 and D2 but should be evaluated since it can cause a degradation in overall performance. A similar clamping circuit could also be used for each input if a differential input signal is being applied.

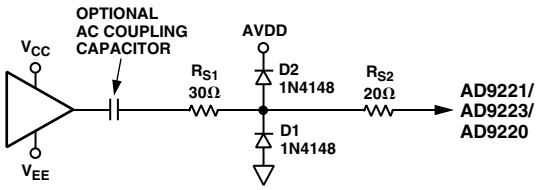


Figure 12. Simple Clamping Circuit

SINGLE-ENDED MODE OF OPERATION

The AD9221/AD9223/AD9220 can be configured for single-ended operation using dc or ac coupling. In either case, the input of the A/D must be driven from an operational amplifier that will not degrade the A/D's performance. Because the A/D operates from a single-supply, it will be necessary to level-shift ground-based bipolar signals to comply with its input requirements. Both dc and ac coupling provide this necessary function, but each method results in different interface issues that may influence the system design and performance.

DC COUPLING AND INTERFACE ISSUES

Many applications require the analog input signal to be dc-coupled to the AD9221/AD9223/AD9220. An operational amplifier can be configured to rescale and level shift the input signal so that it is compatible with the selected input range of the A/D. The input range to the A/D should be selected on the basis of system performance objectives as well as the analog power supply availability since this will place certain constraints on the op amp selection.

Many of the new high performance op amps are specified for only ±5 V operation and have limited input/output swing capabilities. Therefore, the selected input range of the AD9221/AD9223/AD9220 should be sensitive to the headroom requirements of the particular op amp to prevent clipping of the signal. Also, since the output of a dual supply amplifier can swing below –0.3 V, clamping its output should be considered in some applications.

In some applications, it may be advantageous to use an op amp specified for single-supply 5 V operation since it will inherently limit its output swing to within the power supply rails. An amplifier like the AD8041, AD8011, and AD817 are useful for this purpose. Rail-to-rail output amplifiers such as the AD8041 allow the AD9221/AD9223/AD9220 to be configured for larger input spans, which improves the noise performance.

If the application requires the largest input span (i.e., 0 V to 5 V) of the AD9221/AD9223/AD9220, the op amp will require larger supplies to drive it. Various high speed amplifiers in the Op Amp Selection Guide of this data sheet can be selected to accommodate a wide range of supply options. Once again, clamping the output of the amplifier should be considered for these applications.

Two dc-coupled op amp circuits using a noninverting and inverting topology are discussed below. Although not shown, the noninverting and inverting topologies can be easily configured as part of an antialiasing filter by using a Sallen-Key or Multiple-Feedback topology, respectively. An additional R-C network can be inserted between the op amp's output and the AD9221/AD9223/AD9220 input to provide a real pole.

Simple Op Amp Buffer

In the simplest case, the input signal to the AD9221/AD9223/AD9220 will already be biased at levels in accordance with the selected input range. It is simply necessary to provide an adequately low source impedance for the VINA and VINB analog input pins of the A/D. Figure 13 shows the recommended configuration for a single-ended drive using an op amp. In this case, the op amp is shown in a noninverting unity gain configuration driving the VINA pin. The internal reference drives the VINB pin. Note that the addition of a small series resistor of 30 Ω to 50 Ω connected to VINA and VINB will be beneficial in nearly all cases. Refer to the Analog Input Operation section for a discussion on resistor selection. Figure 13 shows the proper connection for a 0 V to 5 V input range. Alternative single-ended input ranges of 0 V to 2 × VREF can also be realized with the proper configuration of VREF (refer to the Using the Internal Reference section).

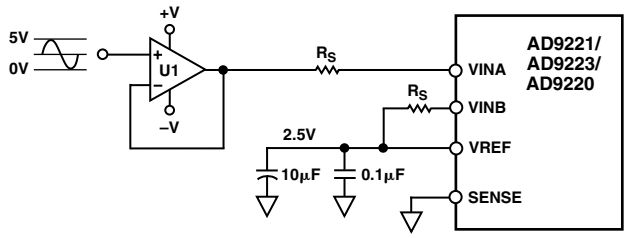


Figure 13. Single-Ended AD9221/AD9223/AD9220 Op Amp Drive Circuit

Op Amp with DC Level Shifting

Figure 14 shows a dc-coupled level shifting circuit employing an op amp, A1, to sum the input signal with the desired dc offset. Configuring the op amp in the inverting mode with the given resistor values results in an ac signal gain of –1. If the signal inversion is undesirable, interchange the VINA and VINB connections to re-establish the original signal polarity. The dc voltage at VREF sets the common-mode voltage of the AD9221/AD9223/AD9220. For example, when VREF = 2.5 V, the output level from the op amp will also be centered around 2.5 V. The use of ratio matched, thin-film resistor networks will minimize gain and offset errors. Also, an optional pull-up resistor, R_P, may be used to reduce the output load on VREF to ±1 mA.

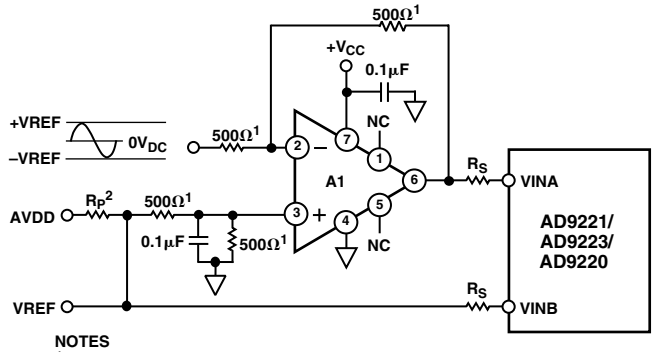


Figure 14. Single-Ended Input with DC-Coupled Level Shift

AC COUPLING AND INTERFACE ISSUES

For applications where ac coupling is appropriate, the op amp's output can be easily level shifted to the common-mode voltage, VCM, of the AD9221/AD9223/AD9220 via a coupling capacitor. This has the advantage of allowing the op amp's common-mode level to be symmetrically biased to its midsupply level (i.e., $(V_{CC} + V_{EE})/2$). Op amps that operate symmetrically with respect to their power supplies typically provide the best ac performance as well as the greatest input/output span. Thus, various high speed/performance amplifiers that are restricted to +5 V/–5 V operation and/or specified for 5 V single-supply operation can be easily configured for the 5 V or 2 V input span of the AD9221/AD9223/AD9220. The best ac distortion performance is achieved when the A/D is configured for a 2 V input span and common-mode voltage of 2.5 V. Note that differential transformer coupling, which is another form of ac coupling, should be considered for optimum ac performance.

Simple AC Interface

Figure 15 shows a typical example of an ac-coupled, single-ended configuration. The bias voltage shifts the bipolar, ground-referenced input signal to approximately VREF. The value for C1 and C2 will depend on the size of the resistor, R. The capacitors, C1 and C2, are typically a 0.1 µF ceramic and 10 µF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. The combination of the capacitor and the resistor form a high-pass filter with a high-pass –3 dB frequency determined by the equation,

$$f_{3\,dB} = 1/\left(2\times\pi\times R\times\left(C1+C2\right)\right)$$

The low impedance VREF voltage source both biases the VINB input and provides the bias voltage for the VINA input. Figure 15 shows the VREF configured for 2.5 V; thus the input range

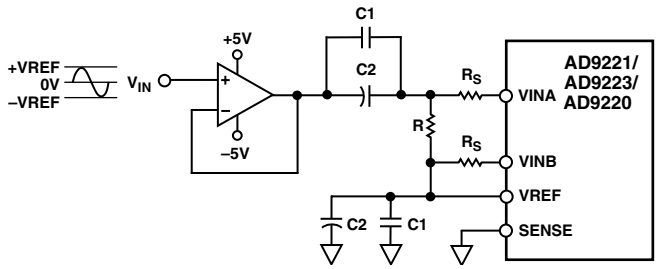


Figure 15. AC-Coupled Input

of the A/D is 0 V to 5 V. Other input ranges could be selected by changing VREF, but the A/D's distortion performance will degrade slightly as the input common-mode voltage deviates from its optimum level of 2.5 V.

Alternative AC Interface

Figure 16 shows a flexible ac-coupled circuit that can be configured for different input spans. Since the common-mode voltage of VINA and VINB are biased to midsupply independent of VREF, VREF can be pin-strapped or reconfigured to achieve input spans between 2 V and 5 V p-p. The AD9221/AD9223/AD9220's CMRR along with the symmetrical coupling R-C networks will reject both power supply variations and noise. The resistors, R, establish the common-mode voltage. They may have a high value (e.g., 5 kΩ) to minimize power consumption and establish a low cutoff frequency. The capacitors, C1 and C2, are typically 0.1 µF ceramic and 10 µF tantalum capacitors in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. R_S isolates the buffer amplifier from the A/D input. The optimum performance is achieved when VINA and VINB are driven via «Immetrical networks. The $f_{-3\,dB}$ point can be approximated by the equation,

$$f_{-3\,dB} = 1/\left(2\times\pi\times R/2\times\left(C1+C2\right)\right)$$

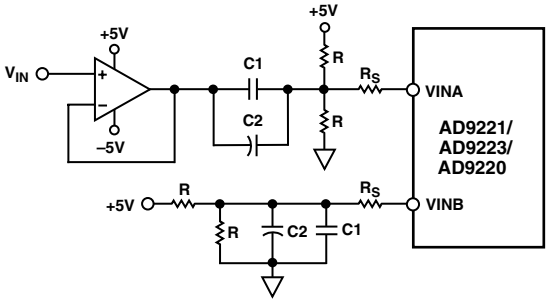


Figure 16. AC-Coupled Input-Flexible Input Span, V_{CM} = 2 V

Op Amp Selection Guide

Op amp selection for the AD9221/AD9223/AD9220 is highly dependent on a particular application. In general, the performance requirements of any given application can be characterized by either time domain or frequency domain parameters. In either case, one should carefully select an op amp that preserves the performance of the A/D. This task becomes challenging when one considers the AD9221/AD9223/AD9220's high performance capabilities coupled with other extraneous system level requirements such as power consumption and cost.

The ability to select the optimal op amp may be further complicated by either limited power supply availability and/or limited *acceptable* supplies for a desired op amp. Newer, high performance op amps typically have input and output range limitations in accordance with their lower supply voltages. As a result, some op amps will be more appropriate in systems where ac-coupling is allowable. When dc-coupling is required, op amps without headroom constraints, such as rail-to-rail op amps or ones where larger supplies can be used, should be considered. The following section describes some op amps currently available from Analog Devices. The system designer is *always* encouraged to contact the factory or local sales office to be updated on Analog Devices' latest amplifier product offerings. Highlights of the areas where the op amps excel and where they may limit the performance of the AD9221/AD9223/AD9220 is also included.

AD817: 50 MHz Unity GBW, 70 ns Settling to 0.01%, +5 V to ±15 V Supplies
Best Applications: Sample Rates < 7 MSPS, Low Noise, 5 V p-p Input Range
Limits: THD above 100 kHz

AD826: Dual Version of AD817
Best Applications: Differential and/or Low Impedance Input
Drivers, Low Noise
Limits: THD above 100 kHz

AD818: 130 MHz @ G = +2 BW, 80 ns Settling to 0.01%, +5 V to ±15 V Supplies
Best Applications: Sample Rates < 7 MSPS, Low Noise, 5 V p-p Input Range, Gains ≥ +2
Limits: THD above 100 kHz

AD828: Dual Version of AD818
Best Applications: Differential and/or Low Impedance Input
Drivers, Low Noise, Gains ≥ +2
Limits: THD above 100 kHz

AD812: Dual, 145 MHz Unity GBW, Single-Supply Current Feedback, +5 V to ±15 V Supplies
Best Applications: Differential and/or Low Impedance Input Drivers, Sample Rates < 7 MSPS
Limits: THD above 1 MHz

AD8011: $f_{-3\ dB}$ = 300 MHz, +5 V or ±5 V Supplies, Current Feedback
Best Applications: Single-Supply, AC-DC-Coupled, Good AC Specs, Low Noise, Low Power (5 mW)
Limits: THD above 5 MHz, Usable Input/Output Range

AD8013: Triple, $f_{-3\ dB}$ = 230 MHz, +5 V or ±5 V Supplies, Current Feedback, Disable Function
Best Applications: 3:1 Multiplexer, Good AC Specs
Limits: THD above 5 MHz, Input Range

AD9631: 220 MHz Unity GBW, 16 ns Settling to 0.01%, ±5 V Supplies
Best Applications: Best AC Specs, Low Noise, AC-Coupled
Limits: Usable Input/Output Range, Power Consumption

AD8047: 130 MHz Unity GBW, 30 ns Settling to 0.01%, ±5 V Supplies
Best Applications: Good AC Specs, Low Noise, AC-Coupled
Limits: THD > 5 MHz, Usable Input Range

AD8041: Rail-to-Rail, 160 MHz Unity GBW, 55 ns Settling to 0.01%, 5 V Supply, 26 mW
Best Applications: Low Power, Single-Supply Systems, DC-Coupled, Large Input Range
Limits: Noise with 2 V Input Range

AD8042: Dual AD8041
Best Applications: Differential and/or Low Impedance Input Drivers
Limits: Noise with 2 V Input Range

DIFFERENTIAL MODE OF OPERATION

Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. In systems that do not need to be dc-coupled, an RF transformer with a center tap is the best method to generate differential inputs for the AD9221/AD9223/AD9220. It provides all the benefits of operating the A/D in the differential mode without contributing additional noise or distortion. An RF transformer also has the added benefit of providing electrical isolation between the signal source and the A/D.

Note that although a single-ended-to-differential op amp topology would allow dc coupling of the input signal, no significant improvement in THD performance was realized when compared to the dc single-ended mode of operation up to the AD9221/AD9223/AD9220's Nyquist frequency (i.e., $f_{IN} < f_S/2$). Also, the additional op amp required in the topology tends to increase the total system noise, power consumption, and cost. Thus, a single-ended mode of operation is recommended for most applications requiring dc coupling.

A dramatic improvement in THD and SFDR performance can be realized by operating the AD9221/AD9223/AD9220 in the differential mode using a transformer. Figure 17 shows a plot of THD versus Input Frequency for the differential transformer coupled circuit for each A/D while Figure 18 shows a plot of SFDR versus Input Frequency. Both figures demonstrate the enhancement in spectral performance for the differential-mode of operation. The performance enhancement between the differential and single-ended mode is most noteworthy as the input frequency approaches and goes beyond the Nyquist frequency (i.e., $f_{IN} > f_S/2$) corresponding to the particular A/D.

The figures are also helpful in determining the appropriate A/D for Direct IF down conversion or undersampling applications. Refer to Analog Devices application notes AN-301 and AN-302 for an informative discussion on undersampling. One should select the A/D that meets or exceeds the distortion performance requirements measured over the required frequency passband. For example, the AD9220 achieves the best distortion performance over an extended frequency range as a result of its greater full-power bandwidth and thus would represent the best selection for an IF undersampling application at 21.4 MHz. Refer to the Applications section of this data sheet for more detailed information and characterization of this particular application.

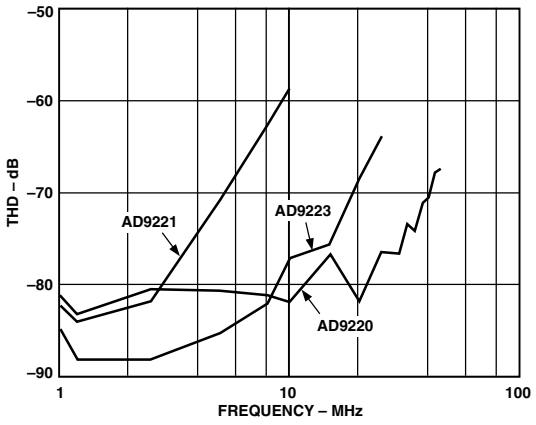


Figure 17. AD9221/AD9223/AD9220 THD vs. Input Frequency (V_{CM} = 2.5 V, 2 V p-p Input Span, A_{IN} = –0.5 dB)

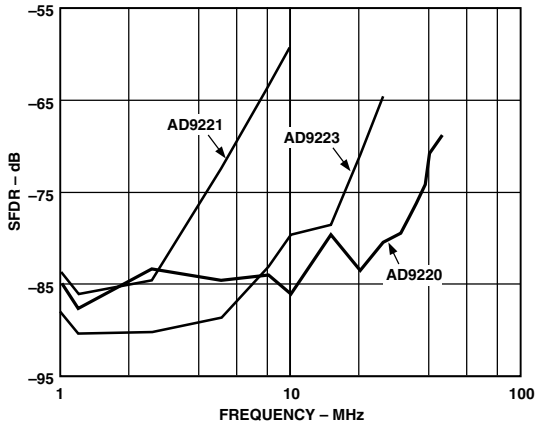


Figure 18. AD9221/AD9223/AD9220 SFDR vs. Input Frequency (V_{CM} = 2.5 V, 2 V p-p Input Span, A_{IN} = –0.5 dB)

Figure 19 shows the schematic of the suggested transformer circuit. The circuit uses a Mini-Circuits RF transformer, model #T4-6T, which has an impedance ratio of 4 (turns ratio of 2). The schematic assumes that the signal source has a 50 Ω source impedance. The 1:4 impedance ratio requires the 200 Ω secondary termination for optimum power transfer and VSWR. The center tap of the transformer provides a convenient means of level shifting the input signal to a desired common-mode voltage. Optimum performance can be realized when the center tap is tied to CML of the AD9221/AD9223/AD9220, which is the common-mode bias level of the internal SHA.

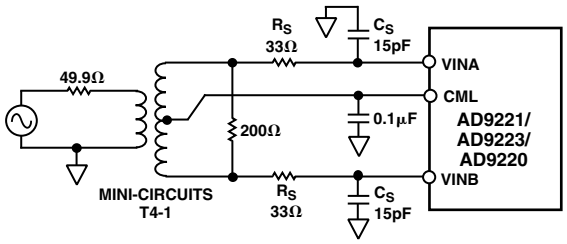


Figure 19. Transformer Coupled Input

Transformers with other turns ratios may also be selected to optimize the performance of a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Therefore, selecting a transformer with a higher impedance ratio (e.g., Mini-Circuits T16-6T with a 1:16 impedance ratio) effectively "steps up" the signal level, thus further reducing the driving requirements of the signal source.

Referring to Figure 19, a series resistor, R_S, and shunt capacitor, C_S, were inserted between the AD9221/AD9223/AD9220 and the secondary of the transformer. The values of 33 Ω and 15 pF were selected to specifically optimize both the THD and SNR performance of the A/D. R_S and C_S help provide some isolation from transients at the A/D inputs reflected back through the primary of the transformer.

The AD9221/AD9223/AD9220 can be easily configured for either a 2 V p-p input span or 5.0 V p-p input span by setting the internal reference (see Table II). Other input spans can be realized with two external gain setting resistors as shown in Figure 23 of this data sheet. Figure 20 demonstrates how both spans of the AD9220 achieve the high degree of linearity and SFDR over a wide range of amplitudes required by the most demanding communication applications. Similar performance is achievable with the AD9221 and AD9223 at their corresponding Nyquist frequency.

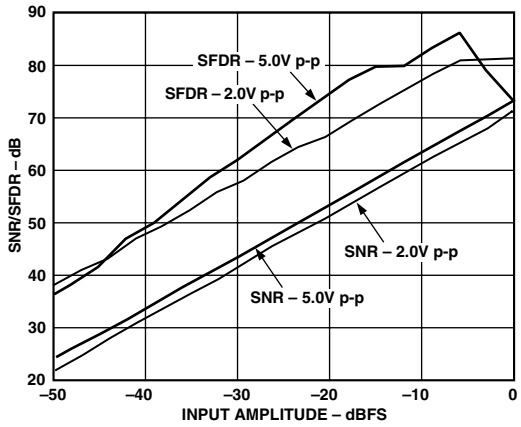


Figure 20. AD9220 SFDR, SNR vs. Input Amplitude (f_{IN} = 5 MHz, f_{CLK} = 10 MSPS, V_{CM} = 2.5 V, Differential)

Figure 20 also reveals a noteworthy difference in the SFDR and SNR performance of the AD9220 between the 2 V p-p and 5 V p-p input span options. First, the SNR performance improves by 2 dB with a 5.0 V p-p input span due to the increase in dynamic range. Second, the SFDR performance of the AD9220 will improve for input signals below approximately –6.0 dBFS. A 3 dB to 5 dB improvement was typically realized for input signal levels between –6.0 dBFS and –36 dBFS. This improvement in SNR and SFDR for a 5.0 V p-p span may be advantageous for communication systems that have additional margin or headroom to minimize clipping of the ADC.

REFERENCE CONFIGURATIONS

The figures associated with this section on internal and external reference operation do not show recommended matching series resistors for VINA and VINB for the purpose of simplicity. Please refer to the Driving the Analog Inputs, Introduction section for a discussion of this topic. Also, the figures do not show the decoupling network associated with the CAPT and CAPB pins. Please refer to the Reference Operation section for a discussion of the internal reference circuitry and the recommended decoupling network shown in Figure 10.

USING THE INTERNAL REFERENCE

Single-Ended Input with 0 to 2 × VREF Range

Figure 21 shows how to connect the AD9221/AD9223/AD9220 for a 0 V to 2 V or 0 V to 5 V input range via pin strapping the SENSE pin. An intermediate input range of 0 to 2 × VREF can be established using the resistor programmable configuration in Figure 23 and connecting VREF to VINB.

In either case, both the common-mode voltage and input span are directly dependent on the value of VREF. More specifically, the common-mode voltage is equal to VREF while the input span is equal to 2 × VREF. Thus, the valid input range extends from 0 to 2 × VREF. When VINA is ≤ 0 V, the digital output will be 000 Hex; when VINA is ≥ 2 × VREF, the digital output will be FFF Hex.

Shorting the VREF pin directly to the SENSE pin places the internal reference amplifier in unity-gain mode and the resultant VREF output is 1 V. Therefore, the valid input range is 0 V to 2 V. However, shorting the SENSE pin directly to the REFCOM pin configures the internal reference amplifier for a gain of 2.5 and the resultant VREF output is 2.5 V. Thus, the valid input range becomes 0 V to 5 V. The VREF pin should be bypassed to the REFCOM pin with a 10 μF tantalum capacitor in parallel with a low inductance 0.1 μF ceramic capacitor.

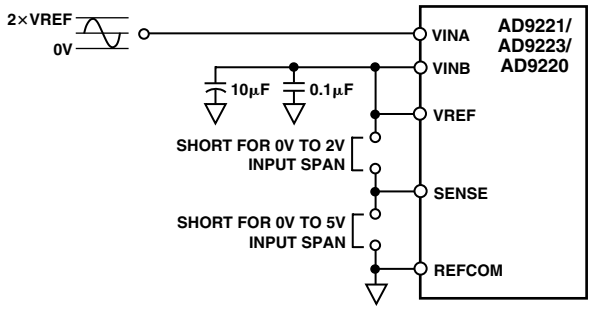


Figure 21. Internal Reference—2 V p-p Input Span, V_{CM} = 1 V, or 5 V p-p Input Span, V_{CM} = 2.5 V

Single-Ended or Differential Input, V_{CM} = 2.5 V

Figure 22 shows the single-ended configuration that gives the best dynamic performance (SINAD, SFDR). To optimize dynamic specifications, center the common-mode voltage of the analog input at approximately by 2.5 V by connecting VINB to a low impedance 2.5 V source. As described above, shorting the VREF pin directly to the SENSE pin results in a 1 V reference voltage and a 2 V p-p input span. The valid range for input signals is 1.5 V to 3.5 V. The VREF pin should be bypassed to the REFCOM pin with a 10 μF tantalum capacitor in parallel with a low inductance 0.1 μF ceramic capacitor.

This reference configuration could also be used for a differential input in which VINA and VINB are driven via a transformer as shown in Figure 19. In this case, the common-mode voltage, V_{CM}, is set at midsupply by connecting the transformer's center tap to CML of the AD9221/AD9223/AD9220. VREF can be configured for 1 V or 2.5 V by connecting SENSE to either VREF or REFCOM respectively. Note that the valid input range for each of the differential inputs is one-half of single-ended input and thus becomes V_{CM} – VREF/2 to V_{CM} + VREF/2.

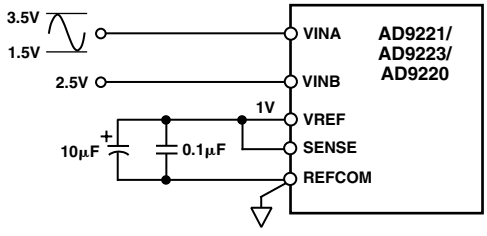


Figure 22. Internal Reference—2 V p-p Input Span, V_{CM} = 2.5 V

Resistor Programmable Reference

Figure 23 shows an example of how to generate a reference voltage other than 1 V or 2.5 V with the addition of two external resistors and a bypass capacitor. Use the equation,

$$VREF = 1V \times (1 + R1/R2)$$

to determine appropriate values for *R*1 and *R*2. These resistors should be in the 2 kΩ to 100 kΩ range. For the example shown, *R*1 equals 2.5 kΩ and *R*2 equals 5 kΩ. From the equation above, the resultant reference voltage on the VREF pin is 1.5 V. This sets the input span to be 3 V p-p. To assure stability, place a 0.1 μF ceramic capacitor in parallel with *R*1.

The common-mode voltage can be set to VREF by connecting VINB to VREF to provide an input span of 0 to 2 × VREF. Alternatively, the common-mode voltage can be set to VREF by connecting VINB to a low impedance 2.5 V source. For the example shown, the valid input single range for VINA is 1 V to 4 V since VINB is set to an external, low impedance 2.5 V source. The VREF pin should be bypassed to the REFCOM pin with a 10 μF tantalum capacitor in parallel with a low inductance 0.1 μF ceramic capacitor.

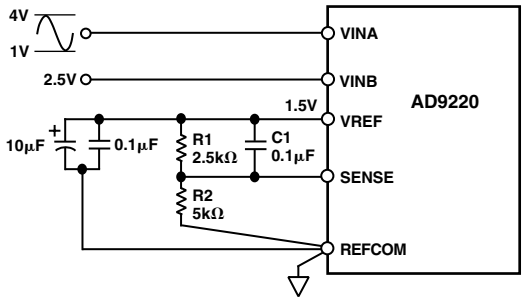


Figure 23. Resistor Programmable Reference—3 V p-p Input Span, V_{CM} = 2.5 V

USING AN EXTERNAL REFERENCE

Using an external reference may enhance the dc performance of the AD9221/AD9223/AD9220 by improving drift and accuracy. Figures 24 through 26 show examples of how to use an external reference with the A/D. Table III is a list of suitable voltage references from Analog Devices. To use an external reference, the user must disable the internal reference amplifier and drive the VREF pin. Connecting the SENSE pin to AVDD disables the internal reference amplifier.

Table III. Suitable Voltage References

	Output Voltage	Drift (ppm/°C)	Initial Accuracy % (max)	Operating Current (μA)
Internal	1.00	26	1.4	N/A
AD589	1.235	10–100	1.2–2.8	50
AD1580	1.225	50–100	0.08–0.8	50
REF191	2.048	5–25	0.1–0.5	45
Internal	2.50	26	1.4	N/A
REF192	2.50	5–25	0.08–0.4	45
REF43	2.50	10–25	0.06–0.1	600
AD780	2.50	3–7	0.04–0.2	1000

The AD9221/AD9223/AD9220 contains an internal reference buffer, A2 (see Figure 9), that simplifies the drive requirements of an external reference. The external reference must be able to drive a ≈5 kΩ (±20%) load. Note that the bandwidth of the reference buffer is deliberately left small to minimize the reference noise contribution. As a result, it is not possible to change the reference voltage rapidly in this mode without the removal of the CAPT/CAPB Decoupling Network.

Variable Input Span with V_{CM} = 2.5 V

Figure 24 shows an example of the AD9221/AD9223/AD9220 configured for an input span of 2 × VREF centered at 2.5 V. An external 2.5 V reference drives the VINB pin, thus setting the common-mode voltage at 2.5 V. The input span can be independently set by a voltage divider consisting of R1 and R2, which generates the VREF signal. A1 buffers this resistor network and drives VREF. Choose this op amp based on accuracy requirements. It is essential that a minimum of a 10 µF capacitor in parallel with a 0.1 µF low inductance ceramic capacitor decouple the reference output to ground.

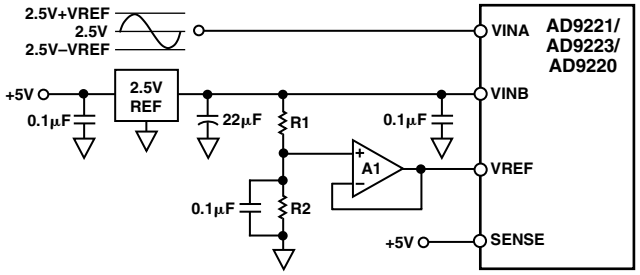


Figure 24. External Reference—V_{CM} = 2.5 V (2.5 V on VINB, Resistor Divider to Make VREF)

Single-Ended Input with 0 to 2 × VREF Range

Figure 25 shows an example of an external reference driving both VINB and VREF. In this case, both the common-mode voltage and input span are directly dependent on the value of VREF. More specifically, the common-mode voltage is equal to VREF while the input span is equal to 2 × VREF. Thus, the valid input range extends from 0 to 2 × VREF. For example, if the REF-191, a 2.048 external reference was selected, the valid input range extends from 0 to 4.096 V. In this case, 1 LSB of the AD9221/AD9223/AD9220 corresponds to 1 mV. It is essential that a minimum of a 10 µF capacitor in parallel with a 0.1 µF low inductance ceramic capacitor decouple the reference output to ground.

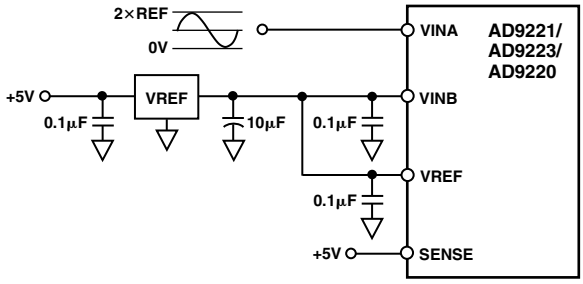


Figure 25. Input Range = 0 V to 2× VREF

Low Cost/Power Reference

The external reference circuit shown in Figure 26 uses a low cost 1.225 V external reference (e.g., AD580 or AD1580) along with an op amp and transistor. The 2N2222 transistor acts in conjunction with 1/2 of an OP282 to provide a very low impedance drive for VINB. The selected op amp need not be a high speed op amp and may be selected based on cost, power, and accuracy.

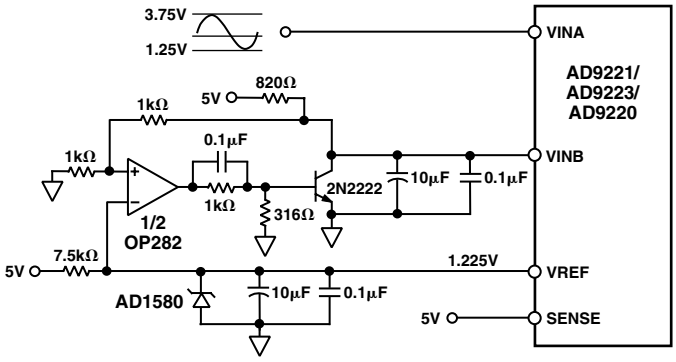


Figure 26. External Reference Using the AD1580 and Low Impedance Buffer

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

The AD9221/AD9223/AD9220 output data is presented in positive true straight binary for all input ranges. Table IV indicates the output data formats for various input ranges regardless of the selected input range. A twos complement output data format can be created by inverting the MSB.

Table IV. Output Data Format

Input (V)	Condition (V)	Digital Output	OTR
VINA –VINB	< – VREF	0000 0000 0000	1
VINA –VINB	= – VREF	0000 0000 0000	0
VINA –VINB	= 0	1000 0000 0000	0
VINA –VINB	= + VREF – 1 LSB	1111 1111 1111	0
VINA –VINB	≥ + VREF	1111 1111 1111	1

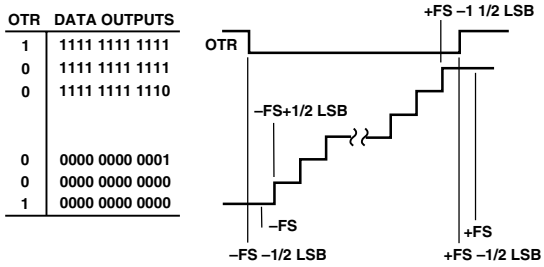


Figure 27. Output Data Format

Out Of Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the converter. OTR is a digital output that is updated along with the data output corresponding to the particular sampled analog input voltage. Thus, OTR has the same pipeline delay (latency) as the digital data. It is LOW when the analog input voltage is within the analog input range. It is HIGH when the analog input voltage exceeds the input range as shown in Figure 27. OTR will remain HIGH until the analog input returns within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions

can be detected. Table V is a truth table for the over/underrange circuit in Figure 28, which uses NAND gates. Systems requiring programmable gain conditioning of the AD9221/AD9223/AD9220 input signal can immediately detect an out-of-range condition, thus eliminating gain selection iterations. Also, OTR can be used for digital offset and gain calibration.

Table V. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

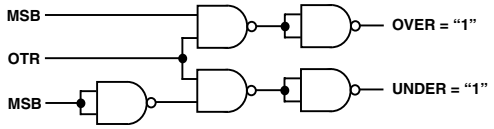


Figure 28. Overrange or Underrange Logic

Digital Output Driver Considerations (DVDD)

The AD9221, AD9223 and AD9220 output drivers can be configured to interface with 5 V or 3.3 V logic families by setting DVDD to 5 V or 3.3 V respectively. The AD9221/AD9223/AD9220 output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect SINAD performance. Applications requiring the AD9221/AD9223/AD9220 to drive large capacitive loads or large fanout may require additional decoupling capacitors on DVDD. In extreme cases, external buffers or latches may be required.

Clock Input and Considerations

The AD9221/AD9223/AD9220 internal timing uses the two edges of the clock input to generate a variety of internal timing signals. The clock input must meet or exceed the minimum specified pulsewidth high and low (t_{CH} and t_{CL}) specifications for the given A/D as defined in the Switching Specifications to meet the rated performance specifications. For example, the clock input to the AD9220 operating at 10 MSPS may have a duty cycle between 45% to 55% to meet this timing requirement since the minimum specified t_{CH} and t_{CL} is 45 ns. For clock rates below 10 MSPS, the duty cycle may deviate from this range to the extent that both t_{CH} and t_{CL} are satisfied.

All high speed high resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due to only aperture jitter (t_A) can be calculated with the following equation:

$$SNR = 20\ log_{10}\left[1 / 2\pi\ f_{IN}\ t_A\right]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all the jitter sources, which include the clock input, analog input signal, and A/D aperture jitter specification. For example, if a 5 MHz full-scale sine wave is sampled by an A/D with a total rms jitter of 15 ps, the SNR performance of the A/D will be limited to 66.5 dB. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9221/AD9223/AD9220. As such, supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other method), it should be retimed by the original clock at the last step.

Most of the power dissipated by the AD9221/AD9223/AD9220 is from the analog power supplies. However, lower clock speeds will reduce digital current slightly. Figure 29 shows the relationship between power and clock rate for each A/D.

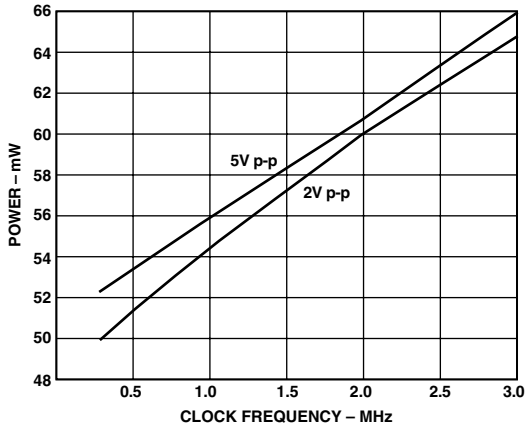


Figure 29a. AD9221 Power Consumption vs. Clock Frequency

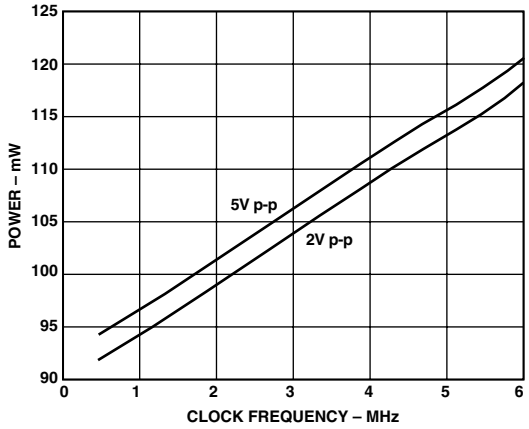


Figure 29b. AD9223 Power Consumption vs. Clock Frequency

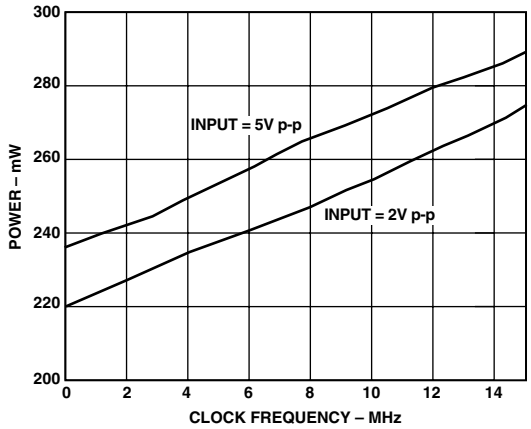


Figure 29c. AD9220 Power Consumption vs. Clock Frequency

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the AD9221/AD9223/AD9220 features separate analog and digital ground pins, it should be treated as an analog component. *The AVSS and DVSS pins must be joined together directly under the AD9221/AD9223/AD9220.* A solid ground plane under the A/D is acceptable if the power and ground return currents are managed carefully. Alternatively, the ground plane under the A/D may contain serrations to *steer* currents in predictable directions where cross-coupling between analog and digital would otherwise be unavoidable. The AD9221/AD9223/AD9220/EB ground layout, shown in Figure 39, depicts the serrated type of arrangement. The analog and digital grounds are connected by a jumper below the A/D.

Analog and Digital Supply Decoupling

The AD9221/AD9223/AD9220 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AVDD, the analog supply, should be decoupled to AVSS, the analog common, as close to the chip as physically possible. Figure 30 shows the recommended decoupling for the analog supplies; 0.1 µF ceramic chip capacitors should provide adequately low impedance over a wide frequency range. Note that the AVDD and AVSS pins are co-located on the AD9221/AD9223/AD9220 to simplify the layout of the decoupling capacitors and provide the shortest possible PCB trace lengths. The AD9221/AD9223/AD9220/EB power plane layout, shown in Figure 40 depicts a typical arrangement using a multilayer PCB.

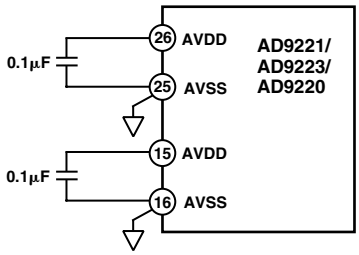


Figure 30. Analog Supply Decoupling

The CML is an internal analog bias point used internally by the AD9221/AD9223/AD9220. This pin must be decoupled with at least a 0.1 µF capacitor as shown in Figure 31. The dc level of CML is approximately AVDD/2. This voltage should be buffered if it is to be used for any external biasing.

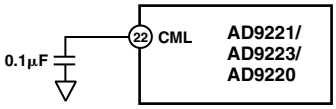


Figure 31. CML Decoupling

The digital activity on the AD9221/AD9223/AD9220 chip falls into two general categories: correction logic and output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits: large capacitive loads are to be avoided. Note, the internal correction logic of the AD9221, AD9223, and AD9220 is referenced to AVDD while the output drivers are referenced to DVDD.

The decoupling shown in Figure 32, a 0.1 µF ceramic chip capacitor, is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionally, and/or using external buffers/latches.

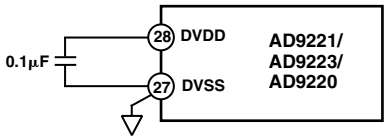


Figure 32. Digital Supply Decoupling

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the PCB to reduce low frequency ripple to negligible levels. Refer to the AD9221/AD9223/AD9220/EB schematic and layouts in Figures 36 to 42 for more information regarding the placement of decoupling capacitors.

APPLICATIONS

Direct IF Down Conversion Using the AD9220

As previously noted, the AD9220's performance in the differential mode of operation extends well beyond its baseband region and into several Nyquist zone regions. Thus, the AD9220 may be well suited as a mix down converter in both narrow and wideband applications. Various IF frequencies exist over the frequency range in which the AD9220 maintains excellent dynamic performance (e.g., refer to Figure 17 and 18). The IF signal will be aliased to the ADC's baseband region due to the sampling process in a similar manner that a mixer will down-convert an IF signal. For signals in various Nyquist zones, the following equation may be used to determine the final frequency after aliasing.

$$f_{1\ NYQUIST} = f_{SIGNAL}$$
$$f_{2\ NYQUIST} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{3\ NYQUIST} = abs\ (f_{SAMPLE} - f_{SIGNAL})$$
$$f_{4\ NYQUIST} = 2 \times f_{SAMPLE} - f_{SIGNAL}$$
$$f_{5\ NYQUIST} = abs\ (2 \times f_{SAMPLE} - f_{SIGNAL})$$

There are several potential benefits in using the ADC to alias (i.e., or mix) down a narrow-band or wideband IF signal. First and foremost is the elimination of a complete mixer stage with its associated amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction, and detection.

One common example is the digitization of a 21.4 MHz IF using a low jitter 10 MHz sample clock. Using the equation above for the fifth Nyquist zone, the resultant frequency after sampling is 1.4 MHz. Figure 33 shows the typical performance of the AD9220 operating under these conditions. Figure 34 demonstrates how the AD9220 is still able to maintain a high degree of linearity and SFDR over a wide amplitude.

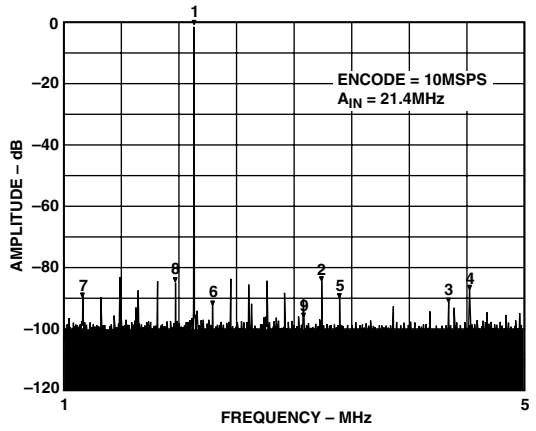


Figure 33. IF Sampling a 21.4 MHz Input Using the AD9220 (V_{CM} = 2.5 V, Input Span = 2 V p-p)

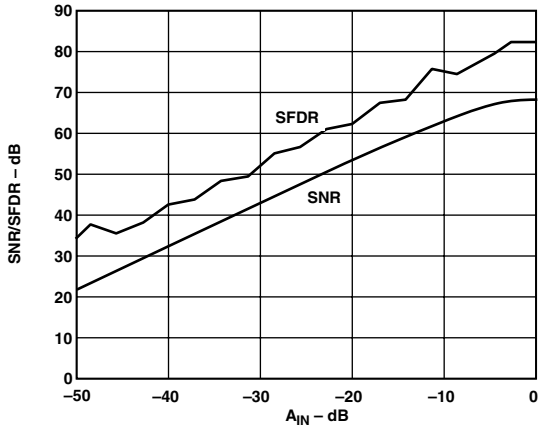


Figure 34. AD9220 Differential Input SNR/SFDR vs. Input Amplitude (A_{IN}) @ 21.4 MHz

Multichannel Data Acquisition with Autocalibration

The AD9221/AD9223/AD9220 is well suited for high performance, low power data acquisition systems. Aside from its exceptional ac performance, it exhibits true 12-bit linearity and temperature drift performance (i.e., excluding internal reference). Furthermore, the A/D product family provides the system designer with an upward or downward component selection path based on power consumption and sampling rate.

A typical multichannel data acquisition system is shown in Figure 35. Also shown is some additional inexpensive gain and offset autocalibration circuitry that is often required in high accuracy data acquisition systems. These additional peripheral components were selected based on their performance, power consumption, and cost.

Referring to Figure 35, the AD9221/AD9223/AD9220 is configured for single-ended operation with a 2.5 V p-p input span and a 2.5 V common-mode voltage using an external, precision 2.5 voltage reference, U1. This configuration and input span allows the buffer amplifier, U4, to be single supply. Also, it simplifies the design of the low temperature drift autocalibration circuitry that uses thin-film resistors for temperature stability and ratiometric accuracy. The input of the AD9221/AD9223/AD9220 can be easily configured for a wider span but it should remain within the input/output swing capabilities of a high speed, rail-to-rail, single-supply amplifier, U4 (e.g., AD8041).

The gain and offset calibration circuitry is based on two 8-bit, current-output DAC08s, U3 and U5. The gain calibration circuitry consisting of U3, and an op amp, U2A, is configured to provide a low drift nominal 1.25 V reference to the AD9221/AD9223/AD9220. The resistor values that set the gain calibration range were selected to provide a nominal adjustment span of ±128 LSBs with 1 LSB resolution with respect to the A/D. Note that the bandwidth of the reference is low and, as a result, it is not possible to change the reference voltage rapidly in this mode.

The offset calibration circuitry consists of a DAC, U5 and the buffer amplifier, U4. The DAC is configured for a bipolar adjustment span of ±64 LSB with a 1/2 LSB resolution span with respect to the AD9221/AD9223/AD9220. Note that both current outputs of U5 were configured to provide a bipolar adjustment span. Also, RC is used to decouple the output of both DACs, U3 and U5, from their respective op amps.

The calibration procedure consists of a two step process. First, the bipolar offset is calibrated by selecting CH2, the 2.5 V system reference, of the analog multiplexer and preloading the DAC, U5, with a midscale code of 1000 0000. If possible, several readings of the A/D should be taken and averaged to determine the required digital offset adjustment code, U5. This averaged offset code requires an extra bit of resolution since 1 LSB of U5 equates to 1/2 LSB of the AD9221/AD9223/AD9220. The required offset correction code to U5 can then be determined. Second, the system gain is calibrated by selecting CH2, a 1.25 V input that corresponds to –FS of the A/D. Before the value is read, U4 should be preloaded with a code of 00 (Hex). Several readings can also be taken and averaged to determine the digital gain adjustment code to U2A. In this case, 1 LSB of the A/D corresponds to 1 LSB of U4.

Due to the AD9221/AD9223/AD9220's excellent INL performance, a two-point calibration procedure (i.e., –FS to midscale) instead of an endpoint calibration procedure was chosen. Also, since the bipolar offset is insensitive to any gain adjustment (due to the differential SHA of the A/D), an iterative calibration process is not required. The temperature stability of the circuit is enhanced by selecting a dual precision op amp for U2 (e.g., OP293) and low temperature drift, thin film resistors. Note that this application circuit was not built at the release of this data sheet. Please consult Analog Devices for application assistance or comments.

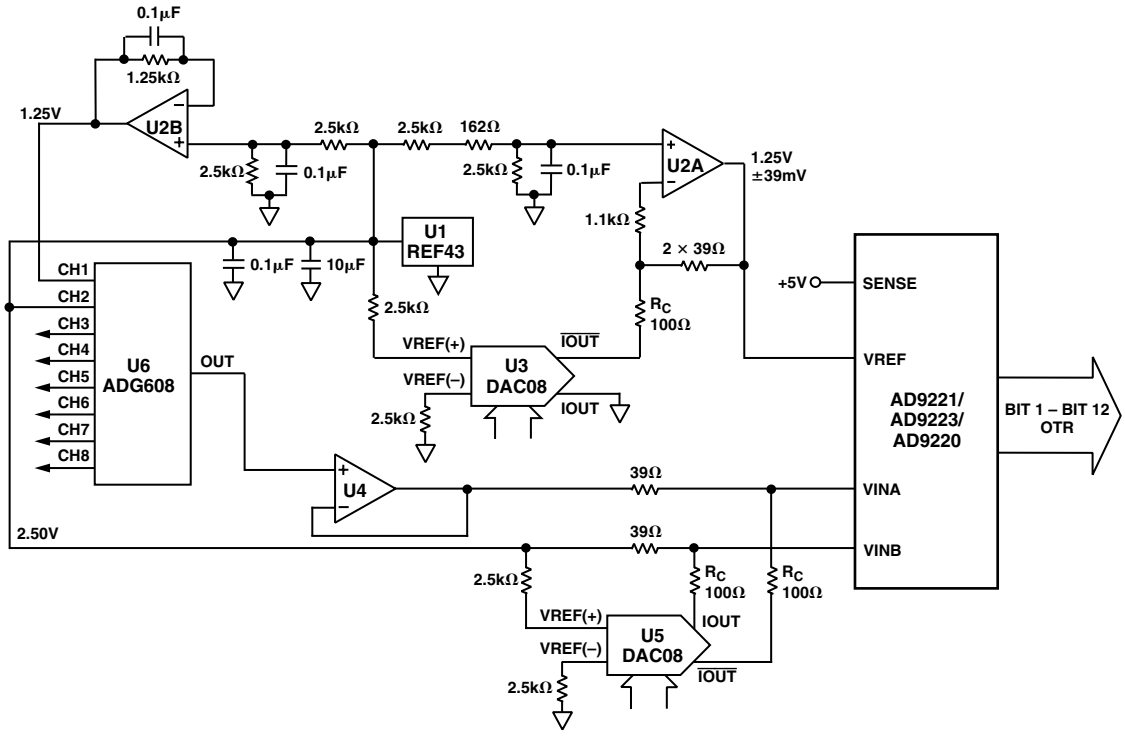


Figure 35. Typical Multichannel Data Acquisition System

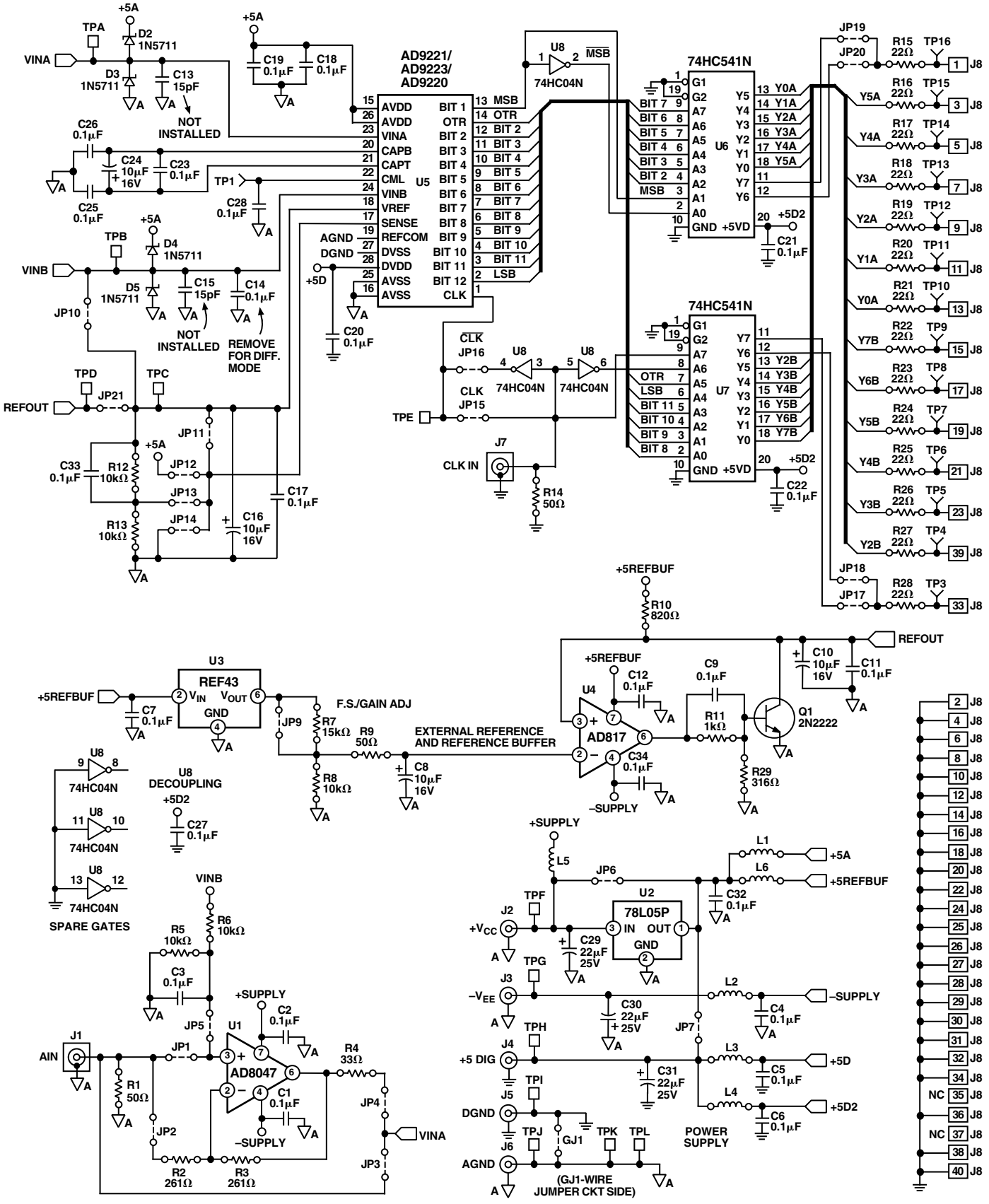


Figure 36. Evaluation Board Schematic

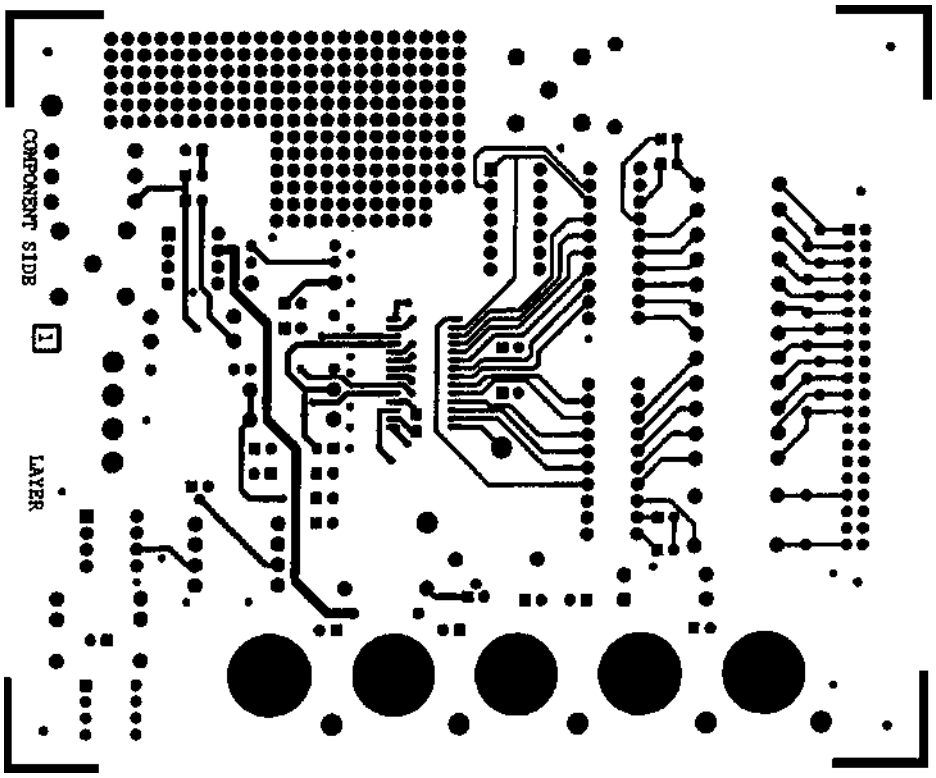


Figure 37. Evaluation Board Component Side Layout (Not to Scale)

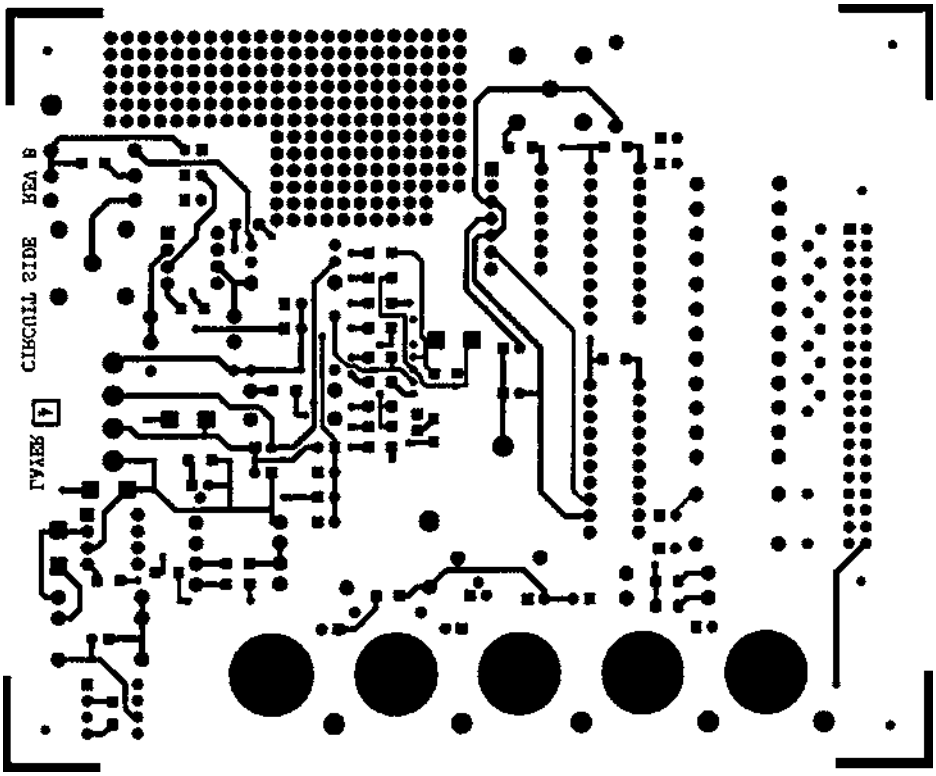


Figure 38. Evaluation Board Solder Side Layout (Not to Scale)

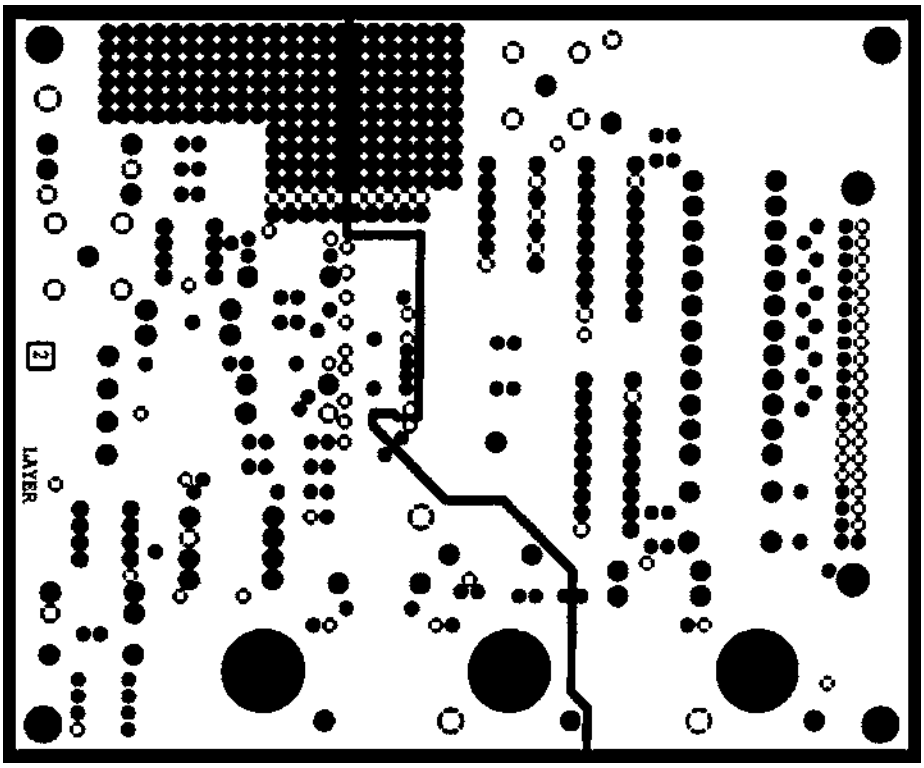


Figure 39. Evaluation Board Ground Plane Layout (Not to Scale)

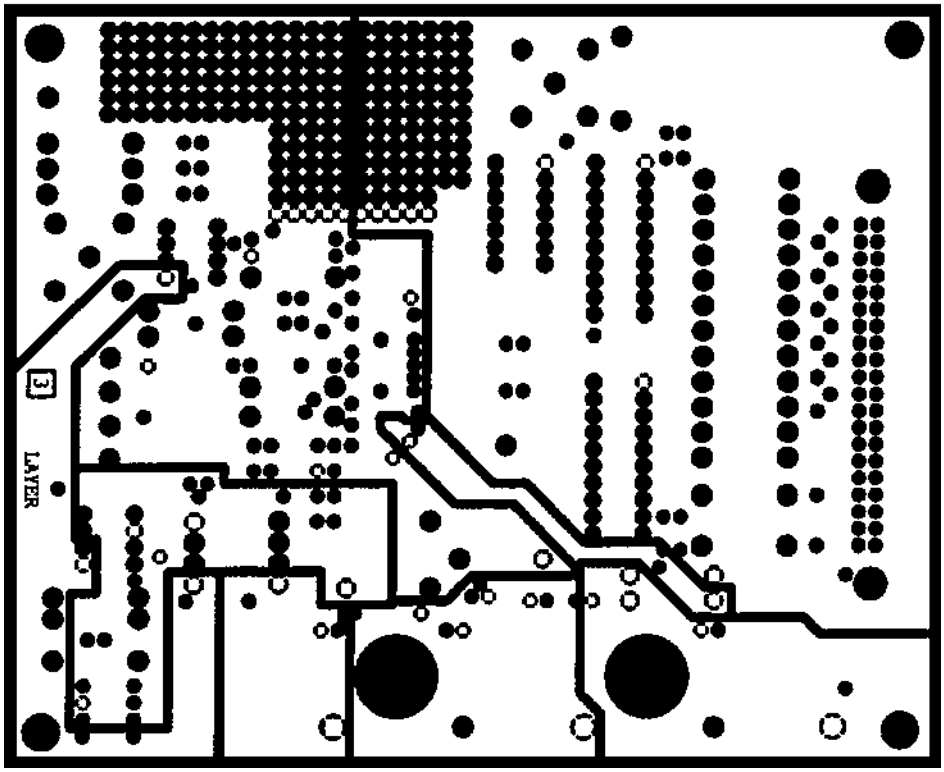


Figure 40. Evaluation Board Power Plane Layout

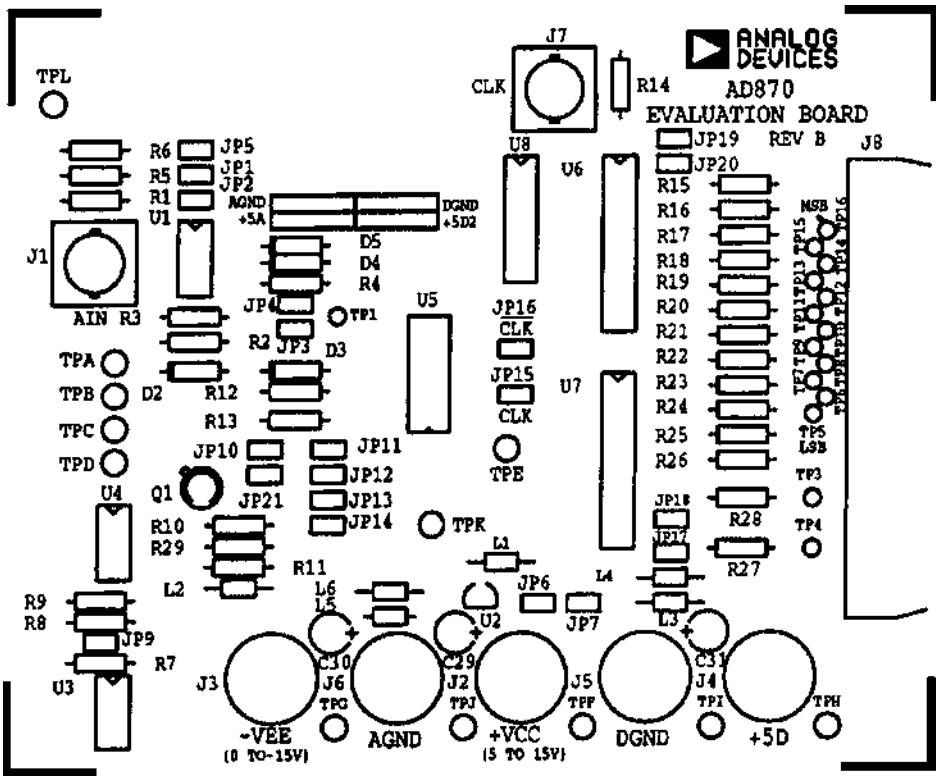


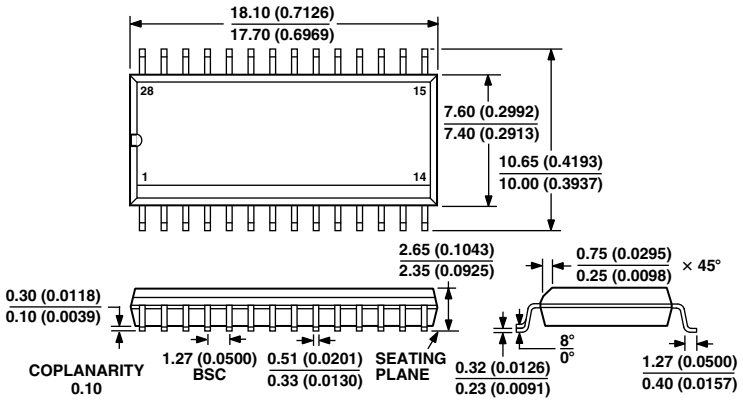
Figure 41. Evaluation Board Component Side Silkscreen (Not to Scale)

Figure 42. Evaluation Board Component Side Silkscreen (Not to Scale)

OUTLINE DIMENSIONS

28-Lead Standard SmWall Outline Package [SOIC]
Wide Body
(R-28)

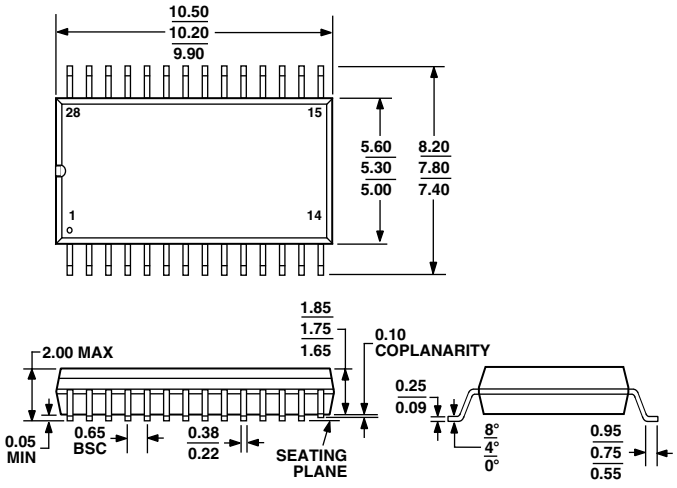
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Shrink Small Outline Package [SSOP]
(RS-28)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150AH

Revision History

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Updated graphic captions	Global
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Changes to ORDERING GUIDE	4
Changes to INTRODUCTION	9
Changes to Digital Output Driver Considerations (DVDD) section	21
Updated OUTLINE DIMENSIONS	29

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