

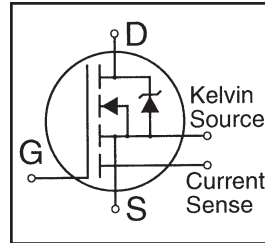


THE DATASHEET OF IRCZ24PBF



HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Current Sense
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

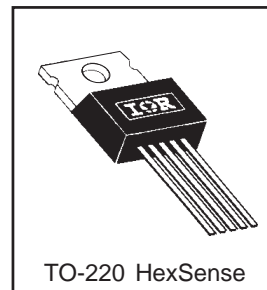


$V_{DSS} = 55V$
$R_{DS(on)} = 0.040\Omega$
$I_D = 26A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device, low on-resistance and cost-effectiveness.

The HEXSense device provides an accurate fraction of the drain current through the additional two leads to be used for control or protection of the device. These devices exhibit similar electrical and thermal characteristics as their IRF-series equivalent part numbers. The provision of a kelvin source connection effectively eliminates problems of common source inductance when the HEXSense is used as a fast, high-current switch in non current-sensing applications.



Absolute Maximum Ratings

Parameter		Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	17	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	
I_{DM}	Pulsed Drain Current ①	68	
$P_D @ T_C = 25^\circ C$	Power Dissipation	60	W
	Linear Derating Factor	0.40	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	6.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	A
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

Parameter	Parameter	Min.	Max.	Units	
$R_{\theta JC}$	Junction-to-Case	—	—	2.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

** When mounted on FR-4 board using minimum recommended footprint. For recommended footprint and soldering techniques refer to application note #AN-994.

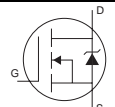
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)DSS}$	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$	
$\Delta V_{(BR)DSS}/\Delta T_J$	—	0.061	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$	
$R_{DS(ON)}$	—	—	0.10	Ω	$V_{GS} = 10V, I_D = 10A$ ②	
$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$	
g_{fs}	5.8	—	—	S	$V_{DS} = 25V, I_D = 10A$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	25		$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100		$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	24		$I_D = 17A$
Q_{gs}	Gate-to-Source Charge	—	—	6.3		$V_{DS} = 48V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.0		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	12	—		$V_{DD} = 30V$
t_r	Rise Time	—	59	—		$I_D = 17A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 18\Omega$
t_f	Fall Time	—	38	—		$R_D = 1.7\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25 in.) from package and center of die contact
L_C	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	720	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	360	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	75	—		$f = 1.0\text{MHz}$, See Fig. 5
r	Current Sensing Ratio	740	—	820		$I_D = 17A, V_{GS} = 10V$
C_{oss}	Output Capacitance of Sensing Cells	—	14	—	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$

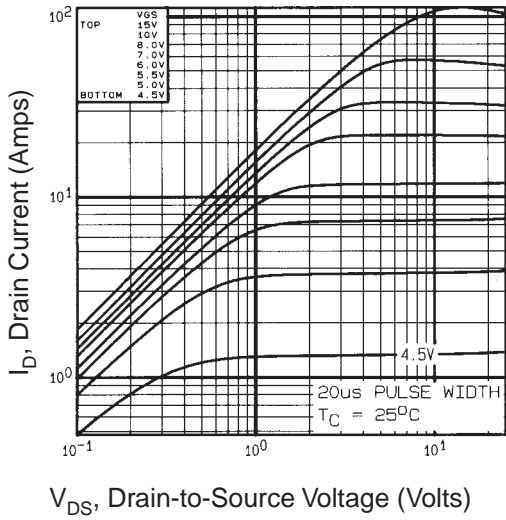
Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Conditions	
I_S	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 	
I_{SM}	—	—	68			
V_{SD}	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ④	
t_{rr}	—	87	180	ns	$T_J = 25^\circ\text{C}, I_F = 17A$	
Q_{rr}	—	0.29	0.60	nC	$di/dt = 100A/\mu s$ ④	
t_{on}	Forward Turn-On Time					Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)

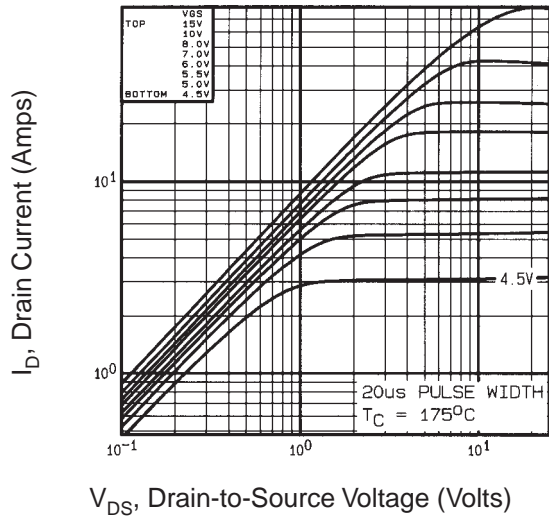
Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 0.024\text{mH}$, $R_G = 25\Omega, I_{AS} = 17A$. (See Figure 12)
- ③ $I_{SD} \leq 17A, di/dt \leq 140A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

C-2



**Fig. 1 Typical Output Characteristics,
 $T_C=25^\circ\text{C}$**



**Fig. 2 Typical Output Characteristics,
 $T_C=175^\circ\text{C}$**

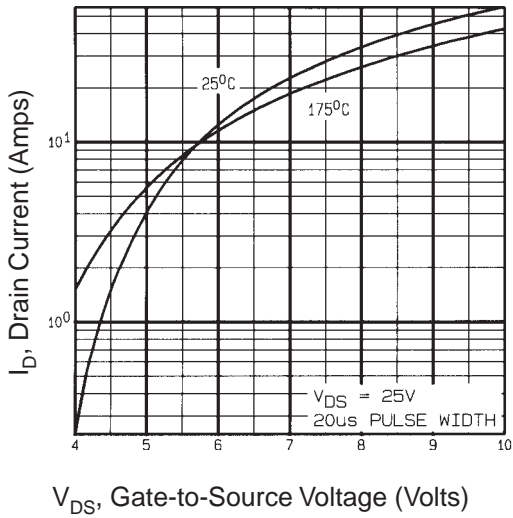
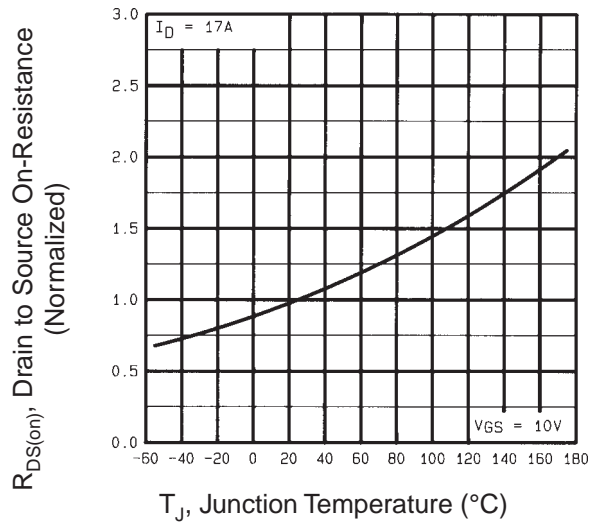


Fig. 3 Typical Transfer Characteristics



**Fig. 4 Normalized On-Resistance vs.
 Temperature**

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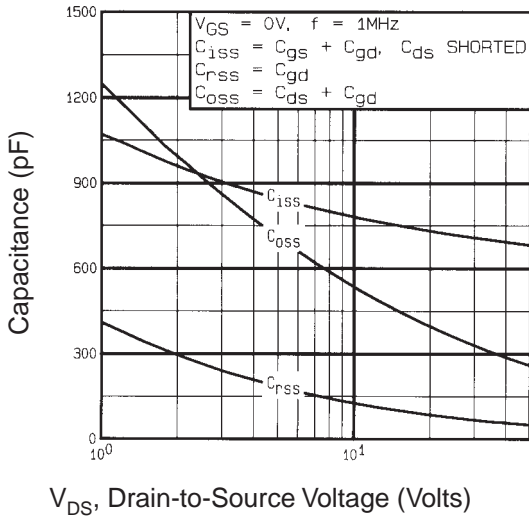


Fig. 5 Typical Capacitance vs. Drain-to-Source Voltage

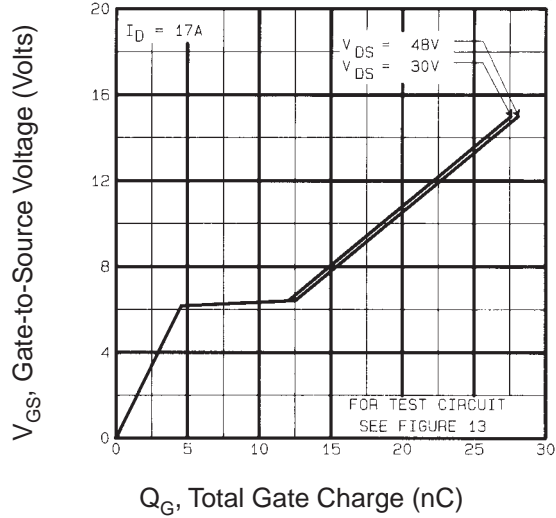


Fig. 6 Typical Gate Charge vs. Gate-to-Source Voltage

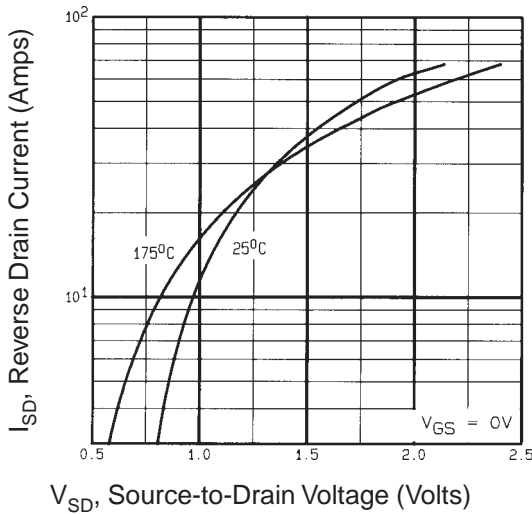


Fig. 7 Typical Source-Drain Diode Forward Voltage

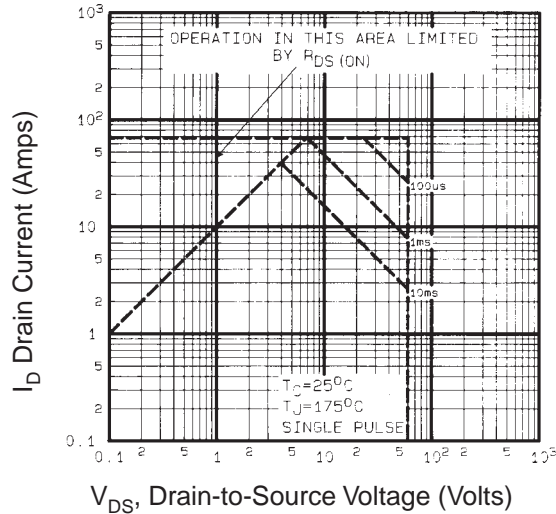


Fig. 8 Maximum Safe Operating Area

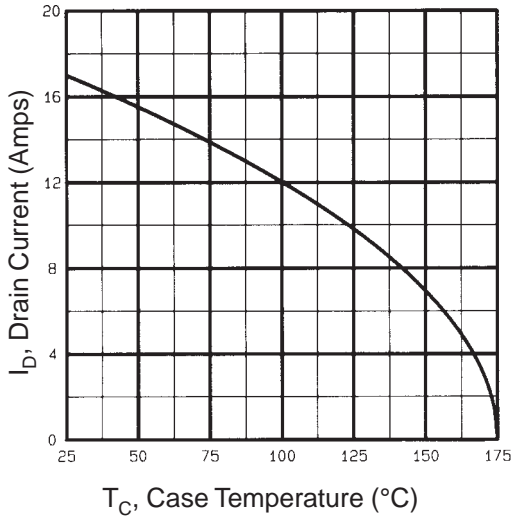


Fig. 9 Maximum Drain Current vs. Case Temperature

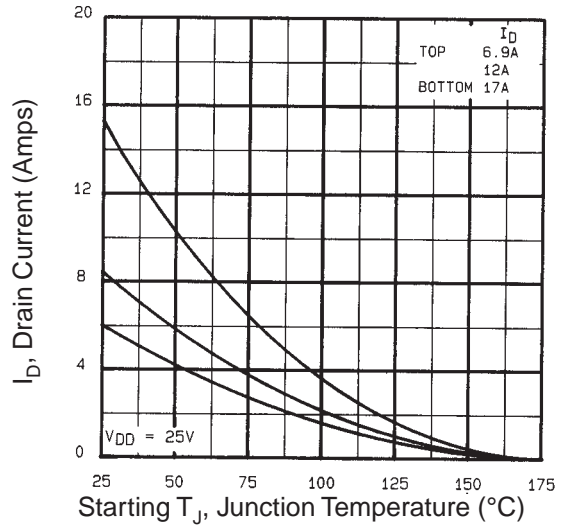


Fig. 12c Maximum Avalanche Energy vs. Drain Current

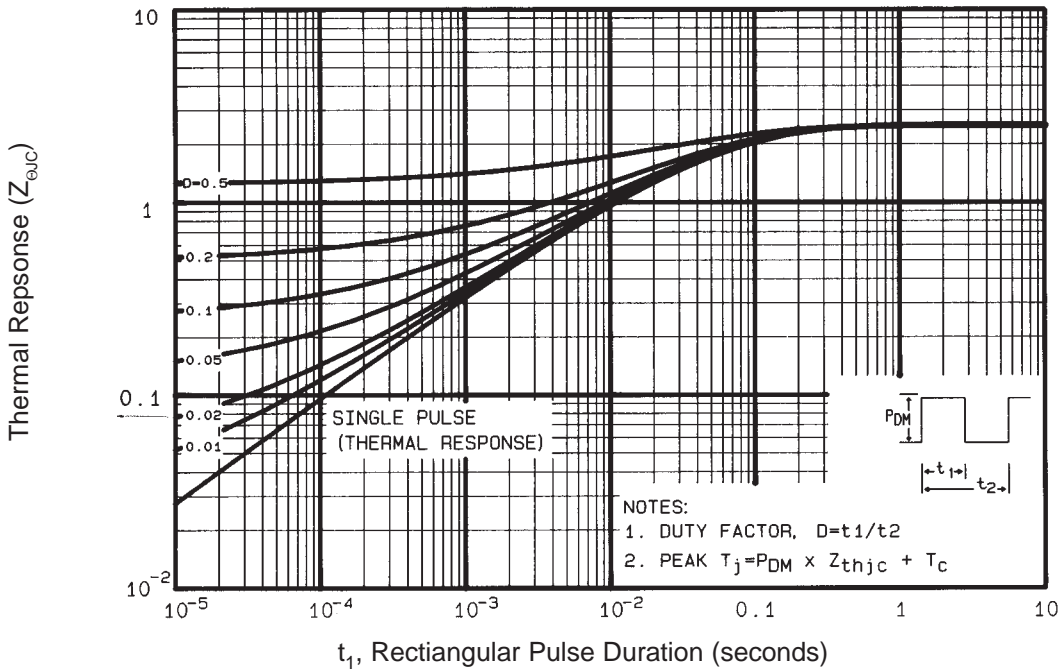


Fig. 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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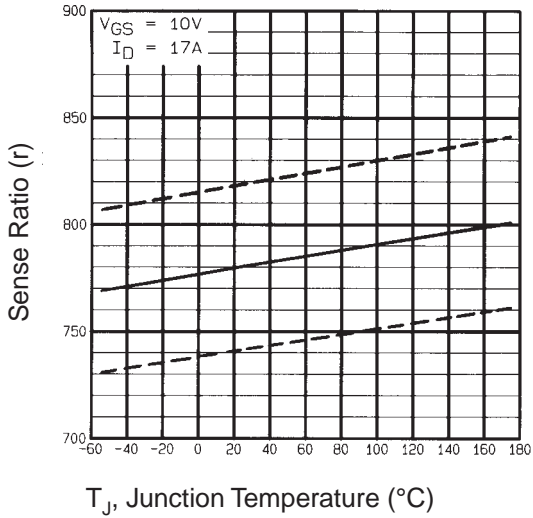


Fig. 15 Typical HEXSense Ratio vs. Junction Temperature

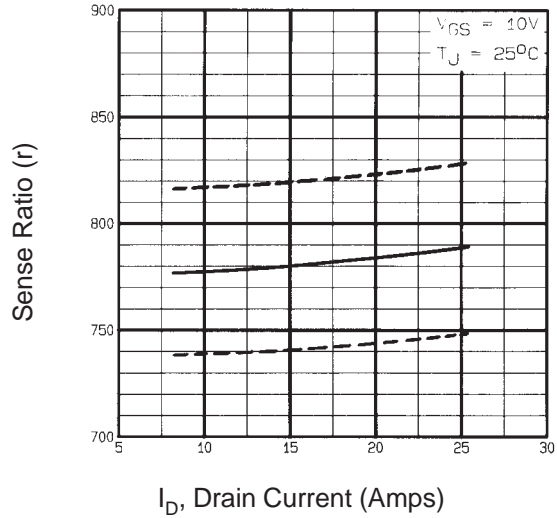


Fig. 16 Typical HEXSense Ratio vs. Drain Current

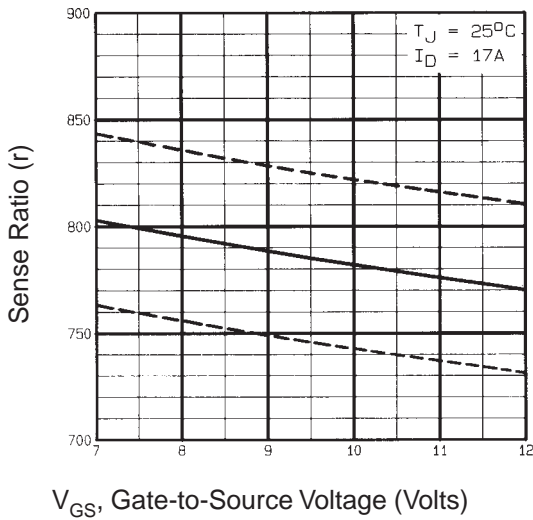


Fig. 17 Typical HEXSense Ratio vs. Gate Voltage

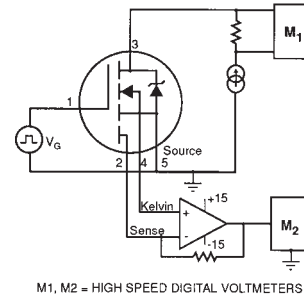


Fig. 18 HEXSense Ratio Test Circuit

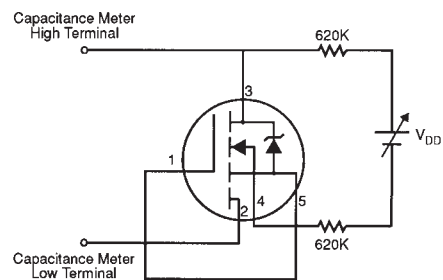


Fig. 19 HEXSense Sensing Cell Output Capacitance Test Circuit

Mechanical drawings, Appendix A
Part marking information, Appendix B
Test Circuit diagrams, Appendix C

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