



**THE DATASHEET OF
PI2DDR3212NCE**



Features

- 14 bit 2:1 switch that supports up to 5Gbps DDR3 signals
- VDD 1.5V or 1.8V +/- 10%
- SEL and Global Enable
- 220 μ A typ. operating current
- High impedance and low Coff channel output when disabled or deselected
- Low R_{ON} : 8 Ω typical
- 3dB Bandwidth: 2.7GHz
- Low insertion loss: -0.6dB ($0 \leq f \leq 1$ GHz)
- Low cross-talk for high speed channels: -18dB typ. ($0 < f < 2$ GHz)
- Low bit-to-bit skew 20ps Max
- ESD: 2KV HBM
- SSTL_15 or SSTL_18 signaling
- Packaging (Pb-free and Green)
 - 52 pin TQFN (3.5x9x0.4mm)
 - 48 pin TFBGA (4.5x4.5x0.8mm) pin compatible with CBTW28DD14

Description

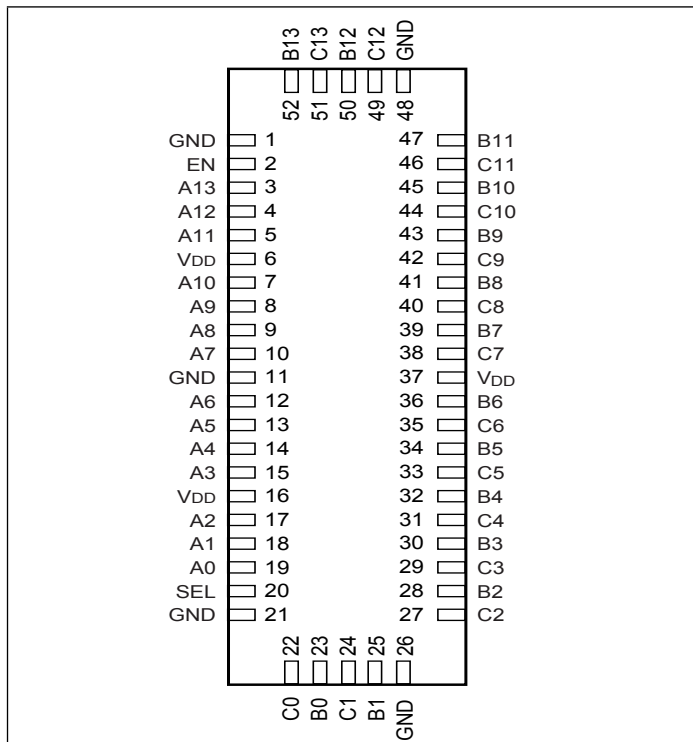
This 14-bit DDR switch is designed for 1.5V or 1.8V supply voltage, SSTL_15 or SSTL_18 signaling and CMOS select input signals. It is designed for DDR2 or DDR3 memory bus with speed up to 5Gbps.

PI2DDR3212 has a 1:2 demux or 2:1 mux topology. All 14-bit channels can be switched to one of the two ports simultaneously with the SEL input. This device also allows all ports to be disconnected.

PI2DDR3212 uses Pericom's proprietary high speed switch technology providing consistent high bandwidth across all channels, with very little insertion loss, cross-talk, and bit to bit skew.

It is available in a 52-pin TQFN 3.5x9x0.4mm package and 48-pin TFBGA 4.5x4.5x0.8mm package. The 48-pin version is pin compatible with CBTW28DD14.

Pin Configuration (52-pin TQFN)



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