



**THE DATASHEET OF  
TPS76715QDR**



# TPS767xxQ Fast-Transient-Response 1-A Low-Dropout Linear Regulators

## 1 Features

- 1 A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Down to 230 mV at 1 A (TPS76750)
- Ultralow 85  $\mu$ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power-On Reset With 200-ms Delay (See TPS768xx for PG Option)
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

## 2 Description

This device is designed to have a fast transient response and be stable with 10  $\mu$ F low ESR capacitors. This combination provides high performance at a reasonable cost.

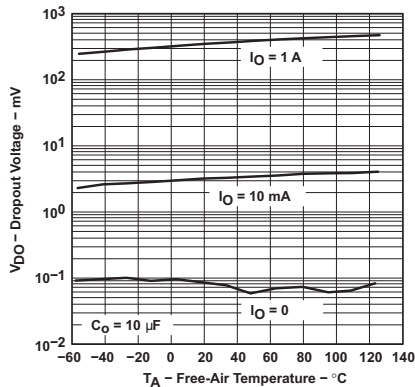
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76750) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85  $\mu$ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 1  $\mu$ A at  $T_j = 25^\circ\text{C}$ .

### Device Information<sup>(1)</sup>

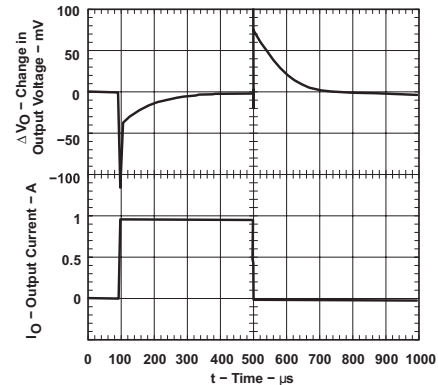
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS767xx	SOIC (8)	4.90 mm x 3.91 mm
	HTSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**TPS76733 Dropout Voltage vs Free-air Temperature**



**TPS76733 Load Transient Response**



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	<b>13</b>
<b>2 Description</b> .....	<b>1</b>	9.3 Feature Description .....	<b>14</b>
<b>3 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	<b>15</b>
<b>4 Description (Continued)</b> .....	<b>3</b>	9.5 Programming .....	<b>15</b>
<b>5 Device Options</b> .....	<b>3</b>	<b>10 Application and Implementation</b> .....	<b>16</b>
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	10.1 Application Information .....	<b>16</b>
<b>7 Specifications</b> .....	<b>5</b>	10.2 Typical Application .....	<b>16</b>
7.1 Absolute Maximum Ratings .....	<b>5</b>	<b>11 Layout</b> .....	<b>18</b>
7.2 ESD Ratings .....	<b>5</b>	11.1 Power Dissipation and Junction Temperature .....	<b>18</b>
7.3 Recommended Operating Conditions .....	<b>5</b>	<b>12 Device and Documentation Support</b> .....	<b>19</b>
7.4 Thermal Information .....	<b>5</b>	12.1 Related Links .....	<b>19</b>
7.5 Electrical Characteristics .....	<b>6</b>	12.2 Community Resources .....	<b>19</b>
7.6 Typical Characteristics .....	<b>8</b>	12.3 Trademarks .....	<b>19</b>
<b>8 Parameter Measurement Information</b> .....	<b>12</b>	12.4 Electrostatic Discharge Caution .....	<b>19</b>
<b>9 Detailed Description</b> .....	<b>13</b>	12.5 Glossary .....	<b>19</b>
9.1 Overview .....	<b>13</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>19</b>

## 3 Revision History

### Changes from Revision I (January 2004) to Revision J

Page

- Added *ESD Ratings* table, *Overview* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**

## 4 Description (Continued)

The **RESET** output of the TPS767xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767xx family is available in 8-pin SOIC and 20-pin PWP packages.

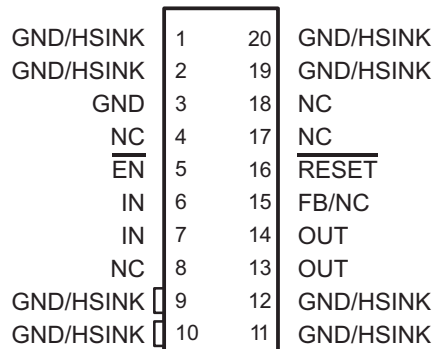
## 5 Device Options

PART NO. <sup>(1)</sup>		VOLTAGE OPTIONS (V)
TSSOP (PWP)	SOIC (D)	TYP
TPS76750Q	TPS76750Q	5
TPS76733Q	TPS76733Q	3.3
TPS76730Q	TPS76730Q	3
TPS76728Q	TPS76728Q	2.8
TPS76727Q	TPS76727Q	2.7
TPS76725Q	TPS76725Q	2.5
TPS76718Q	TPS76718Q	1.8
TPS76715Q	TPS76715Q	1.5
TPS76701Q	TPS76701Q	Adjustable 1.5 V to 5.5 V

(1) The TPS76701 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS76701QDR).

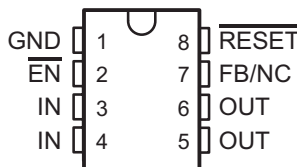
## 6 Pin Configuration and Functions

**PWP Package  
20 Pin HTSSOP  
Top View**



NC – No internal connection

**D Package  
8 Pin SOIC  
Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
<b>SOIC PACKAGE</b>			
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
$\overline{\text{RESET}}$	8	O	RESET output
<b>HTSSOP PACKAGE</b>			
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
$\overline{\text{RESET}}$	16	O	RESET output

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.3	13.5	V
	Voltage range at EN	-0.3	V <sub>I</sub> + 0.3	V
	Maximum RESET voltage		16.5	
	Peak output current		Internally limited	
V <sub>O</sub>	Output voltage (OUT, FB)		7	V
	Continuous total power dissipation		See <a href="#">Thermal Information</a>	
T <sub>J</sub>	Operating junction temperature range	-40	125	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network terminal ground.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>I</sub> <sup>(1)</sup>	Input voltage	2.7	10	V
V <sub>O</sub>	Output voltage range	1.2	5.5	V
I <sub>O</sub> <sup>(2)</sup>	Output current	0	1.0	A
T <sub>J</sub> <sup>(2)</sup>	Operating junction temperature	-40	125	°C

- (1) Maximum V<sub>IN</sub> = V<sub>OUT</sub> + V<sub>DO</sub> or 2.7V, whichever is greater.
- (2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPS767xxQ		UNIT	
	PWP (HTSSOP)	D (SOIC)		
	(20 PINS)	(8 PINS)		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	35.8	106.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26.1	52.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	8.7	47.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	9.0	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.6	47.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.6	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 1 \text{ mA}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 10 \mu\text{F}$  (over recommended operating free-air temperature range, unless otherwise noted)

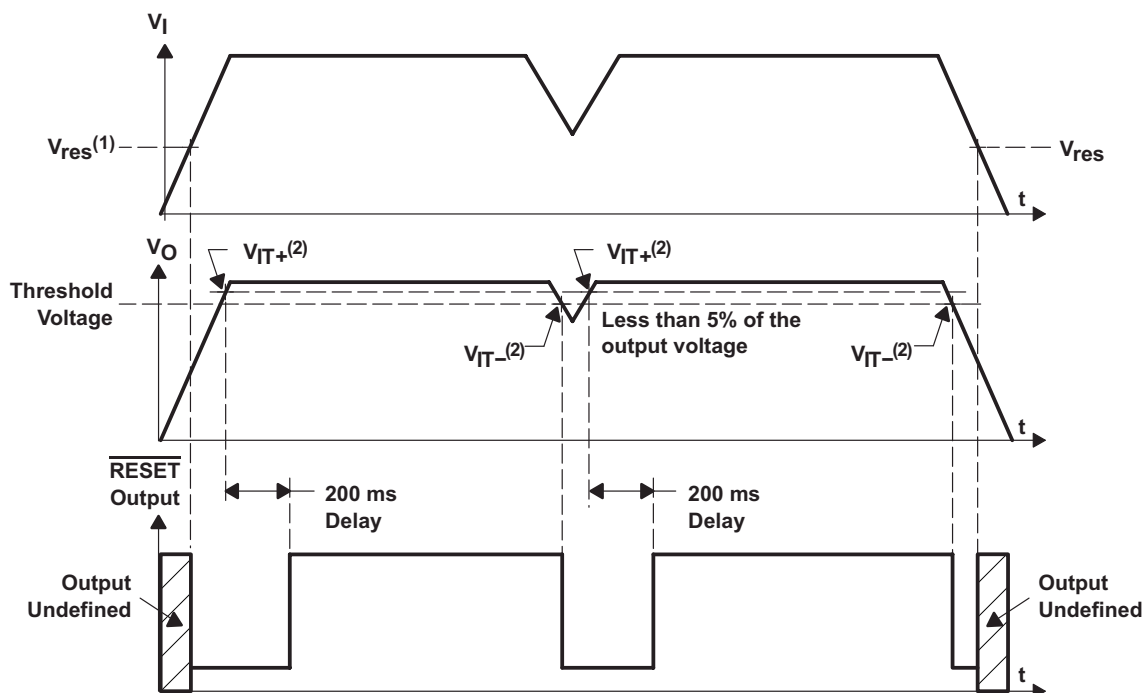
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 $\mu\text{A}$ to 1 A load)	TPS76701	$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = 25^\circ\text{C}$		$V_O$		V
		$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	0.98 $V_O$		1.02 $V_O$	
	TPS76715	$T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.5		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.470		1.530	
	TPS76718	$T_J = 25^\circ\text{C}$ , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.8		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.7646		1.836	
	TPS76725	$T_J = 25^\circ\text{C}$ , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.5		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.450		2.550	
	TPS76727	$T_J = 25^\circ\text{C}$ , $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.7		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.646		2.754	
	TPS76728	$T_J = 25^\circ\text{C}$ , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.8		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.7446		2.856	
	TPS76730	$T_J = 25^\circ\text{C}$ , $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.9400		3.060	
	TPS76733	$T_J = 25^\circ\text{C}$ , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.3		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.2346		3.366	
	TPS76750	$T_J = 25^\circ\text{C}$ , $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		5		V
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	4.900		5.100	
Quiescent current (GND current) $\overline{\text{EN}} = 0\text{V}$		$10 \mu\text{A} < I_O < 1 \text{ A}$ , $T_J = 25^\circ\text{C}$		85		$\mu\text{A}$
		$I_O = 1 \text{ A}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$			125	
Output voltage line regulation ( $\Delta V_O/V_O$ )		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$ , $T_J = 25^\circ\text{C}$		0.01		%/V
Load regulation				3		mV
Output noise voltage	TPS76718	BW = 200 Hz to 100 kHz, $C_O = 10 \mu\text{F}$ , $I_C = 1 \text{ A}$ , $T_J = 25^\circ\text{C}$		55		$\mu\text{V}_{\text{rms}}$
Output current limit		$V_O = 0 \text{ V}$	1.2	1.7	2	A
Thermal shutdown junction temperature				150		$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_I$ , $T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_I < 10 \text{ V}$		1		$\mu\text{A}$
		$\overline{\text{EN}} = V_I$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.7 \text{ V} < V_I < 10 \text{ V}$			10	$\mu\text{A}$
FB input current	TPS76701	FB = 1.5 V		2		nA
High level enable input voltage			1.7			V
Low level enable input voltage					0.9	V
Power supply ripple rejection		$f = 1 \text{ kHz}$ , $C_O = 10 \mu\text{F}$ , $T_J = 25^\circ\text{C}$		60		dB
Reset	Minimum input voltage for valid RESET	$I_{O(\text{RESET})} = 300 \mu\text{A}$		1.1		
	Trip threshold voltage	$V_O$ decreasing	92		98	
	Hysteresis voltage	Measured at $V_O$		0.5		
	Output low voltage	$V_I = 2.7 \text{ V}$ , $I_{O(\text{RESET})} = 1 \text{ mA}$		0.15		0.4
	Leakage current	$V_{(\text{RESET})} = 5 \text{ V}$				1
RESET time-out delay				200		
Input current ( $\overline{\text{EN}}$ )		$\overline{\text{EN}} = 0 \text{ V}$	-1	0	1	$\mu\text{A}$
		$\overline{\text{EN}} = V_I$	-1		1	

**Electrical Characteristics (continued)**

$V_I = V_{O(typ)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 10\text{ }\mu\text{F}$  (over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage <sup>(1)</sup>	TPS76728	$I_O = 1\text{ A}$	$T_J = 25^\circ\text{C}$	500		mV
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		825	
	TPS76730	$I_O = 1\text{ A}$	$T_J = 25^\circ\text{C}$	450		mV
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		675	
	TPS76733	$I_O = 1\text{ A}$	$T_J = 25^\circ\text{C}$	350		mV
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		575	
	TPS76750	$I_O = 1\text{ A}$	$T_J = 25^\circ\text{C}$	230		mV
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		380	

(1) IN voltage equals  $V_{O(typ)} - 100\text{ mV}$ ; TPS76701 output voltage set to 3.3 V nominal with external resistor divider. TPS76715, TPS76718, TPS76725, and TPS76727 dropout voltage limited by input voltage range limitations (i.e., TPS76730 input voltage needs to drop to 2.9 V for purpose of this test).



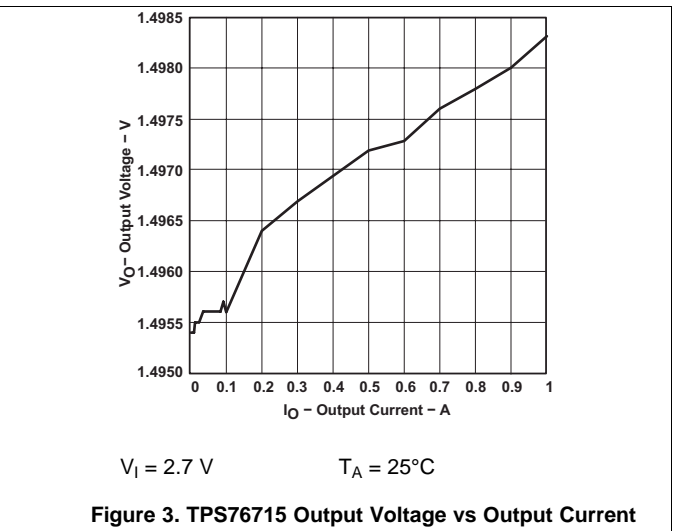
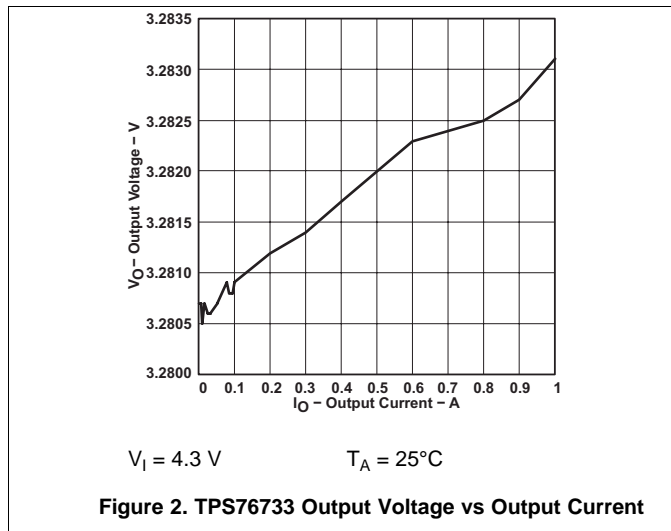
**Figure 1. Timing Diagram**

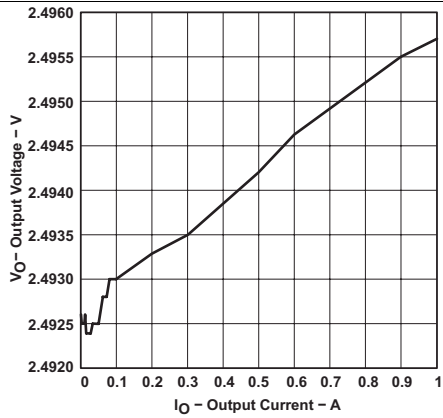
## 7.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
V <sub>O</sub>	Output voltage	vs Output current
		vs Free-air temperature
	Ground current	vs Free-air temperature
	Power supply ripple rejection	vs Frequency
	Output spectral noise density	vs Frequency
	Input voltage (min)	vs Output voltage
Z <sub>o</sub>	Output impedance	vs Frequency
V <sub>DO</sub>	Dropout voltage	vs Free-air temperature
	Line transient response	
	Load transient response	
V <sub>O</sub>	Output voltage	vs Time
	Dropout voltage	vs Input voltage
	Equivalent series resistance (ESR) <sup>(1)</sup>	vs Output current

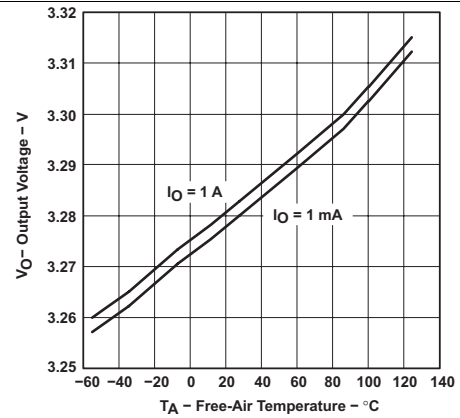
(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C<sub>o</sub>.





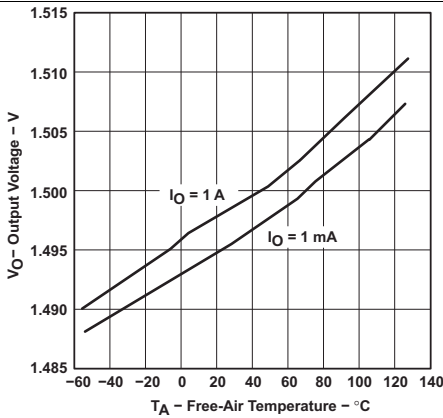
$V_I = 3.5 \text{ V}$        $T_A = 25^\circ\text{C}$

Figure 4. TPS76725 Output Voltage vs Output Current



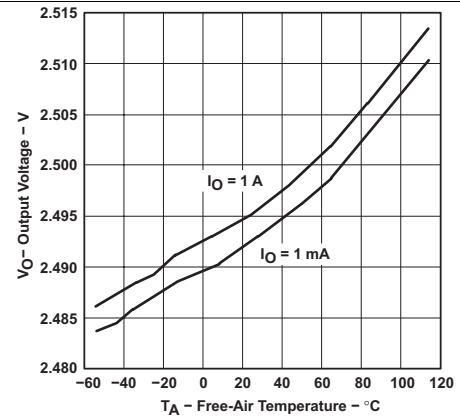
$V_I = 4.3 \text{ V}$

Figure 5. TPS76733 Output Voltage vs Free-Air Temperature



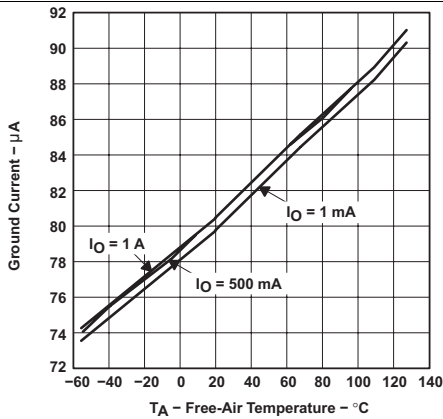
$V_I = 2.7 \text{ V}$

Figure 6. TPS76715 Output Voltage vs Free-Air Temperature



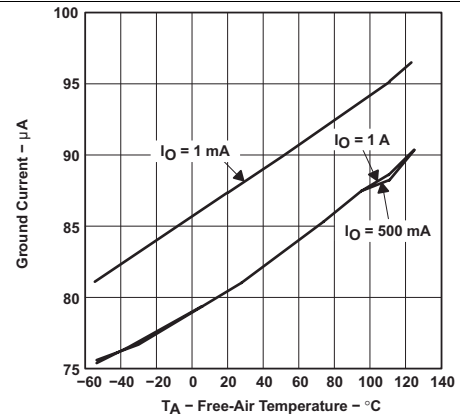
$V_I = 3.5 \text{ V}$

Figure 7. TPS767125 Output Voltage vs Free-Air Temperature



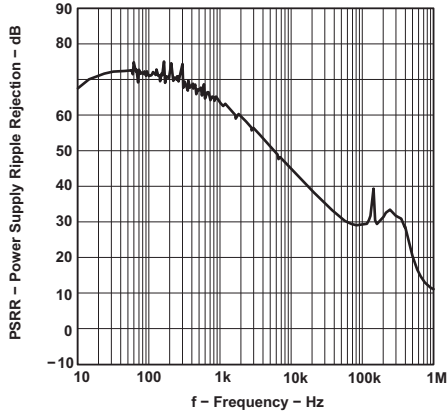
$V_I = 4.3 \text{ V}$

Figure 8. TPS76733 Ground Current vs Free-Air Temperature



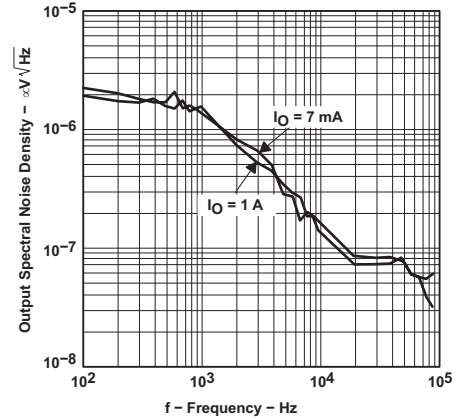
$V_I = 2.7 \text{ V}$

Figure 9. TPS76715 Ground Current vs Free-Air Temperature



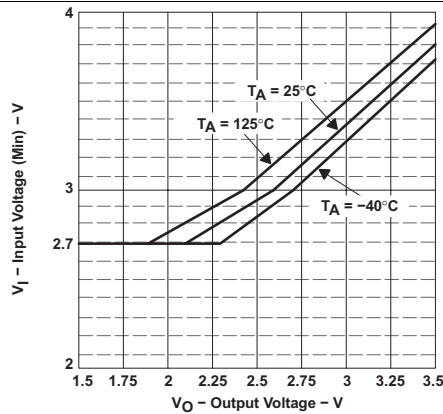
$V_I = 4.3\text{ V}$        $C_O = 10\ \mu\text{F}$   
 $I_O = 1\ \text{A}$        $T_A = 25^\circ\text{C}$

Figure 10. TPS76733 Power Supply Ripple Rejection vs Frequency



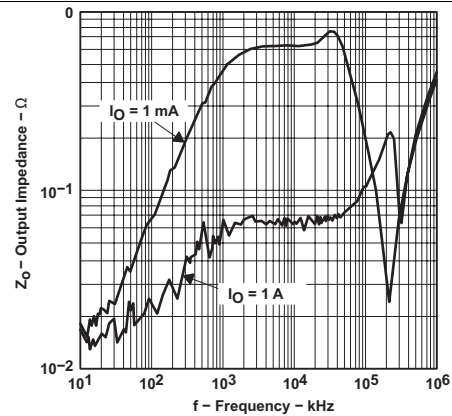
$V_I = 4.3\text{ V}$        $C_O = 10\ \mu\text{F}$        $T_A = 25^\circ\text{C}$

Figure 11. TPS76733 Output Spectral Noise Density vs Frequency



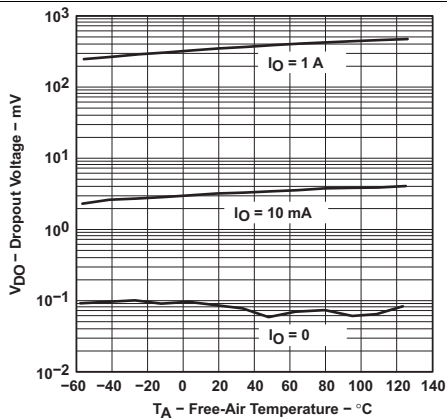
$I_O = 1\ \text{A}$

Figure 12. Input Voltage (MIN) vs Output Voltage



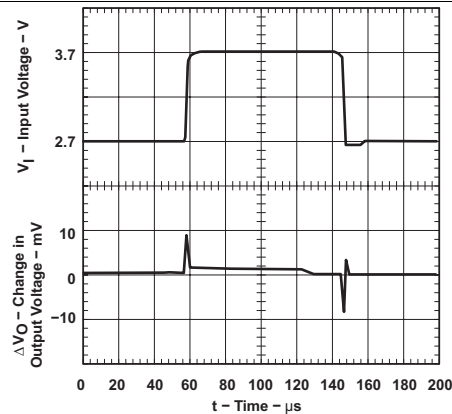
$V_I = 4.3\text{ V}$        $C_O = 10\ \mu\text{F}$        $T_A = 25^\circ\text{C}$

Figure 13. TPS76733 Output Impedance vs Frequency



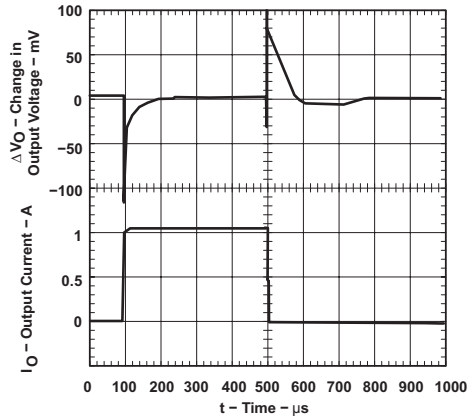
$C_O = 10\ \mu\text{F}$

Figure 14. TPS76733 Dropout Voltage vs Free-Air Temperature



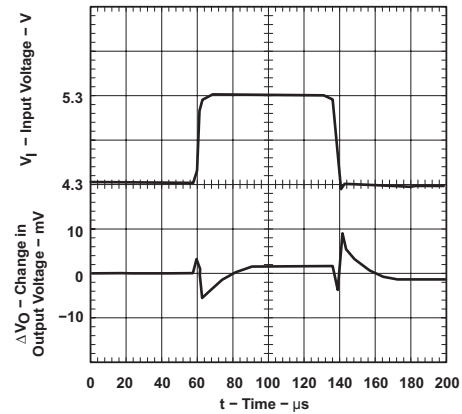
$C_O = 10\ \mu\text{F}$        $T_A = 25^\circ\text{C}$

Figure 15. TPS76715 Line Transient Response



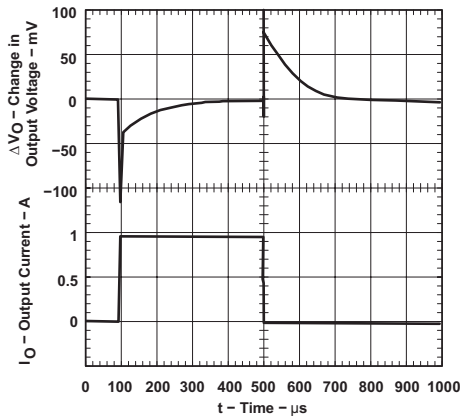
$C_O = 10 \mu\text{F}$        $T_A = 25^\circ\text{C}$

Figure 16. TPS76715 Load Transient Response



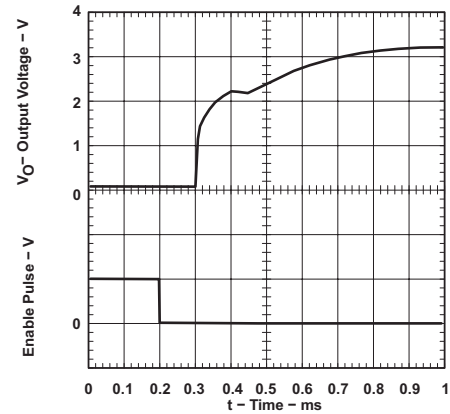
$C_O = 10 \mu\text{F}$        $T_A = 25^\circ\text{C}$

Figure 17. TPS76733 Line Transient Response



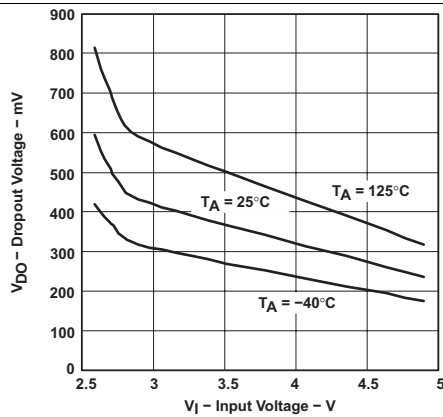
$C_O = 10 \mu\text{F}$        $T_A = 25^\circ\text{C}$

Figure 18. TPS76733 Load Transient Response



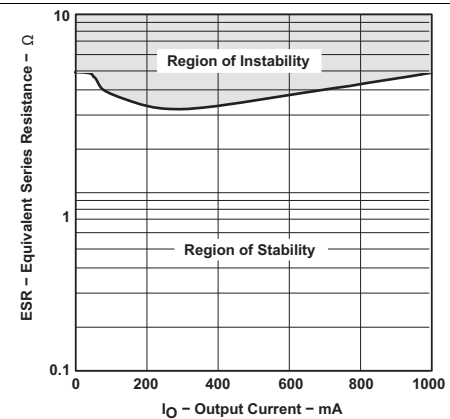
$C_O = 10 \mu\text{F}$        $I_O = 1 \text{ A}$        $T_A = 25^\circ\text{C}$

Figure 19. TJPS7633 Output Voltage vs Time (At Startup)



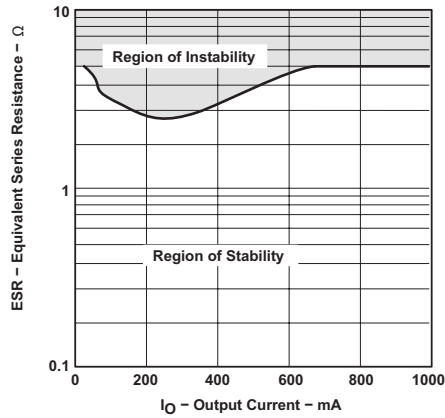
$I_O = 1 \text{ A}$

Figure 20. TPS76701 Dropout Voltage vs Input Voltage



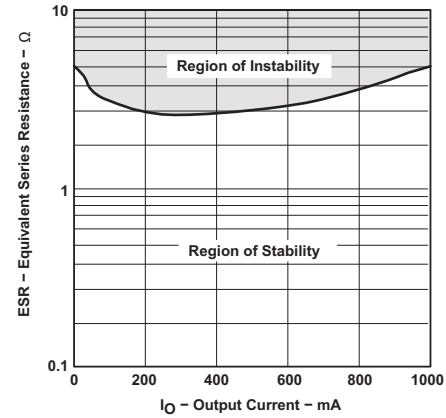
$V_O = 3.3 \text{ V}$        $C_O = 4.7 \mu\text{F}$   
 $V_I = 4.3 \text{ A}$        $T_A = 25^\circ\text{C}$

Figure 21. Typical Region of Stability Equivalent Series Resistance vs Output Current



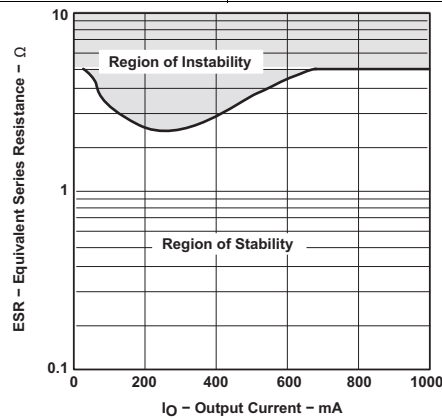
$V_O = 3.3\text{ V}$        $C_O = 4.7\ \mu\text{F}$   
 $V_I = 4.3\text{ A}$        $T_A = 125^\circ\text{C}$

Figure 22. Typical Region of Stability  
Equivalent Series Resistance vs Output Current



$V_O = 3.3\text{ V}$        $C_O = 22\ \mu\text{F}$   
 $V_I = 4.3\text{ A}$        $T_A = 25^\circ\text{C}$

Figure 23. Typical Region of Stability  
Equivalent Series Resistance vs Output Current



$V_O = 3.3\text{ V}$        $C_O = 22\ \mu\text{F}$   
 $V_I = 4.3\text{ A}$        $T_A = 125^\circ\text{C}$

Figure 24. Typical Region of Stability  
Equivalent Series Resistance vs Output Current

## 8 Parameter Measurement Information

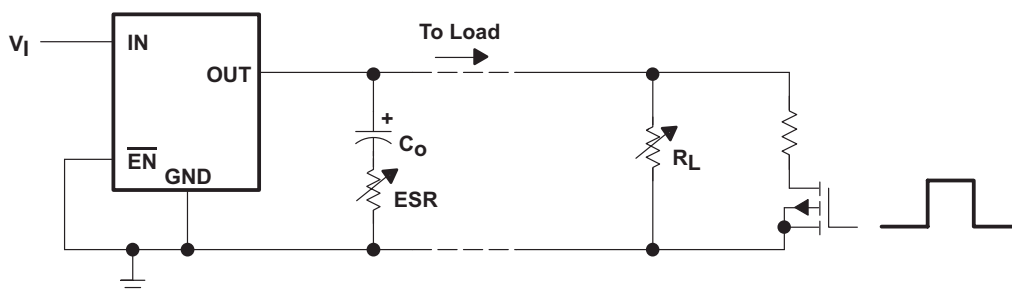
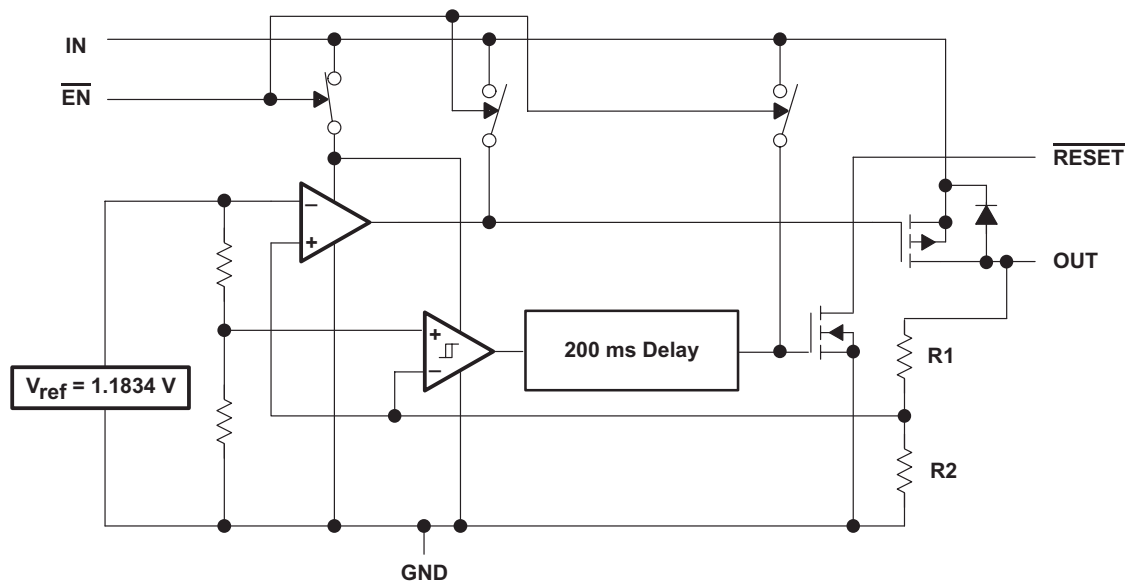


Figure 25. Test Circuit for Typical Regions of Stability (Figure 21 through Figure 24) (Fixed Output Options)



**Functional Block Diagram (continued)**

**Figure 27. Fixed-Voltage Version**
**9.3 Feature Description**
**9.3.1 FB—Pin Connection (adjustable version only)**

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as shown in [Figure 28](#). Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

**9.3.2 Reset Indicator**

The TPS767xx features a  $\overline{\text{RESET}}$  output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the  $\overline{\text{RESET}}$  output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating.  $\overline{\text{RESET}}$  can be used to drive power-on reset circuitry or as a low-battery indicator.  $\overline{\text{RESET}}$  does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to [Figure 1](#) timing diagram for start-up sequence).

**9.3.3 Regulator Protection**

The TPS767xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767xx also features internal current limiting and thermal protection. During normal operation, the TPS767xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

## 9.4 Device Functional Modes

### 9.4.1 Minimum Load Requirements

The TPS767xx family is stable even at zero load; no minimum load is required for operation.

## 9.5 Programming

### 9.5.1 Programming the TPS76701 Adjustable LDO Regulator

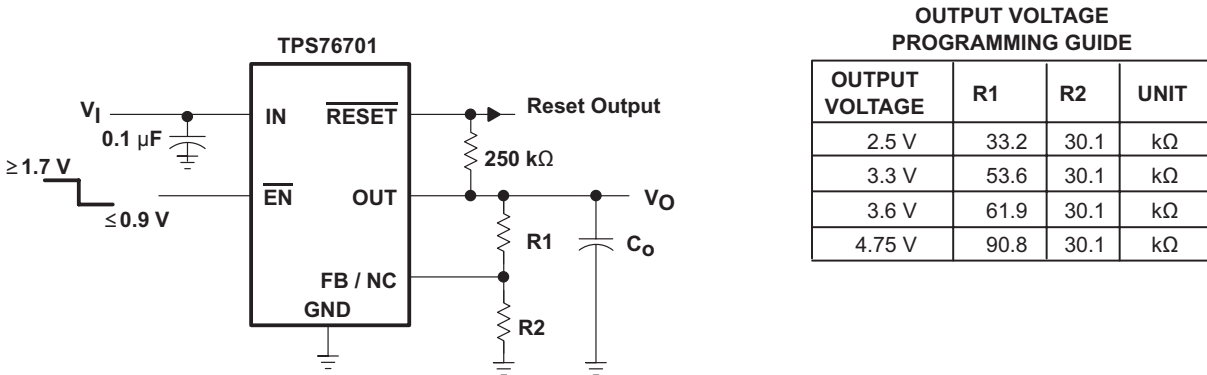
The output voltage of the TPS76701 adjustable regulator is programmed using an external resistor divider as shown in [Figure 28](#). The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:  $f = 1.1834 \text{ V typ}$  (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50- $\mu\text{A}$  divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose  $R2 = 30.1 \text{ k}\Omega$  to set the divider current at 50  $\mu\text{A}$  and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



**Figure 28. TPS76701 Adjustable LDO Regulator Programming**

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TPS767xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76701 (adjustable from 1.5 V to 5.5 V).

#### 10.1.1 External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047  $\mu\text{F}$  or larger) improves load transient response and noise rejection if the TPS767xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10  $\mu\text{F}$  and the ESR (equivalent series resistance) must be between 50 m $\Omega$  and 1.5  $\Omega$ . Capacitor values 10  $\mu\text{F}$  or larger are acceptable, provided the ESR is less than 1.5  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10  $\mu\text{F}$  surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.

### 10.2 Typical Application

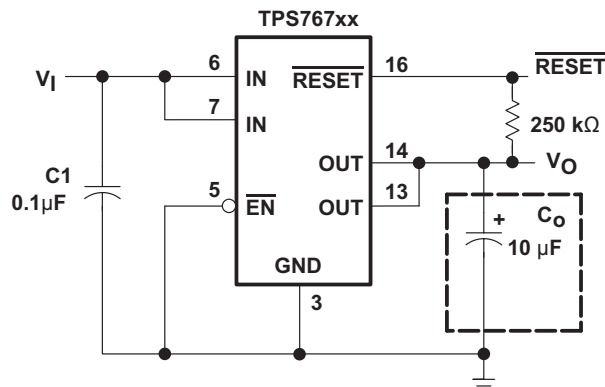
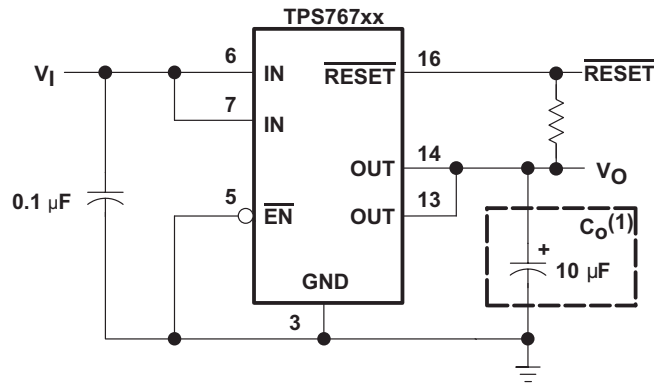


Figure 29. Typical Application Circuit (Fixed Versions)

Typical Application (continued)



(1) See application information section for capacitor selection details.

Figure 30. Typical Application Configuration (For Fixed Output Options)

## 11 Layout

### 11.1 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (3)$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature.

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS76715	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76718	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76725	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76727	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76728	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76730	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76733	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76750	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS76701	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76701QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76701	<a href="#">Samples</a>
TPS76701QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76701	<a href="#">Samples</a>
TPS76701QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701	<a href="#">Samples</a>
TPS76701QPWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701	<a href="#">Samples</a>
TPS76701QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701	<a href="#">Samples</a>
TPS76701QPWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701	<a href="#">Samples</a>
TPS76715QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76715	<a href="#">Samples</a>
TPS76715QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76715	<a href="#">Samples</a>
TPS76715QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76715	<a href="#">Samples</a>
TPS76715QPWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76715	<a href="#">Samples</a>
TPS76718QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76718	<a href="#">Samples</a>
TPS76718QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76718 X	<a href="#">Samples</a>
TPS76718QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76718	<a href="#">Samples</a>
TPS76718QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76718	<a href="#">Samples</a>
TPS76725QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76725	<a href="#">Samples</a>
TPS76725QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725	<a href="#">Samples</a>
TPS76725QPWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76725QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725	<a href="#">Samples</a>
TPS76727QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76727	<a href="#">Samples</a>
TPS76727QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76727	<a href="#">Samples</a>
TPS76728QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76728	<a href="#">Samples</a>
TPS76730QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76730	<a href="#">Samples</a>
TPS76730QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730	<a href="#">Samples</a>
TPS76730QPWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730	<a href="#">Samples</a>
TPS76730QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730	<a href="#">Samples</a>
TPS76733QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76733	<a href="#">Samples</a>
TPS76733QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76733	<a href="#">Samples</a>
TPS76733QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733	<a href="#">Samples</a>
TPS76733QPWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733	<a href="#">Samples</a>
TPS76733QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733	<a href="#">Samples</a>
TPS76733QPWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733	<a href="#">Samples</a>
TPS76750QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76750	<a href="#">Samples</a>
TPS76750QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76750	<a href="#">Samples</a>
TPS76750QPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76750	<a href="#">Samples</a>
TPS76750QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76750	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### **OTHER QUALIFIED VERSIONS OF TPS767 :**

- Automotive: [TPS767-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76701QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76701QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76715QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76718QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76718QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76725QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76730QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76733QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76733QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76750QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76750QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76701QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76701QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76715QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76718QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76718QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76725QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76730QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76733QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76733QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76750QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76750QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

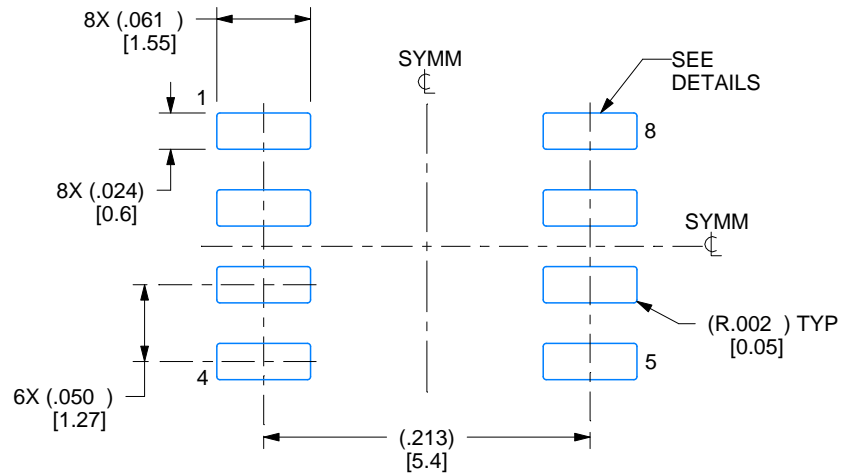
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

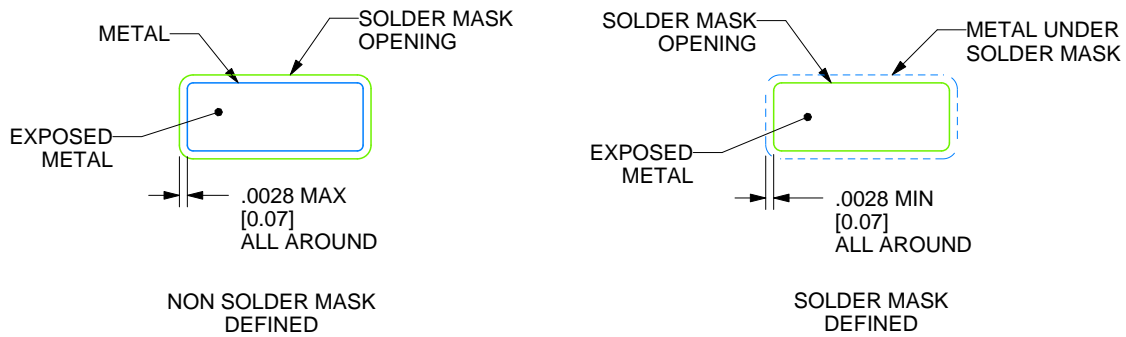
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

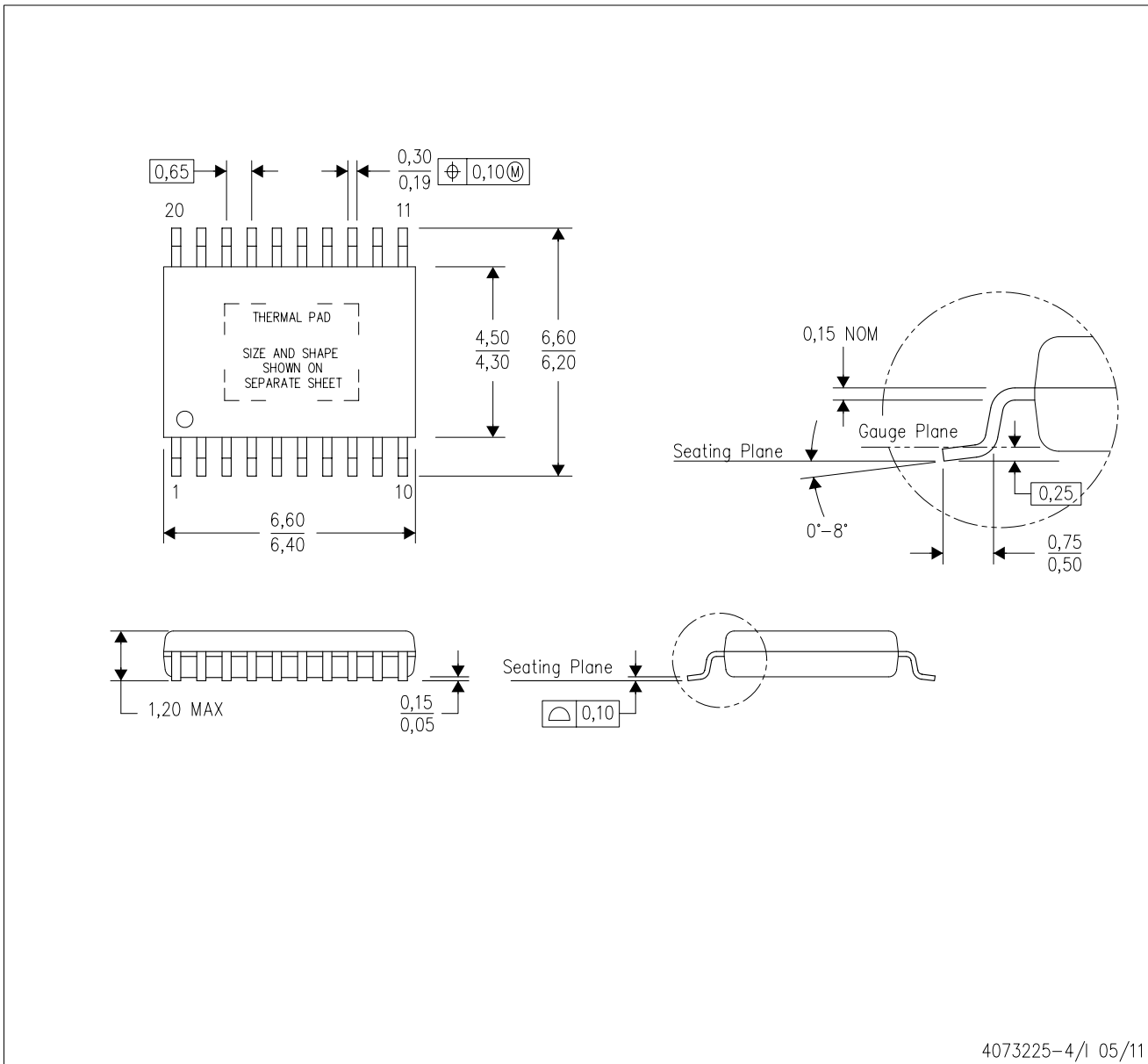
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

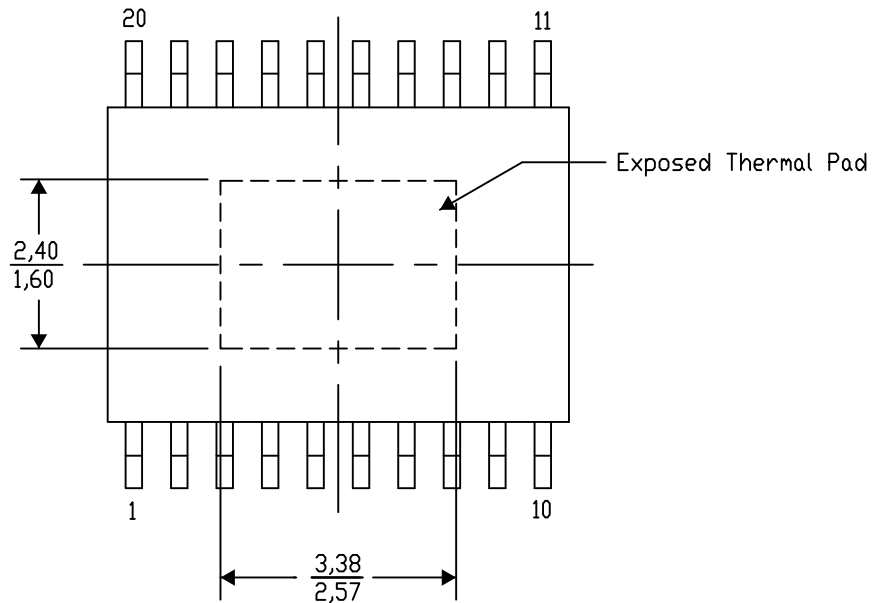
### PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

#### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

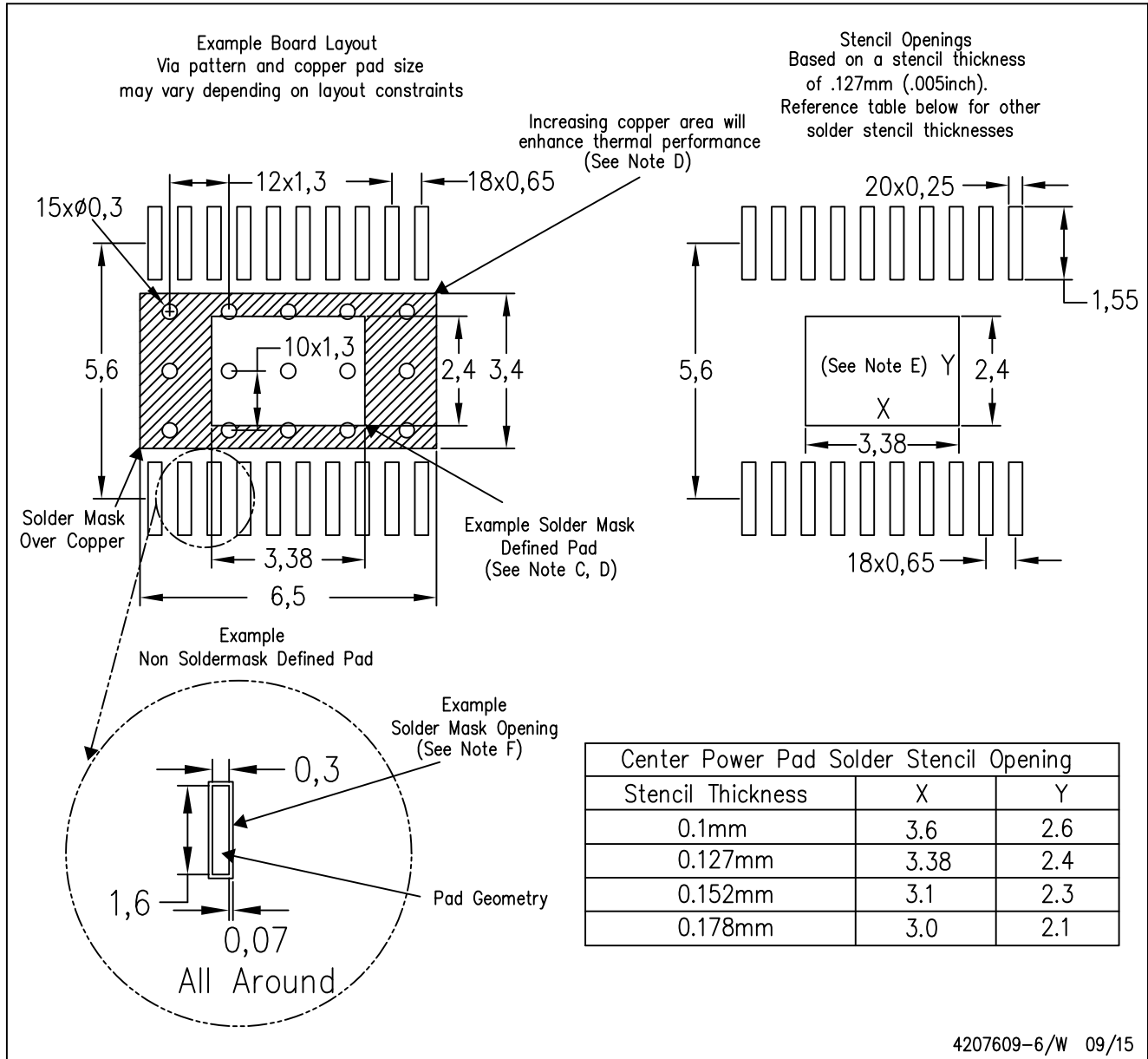
4206332-13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# THERMAL PAD MECHANICAL DATA

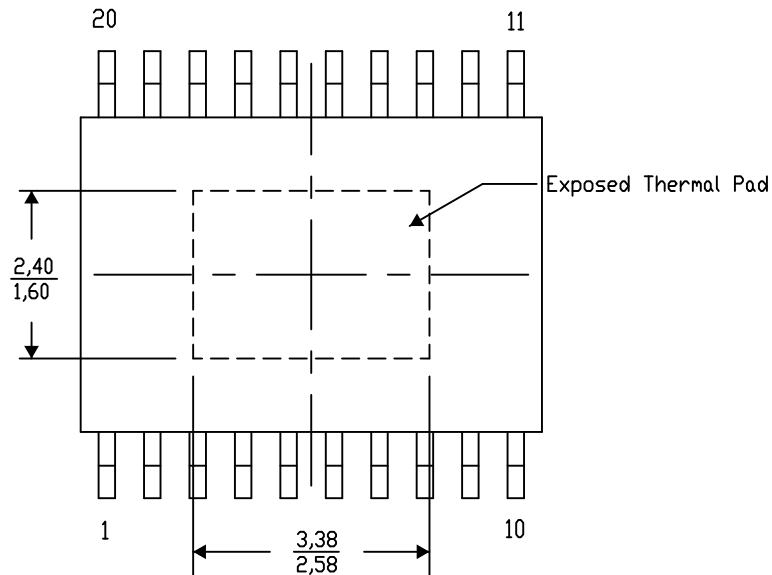
## PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206332-21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TPS76715QDR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management